High Resolution LVDT to Digital Converters

2S54/2S56/2S58

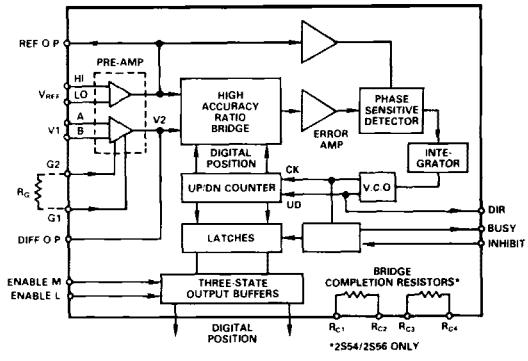
FEATURES

- Direct Conversion of LVDT and RVDT Outputs into Digital Format
- Ratiometric Conversion for Extremely High Stability
- High Resolution (14-16 Bit) Parallel Digital Output
- User Definable Input Gain
- Quadrature Rejection
- Operation Over 360 Hz to 11 kHz Frequency Range
- Linearity Better than ±0.01%
- Internal Bridge Completion Resistors
- 1 LSB Repeatability
- 75% Overrange Capability
- Extended Temperature Range Versions

APPLICATIONS

- Direct LVDT/RVDT-to-Digital Conversion
- Industrial Measurement and Gauging
- Valve and Actuator Control
- Limit Sensing
- Aircraft Control Systems
- Semiconductor Wafer Profiling
- AC-to-Digital Conversion

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 2S56 series of converters linearly converts the outputs of ac energized Linear and Rotary Variable Differential Transformers (LVDTs, RVDTs) directly into a high resolution digital format. For example, with a ±1 mm stroke LVDT, the least significant bit (LSB) of the 2S56 will represent 0.061 microns.

The 2S58, a high gain variant of the 2S56, can offer even higher positional resolution. Using the same ±1 mm stroke LVDT over a reduced range, the 2S58 can realize an LSB weighting of 1.22 nm.

The ratiometric conversion technique employed by the converters obviates the need for high stability oscillators. The performance quoted for the devices can be achieved with as much as a ±10% variation in reference amplitude.

The converters are complete – no signal conditioning, preamplifiers or filters are required. The user need only supply a suitable reference oscillator.

The converters operate on a Type II, tracking, servo loop principle which means that the digital output continuously follows the transducer input without the need for external convert commands as in conventional A-to-D converters. The conversion technique also ensures that there is no lag between digital output and transducer input under constant velocity conditions.

To facilitate interfacing with various types of LVDTs and RVDTs, all inputs are fully differential. In addition, the converters have the flexibility of setting the input gain with a single external resistor or link. In order to simplify the transducer interface, both the output of the gain stage as well as the reference voltage are brought out to enable simplified measurement.

The parallel digital output word is through tri-state drivers to enable direct connection to system data buses. Included is a High/Low byte enable which allows communication on both 8 and 16-bit busses. A separate line is provided to indicate the direction of transducer travel. A BUSY pulse is provided indicating that data is changing and not valid for transfer.

APPLICATIONS/USER BENEFITS

Because the 2S56 series of converters operates on the ratio of the transducer output signal to the excitation (reference) voltage, the entire measurement system is insensitive to changes in reference voltage, frequency and wave shape. The resulting stability makes conversion technique unrivaled, particularly in applications with poor voltage regulation.

The converters can also be connected in a mode which allows the 2S54/56/58 to be galvanically isolated from the excitation source. This configuration has the added benefit of minimizing the effect of phase shifts and signal input quadrature.

Because of the use of a phase sensitive demodulator in the tracking loop, the system has extremely high rejection of signals which are not phase and frequency coherent with the excitation voltage. The resulting noise immunity makes the converters an ideal choice for industrial and airborne applications.

The high precision of the conversion, together with the stability offered by ratiometric conversion, make the 2S56 series good candidates for applications previously beyond the capability of LVDTs. For example, the 2S58 can realize performance competitive with optical interferometric measurement systems.

2S54/2S56/2S58—SPECIFICATIONS[1]

Models	2S54	2S56	2S58	Comments	Units
DIGITAL OUTPUT				Output Coding Parallel	
Format	14-Bit Binary	16-Bit Binary	16-Bit Binary	Natural Binary	
Overrange[2]	75% of FS	*	*		
INPUTS (DIFFERENTIAL)					
V_{REF}	2	*	*		V rms
V_2	2	*	*		V rms
V_1[3]	0.2 (min) 2.0 (max)	*	0.04 (min) 0.2 (max)	See "INPUT GAIN" and	V rms
Input Gain	×1 to ×10	*	×10 to ×50	"SCALING INPUTS"	
Input Impedance (V_{REF}, V_1)[2]	1 GΩ	*	6 MΩ		
CMRR[2]					
@ ×1 Gain	100 (min)	*	NA		dB
@ ×10 Gain	100 (min)	*	120 (min)		dB
@ ×50 Gain	NA	NA	120 (min)		dB
BRIDGE COMPLETION RESISTORS[2]				(Only in 2S54/2S56)	
Value (XYO Options)	9990 (min) 10010 (max)	*	NA		Ω
Ratio Match	0.025	*	NA		%
Tracking Temperature Coefficient	2	*	NA		ppm/°C
REFERENCE FREQUENCY[2]					
50 Hz Bandwidth Option (2S54, 2S56)	360 (min) 5000 (max)	*	NA		Hz
140 Hz Bandwidth Option (2S54, 2S56)	1000 (min) 5000 (max)	*	NA		Hz
300 Hz Bandwidth Option (2S58 Only)	NA	NA	7000 (min) 11000 (max)		Hz
DIGITAL OUTPUT (BIT 1–BIT 16)					
Output Voltage				V_L = +5 V dc	
(Logic Low I_{OL}=8.0 mA)	0.4 (max)	*	*	Logic Low I_{OL} = 8.0 mA	V dc
(Logic High I_{OH}=−0.4 mA)	2.4 (min)	*	*	Logic High I_{OH} = −0.4 mA	V dc
Tristate Leakage Current				V_L = +5 V dc	
(V_{OZL}=0.4 V dc)	±20 (max)	*	*	Logic Low V_{OZL} = 0.4 V dc	μA
(V_{OZH}=2.4 V dc)	±20 (max)	*	*	Logic High V_{OZH} = 2.4V dc	μA
DIGITAL INPUT					
($\overline{\text{INHIBIT}}$, ENABLE M, $\overline{\text{ENABLE L}}$)					
Low Input Voltage	0.7 (max)	*	*	V_L = +5 V dc	V dc
High Input Voltage	2.0 (min)	*	*	V_L = +5 V dc	V dc
Low Input Current	−400 (max)	*	*	V_{IL} = 0.4 V dc	μA
High Input Current	20 (max)	*	*	V_{IH} = +2.4 V dc	μA
DATA TRANSFER[2]				See Figure 12	
BUSY Pulse Width	380 (min) 530 (max)	*	*		ns
BUSY Pulse Load[4]	6	*	*	BUSY Is "Hi" When Output Is Changing	LSTTL Loads
Enable/Disable Time	120 (typ) 220 (max)	*	*		ns
Data Setup Time	600	*	*		ns
ACCURACY[5]					
Conversion Accuracy	±0.7	±2.5	±1		LSB
Gain Accuracy[6, 7]					
@ ×1 Gain					
0 to +70°C (5Y0)	±0.03 (max)	*	NA	2S54/2S56 Only	% FSR
−55°C to +125°C (4Y0)	±0.03 (max)	*	NA		% FSR
@ ×10 Gain					
0 to +70°C (5Y0)	±0.07 (max)	*	*	2S54/2S56 and 2S58	% FSR
−55°C to +125°C (4Y0)	±0.10 (max)	*	*		% FSR
@ ×50 Gain					
0 to +70°C (5Y0)	NA	NA	±0.09 (max)	2S58 Only	% FSR
−55°C to +125°C (4Y0)	NA	NA	±0.12 (max)		% FSR

Models	2S54	2S56	2S58	Comments	Units
Integral Linearity[6, 7]					
0° Phase Shift, V_{REF} to V_1	±0.006 (max)	*	±0.00312 (max)	See "PHASE SHIFT	% FSR
1° Phase Shift, V_{REF} to V_1	±0.008 (max)	*	±0.00437 (max)	AND QUADRATURE	% FSR
5° Phase Shift, V_{REF} to V_1	±0.01 (max)	*	±0.00625 (max)	EFFECTS"	% FSR
Differential Linearity[6]	±0.5 (max)	*	*		LSB
Temperature Dependent					
Position Offset[2]	±0.04 (max)	*	*		% FSR
REPEATABILITY[5]					
Over 0 to +70°C[2]	±1	*	*		LSB
Hysterisis	0.5 (min) 1 (max)	*	*		LSB
DYNAMIC CHARACTERISTICS[5]					
Slew Rate[2]					
50 Hz Bandwidth Option (2S54, 2S56)	150	*	NA		LSB/ms
140 Hz Bandwidth Option (2S54, 2S56)	360	*	NA		LSB/ms
300 Hz Bandwidth Option (2S58 Only)	NA	NA	688		LSB/ms
Settling Time (Half FS Step)					
50 Hz Bandwidth Option (2S54, 2S56)	160	300	NA	Half FS Step	ms
140 Hz Bandwidth Option (2S54, 2S56)	70	160	NA	Half FS Step	ms
300 Hz Bandwidth Option (2S58 Only)	NA	NA	65	Step From −FSR to −FSR	ms
ANALOG OUTPUTS					
DIFF O/P (Max Allowable Swing)	10	*	*		V p-p
REF O/P (Max Allowable Swing)	10	*	*		V p-p
POWER REQUIREMENTS					
$+V_S$	+15 ±5%	*	*		V dc
$-V_S$	−15 ±5%	*	*		V dc
+5 V	+5 ±5%	*	*		V dc
Supply Currents					
$\pm V_S$	25 (typ) 40 (max)	*	*	Quiescent Condition	mA
+5 V	105 (typ) 125 (max)	*	*		mA
Power Dissipation	1.3 (typ) 1.8 (max)	*	*		Watts
TEMPERATURE RANGE					
Operating	0 to +70 (5Y0 Option)	*	*		°C
	−55 to +125 (4Y0 Option	*	*		°C
Storage	−55 to +125	*	*		°C
DIMENSIONS	2.145 × 1.145 × 0.227 (max)	*	*	See Packaging	Inches
	54.5 × 29.1 × 5.76 (max	*	*	Specifications	mm
WEIGHT	1	*	*		Ounces
	28	*	*		Grams
PACKAGE OPTIONS[8]	DH-40A	DH-40A	DH-40A		

NOTES

[1]Tested with nominal supply (±15 V dc, +5 V dc), reference/signal voltages and frequency.

[2]Guaranteed by design, test not required.

[3]V_1 is the signal input to the converter directly from the transducer. V_2 is the output of the internal gain stage. Because V_2 needs to be maintained at 2 V ±10% in order to meet the converter accuracy (see Note 5), the gain and the maximum value of V_1 should be carefully chosen. Furthermore, because the converter operates on the ratio of V_2 and V_{REF}, care should be taken to see these voltages are matched in order to achieve the full dynamic range of the converter.

[4]Maximum output current is 2.4 mA.

[5]Specified over the operating temperature range of the option and for:

a. ±10% difference in both V_{REF} and V_2 amplitudes

b. 10% harmonic distortion in V_{REF} and V_1.

c. The accuracy is specified for the preset gains of ×1, ×10, and ×50. For accuracy in the intermediate range, see Section "PHASE SHIFT AND QUADRATURE EFFECTS."

[6]Tested with input gains 1, 10 and 50 with V_1 attenuated by 1, 10 and 50, respectively.

[7]Full-Scale Range (FSR) is defined as $V_2 = +V_{REF}$ to $V_2 = -V_{REF}$. This would usually correspond to the utilized LVDT stroke.

[8]DH-40A = Hermetic Metal Can DIP.

*Specifications the same as the 2S54.

Specifications subject to change without notice.

MODELS AVAILABLE

The 2S56 series is available in three versions:

2S54	14-Bits	Input Gain	1–10
2S56	16-Bits	Input Gain	1–10
2S58	16-Bits	Input Gain	10–50

The 2S54 and 2S56 are available in two bandwidth options. The 50 Hz bandwidth option operates over the reference frequency range of 360 Hz to 5 kHz, while the 140 Hz bandwidth option operates over the range of 1 kHz to 5 kHz. The 2S58 is available only in a 300 Hz bandwidth version which operates with reference frequencies between 7 kHz and 11 kHz.

All three devices are available in both commercial (0 to +70°C) and military (−50°C to +125°C) operating temperature versions.

Full ordering information is given on the back page of this data sheet.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to GND . . . . . +17 V dc
$-V_S$ to GND . . . . . −17 V dc
V_{REF} . . . . . 35 V p-p
$+V_L$ to GND . . . . . +7 V dc
V1 . . . . . 35 V p-p
Logical Input to GND (max) . . . . . +5.5 V dc
Logical Input to GND (min) . . . . . −0.4 V dc
Case to GND . . . . . ±20 V dc
Power Dissipation . . . . . 1.8 Watts
Junction Temperature . . . . . +150°C

CAUTION:

1. Absolute Maximum Ratings are the limits beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
3. The +5 V power supply must never go below GND.

PRINCIPLES OF OPERATION

The principle of operation is shown in Figure 1.

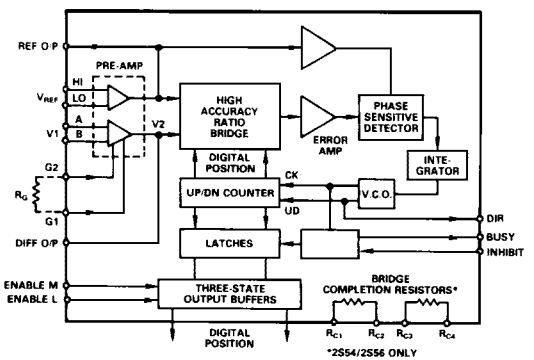


Figure 1. Principle of Operation of the 2S56 Series Converters

USING THE 2S56 SERIES CONVERTERS

The 2S56 series of converters operates on a tracking principle. This means that the output digital word always automatically represents the position of the LVDT or RVDT without the need for external convert commands and status wait loops. As the transducer moves through a position equivalent to 1 Least Significant Bit (LSB) on the output, the output digital word is automatically updated. Each LSB update initiates a BUSY pulse.

INPUT GAIN

Since the transformation ratio of an LVDT or RVDT from excitation voltage to signal voltage is typically in the order of 1:0.15, provision for gain scaling has been provided. The gain can, therefore, be selected to ensure that the full-scale output of the converter represents the maximum stroke position of the transducer.

The gain setting is accomplished by means of Pins 21 and 22 (G1 and G2). A link between the two pins gives a preset gain of ×10 (×50 on the 2S58) whereas no connections between them gives a preset gain of ×1 (×10 on the 2S58).

$$G = \frac{R_1}{R_G + R_2} + G\infty$$

where R_G is the value of the external resistor in kΩ and G is the realized gain.

For the 2S54 and 2S56:

R_1 = 27 [kΩ]

R_2 = 3 [kΩ]

$G\infty$ = 1

For the 2S58:

R_1 = 108 [kΩ]

R_2 = 2.7 [kΩ]

$G\infty$ = 10

The internal resistors each have absolute accuracies of 0.02% at 25°C. Their absolute temperature coefficient is ±25 ppm/°C. Therefore, if the temperature coefficient and absolute accuracy of the external gain setting resistor, R_G, is known, the accuracy of the input gain stage can be calculated. This additional inaccuracy must be added to the gain error of the converter.

DIGITAL OUTPUT CODES

The 2S56 series of converters employs an offset binary output code, the null position of the LVDT being represented by the MSB being high and all other bits low. Representative digital output codes are shown in Figure 2. For the 2S54 (14-bit resolution), the two least significant bits are unused.

NOTE: A negative position is defined as being when the V1 and V_{REF} are out of phase. A positive position is when they are in phase.

OVERRANGE

The digital output code format shown in Figure 2 enables the user to determine if the LVDT has exceeded the negative or positive full-scale position and has gone into overrange. An indication of overrange can be obtained by performing an "exclusive OR" on Bits 1 and 2 (MSB and 2nd MSB). Alternatively this function can be performed in software.

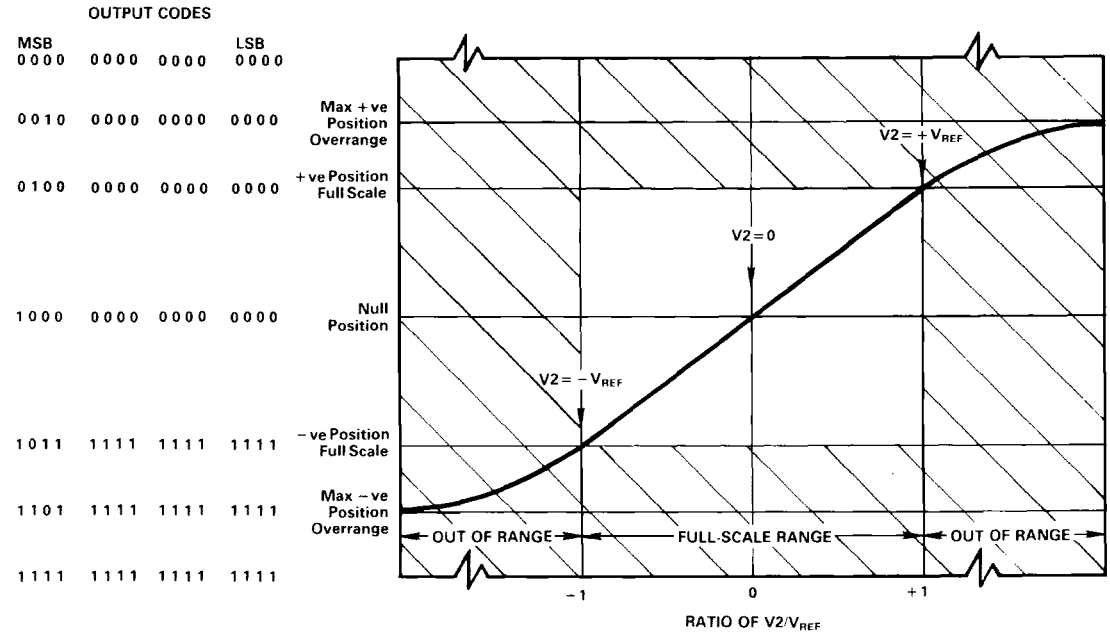


Figure 2. Output Code Format

PHASE SHIFT AND QUADRATURE EFFECTS

Reference to signal phase shift can be high in LVDTs, sometimes in the order of 70 degrees. If the converter is connected as in Figures 3 and 4, any effects due to this phase shift are minimized. This connection method, therefore, provides outstanding benefits.

The additional gain error caused by reference to signal phase shifts is given by:

$$(1 - cos\theta) \times 100\% \; of \; FSR$$

where

θ = phase shift between V_{REF} and V1.

When the phase shift between V_{REF} and V1 is zero, additional quadrature on the signal will have no effect on the converter. This is another benefit of the conversion method.

CONNECTING LVDTS

Since all input connections to 2S56 converters are truly differential, there is great flexibility in the input sensor connection configuration. Some of the various methods are shown in Figures 3, 4 and 5.

(It should be noted that a ground reference point should always be included and connected to either the V_{REF} or V1 inputs.)

It is suggested that decoupling capacitors be connected in parallel between the power supply lines ($+V_S$, $-V_S$, +5 V) and GND, adjacent to the converter. Suggested values are: 6.8 μF tantalum and 47 nF disc capacitors connected in parallel. When more than one converter is on a card, separate decoupling should be used for each converter, particularly the 47 nF capacitors.

The $+V_S$ and the $-V_S$ pins should be connected to dc power supplies of the appropriate polarity in the range of ±15 V ±5%. Care should be taken to ensure that the polarity can never become reversed. The +5 V pins should be connected to a +5 V ±5% dc supply. The +5 V supply must never be allowed to go negative with respect to ground.

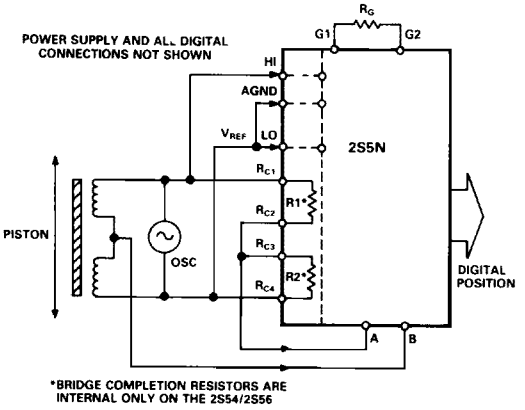


Figure 3. Half Bridge LVDT Connection

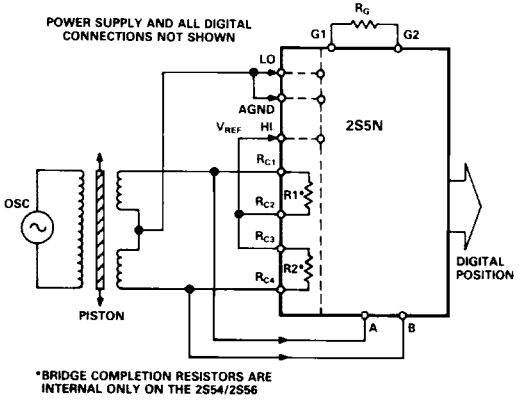


Figure 4. Three- or Four-Wire LVDT Connection

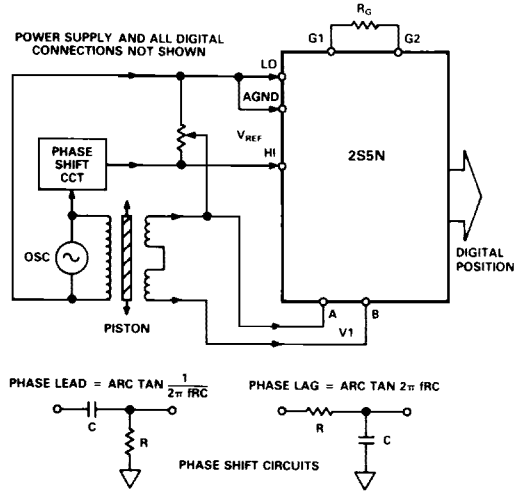


Figure 5. Two-Wire LVDT Connection

Half Bridge Type LVDT Connection

In this method of connection, shown in Figure 3, the internal bridge completion resistors, R1 and R2, in the 2S54 and 2S56 are used. If this configuration is used with the 2S58, external precision resistors must be employed. The "BRIDGE COMPLETION RESISTORS" in the SPECIFICATIONS section details the required precision. The internal resistors in the 2S54 and 2S56 have nominal values of 10 kΩ and are matched sufficiently to ensure that the null position of the LVDT is represented by the correct output code. The common connection between the two resistors (i.e., R_{C2} to R_{C3} on the 2S54, 2S56) can be replaced by a potentiometer if the null needs to be adjusted. For differential measurements, the resistors can be replaced by another LVDT. The system is nonisolated.

Three or Four Wire LVDT Connection

In this method of connection, shown in Figure 4, the converters digital output is proportional to the ratio:

$$\frac{(A-B)}{(A+B)/2}$$

where A and B are the individual LVDT secondary output voltages. Inspection of Figure 4 should demonstrate why this relationship is true. (A−B) is simply the voltage across the series connected secondaries of the LVDT and is applied to the V1 input to the converter. (A+B)/2 is effectively the average of the two secondary voltages as computed by the balanced bridge completion resistors and the grounding of the secondary center-tap.

Note: This method of connection is appropriate only for where (A+B) is a constant, independent of LVDT position. Any lack of constancy in (A+B) will be reflected as an additional non-linearity in the output. It is up to the user to determine if (A+B) is sufficiently constant over the particular stroke length employed. (A+B)/2 can be monitored on the "REF O/P" pin.

This method will usually restrict the usable LVDT range to half of its full range. The restriction can be eliminated, however, by attenuating V1 by a factor of 2 or increasing V_{REF} by a factor of 2.

This connection method has the tremendous advantage of being insensitive to temperature related phase shifts and excitation oscillator instabililty effects usually associated with more conventional LVDT conversion systems.

As in the case of the Half Bridge Type LVDT Connection, R1 and R2 are the bridge completion resistors (internal on the 2S54, 2S56; external on the 2S58) and are matched to a degree sufficient to ensure that the digital output representing the null position does not vary from the LVDT's natural null position. If null adjustment is required, a potentiometer can be used in place of the common connection between the two resistors.

Two-Wire LVDT Connection

This method should be used in cases where the sum of the LVDT secondary output voltages (A+B) is not constant with LVDT displacement over the desired stroke length. The method of connection, shown in Figure 5, still maintains the ratiometric operation and the insensitivity to variations in reference amplitude and frequency. However, the phase shift between V_{REF} and V1 should be minimized to maintain accuracy (see Section "PHASE SHIFT AND QUADRATURE EFFECTS"). Suggested phase compensation circuits are shown in Figure 5.

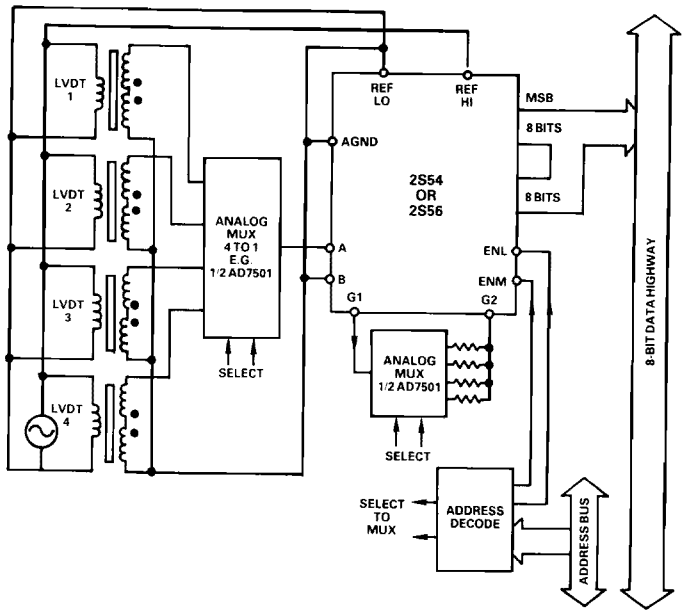


Figure 6. Multiplexing 4 LVDTs into the 2S54/2S56

MULTIPLEXING THE CONVERTERS

Although the 2S56 series of converters are primarily intended for use as single channel, continuous conversion devices, they can also be used in small multiplexed systems as shown in Figure 6. However, when switching between LVDT channels, ample time must be allowed for the converters to settle prior to transferring data.

Using the 2S54/X40 as in Figure 6 and allowing a time between samples of 70 ms, the maximum settling time of the converter can yield four 14-bit results from the 4 LVDTs in 280 ms. The gain can be programmed, as shown, to accommodate various transformation rations of dissimilar LVDTs. Note, however, that the finite "ON" resistance of the analog switch used with the gain setting resistor can introduce gain inaccuracies. This error is minimized for lower gains as the "ON" resistance of the switch will be negligible compared to the gain setting resistor. The error introduced can be calculated from the equation for the preamplifier gain in the "INPUT GAIN" section.

SCALING THE INPUTS

In cases where there is a requirement for a particular LVDT stroke length to correspond to full-scale on the digital output, the input gain must be chosen accordingly. It is important to remember that it is the relationship between V2 and V_{REF}, not V1 and V_{REF}, which determines the full-scale digital output. Furthermore, it should be ensured that these voltages are each 2 V rms ±10%, respectively. For monitoring purposes, V2 is brought to the "DIFF O/P" pin and V_{REF} is brought to the "REF O/P" pin.

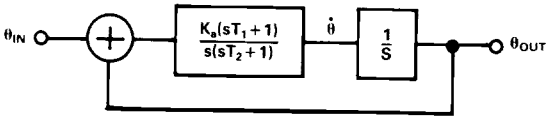


Figure 7. Transfer Function

DYNAMIC PERFORMANCE

The transfer function of the converters, shown in Figure 7 is given by:

Open Loop Gain:

$$\frac{\Delta_{OUT}}{\Delta_{IN}} = \frac{K_a}{S^2} \cdot \frac{1+sT_1}{1+sT_2}$$

Closed Loop Gain:

$$\frac{\Delta_{OUT}}{\Delta_{IN}} = \frac{1+sT_1}{1+sT_1+s^2/K_a+s^3T_2/K_a}$$

where:

	k_a	T1	T2
2S54/56 X10 options	12000 sec^{-2}	14.7 ms	2.3 ms
2S54/56 X40 options	93600 sec^{-2}	5.9 ms	1.0 ms
2S58	450000 sec^{-2}	2.4 ms	0.4 ms

The gain and phase response of each of the three options is shown in Figures 8, 9, 10, 11, 12 and 13.

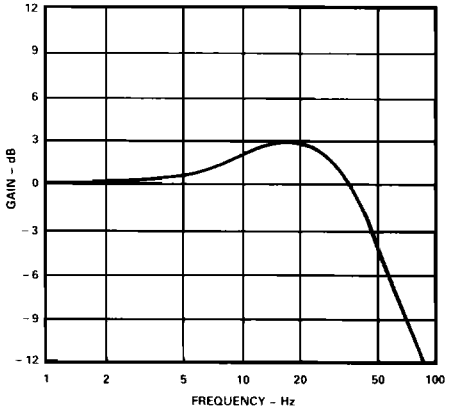


Figure 8. Gain Plot 410 and 510 Options (2S54/2S56)

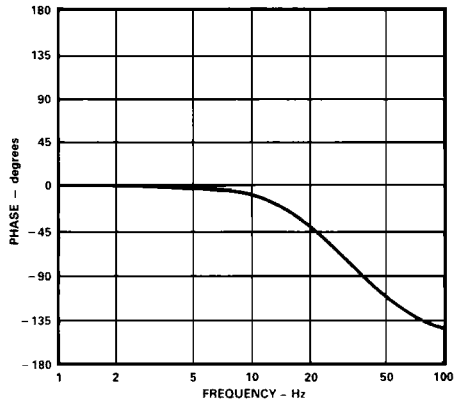


Figure 9. Phase Plot 410 and 510 Options (2S54/2S56)

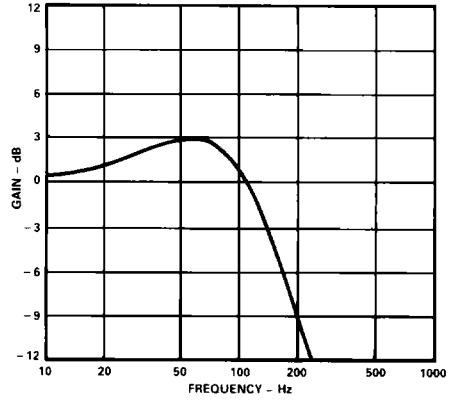


Figure 10. Gain Plot 440 and 540 Options (2S54/2S56)

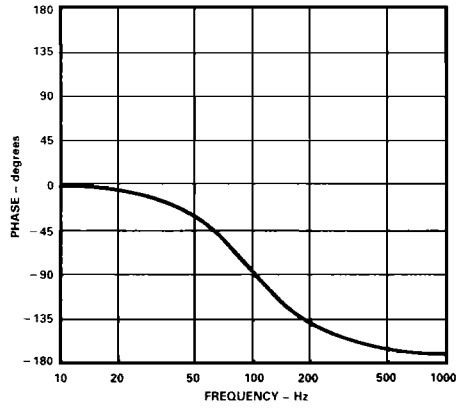


Figure 11. Phase Plot 440 and 540 Options (2S54/2S56)

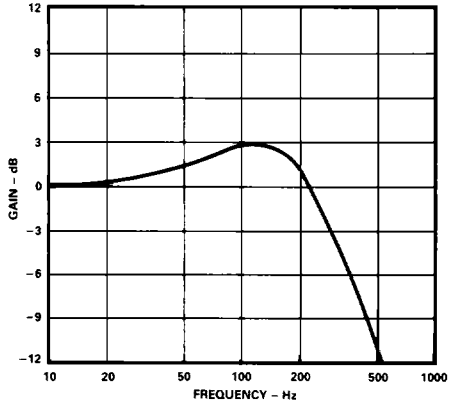


Figure 12. Gain Plot for 2S58

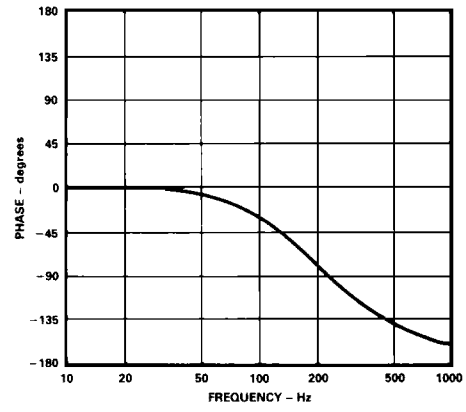


Figure 13. Phase Plot for 2S58

ACCELERATION ERROR

Tracking converters such as the 2S56 series, employing a type 2 servo loop, do not suffer any velocity lag. However, there is an additional error when the LVDT is undergoing periods of acceleration.

The additional error can be defined using the K_a constant of the converter (see DYNAMIC PERFORMANCE section) as follows:

$$K_a = \frac{\textit{Input acceleration}}{\textit{Error in output position}}$$

where the numerator and the denominator are defined in the same units.

K_a does not define the maximum acceleration, only the error due to the acceleration.

DATA TRANSFER

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, due to a change in displacement of the LVDT, the signal appearing on the converter's BUSY output pin is a series of pulses of TTL levels. A BUSY pulse is initiated each time the input moves by the equivalent of an LSB and the internal up-down counter is incremented or decremented.

With the INHIBIT input pin in the "Hi" state, data will be transferred automatically to the output latches.

The two three-state enable inputs, ENABLE L and ENABLE M, allow the digital input to be transferred on to a data bus in two separate bytes. ENABLE M enables the most significant 8 bits of the output word while ENABLE L enables the remaining least significant bits.

Figure 14 shows the timing diagram.

There are two methods of transferring the output data. The first is to detect the state of the "BUSY" which is 'Hi" for 1 μs max and then transfer the data when the BUSY is "Lo". Both INHIBIT, ENABLE M and ENABLE L must be in their correct state of "Hi" and "Lo" respectively, in order that the data is presented to the output.

The alternative method is to use the INHIBIT input. Taking this input to a "Lo" state prevents the internal monostable circuits being triggered and consequently the latches being updated. Data will always be valid 1 μs after the application of a logic "Lo" to the INHIBIT. However, if INHIBIT is applied while BUSY is in the "Lo" state (with ENABLE M and ENABLE L also "Lo"), data is valid instantaneously.

The internal tracking operation of the converter cannot in any way be affected by the logic state present on either the INHIBIT or the ENABLE pins.

OTHER INPUTS AND OUTPUTS

Differential Output (DIFF O/P)

This signal is in fact V2 and is brought out to a pin in order to simplify scaling of the V1 signal.

Direction (DIR)

This TTL output signal indicates the direction of the transducer. It is a logic "Hi" when counting up and a logic "Lo" when counting down.

Reference Output (REF O/P)

This is the reference signal after the input buffer stage. It can be used as a single ended measurement point for the V_{REF} input.

It can also be used as a BITE (Built in Test Equipment) signal to detect if the LVDT has become disconnected or the reference supply has failed.

SUPPORT OSCILLATOR

A power oscillator, OSC1758, is available for use as a reference generator for LVDT and RVDT transducers. It is capable of providing up to 7 volts rms at 1.4 VA.

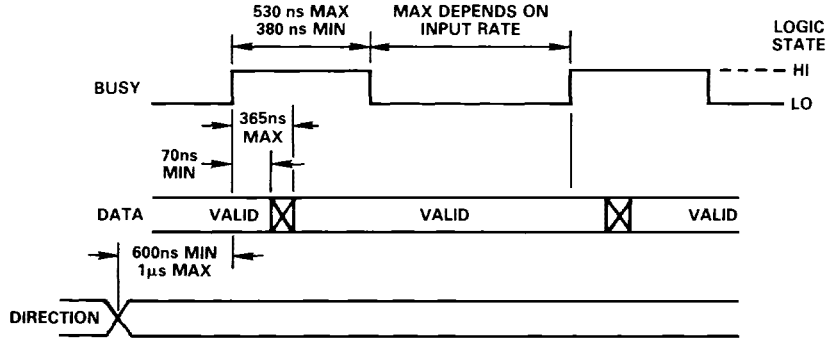
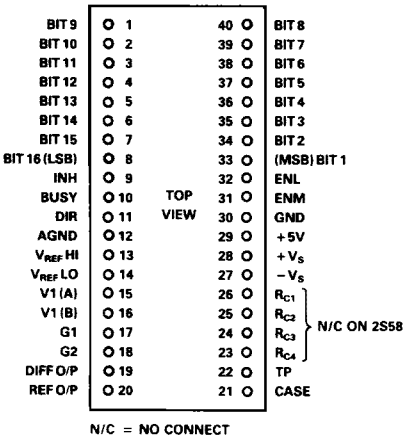


Figure 14. 2S56 Data Transfer Timing Diagram

PIN CONFIGURATIONS



N/C = NO CONNECT

MEAN TIME BETWEEN FAILURES (MTBF)

The predicted reliability of these converters is exceptionally high due to the extensive uses of LSI custom circuitry. Figure 15 shows the MTBF of the 4YZ options as calculated according to MIL HDBK 217D at various temperatures under ground benign environment. For MTBF calculations under other environments, please consult the factory.

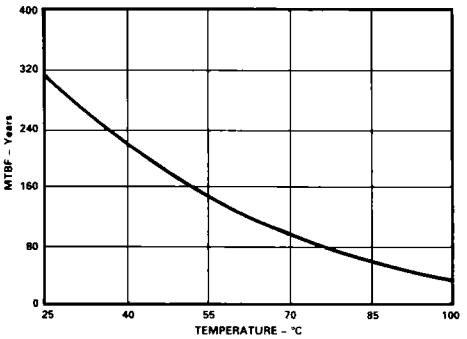


Figure 15.

PIN FUNCTION DESCRIPTION

$-V_S$	Main negative power supply.
$+V_S$	Main positive power supply.
+5 V	Logic power supply.
GND	Power supply ground. Digital ground.
Bit 1–14 (2S54) Bit 1–16	Parallel output data bits. (2S56, 2S58))
$\overline{\text{INHIBIT}}$	Inhibit logic input. Taking this pin "Lo" inhibits data transfer from counter to output latches. The conversion loop continues to track.
BUSY	Converter BUSY. A "Hi" output indicates that the output latches are being updated. Data should not be transferred from the converter while BUSY is "Hi."
$\overline{\text{ENABLE M}}$	The 8 most significant output data bits are set to a high impedance state by application of a logic "Hi."
$\overline{\text{ENABLE L}}$	The 6 least significant bits of a 2S54, or the 8 least significant bits of a 2S56 "and 2S58," are set to a high impedance state by application of a logic "Hi."
R_{C1} R_{C2}	Connections to R1, internal bridge completion resistor (2S54/2S56 only).
R_{C3} R_{C4}	Connections to R2, internal bridge completion resistor (2S54/2S56 only).
DIR	TTL output indicating the direction of movement of the transducer.
AGND	Analog ground.
V_{REF} HI V_{REF} LO	Input pins for the Reference signal.
V1 (A) V1 (B)	Input pins for the Signal.
G1 G2	A gain setting resistor, or a link, can be connected between these pins.
DIFF O/P	This is a V1 after scaling (V2).
REF O/P	This is the reference signal after the input buffer stage.
CASE	This should normally be grounded. Case can be taken to any voltage with a low impedance up to ±20 V.
TP	Test Point. Do not make connections to this pin.

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Condition
1. Preseal Burn In	64 Hours at +125°C
2. Precap Visual Inspection	In-House Criteria
3. Seal Test, Fine and Gross	In-House Criteria
4. Final Electrical Test	

Extended temperature range versions receive additional processing as follows:

4. Final Electrical Test	Performed at Maximum and Minimum Operating Temperatures

PROCESSING FOR HIGH RELIABILITY

All extended temperature range models are available with high reliability screening. The parts are identified with a B suffix, and will receive the following processing.

Process	Conditions
1. Preseal Burn In	64 Hours at +125°C
2. Precap Visual Inspection	MIL-STD-883, Method 2017
3. Temperature Cycling	10 Cycles, −65°C to +150°C
4. Constant Acceleration	5000G, Y1 Plane
5. Interim Electrical Tests	
6. Operating Burn In	96 Hours at +125°C
7. Seal Test, Fine and Gross	MIL-STD-883, Method 1014
8. Final Electrical Testing (Group A)	Performed at T_{min}, T_{AMB}, and T_{max}
9. External Visual Inspection	MIL-STD-883, Method 2009

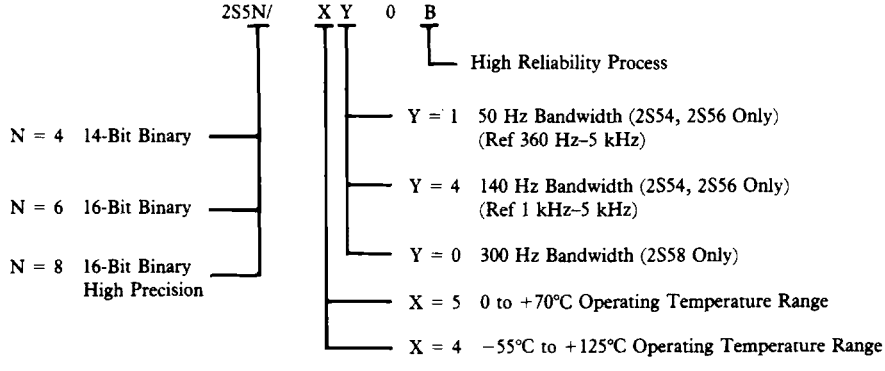
NOTE: Test and screening data can be supplied. Further information on request.

OTHER TRANSDUCER INTERFACE PRODUCTS

2S80/2S81/2S82	10–16 Bit Variable Resolution Resolver to Digital Converter (Monolithic IC)
2S50	10 Bit + Sign, LVDT to Digital Converter (Hybrid)
OSC1758	Power Oscillator (Hybrid)
IPA1764	Inductosyn Pre-Amplifier (Hybrid)

3

ORDERING INFORMATION



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

40-Pin Bottom Brazed Ceramic DIP (DH-40A)