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ECL Products	

# 10136

## Universal Counter

### Universal Hexadecimal Counter

#### FEATURES

- Typical propagation delay: 3.3ns
- Typical supply current ( $-I_{EE}$ ): 120mA

#### DESCRIPTION

The 10136 is a high-speed Hexadecimal Synchronous Counter that can count up, count down, preset, or stop count at frequencies exceeding 100MHz. The operation mode of the counter is programmed by three control lines ( $S_0$ ,  $S_1$ , and CP) as can be seen in the Function Select Table. In the preset mode (loading step), a clock pulse is needed for the information present on the data inputs ( $D_0$ ,  $D_1$ ,  $D_2$ , and  $D_3$ ) to be entered into the counter.  $C_{OUT}$  goes Low on the terminal count, or when the counter is being preset.

The counter changes state only on the positive-going edge of the clock, so at any other time any other input may change without any result (except for  $C_{OUT}$ ).

This binary counter can be used in many applications, such as in computing for high-speed control processors and peripheral controllers. Unused inputs must be tied Low to  $V_{IL}$  or  $V_{EE}$ .

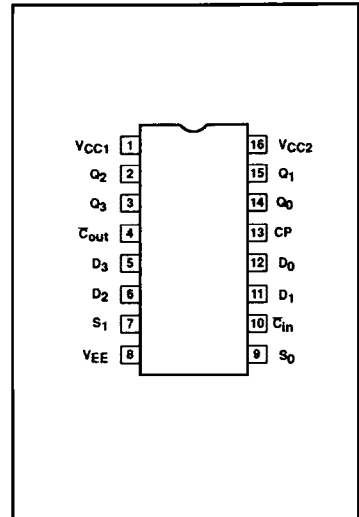
#### ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic DIP	10136N
16-Pin Ceramic DIP	10136F

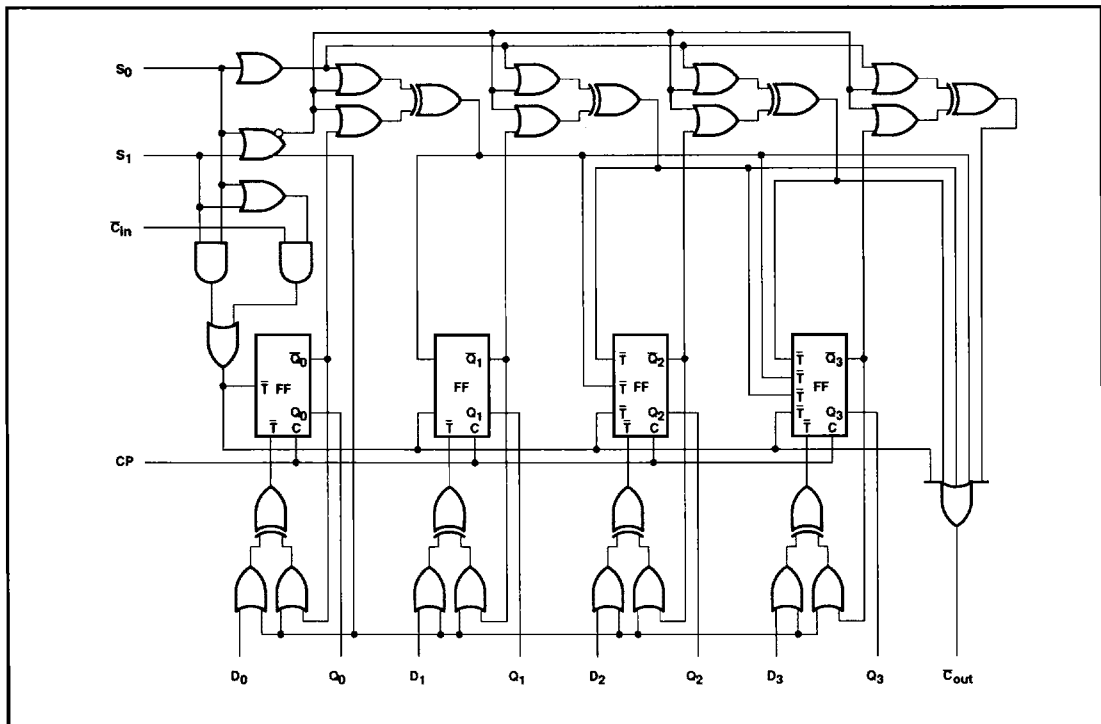
#### PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$	Data Inputs
CP	Clock Input
$C_{IN}$	Carry-in Input
$S_0, S_1$	Select Inputs
$C_{OUT}$	Carry-out Output
$Q_0 - Q_3$	Data Outputs

#### PIN CONFIGURATION



#### LOGIC DIAGRAM



# Universal Counter

# 10136

## FUNCTION SELECT TABLE

$\overline{C}_{IN}$	$S_0$	$S_1$	OPERATING MODE
X	L	L	Preset (Program)
L	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
X	H	H	Hold (Stop Count)

H = High Voltage Level

L = Low Voltage Level

X = Don't Care

## SEQUENTIAL FUNCTION TABLE

INPUTS								OUTPUTS				
$S_0$	$S_1$	$D_0$	$D_1$	$D_2$	$D_3$	$\overline{C}_{IN}$	CP	$Q_0$	$Q_1$	$Q_2$	$Q_3$	$\overline{C}_{OUT}$
L	L	L	L	H	H	X	↑	L	L	H	H	L
L	H	X	X	X	X	L	↑	H	L	H	H	H
L	H	X	X	X	X	L	↑	L	H	H	H	H
L	H	X	X	X	X	L	↑	H	H	H	H	L
L	H	X	X	X	X	H	L	H	H	H	H	H
L	H	X	X	X	X	H	↑	H	H	H	H	H
L	L	H	H	L	L	X	↑	H	H	L	L	L
H	L	X	X	X	X	L	↑	L	H	L	L	H
H	L	X	X	X	X	L	↑	H	L	L	L	H
H	L	X	X	X	X	L	↑	L	L	L	L	L
H	L	X	X	X	X	L	↑	H	H	H	H	H

### NOTE:

This function table shows logic states assuming inputs vary in the sequence shown from top to bottom.

H = High Voltage Level

L = Low Voltage Level

X = Don't Care

↑ = Low-to-High transition

## Universal Counter

10136

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMITS	UNIT	
$V_{EE}$	Supply voltage	-8.0	V	
$V_{IN}$	Input voltage ( $V_{IN}$ should never be more negative than $V_{EE}$ )	0 to $V_{EE}$	V	
$I_O$	Output source current (continuous)	-50	mA	
$T_S$	Storage temperature range	-55 to +150	°C	
$T_J$	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

## NOTE:

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

## DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
$V_{CC1}, V_{CC2}$	Circuit ground		0	0	0	V
$V_{EE}$	Supply voltage (negative)			-5.2		V
$V_{IH}$	High level input voltage	$T_A = -30^\circ\text{C}$			-890	mV
		$T_A = +25^\circ\text{C}$			-810	mV
		$T_A = +85^\circ\text{C}$			-700	mV
$V_{IHT}$	High level input threshold voltage	$T_A = -30^\circ\text{C}$	-1205			mV
		$T_A = +25^\circ\text{C}$	-1105			mV
		$T_A = +85^\circ\text{C}$	-1035			mV
$V_{ILT}$	Low level input threshold voltage	$T_A = -30^\circ\text{C}$			-1500	mV
		$T_A = +25^\circ\text{C}$			-1475	mV
		$T_A = +85^\circ\text{C}$			-1440	mV
$V_{IL}$	Low level input voltage	$T_A = -30^\circ\text{C}$	-1890			mV
		$T_A = +25^\circ\text{C}$	-1850			mV
		$T_A = +85^\circ\text{C}$	-1825			mV
$T_A$	Operating ambient temperature range		-30	+25	+85	°C

## NOTE:

When operating at other than the specified  $V_{EE}$  voltage (-5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

## Universal Counter

10136

**DC ELECTRICAL CHARACTERISTICS**  $V_{CC1} = V_{CC2} = \text{ground}$ ,  $V_{EE} = -5.2V \pm 0.010V$ ,  $T_A = -30^\circ\text{C}$  to  $+85^\circ\text{C}$  output loading  $50\Omega$  to  $-2.0V \pm 0.010V$  unless otherwise specified<sup>1,3</sup>

SYMBOL	PARAMETER	TEST CONDITIONS <sup>2</sup>		LIMITS			UNIT
				MIN.	TYP.	MAX.	
$V_{OH}$	High level output voltage	$T_A = -30^\circ\text{C}$	For $Q_n$ outputs, apply $V_{ILMIN}$ to CP, $S_0$ , and $S_1$ inputs. After applying $V_{IHMAX}$ to all other inputs, change the CP input from $V_{ILMIN}$ to $V_{IHMAX}$ . For $\overline{C}_{OUT}$ , apply $V_{ILMIN}$ to CP, $\overline{C}_{IN}$ , $S_0$ , and $S_1$ inputs. After applying $V_{IHMAX}$ to $D_n$ inputs, change CP from $V_{ILMIN}$ to $V_{IHMAX}$ then change $S_0$ and $\overline{C}_{IN}$ from $V_{ILMIN}$ to $V_{IHMAX}$ .	-1060		-890	mV
		$T_A = +25^\circ\text{C}$		-960		-810	mV
		$T_A = +85^\circ\text{C}$		-890		-700	mV
$V_{OHT}$	High level output threshold voltage	$T_A = -30^\circ\text{C}$	For $Q_0$ output, apply $V_{IHT}$ to $D_0$ input and $V_{ILMIN}$ to CP, $S_0$ , $S_1$ , and $D_1$ , $D_2$ , and $D_3$ . Raise CP from $V_{ILMIN}$ to $V_{IHMAX}$ and measure $Q_0$ . Repeat this process for $Q_1$ , $Q_2$ , and $Q_3$ by applying $V_{IHT}$ to $D_1$ , $D_2$ , and $D_3$ , respectively, one at a time. For $\overline{C}_{OUT}$ , apply $V_{ILMIN}$ to CP, $\overline{C}_{IN}$ , $S_0$ , and $S_1$ inputs. After applying $V_{IHMAX}$ to $D_n$ inputs, change CP from $V_{ILMIN}$ to $V_{IHT}$ , then change $S_0$ and $\overline{C}_{IN}$ from $V_{ILMIN}$ to $V_{IHMAX}$ .	-1080			mV
		$T_A = +25^\circ\text{C}$		-980			mV
		$T_A = +85^\circ\text{C}$		-910			mV
$V_{OLT}$	Low level output threshold voltage	$T_A = -30^\circ\text{C}$	For $Q_n$ outputs, apply $V_{ILMIN}$ to $D_n$ inputs and to CP, $S_0$ , and $S_1$ inputs. Raise CP from $V_{ILMIN}$ to $V_{IHT}$ and measure $Q_n$ outputs. For $\overline{C}_{OUT}$ , apply $V_{ILT}$ to CP, $\overline{C}_{IN}$ , $S_0$ , and $S_1$ inputs. After applying $V_{IHMAX}$ to $D_n$ inputs, change CP from $V_{ILMIN}$ to $V_{IHMAX}$ and measure $\overline{C}_{OUT}$ .			-1655	mV
		$T_A = +25^\circ\text{C}$				-1630	mV
		$T_A = +85^\circ\text{C}$				-1595	mV
$V_{OL}$	Low level output voltage	$T_A = -30^\circ\text{C}$	For $Q_n$ outputs, apply $V_{ILMIN}$ to $D_n$ inputs and to CP, $S_0$ , and $S_1$ inputs. Raise CP from $V_{ILMIN}$ to $V_{IHMAX}$ and measure $Q_n$ outputs. For $\overline{C}_{OUT}$ , apply $V_{ILMIN}$ to CP, $\overline{C}_{IN}$ , $S_0$ , and $S_1$ inputs. After applying $V_{IHMAX}$ to $D_n$ inputs, change CP from $V_{ILMIN}$ to $V_{IHMAX}$ and measure $\overline{C}_{OUT}$ .	-1890		-1675	mV
		$T_A = +25^\circ\text{C}$		-1850		-1650	mV
		$T_A = +85^\circ\text{C}$		-1825		-1615	mV
$I_{IH}$	High level input current	$D_n$ inputs	Apply $V_{IHMAX}$ to each input, under test, one at a time, with $V_{ILMIN}$ applied to all other inputs.	$T_A = -30^\circ\text{C}$		350	$\mu\text{A}$
				$T_A = +25^\circ\text{C}$		220	$\mu\text{A}$
				$T_A = +85^\circ\text{C}$		220	$\mu\text{A}$
		$S_1$ input		$T_A = -30^\circ\text{C}$		425	$\mu\text{A}$
				$T_A = +25^\circ\text{C}$		265	$\mu\text{A}$
				$T_A = +85^\circ\text{C}$		265	$\mu\text{A}$
		$S_0$ input		$T_A = -30^\circ\text{C}$		390	$\mu\text{A}$
				$T_A = +25^\circ\text{C}$		245	$\mu\text{A}$
				$T_A = +85^\circ\text{C}$		245	$\mu\text{A}$
		$\overline{C}_{IN}$ inputs		$T_A = -30^\circ\text{C}$		460	$\mu\text{A}$
				$T_A = +25^\circ\text{C}$		290	$\mu\text{A}$
				$T_A = +85^\circ\text{C}$		290	$\mu\text{A}$
CP input	$T_A = -30^\circ\text{C}$		460	$\mu\text{A}$			
	$T_A = +25^\circ\text{C}$		290	$\mu\text{A}$			
	$T_A = +85^\circ\text{C}$		290	$\mu\text{A}$			

## Universal Counter

10136

## DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>2</sup>		LIMITS			UNIT
				MIN.	TYP.	MAX.	
I <sub>IL</sub>	Low level input current	T <sub>A</sub> = -30°C	Apply V <sub>ILMIN</sub> to each input under test, one at a time, with V <sub>IHMAX</sub> applied to all other inputs.	0.5			μA
		T <sub>A</sub> = +25°C		0.5			μA
		T <sub>A</sub> = +85°C		0.3			μA
-I <sub>EE</sub>	V <sub>EE</sub> supply current	T <sub>A</sub> = -30°C				165	mA
		T <sub>A</sub> = +25°C			120	150	mA
		T <sub>A</sub> = +85°C				165	mA
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	T <sub>A</sub> = +25°C			0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation				0.250		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation				0.148		V/V

## NOTES:

- The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
- Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
- The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

AC ELECTRICAL CHARACTERISTICS V<sub>CC1</sub> = V<sub>CC2</sub> = ground, V<sub>EE</sub> = -5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT	
			T <sub>A</sub> = -30°C		T <sub>A</sub> = +25°C			T <sub>A</sub> = +85°C		
			Min	Max	Min	Typ	Max	Min		Max
f <sub>MAX</sub>	Maximum clock frequency	Waveform 1	125		125	150		125		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub>	Waveform 1, 2, 3	0.80	4.80	1.00	3.30	4.50	1.40	5.00	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to C <sub>OUT</sub>		2.00	10.90	2.50	7.00	10.50	2.50	11.50	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay C <sub>IN</sub> to C <sub>OUT</sub>	Waveform 4	1.60	7.40	1.60	5.00	6.90	1.90	7.50	ns
t <sub>s</sub>	Setup time D <sub>n</sub> to CP		3.50		3.50			3.50		ns
t <sub>h</sub>	Hold time CP to D <sub>n</sub>	Waveform 5	0.00		0.00			0.00		ns
t <sub>s</sub>	Setup time S <sub>n</sub> to CP		7.50		7.50			7.50		ns
t <sub>h</sub>	Hold time CP to S <sub>n</sub>	Waveform 1, 2, 3	-1.00		-1.00			-1.00		ns
t <sub>s</sub>	Setup time C <sub>IN</sub> to CP		4.50		3.70			4.50		ns
t <sub>h</sub>	Hold time CP to C <sub>IN</sub>		-1.00		-1.00			-1.00		ns
t <sub>s</sub>	Setup time CP to C <sub>IN</sub>		-1.00		-1.00			-1.00		ns
t <sub>h</sub>	Hold time C <sub>IN</sub> to CP		4.00		3.10			4.00		ns
t <sub>TLH</sub> t <sub>THL</sub>	Transition time 20% to 80%, 80% to 20%	Waveform 1, 2, 3	0.90	3.30	1.10	2.00	3.30	1.10	3.50	ns
			0.90	3.30	1.10	2.00	3.30	1.10	3.50	ns

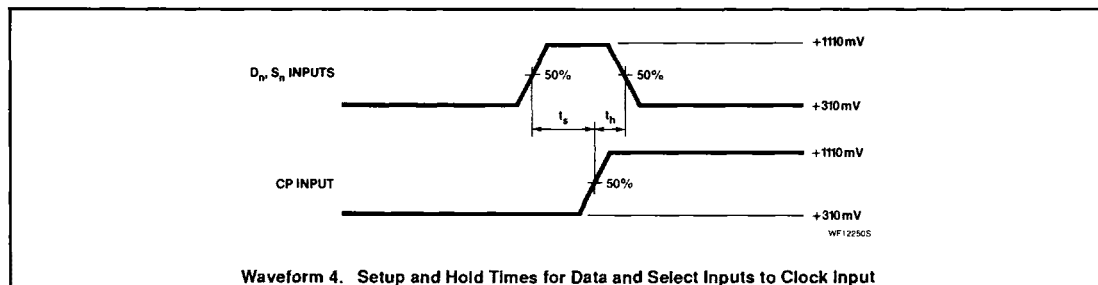
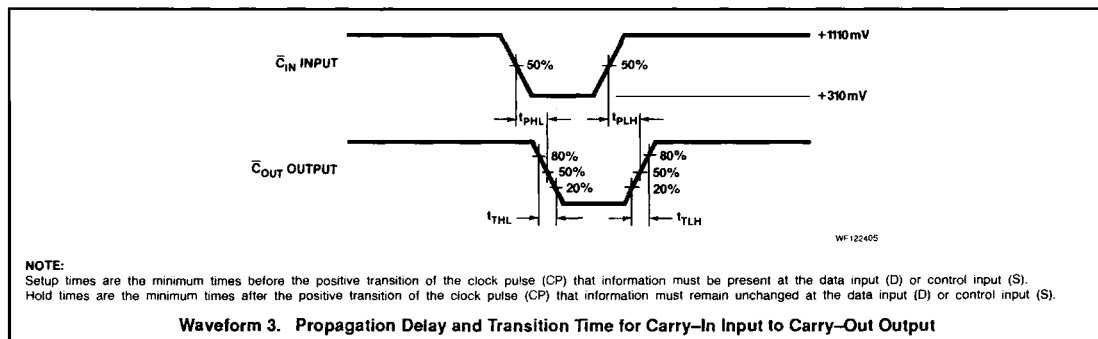
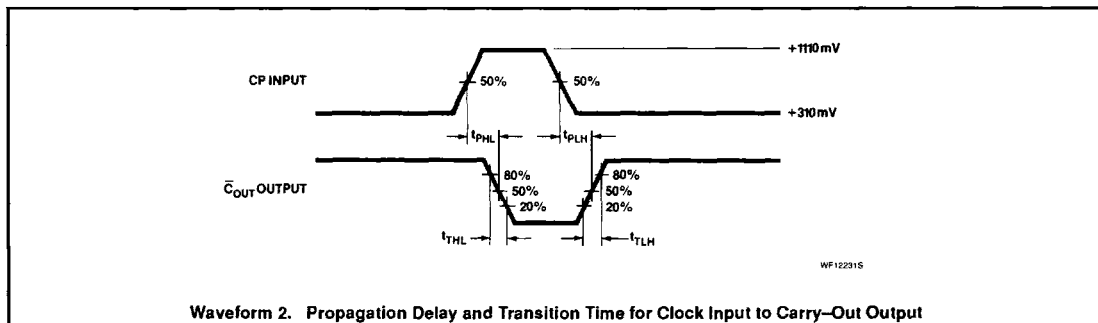
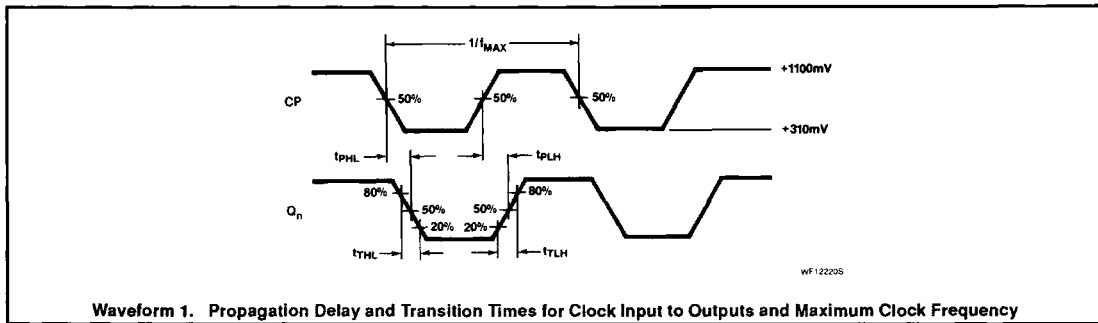
## NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

# Universal Counter

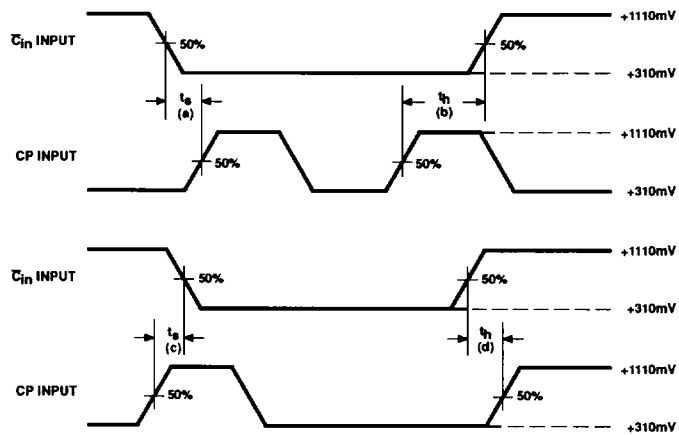
10136

## AC WAVEFORMS



## Universal Counter

10136

**NOTES:**

- (a) is the minimum time to wait to clock the counter after it is enabled.
- (b) is the minimum time that the counter may be clocked before it is disabled.
- (c) is the minimum time that a clock pulse may be applied with no effect on the state of the counter before it is enabled.
- (d) is the minimum time to wait before a clock pulse may be applied with no effect on the state of the counter after it is disabled.
- (b) and (c) may be negative numbers.

**Waveform 5. Setup and Hold Times for  $\overline{C}_{IN}$  to CP**