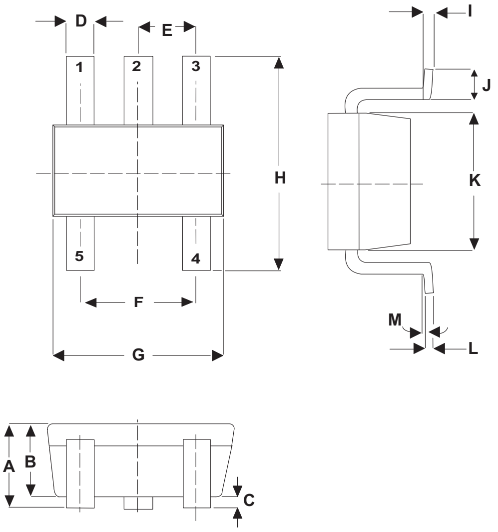
TetraFET

D2090UK.01

METAL GATE RF SILICON FET

MECHANICAL DATA

Dimensions in mm.



SOT–23

PIN 1	SOURCE	PIN 2	DRAIN	PIN 5 GATE
PIN 3	SOURCE	PIN 4	SOURCE	

DIM	Min	Max
A	0.90	1.45
B	0.90	1.30
C	0.00	0.15
D	0.25	0.50
E	0.95 ref	
F	1.90 ref	
G	2.80	3.10
H	2.60	3.00
I	0.20	
J	0.35	0.55
K	1.50	1.75
L	0.09	0.20
M	0°	10°

GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET 750mW – 12V – 1GHz SINGLE ENDED

FEATURES

- **SIMPLIFIED AMPLIFIER DESIGN**
- **SUITABLE FOR BROAD BAND APPLICATIONS**
- **LOW C_{rss}**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE (Typical < 2dB NF)**
- **HIGH GAIN – 11dB MINIMUM**
- **SURFACE MOUNT**

APPLICATIONS

- VHF/UHF COMMUNICATIONS from DC to 2.5 GHz

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

P_D	Power Dissipation	2W
BV_{DSS}	Drain – Source Breakdown Voltage	65V
BV_{GSS}	Gate – Source Breakdown Voltage	±20V
$I_{D(sat)}$	Drain Current	200mA
T_{stg}	Storage Temperature	–65 to 125°C
T_j	Maximum Operating Junction Temperature	150°C

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ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$	$I_D = 10mA$	65			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 28V$	$V_{GS} = 0$			1	mA
I_{GSS}	Gate Leakage Current	$V_{GS} = 20V$	$V_{DS} = 0$			1	µA
$V_{GS(th)}$	Gate Threshold Voltage*	$I_D = 10mA$	$V_{DS} = V_{GS}$	1		7	V
g_{fs}	Forward Transconductance*	$V_{DS} = 10V$	$I_D = 0.2A$	0.18			mhos
G_{PS}	Common Source Power Gain	$P_O = 750mW$		11			dB
η	Drain Efficiency	$V_{DS} = 12V$	$I_{DQ} = 75mA$	40			%
VSWR	Load Mismatch Tolerance	f = 1GHz		10:1			—
C_{iss}	Input Capacitance	$V_{DS} = 0V$ $V_{GS} = -5V$	f = 1MHz			12	pF
C_{oss}	Output Capacitance	$V_{DS} = 28V$ $V_{GS} = 0$	f = 1MHz			6	
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 28V$ $V_{GS} = 0$	f = 1MHz			0.5	

* Pulse Test: Pulse Duration = 300 µs , Duty Cycle ≤ 2%

THERMAL DATA

$R_{THj-case}$	Thermal Resistance Junction – Case	Max. 81°C / W