Standard Products

Preliminary

RadHard-by-Design RHD5950 16-Channel Multiplexed 14-Bit Analog-to-Digital Converter

www.aeroflex.com/RHDseries

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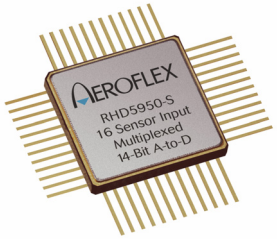


FEATURES

- Single power supply operation 5.0V or Dual power supply for 3.3V I/O
- Radiation performance
  - Total dose: > 1 Mrad(Si); Dose rate = 50 - 300 rads(Si)/s
  - ELDRS Immune
  - SEL Immune > 100 MeV-cm^2/mg
  - Neutron Displacement Damage > 10^{14} neutrons/cm^2
- 16-Channel Input Multiplexer
- Successive Approximation A-to-D
- Level Shifting Digital I/O Receiver/Drivers allow interfaces to 5.0 or 3.3 volt logic
- Tri-State digital outputs
- Power Down (Sleep) mode
- Single or continuous conversion
- 20 clock conversion period
- Multiplexer address is latched on first clock rising edge of a cycle
- Busy (Prime) and End-of-Conversion status outputs
- 2000V Input/Output ESD protection
- Full military temperature range
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic Ceramic
  - 48 leads, 0.700"Sq x 0.125"Ht quad flat pack
  - Weight - 6 grams max

- **Aeroflex Plainview's Radiation Hardness Assurance Plan is DLA Certified to MIL-PRF-38534, Appendix G.**

GENERAL DESCRIPTION

Aeroflex's RHD5950 is a radiation hardened, single supply, 16-Channel Multiplexed Analog-to-Digital converter in a 48-pin Ceramic Quad Flat Package. The RHD5950 design uses specific circuit topology and layout methods to mitigate total ionizing dose effects and single event latchup. These characteristics make the RHD5950 especially suited for the harsh environment encountered in Deep Space missions. It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534 Class K, the RHD5950 is ideal for demanding military and space applications.

ORGANIZATION AND APPLICATION

The RHD5950 takes 16 analog sensor signals and using 4 address inputs and an enable input, selects one of the 16 analog inputs and performs a 14-bit successive approximation analog-to-digital conversion in a nominal period of 40uS. The 14-bit digital output has a tri-state control allowing the connection of multiple RHD5950s. This provides the ability to interface many sensor voltage readings to the digital processor data bus. The full-scale range is determined by reference input voltages which will typically include any ~ 4 volt span anywhere in the power supply range (nominal 5V supply). The input impedance of the reference/span terminals is a constant 4K ohms.

Gain compression will occur near either power supply extremes but can be avoided if the references are more than 200mV away from the respective supply terminals. The input span can be less than 4 volts at the expense of ultimate resolution

The analog channels input impedance is primary capacitance (20pF). The input voltage charges a track-and-hold hold capacitor through transmission gates. The input bandwidth is determined by the slew rate of the hold amplifier and is adequate to allow input sampling in three clock periods (6uS nominal). The ultimate bandwidth is determined by the aperture uncertainty associated with the closing of the sample gate (approximately 5nS). The converter bandwidth is then determined by the sampling Nyquist frequency rather than the input signal; change rate (dv/dt) and the LSB weight in volts as would be the case if there were no sample and hold.

Start-Convert (STCNV_H), Busy (BUSY_L) and End-Of-Convert (EOC_H) status and control line are provided. The converter will operate in either continuous or single conversion modes. To operate in continuous mode, STCNV_H should be tied to BUSY_L. The digital output register changes at the end of a conversion and is available while EOC_H is High. Digital input and output circuits operate from a voltage independent of the remainder of the chip such that I/O is compatible with digital systems from, less than 3.3 volts, to 5 volts.

The converter divides the reference voltage into 16 segments with a linear weighted resistor network. The voltage on any segment is passed to a linear 10-bit DAC for interpolation. The architecture is inherently capable of monotonic operation. INL is ±10 LSBs. DNL is ±1/2 LSB. The sampled input voltage is compared to the output of the two stage DAC for a 14-bit successive approximation conversion.

All inputs are protected to both power supply rails by semiconductor diodes. Inputs should be constrained to Vcc +0.4 and Vee-0.4 to avoid forward biasing protection paths.

The devices will not latch with SEU events to above 100 MeV-cm^2/mg. Total dose degradation is minimal to above 1 Mrad(Si). Displacement damage environments to neutron fluence equivalents in the mid 10^{14} neutrons per cm^2 range are readily tolerated. There is no sensitivity to low-dose rate (ELDRS) effects. SEU effects are application dependent.

Notes: - The STCNV_H is a dynamic input and should not be tied to a static voltage.

- The input signals should be low pass filtered to reduce high frequency noise

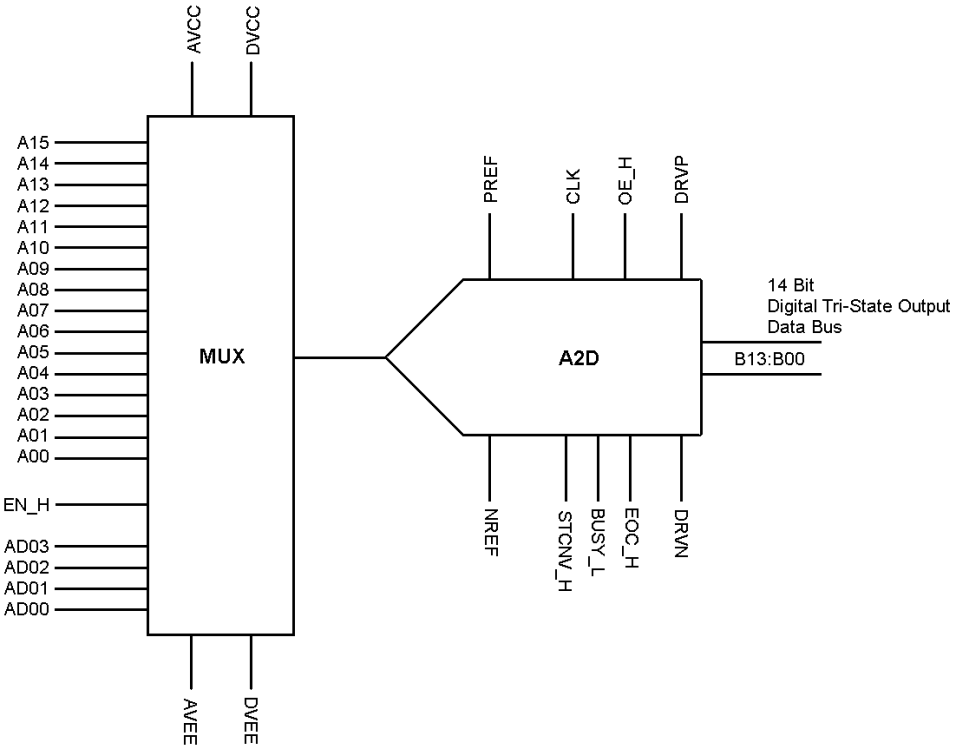


FIGURE 1: BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Junction Temperature	+150	°C
Supply Voltage VCC - VEE	+6.0	V
Input Voltage	VCC +0.4 VEE -0.4	V
Lead Temperature (soldering, 10 seconds)	300	°C
Thermal Resistance, Junction to Case, Θjc	3.5	°C/W
ESD Rating (per MIL-STD-883, Method 3015, Class 2)	2,000 - 3,999	V

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Typical	Units
+AVCC	Analog Power Supply Voltage	5.0	V
+DVCC	Digital Power Supply Voltage	5.0	V
DRVP	Digital Output High Reference Level	3.3 to 5.0	V
DRVN	Digital Output Low Reference Level	0	V

ELECTRICAL PERFORMANCE CHARACTERISTICS 1/

(TC = -55°C TO +125°C, +VCC = +5.0V)

Parameter	Symbol	Conditions	Min	Max	Units
Digital Supply Current Sleep	$D_{ICC}S$			1	mA
Digital Supply Current Active	$D_{ICC}A$			1	mA
Analog Supply Current Sleep	$A_{ICC}S$			2	mA
Analog Supply Current Active	$A_{ICC}A$			10	mA
Digital IO Supply Current Sleep	$DIO_{ICC}S$			1	mA
Digital IO Supply Current Active	$DIO_{ICC}A$			10	mA
Input Leakage Current	ILK			500	pA
Input Range	VIN		1	5	V
Full-scale Input Range			0	PREF - NREF	V
Operating Range			-0.1	PREF - NREF+0.1	V
Input Capacitance 2/	CIN			50	pF
High Analog Reference Current	IPREF			2	mA
High Analog Reference Voltage	VPREF			5	V
Low Analog Reference Voltage	VNREF		1		V
Integral Non Linearity	INL	10 Typical			LSB
Differential Non Linearity	DNL	1.5 Typical			LSB
DC Offset	VOS	PREF-NREF ≥ 4.0V		2	mV
DC Gain	AE	PREF-NREF ≥ 4.0V	0.1		% FSR
Channel Isolation 2/			80		dB
Maximum Sampling Rate	fSAMPLE (MAX)			25	kSPS
Conversion Time 2/	tCONV	16 Typical			Clk Cycles
Clock Frequency	fC			500	KHz

ELECTRICAL PERFORMANCE CHARACTERISTICS 1/ (continued)

(T_C = -55°C TO +125°C, +V_{CC} = +5.0V)

Parameter	Symbol	Conditions	Min	Max	Units
Address Input Voltage $V_{(A0-A3)}$	V_{AHI}		3.5		V
	V_{ALO}			1.5	V
Address Input Current (A0-A3)	I_{AL}	V_A = GND		50	nA
	I_{AH}	V_A = V_{CC}		50	nA
Enable Input Voltage V_{EN}	V_{ENHI}		3.5		V
	V_{ENLO}			1.5	V
Enable Input Current ($\overline{EN}$)	I_{ENL}	V_{EN} =GND		50	nA
	I_{ENH}	V_{EN} =V_{CC}		50	nA
High Input Leakage Current (CH0-CH15)	I_{INLK_5}	Input under test = +5V, V_{EN} = V_{CC},		50	nA
Low Input Leakage Current (CH0-CH15)	I_{INLK_0}	Input under test = 0V, V_{EN} = V_{CC}		50	nA
Multiplexer Settling Time 2/	t_S	A_{0-3}-to-Out & EN-to-Out		200	nS

Notes:

1/ Specification derated to reflect Total Dose exposure to 1 Mrad(Si) @ +25°C.

2/ Not tested. Shall be guaranteed by design, characterization, or correlation to other test parameters.

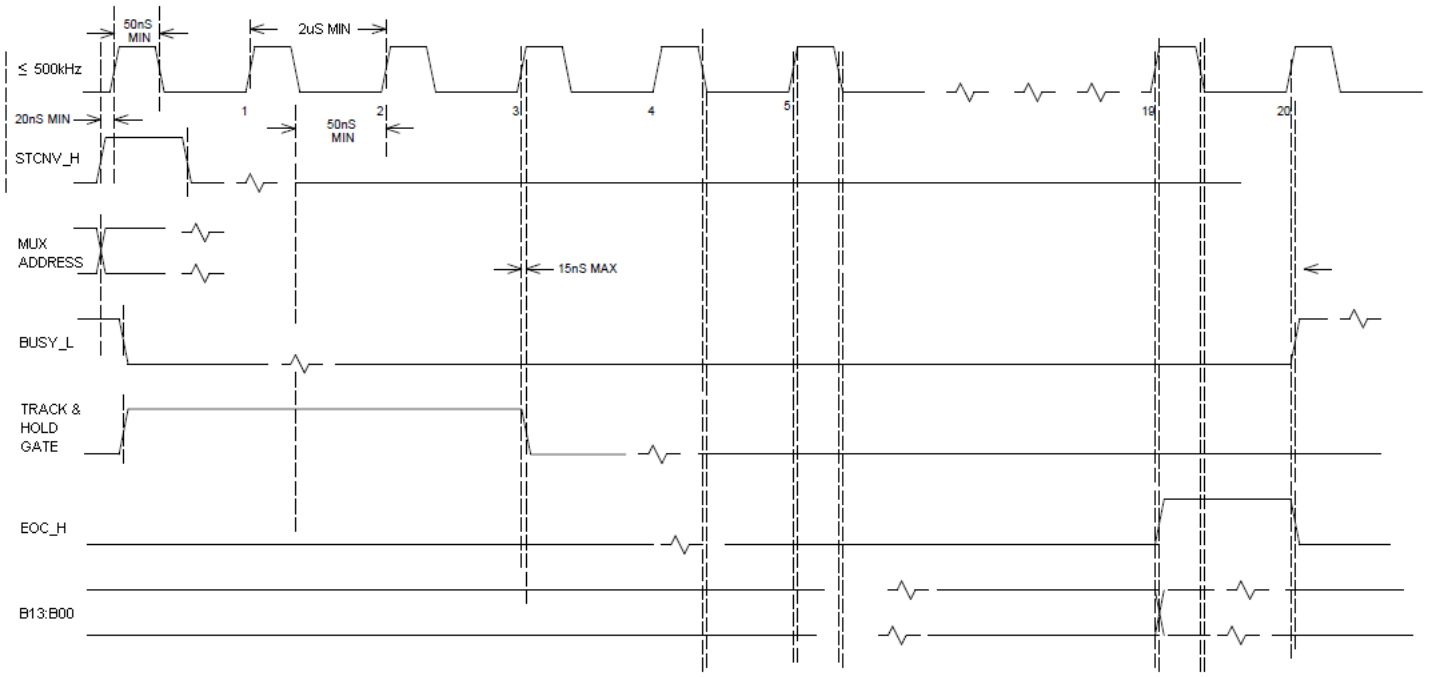


FIGURE 2: BASIC TIMING DIAGRAM

Pin #	Signal	Definition	Pin #	Signal	Definition
1	AIN01	Analog Multiplexer Input 01	25	B11	Digital Output 11
2	AIN00	Analog Multiplexer Input 00	26	B12	Digital Output 12
3	NREF	Low Analog Reference Voltage	27	B13	Digital Output 13
4	AVCC	Analog Supply Voltage	28	EOC_H	End of Convert
5	DVCC	Digital Supply Voltage	29	BUSY_L	Busy
6	AD03	Multiplexer Address 03	30	DRVN	Digital Output Low Reference Level
7	AD02	Multiplexer Address 02	31	DRVP	Digital Output High Reference Level
8	AD01	Multiplexer Address 01	32	DVEE	Digital Supply Return
9	AD00	Multiplexer Address 00	33	AVEE	Analog Supply Return
10	STCNV_H	Start Conversion	34	PREF	High Analog Reference Voltage
11	EN	Multiplexer Enable	35	AIN15	Analog Multiplexer Input 15
12	OE	Output Enable	36	AIN14	Analog Multiplexer Input 14
13	CLK	Clock Input	37	AIN13	Analog Multiplexer Input 13
14	B00	Digital Output 00	38	AIN12	Analog Multiplexer Input 12
15	B01	Digital Output 01	39	AIN11	Analog Multiplexer Input 11
16	B02	Digital Output 02	40	AIN10	Analog Multiplexer Input 10
17	B03	Digital Output 03	41	AIN09	Analog Multiplexer Input 09
18	B04	Digital Output 04	42	AIN08	Analog Multiplexer Input 08
19	B05	Digital Output 05	43	AIN07	Analog Multiplexer Input 07
20	B06	Digital Output 06	44	AIN06	Analog Multiplexer Input 06
21	B07	Digital Output 07	45	AIN05	Analog Multiplexer Input 05
22	B08	Digital Output 08	46	AIN04	Analog Multiplexer Input 04
23	B09	Digital Output 09	47	AIN03	Analog Multiplexer Input 03
24	B10	Digital Output 10	48	AIN02	Analog Multiplexer Input 02

FIGURE 3: PACKAGE PIN-OUT AND SIGNAL DEFINITION

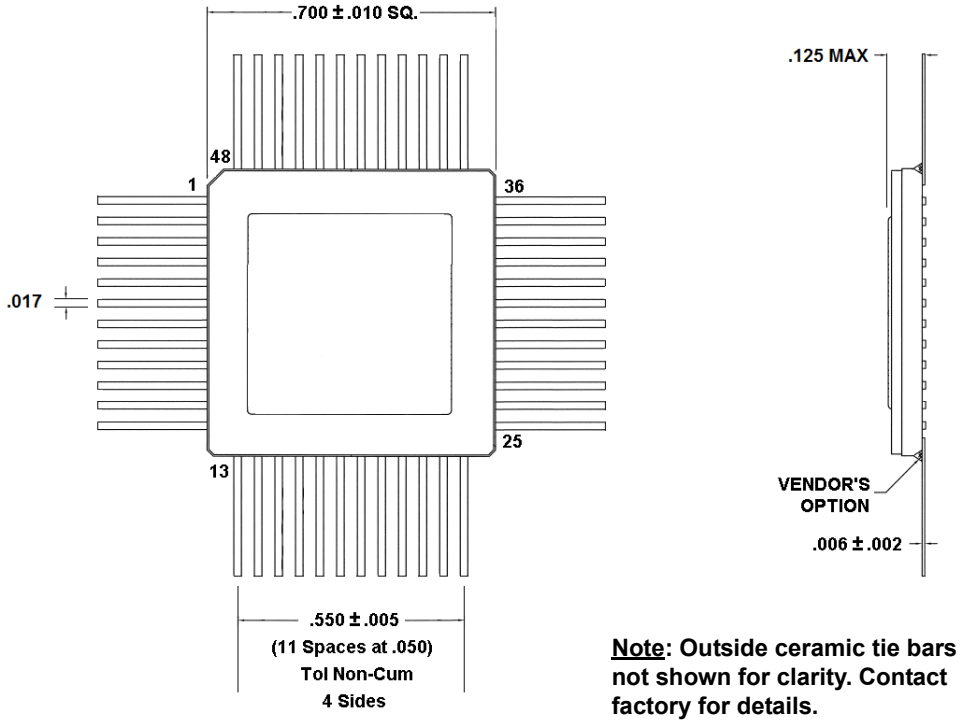
TRUTH TABLE (CH0 – CH15)

A3	A2	A1	A0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	CH0
L	L	L	H	H	CH1
L	L	H	L	H	CH2
L	L	H	H	H	CH3
L	H	L	L	H	CH4
L	H	L	H	H	CH5
L	H	H	L	H	CH6
L	H	H	H	H	CH7
H	L	L	L	H	CH8
H	L	L	H	H	CH9
H	L	H	L	H	CH10
H	L	H	H	H	CH11
H	H	L	L	H	CH12
H	H	L	H	H	CH13
H	H	H	L	H	CH14
H	H	H	H	H	CH15

FIGURE 4: TRUTH TABLE

ORDERING INFORMATION

Model	DLA SMD #	Screening	Package
RHD5950-7	-	Commercial Flow, +25°C testing only	48-lead CQFP
RHD5950-S	-	Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
RHD5950-201-1S	5962-1220301KXC	DLA SMD Pending	
RHD5950-901-1S	5962H1220301KXC	DLA SMD and Radiation Certification Pending	



Note: Outside ceramic tie bars not shown for clarity. Contact factory for details.

FIGURE 4: PACKAGE OUTLINE

EXPORT CONTROL:

This product is controlled for export under the International Traffic in Arms Regulations (ITAR). A license from the U.S. Department of State is required prior to the export of this product from the United States.

EXPORT WARNING:

Aeroflex's military and space products are controlled for export under the International Traffic in Arms Regulations (ITAR) and may not be sold or proposed or offered for sale to certain countries. (See ITAR 126.1 for complete information.)

PLAINVIEW, NEW YORK
Toll Free: 800-THE-1553
Fax: 516-694-6715

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST
Tel: 603-888-3975
Fax: 603-888-4585

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WEST COAST
Tel: 949-362-2260
Fax: 949-362-2266

CENTRAL
Tel: 719-594-8017
Fax: 719-594-8468

www.aeroflex.com info-ams@aeroflex.com

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