# 1.8 pF Passive Tunable Integrated Circuits (PTIC)

*Product Preview*

# TCP-5118XA

### Introduction

ON Semiconductor’s PTICs have excellent RF performance and power consumption, making them suitable for any mobile handset or radio application. The fundamental building block of our PTIC product line is a tunable material called ParaScan™, based on Barium Strontium Titanate (BST). PTICs have the ability to change their capacitance from a supplied bias voltage generated by the Control IC. The 1.8 pF Sub−6GHz PTICs are available as wafer−level chip scale packages (WLCSP).

### Key Features

- High Tuning Range
- High Quality Factor (Q) for Low Loss
- Optimized for Frequency Range from 0.6 – 6.0 GHz
- Compatible with PTIC Control ICs from ON Semiconductor
- These devices are Pb−Free and RoHS Compliant

### Typical Applications

- Tunable Antenna Matching Networks
- 5G Mobile Devices
- LTE Smartphones

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

**ON Semiconductor®**

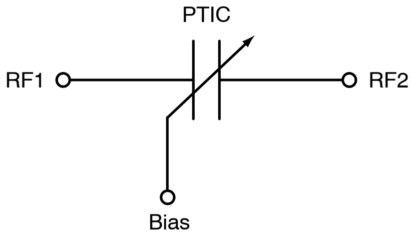
www.onsemi.com

**WLCSP3**
**0.94x0.772**
**CASE 567PE**

### MARKING DIAGRAM

O = Specific Device Code
Y = Year
W = Work Week

### FUNCTIONAL BLOCK DIAGRAM



**PTIC Functional Block Diagram**

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| TCP−5118XA−DT | WLCSP3<br>(Pb−Free) | 4000 Units /<br>7” Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

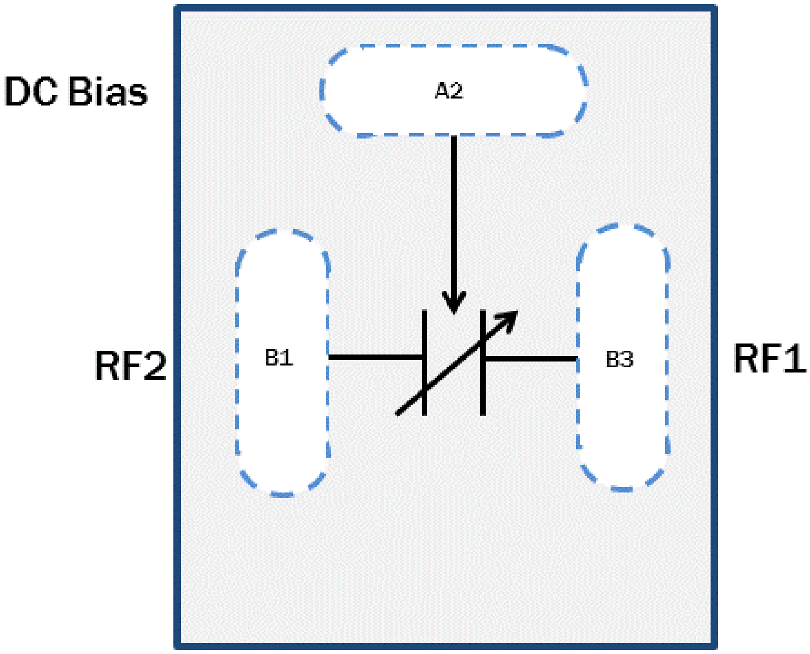


Figure 1. PTIC Functional Block Diagram (Top View)

**Table 1. SIGNAL DESCRIPTIONS**

| Ball / Pad Number | Pin Name | Description |
|---|---|---|
| A2 | DC Bias 1 | DC Bias Voltage |
| B3 | RF1 | RF Input |
| B1 | RF2 | RF Output |

## TYPICAL SPECIFICATIONS

### Representative Performance Data at 25°C

Table 2. PERFORMANCE DATA

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Operating Bias Voltage | 0 | | 12 | V |
| Capacitance ($V_{bias}$ = 1 V) | 1.64 | 1.80 | 1.96 | pF |
| Capacitance ($V_{bias}$ = 12 V) | TBD | 0.63 | TBD | pF |
| Tuning Range (0 V – 12 V) | 3.0 | 3.1 | TBD | |
| Tuning Range (1 V – 12 V) | 2.9 | 3.0 | TBD | |
| Leakage Current ($V_{bias}$ = 12 V) | | | 0.1 | μA |
| Operating Frequency | 0.6 | | 6.0 | GHz |
| Quality Factor @ 1 GHz, 1 V (Note 1) | 50 | 55 | | |
| Quality Factor @ 1 GHz, 12 V (Note 1) | 55 | 60 | | |
| Quality Factor @ 2.7 GHz, 1 V (Note 1) | 30 | 35 | | |
| Quality Factor @ 2.7 GHz, 12 V (Note 1) | 30 | 35 | | |
| Quality Factor @ 3.4 GHz, 1 V (Note 1) | 25 | 30 | | |
| Quality Factor @ 3.4 GHz, 12 V (Note 1) | 15 | 20 | | |
| Quality Factor @ 5.0 GHz, 1 V (Note 1) | 20 | 25 | | |
| Quality Factor @ 5.0 GHz, 12 V (Note 1) | 10 | 15 | | |
| 2nd Harmonic ($V_{bias}$ = 1 V) (Notes 1, 2) | | TBD | | dBm |
| 2nd Harmonic ($V_{bias}$ = 12 V) (Notes 1, 2) | | TBD | | dBm |
| 3rd Harmonic ($V_{bias}$ = 1 V) (Notes 1, 2) | | TBD | | dBm |
| 3rd Harmonic ($V_{bias}$ = 12 V) (Notes 1, 2) | | TBD | | dBm |
| Average Transition Time (Cmin → Cmax) (Notes 1, 3) | | 66 | | μs |
| Average Transition Time (Cmax → Cmin) (Notes 1, 3) | | 48 | | μs |

1. Sample testing only.
2. 850 MHz, Pin +34 dBm, Harmonics are measured in the series configuration in a 50 Ω environment.
3. $RF_{IN}$ and $RF_{OUT}$ are both connected to DC ground. PTIC control IC Turbo Mode is used.

## Representative performance data at 25°C for 1.8 pF WLCSP Package

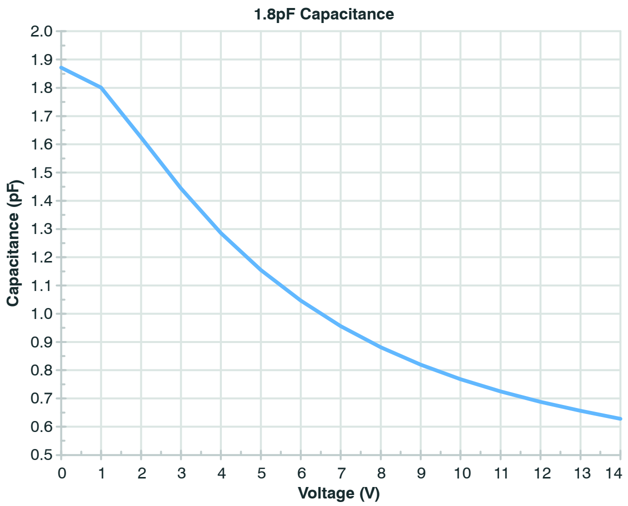


Figure 2. Capacitance

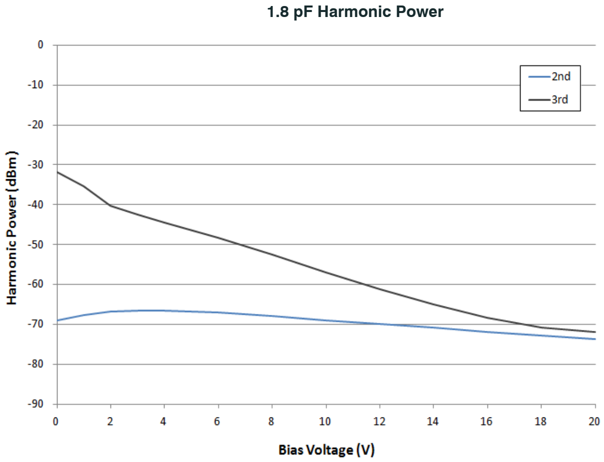


Figure 3. Harmonic Power*

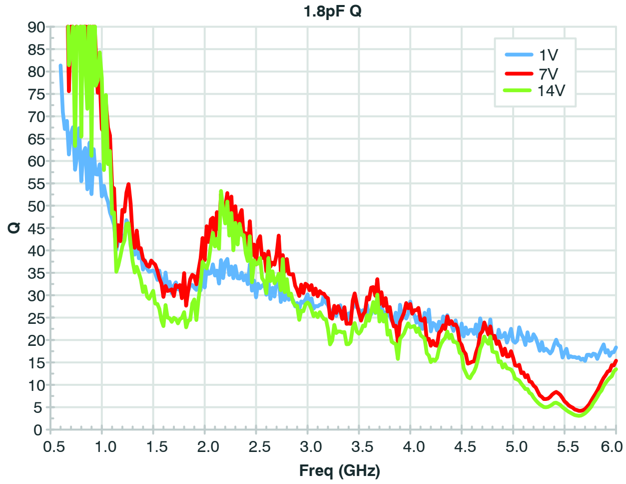


Figure 4. Q*

*Data shown is representative only.

### Table 3. ABSOLUTE MAXIMUM RATINGS

| Parameter | Rating | Units |
|---|---|---|
| Input Power | +40 | dBm |
| Bias Voltage | +20 | V |
| Operating Temperature Range | −30 to +85 | °C |
| Storage Temperature Range | −55 to +125 | °C |
| ESD – Human Body Model | Class 1A JEDEC HBM Standard (Note 4) | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Class 1A defined as passing 250 V, but may fail after exposure to 500 V ESD pulse.

## ASSEMBLY CONSIDERATIONS AND REFLOW PROFILE

The following assembly considerations should be observed:

### Cleanliness

These chips should be handled in a clean environment.

### Electro−static Sensitivity

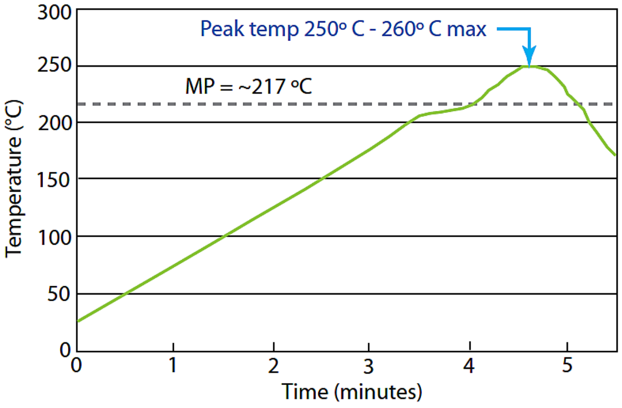
ON Semiconductor's PTICs are ESD Class 1A sensitive. The proper ESD handling procedures should be used.

### Mounting

The WLCSP PTIC is fabricated for Flip Chip solder mounting. Connectivity to the RF and Bias terminations on the PTIC die is established through SAC305 solder balls with 65 μm nominal height (45 μm to 85 μm height variation). The PTIC die is RoHS−compliant and compatible with lead−free soldering profile.

### Molding

The PTIC die is compatible for over−molding or under−fill.



*This reflow profile is a guideline for Pb-free solder materials. Adjustments to this profile are necessary based on specific process requirements and board size, thickness and density.* ***Not to exceed 260° C for 5 seconds.***

**Figure 5. Reflow Profile**

## ORIENTATION OF THE PTIC FOR OPTIMUM LOSSES

When configuring the PTIC in your specific circuit design, at least one of the RF terminals must be connected to DC ground. If minimum transition times are required, DC ground on both RF terminals is recommended. To minimize losses, the PTIC should be oriented such that RF2 is at the lower RF impedance of the two RF nodes. A shunt PTIC, for example, should have RF2 connected to RF ground.

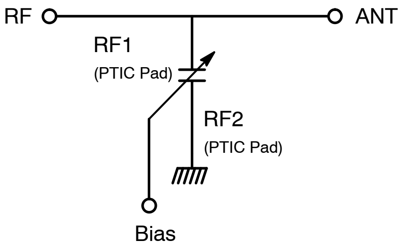


**Figure 6. PTIC Orientation Functional Block Diagram**

## PART NUMBER DEFINITION

**Table 4. PART NUMBERS**

| Part Number | Capacitance | | Marking | | Package* |
|---|---|---|---|---|---|
| | **1 V** | **12 V** | **Device ID** | **Trace Code** | |
| TCP−5118XA−DT | 1.8 | 0.63 | O | YW** | 3−bump WLCSP |

*See PTIC package dimensions on following page.
**Refer to table below (Table 5) for YW trace code.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

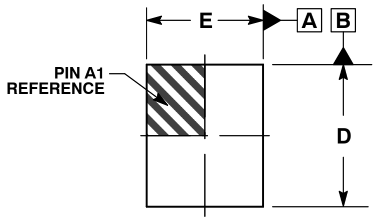
**Table 5. TWO DIGITS YEAR AND WORK WEEK DATE CODING (YW)** − In Process Product / Traceability Date Code Marking

| Code | Term | Definition | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **YW** | **Year and Work Week** | **Two−character Alpha Code. Example: 2005, workweek 10 = GJ** | | | | | | | | |
| | | YEAR | WORK WEEK | CODE | YEAR | WORK WEEK | CODE | YEAR | WORK WEEK | CODE |
| | | 2003 | 1 | CA | 2004 | 1 | EA | 2005 | 1 | GA |
| | | | 26 | CZ | | 26 | EZ | | 26 | GZ |
| | | | 27 | DA | | 27 | FA | | 27 | HA |
| | | | 52 | DZ | | 52 | FZ | | 52 | HZ |
| | | 2006 | 1 | IA | 2007 | 1 | KA | 2008 | 1 | MA |
| | | | 26 | IZ | | 26 | KZ | | 26 | MZ |
| | | | 27 | JA | | 27 | LA | | 27 | NA |
| | | | 52 | JZ | | 52 | LZ | | 52 | NZ |
| | | 2009 | 1 | PA | 2010 | 1 | SA | 2011 | 1 | UA |
| | | | 26 | PZ | | 26 | SZ | | 26 | UZ |
| | | | 27 | RA | | 27 | TA | | 27 | VA |
| | | | 52 | RZ | | 52 | TZ | | 52 | VZ |
| | | 2012 | 1 | WA | 2013 | 1 | YA | 2014 | 1 | AA |
| | | | 26 | WZ | | 26 | YZ | | 26 | AZ |
| | | | 27 | XA | | 27 | ZA | | 27 | BA |
| | | | 52 | XZ | | 52 | ZZ | | 52 | BZ |
| | | 2015 | 1 | CA | 2016 | 1 | EA | 2017 | 1 | GA |
| | | | 26 | CZ | | 26 | EZ | | 26 | GZ |
| | | | 27 | DA | | 27 | FA | | 27 | HA |
| | | | 52 | DZ | | 52 | FZ | | 52 | HZ |

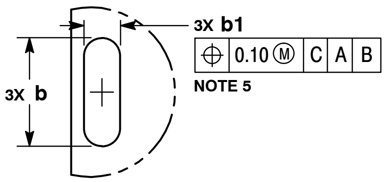
For dates outside of the table: the first character of the code is incremented at the start of workweek 01 and workweek 27 each year. The second character begins with “A” in workweek 01 of each year and increments weekly. “A” follows “Z” to make the code continuous.

## PACKAGE DIMENSIONS

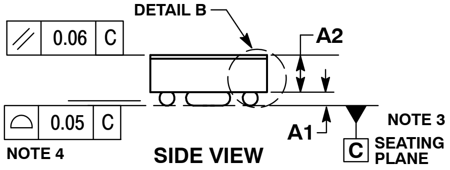
### WLCSP3, 0.94x0.772
CASE 567PE
ISSUE B



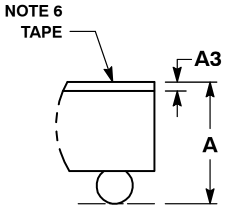
TOP VIEW



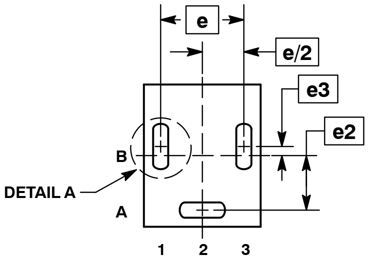
DETAIL A



SIDE VIEW



DETAIL B

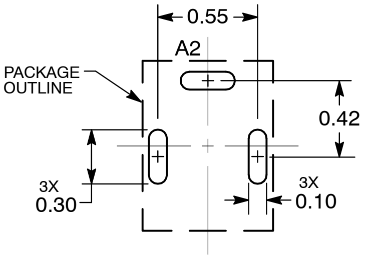


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACTS.
4. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.
5. DIMENSIONS b AND b1 ARE MEASURED AT THE MAXIMUM CONTACT DIAMETER PARALLEL TO DATUM C. POSITIONAL TOLERANCE APPLIES TO ALL THREE CONTACTS IN BOTH THE X AND Y AXIS.
6. BACKSIDE TAPE APPLIED TO IMPROVE PIN 1 MARKING.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.295 | 0.335 | 0.375 |
| A1 | 0.065 | 0.090 | 0.115 |
| A2 | 0.260 REF | | |
| A3 | 0.025 REF | | |
| b | 0.275 | 0.300 | 0.325 |
| b1 | 0.075 | 0.100 | 0.125 |
| D | 0.890 | 0.940 | 0.990 |
| E | 0.722 | 0.772 | 0.822 |
| e | 0.55 BSC | | |
| e2 | 0.35 BSC | | |
| e3 | 0.074 BSC | | |

### RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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