

CMOS LOGIC CIRCUITS

TYPES TF4376B, TP4376B QUAD S-R LATCHES

SEPTEMBER 1976

- Same as TF4043B and TP4043B except with Normal 2-State Totem-Pole Outputs

description

The '4376B is a quadruple S-R latch with normal two-state totem-pole outputs. Each latch has separate active-high set and reset inputs.

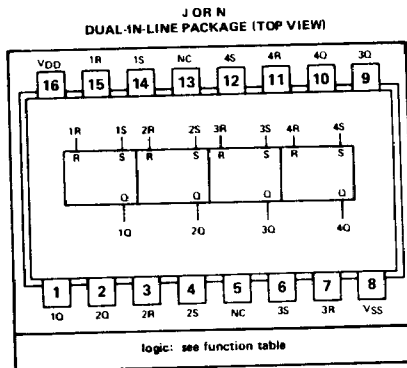
FUNCTION TABLE
(EACH LATCH)

INPUTS		OUTPUT
S	R	Q
L	L	No change
H	L	H
L	H	L
H	H	H*

*This output level is pseudo stable, that is, it may not persist when the S and R inputs return to their inactive (low) level. See explanation of function tables, pages 16 and 17.

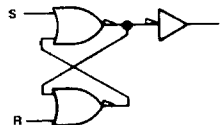
specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
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NC—No internal connection

functional block diagram (each latch)



switching characteristics at 25°C free-air temperature

PARAMETER	TEST CONDITIONS	V _{DD} = 5 V		V _{DD} = 10 V		V _{DD} = 15 V		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	
t _{PLH} Propagation delay time, low-to-high-level output	C _L = 50 pF, R _L = 200 kΩ, See Note 1	165	70	60	25	ns		
t _{PHL} Propagation delay time, high-to-low-level output		165	70	60	25	ns		
t _{TLH} Transition time, low-to-high-level output		85	30	25	ns			
t _{THL} Transition time, high-to-low-level output		85	30	25	ns			
t _{w(min)} Minimum R and S pulse width		80	40	35	ns			

NOTE 1: See load circuit and voltage waveforms on page 170.