TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

512Mbits Network FCRAM1 (SSTL_18 / HSTL_Interface)

– 4,194,304-WORDS × 8 BANKS × 16-BITS

– 8,388,608-WORDS × 8 BANKS × 8-BITS

DESCRIPTION

Network FCRAM™ is Double Data Rate Fast Cycle Random Access Memory. TC59LM914/06AMG is Fast Cycle Random Access Memory (Network FCRAM™) containing 536,870,912 memory cells. TC59LM914AMG is organized as 4,194,304-words × 8 banks × 16 bits, TC59LM906AMG is organized as 8,388,608-words × 8 banks × 8 bits. TC59LM914/06AMG feature a fully synchronous operation referenced to clock edge whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. TC59LM914/06AMG can operate fast core cycle compared with regular DDR SDRAM.

TC59LM914/06AMG is suitable for Network, Server and other applications where large memory density and low power consumption are required. The Output Driver for Network FCRAM™ is capable of high quality fast data transfer under light loading condition.

FEATURES

PARAMETER			TC59LM914/06	
			-37	-50
t_{CK}	Clock Cycle Time (min)	CL = 3	5.5 ns	6.0 ns
		CL = 4	4.5 ns	5.5 ns
		CL = 5	3.75 ns	5.0 ns
t_{RC}	Random Read/Write Cycle Time (min)		22.5 ns	27.5 ns
t_{RAC}	Random Access Time (max)		22.0 ns	24.0 ns
I_{DD1S}	Operating Current (single bank) (max)		280 mA	240 mA
I_{DD2P}	Power Down Current (max)		90 mA	80 mA
I_{DD6}	Self-Refresh Current (max)		20 mA	20 mA

- Fully Synchronous Operation
  - Double Data Rate (DDR)
    Data input/output are synchronized with both edges of DQS.
  - Differential Clock (CLK and $\overline{CLK}$) inputs
    $\overline{CS}$, FN and all address input signals are sampled on the positive edge of CLK.
    Output data (DQs and DQS) is aligned to the crossings of CLK and $\overline{CLK}$.
- Fast clock cycle time of 3.75 ns minimum
  Clock: 266 MHz maximum
  Data: 533 Mbps/pin maximum
- Fast cycle and Short Latency
- Eight independent banks operation
  When BA2 input assign to A14 input, TC59LM914/06AMG can function as 4 bank device
  (Keep backward compatibility to 256Mb)
- Bidirectional differential data strobe signal : TC59LM906AMG
- Bidirectional data strobe signal per byte : TC59LM914AMG
- Distributed Auto-Refresh cycle in 3.9 μs
- Self-Refresh
- Power Down Mode
- Variable Write Length Control
- Write Latency = $\overline{CAS}$ Latency-1
- Programable $\overline{CAS}$ Latency and Burst Length
  $\overline{CAS}$ Latency = 3, 4, 5
  Burst Length = 2, 4
- Organization: TC59LM914AMG : 4,194,304 words × 8 banks × 16 bits
  TC59LM906AMG : 8,388,608 words × 8 banks × 8 bits
- Power Supply Voltage V_{DD}: 2.5 V ± 0.125V
  V_{DDQ}: 1.4 V ~ 1.9 V
- 1.8 V CMOS I/O comply with SSTL_18 and HSTL
- Package: 60Ball BGA, 1mm × 1mm Ball pitch (P–BGA64–1317–1.00AZ)

Notice : FCRAM is trademark of Fujitsu Limited, Japan.

TC59LM906AMG

PIN NAMES

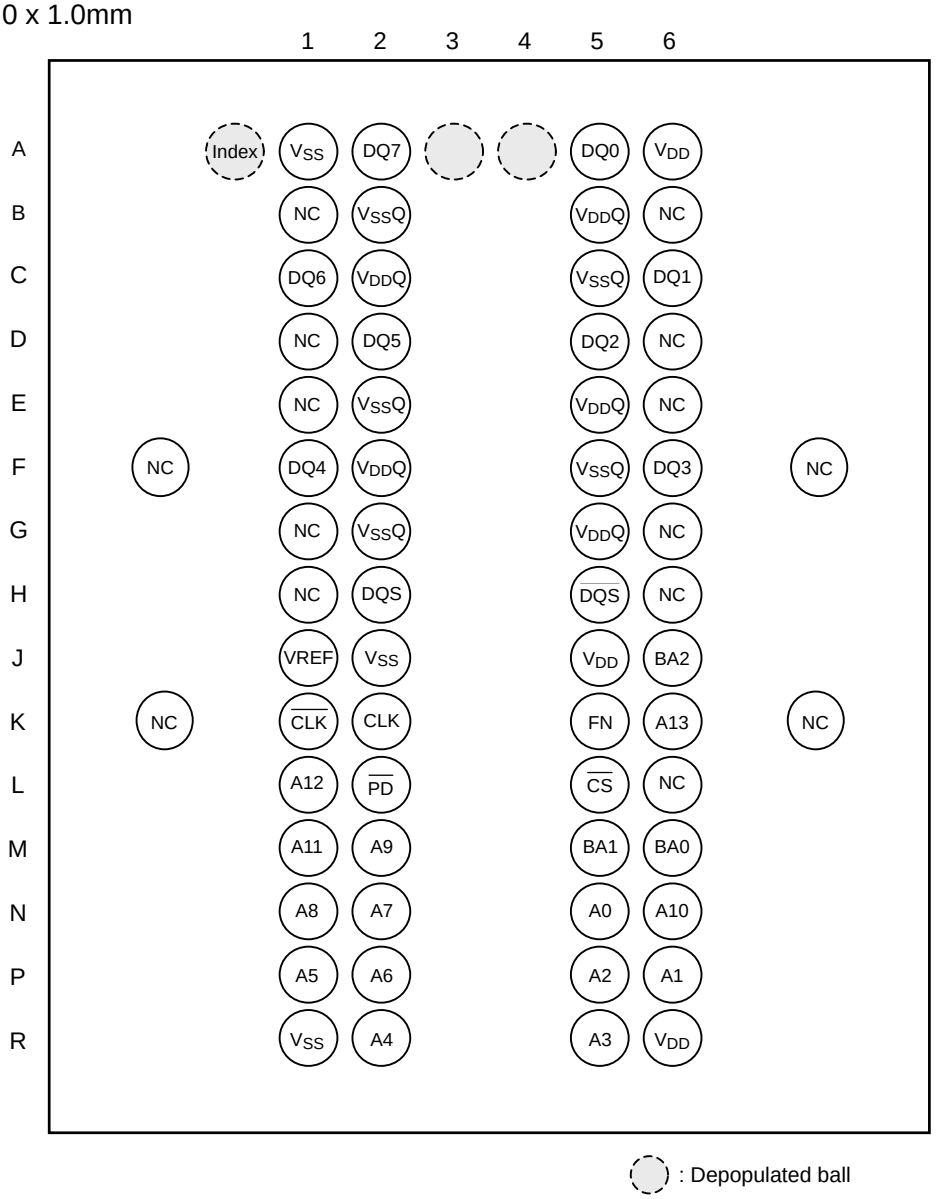
PIN	NAME
A0~A13	Address Input
BA0~BA2	Bank Address
DQ0~DQ7	Data Input / Output
$\overline{CS}$	Chip Select
FN	Function Control
$\overline{PD}$	Power Down Control
CLK, $\overline{CLK}$	Clock Input

PIN	NAME
DQS / $\overline{DQS}$	Write/Read Data Strobe
V_{DD}	Power (+2.5 V)
V_{SS}	Ground
V_{DDQ}	Power (+1.5 V / +1.8 V) (for I/O buffer)
V_{SSQ}	Ground (for I/O buffer)
V_{REF}	Reference Voltage
NC	Not Connected

4 bank operation can be performed using BA2 as A14.

PIN ASSIGNMENT (TOP VIEW)

ball pitch=1.0 x 1.0mm
x 8



: Depopulated ball

TC59LM914AMG

PIN NAMES

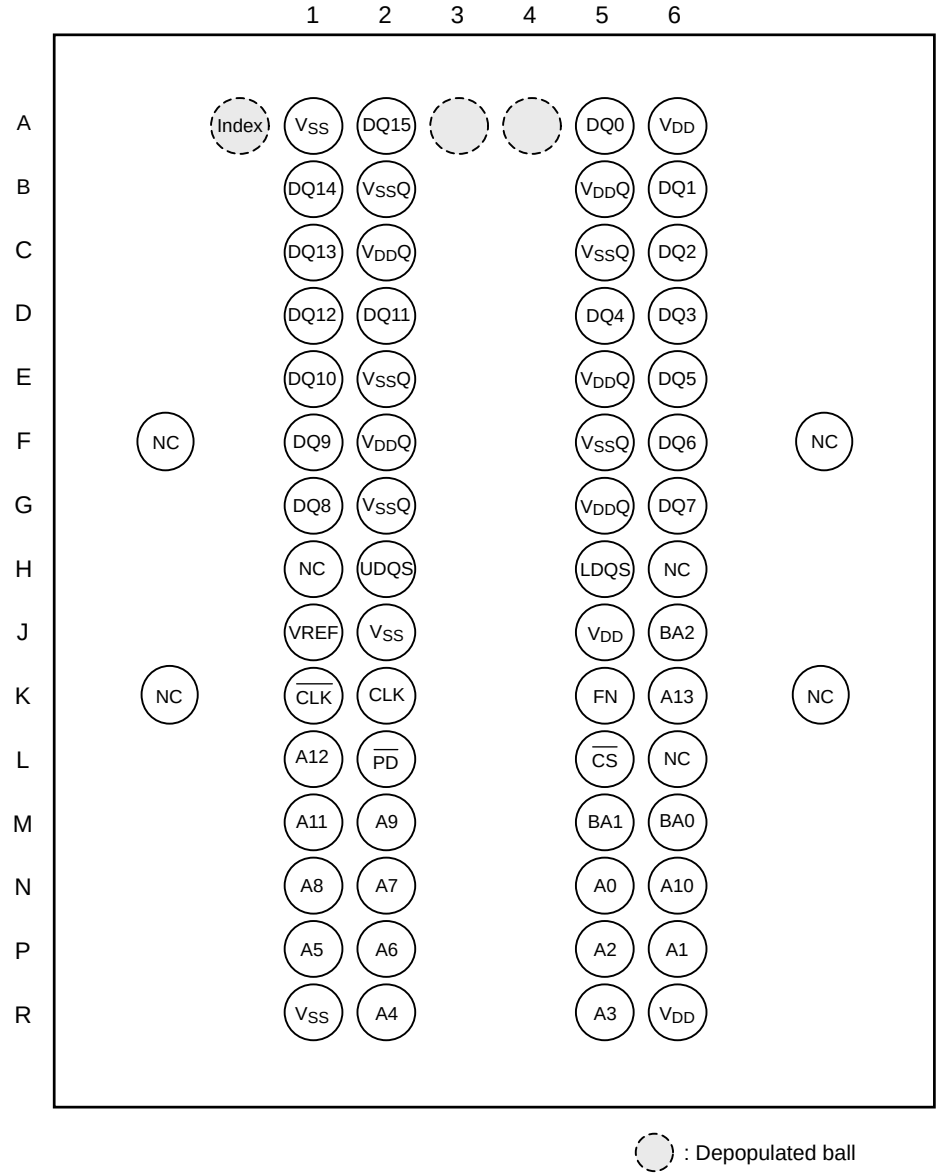
PIN	NAME
A0~A13	Address Input
BA0~BA2	Bank Address
DQ0~DQ15	Data Input / Output
$\overline{CS}$	Chip Select
FN	Function Control
$\overline{PD}$	Power Down Control
CLK, $\overline{CLK}$	Clock Input

PIN	NAME
UDQS/LDQS	Write/Read Data Strobe
V_{DD}	Power (+2.5 V)
V_{SS}	Gorund
V_{DDQ}	Power (+1.5 V / +1.8 V) (for I/O buffer)
V_{SSQ}	Power (for I/O buffer)
V_{REF}	Reference Voltage
NC	Not Conneted

4 bank operation can be performed using BA2 as A14.

PIN ASSIGNMENT (TOP VIEW)

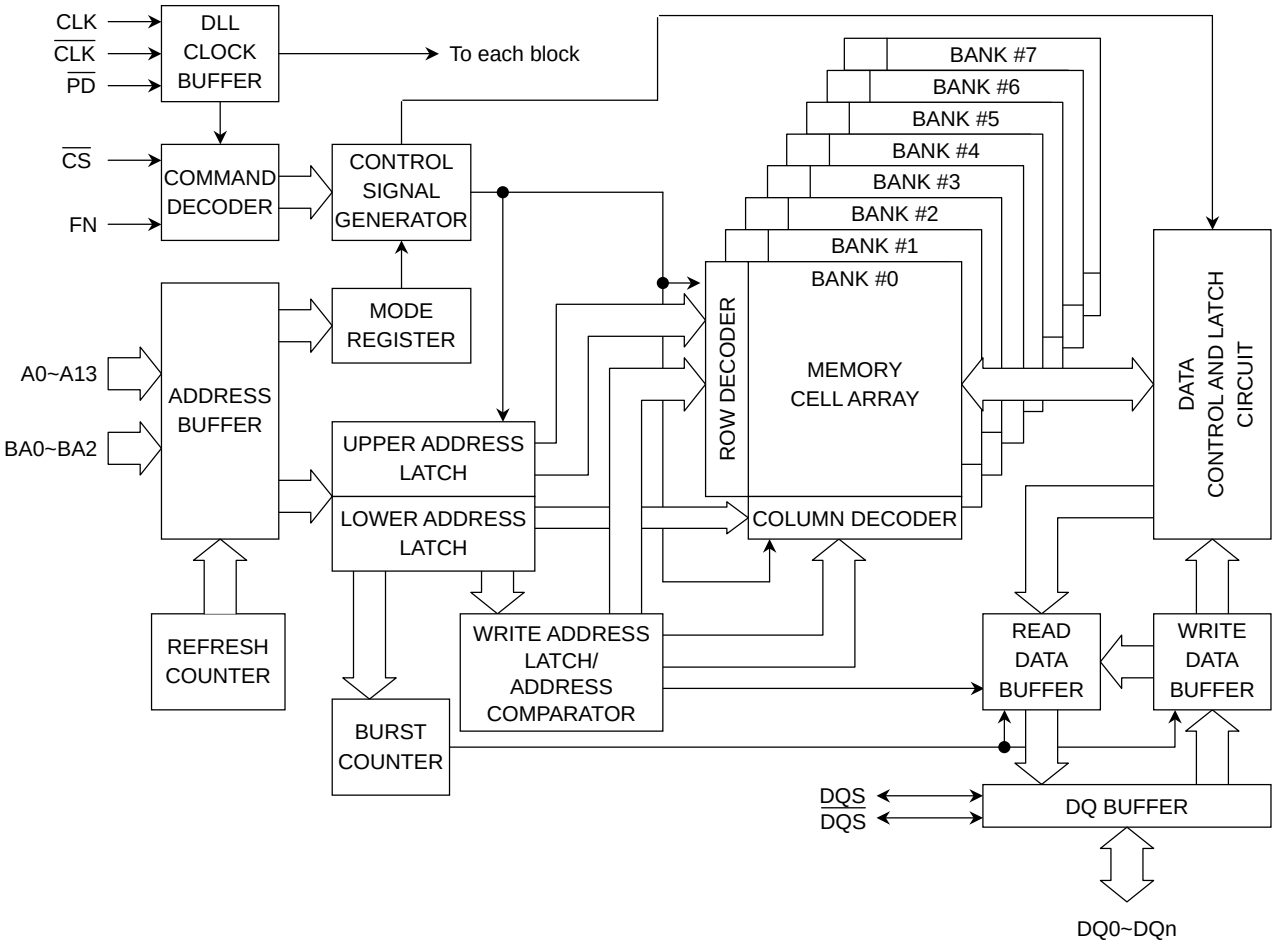
ball pitch=1.0 x 1.0mm
x 16



: Depopulated ball

Rev 1.0

BLOCK DIAGRAM



Note: The TC59LM906AMG configuration is 8 Banks of 16384 × 512 × 8 of cell array with the DQ pins numbered DQ0~DQ7.
The TC59LM914AMG configuration is 8 Banks of 16384 × 256 × 16 of cell array with the DQ pins numbered DQ0~DQ15.
TC59LM906AMG has DQS, $\overline{\text{DQS}}$ pin for Differential Data Strobe.
TC59LM914AMG has UDQS and LDQS.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT	NOTES
V_{DD}	Power Supply Voltage	−0.3~ 3.3	V	
V_{DDQ}	Power Supply Voltage (for I/O buffer)	−0.3~V_{DD}+ 0.3	V	
V_{IN}	Input Voltage	−0.3~V_{DD}+ 0.3	V	
V_{OUT}	Output and I/O pin Voltage	−0.3~V_{DDQ} + 0.3	V	
V_{REF}	Input Reference Voltage	−0.3~V_{DD}+ 0.3	V	
T_{opr}	Operating Temperature (case)	0~85	°C	
T_{stg}	Storage Temperature	−55~150	°C	
T_{solder}	Soldering Temperature (10 s)	260	°C	
P_D	Power Dissipation	2	W	
I_{OUT}	Short Circuit Output Current	±50	mA	

Caution: Conditions outside the limits listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.
Exposure to “ABSOLUTE MAXIMUM RATINGS” conditions for extended periods may affect device reliability.

RECOMMENDED DC, AC OPERATING CONDITIONS (Notes: 1)(T_{CASE} = 0~85°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V_{DD}	Power Supply Voltage	2.375	2.5	2.625	V	
V_{DDQ}	Power Supply Voltage (for I/O buffer)	1.4	—	1.9	V	
V_{REF}	Input Reference Voltage	$V_{DDQ}/2 \times 95\%$	$V_{DDQ}/2$	$V_{DDQ}/2 \times 105\%$	V	2
V_{IH} (DC)	Input DC High Voltage	V_{REF} + 0.125	—	V_{DDQ} + 0.2	V	5
V_{IL} (DC)	Input DC Low Voltage	−0.1	—	V_{REF} − 0.125	V	5
V_{ICK} (DC)	Differential DC Input Voltage	−0.1	—	V_{DDQ} + 0.1	V	10
V_{ID} (DC)	Input DC Differential Voltage.	0.4	—	V_{DDQ} + 0.2	V	7, 10
V_{IH} (AC)	Input AC High Voltage	V_{REF} + 0.2	—	V_{DDQ} + 0.2	V	3, 6
V_{IL} (AC)	Input AC Low Voltage	−0.1	—	V_{REF} − 0.2	V	4, 6
V_{ID} (AC)	Input AC Differential Voltage	0.5	—	V_{DDQ} + 0.2	V	7, 10
V_X (AC)	Differential AC Input Cross Point Voltage	$V_{DDQ}/2$ − 0.125	—	$V_{DDQ}/2$ + 0.125	V	8, 10
V_{ISO} (AC)	Differential AC Middle Level	$V_{DDQ}/2$ − 0.125	—	$V_{DDQ}/2$ + 0.125	V	9, 10

Note:

(1) All voltages referenced to V_{SS}, V_{SSQ}.

(2) V_{REF} is expected to track variations in V_{DDQ} DC level of the transmitting device. Peak to peak AC noise on V_{REF} may not exceed ±2% V_{REF} (DC).

(3) Overshoot limit: $V_{IH\ (max)} = V_{DDQ} + 0.7$ V with a pulse width ≤ 5 ns.

(4) Undershoot limit: $V_{IL\ (min)} = -0.7$ V with a pulse width ≤ 5 ns.

(5) V_{IH} (DC) and V_{IL} (DC) are levels to maintain the current logic state.

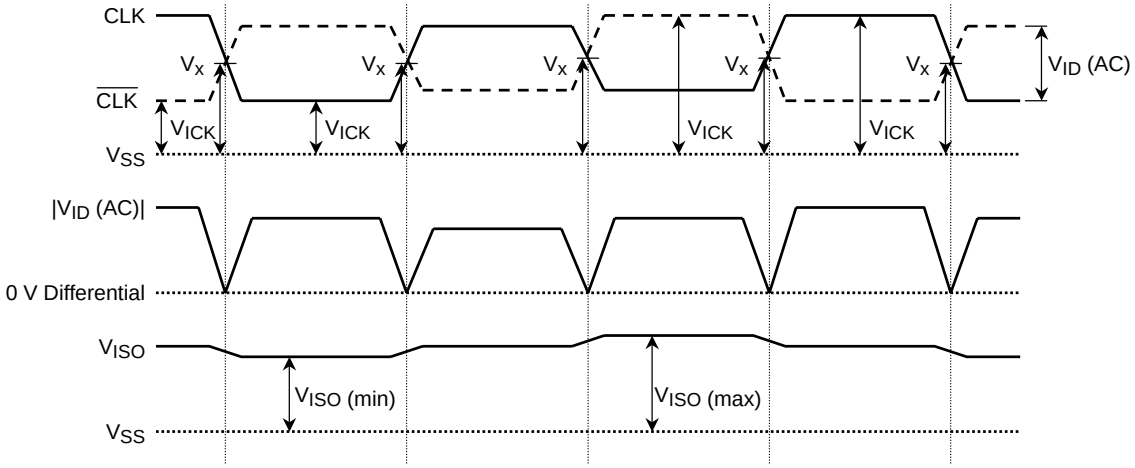
(6) V_{IH} (AC) and V_{IL} (AC) are levels to change to the new logic state.

(7) V_{ID} is magnitude of the difference between V_{TR} input level and V_{CP} input level.

(8) The value of V_X (AC) is expected to equal $V_{DDQ}/2$ of the transmitting device.

(9) V_{ISO} means {V_{ICK} (V_{TR}) + V_{ICK} (V_{CP})} /2.

(10) Refer to the figure below. VTR is the true input (such as CLK, DQS) level and VCP is the complementary input (such as $\overline{\text{CLK}}$, $\overline{\text{DQS}}$) level.



(11) In the case of external termination, VTT (termination voltage) should be gone in the range of V_{REF} (DC) ± 0.04 V.

CAPACITANCE (V_{DD} = 2.5V, V_{DDQ} = 1.8 V, f = 1 MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN	MAX	Delta	UNIT
C_{IN}	Input pin Capacitance	1.5	2.5	0.25	pF
C_{INC}	Clock pin (CLK, $\overline{\text{CLK}}$) Capacitance	1.5	2.5	0.25	pF
$C_{I/O}$	DQ, DQS, UDQS, LDQS, $\overline{\text{DQS}}$ Capacitance	2.5	4	0.5	pF
C_{NC}	NC pin Capacitance	—	4	—	pF

Note: These parameters are periodically sampled and not 100% tested.

RECOMMENDED DC OPERATING CONDITIONS

(V_{DD}=2.5V ± 0.125V, V_{DDQ}=1.4V ~ 1.9V, T_{CASE} = 0~85°C)

SYMBOL	PARAMETER	MAX		UNIT	NOTES
		-37	-50		
I_{DD1S}	Operating Current t_{CK} = min, I_{RC} = min ; Read/Write command cycling ; 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ} ; 1 bank operation, Burst length = 4 ; Address change up to 2 times during minimum I_{RC}.	280	240	mA	1, 2
I_{DD2N}	Standby Current t_{CK} = min, $\overline{CS}$ = V_{IH}, $\overline{PD}$ = V_{IH} ; 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ} ; All banks: inactive state ; Other input signals are changed one time during 4 × t_{CK}.	120	100		1, 2
I_{DD2P}	Standby (Power Down) Current t_{CK} = min, $\overline{CS}$ = V_{IH}, $\overline{PD}$ = V_{IL} (Power Down) ; 0 V ≤ V_{IN} ≤ V_{DDQ} ; All banks: inactive state	90	80		1, 2
I_{DD4W}	Write Operating Current (4 Banks) 8 Bank Interleaved continuos burst wirte operation ; t_{CK} = min, I_{RC} = min Burst Length = 4, $\overline{CAS}$ Latency = 5 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ} ; Address inputs change once per clock cycle ; DQ and DQS inputs change twice per clock cycle.	450	350		1, 2
I_{DD4R}	Read Operating Current (4 Banks) 8 Bank Interleaved continuos burst wirte operation ; t_{CK} = min, I_{RC} = min, I_{OUT} = 0mA ; Burst Length = 4, $\overline{CAS}$ Latency = 5 ; 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ} ; Address inputs change once per clock cycle ; Read data change twice per clock cycle.	450	350		1, 2
I_{DD5B}	Burst Auto Refresh Current Refresh command at every I_{REFC} at interval ; t_{CK} = min、 I_{REFC} = min $\overline{CAS}$ Latency = 5 0 V ≤ V_{IN} ≤ V_{IL} (AC) (max), V_{IH} (AC) (min) ≤ V_{IN} ≤ V_{DDQ} ; Address inputs change up to 2 times during minimum I_{REFC}. DQ and DQS inputs change twice per clock cycle.	280	250		1, 2, 3
I_{DD6}	Self-Refresh Current Self-Refresh mode $\overline{PD}$ = 0.2 V, 0 V ≤ V_{IN} ≤ V_{DDQ}	20	20		2

Notes: 1. These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK}, t_{RC} and I_{RC}.
2. These parameters define the current between V_{DD} and V_{SS}.
3. I_{DD5B} is specified under burst refresh condition. Actual system should use distributed refresh that meet t_{REFI} specification.

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD}=2.5V ± 0.125V, V_{DDQ}=1.4V ~ 1.9V, T_{CASE} = 0~85°C)

SYMBOL	PARAMETER			MIN	MAX	UNIT	NOTES
I_{LI}	Input Leakage Current (0 V ≤ V_{IN} ≤ V_{DDQ}, all other pins not under test = 0 V)			−5	5	μA	
I_{LO}	Output Leakage Current (Output disabled, 0 V ≤ V_{OUT} ≤ V_{DDQ})			−5	5	μA	
I_{REF}	V_{REF} Current			−5	5	μA	
I_{OH} (DC)	Normal Output Driver	Output Source DC Current (V_{DDQ} = 1.7V ~ 1.9V)	V_{OH} = 1.420V	−5.6	—	mA	1
I_{OL} (DC)			V_{OL} = 0.280V	5.6	—		
I_{OH} (DC)	Strong Output Driver		V_{OH} = 1.420V	−9.8	—		
I_{OL} (DC)			V_{OL} = 0.280V	9.8	—		
I_{OH} (DC)	Weak Output Driver		V_{OH} = 1.420V	−2.8	—		
I_{OL} (DC)			V_{OL} = 0.280V	2.8	—		
I_{OH} (DC)	Full Strength Output Driver		V_{OH} = 1.420V	−13.4	—		1, 2
I_{OL} (DC)			V_{OL} = 0.280V	13.4	—		
I_{OH} (DC)	Normal Output Driver	Output Source DC Current (V_{DDQ} = 1.4V ~ 1.6V)	V_{OH} = V_{DDQ}−0.4V	−4	—	mA	1
I_{OL} (DC)			V_{OL} = 0.4V	4	—		
I_{OH} (DC)	Strong Output Driver		V_{OH} = V_{DDQ}−0.4V	−8	—		
I_{OL} (DC)			V_{OL} = 0.4V	8	—		
I_{OH} (DC)	Weak Output Driver		Not defined	—	—		
I_{OL} (DC)			Not defined	—	—		
I_{OH} (DC)	Full Strength Output Driver		V_{OH} = V_{DDQ}−0.4V	−10	—		1, 2
I_{OL} (DC)			V_{OL} = 0.4V	10	—		

Notes: 1. Refer to output driver characteristics for the detail. Output Driver Strength is selected by Extended Mode Register.
2. In case of Full Strength Output Driver, OCD calibration (Off chip Driver impedance adjustment) can be used. The specification of Full Strength Output Driver defines the default value after power-up.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Notes: 1, 2)

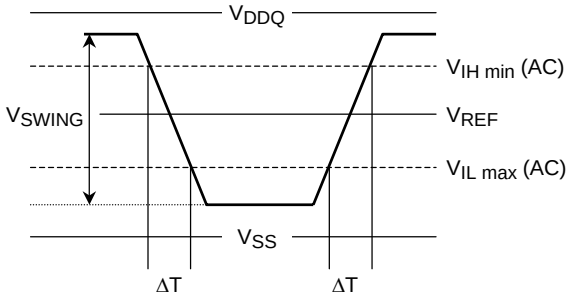
SYMBOL	PARAMETER		-37		-50		UNIT	NOTES
			MIN	MAX	MIN	MAX		
t_{RC}	Random Cycle Time		22.5	—	27.5	—	ns	3
t_{CK}	Clock Cycle Time	$C_L = 3$	5.5	8.5	6.0	8.5		3
		$C_L = 4$	4.5	8.5	5.5	8.5		3
		$C_L = 5$	3.75	8.5	5.0	8.5		3
t_{RAC}	Random Access Time		—	22.0	—	24		3
t_{CH}	Clock High Time		$0.45 \times t_{CK}$	—	$0.45 \times t_{CK}$	—		3
t_{CL}	Clock Low Time		$0.45 \times t_{CK}$	—	$0.45 \times t_{CK}$	—		3
t_{CKQS}	DQS Access Time from CLK		−0.45	0.45	−0.6	0.6		3,8,10
t_{QSQ}	Data Output Skew from DQS		—	0.25	—	0.35		4
t_{AC}	Data Access Time from CLK		−0.5	0.5	−0.65	0.65		3,8,10
t_{OH}	Data Output Hold Time from CLK		−0.5	0.5	−0.65	0.65		3, 8
t_{QSPRE}	DQS (read) Preamble Pulse Width		$0.9 \times t_{CK}$	$1.1 \times t_{CK}$	$0.9 \times t_{CK}$	$1.1 \times t_{CK}$		3, 8
t_{HP}	CLK half period (minimum of Actual t_{CH}, t_{CL})		$\min(t_{CH}, t_{CL})$	—	$\min(t_{CH}, t_{CL})$	—		3
t_{QSP}	DQS (read) Pulse Width		$t_{HP}-t_{QHS}$	—	$t_{HP}-t_{QHS}$	—		4, 8
t_{QSQV}	Data Output Valid Time from DQS		$t_{HP}-t_{QHS}$	—	$t_{HP}-t_{QHS}$	—		4, 8
t_{QHS}	DQ, DQS Hold Skew factor		—	$0.055 \times t_{CK}$ +0.17	—	$0.055 \times t_{CK}$ +0.17		
t_{DQSS}	DQS (write) Low to High Setup Time		$0.75 \times t_{CK}$	$1.25 \times t_{CK}$	$0.75 \times t_{CK}$	$1.25 \times t_{CK}$		3
t_{DSPRE}	DQS (write) Preamble Pulse Width		$0.25 \times t_{CK}$	—	$0.25 \times t_{CK}$	—		4
t_{DSPRES}	DQS First Input Setup Time		0	—	0	—		3
t_{DSPREH}	DQS First Low Input Hold Time		$0.25 \times t_{CK}$	—	$0.25 \times t_{CK}$	—		3
t_{DSP}	DQS High or Low Input Pulse Width		$0.35 \times t_{CK}$	$0.65 \times t_{CK}$	$0.35 \times t_{CK}$	$0.65 \times t_{CK}$		4
t_{DSS}	DQS Input Falling Edge to Clock Setup Time	$C_L = 3$	0.75	—	1.0	—		3, 4
		$C_L = 4$	0.75	—	1.0	—		3, 4
		$C_L = 5$	0.75	—	1.0	—		3, 4
t_{DSH}	DQS Input Falling Edge Hold Time from CLK		0.55	—	0.75	—		3, 4
t_{DSPST}	DQS (write) Postamble Pulse Width		$0.4 \times t_{CK}$	—	$0.4 \times t_{CK}$	—		4
t_{DSPSTH}	DQS (write) Postamble Hold Time	$C_L = 3$	0.75	—	1.0	—		3, 4
		$C_L = 4$	0.75	—	1.0	—		3, 4
		$C_L = 5$	0.75	—	1.0	—		3, 4
t_{DSSK}	UDQS – LDQS Skew (×16)		$-0.5\times t_{CK}$	$0.5\times t_{CK}$	$-0.5\times t_{CK}$	$0.5\times t_{CK}$		
t_{DS}	Data Input Setup Time from DQS		0.35	—	0.45	—		4
t_{DH}	Data Input Hold Time from DQS		0.35	—	0.45	—		4
t_{IS}	Command/Address Input Setup Time		0.5	—	0.7	—		3
t_{IH}	Command/Address Input Hold Time		0.5	—	0.7	—		3

AC CHARACTERISTICS AND OPERATING CONDITIONS (Notes: 1, 2) (continued)

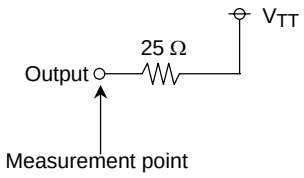
SYMBOL	PARAMETER		-37		-50		UNIT	NOTES
			MIN	MAX	MIN	MAX		
t_{LZ}	Data-out Low Impedance Time from CLK		–0.5	—	–0.65	—		3,6,8
t_{HZ}	Data-out High Impedance Time from CLK		—	0.5	—	0.65		3,7,8
t_{QSLZ}	DQS-out Low Impedance Time from CLK		–0.5	—	–0.65	—		3,6,8
t_{QSHZ}	DQS-out High Impedance Time from CLK		–0.5	0.5	–0.65	0.65		3,7,8
t_{QPDH}	Last output to $\overline{PD}$ High Hold Time		0	—	0	—		
t_{PDEX}	Power Down Exit Time		0.6	—	0.8	—	ns	3
t_T	Input Transition Time		0.1	1	0.1	1		
t_{FPDL}	$\overline{PD}$ Low Input Window for Self-Refresh Entry		$-0.5 \times t_{CK}$	5	$-0.5 \times t_{CK}$	5		3
t_{OIT}	OCD drive mode output delay time		0	12	0	12		
t_{REFI}	Auto-Refresh Average Interval		0.4	3.9	0.4	3.9	µs	5
t_{PAUSE}	Pause Time after Power-up		200	—	200	—		
I_{RC}	Random Read/Write Cycle Time (applicable to same bank)	$C_L = 3$	5	—	5	—		
		$C_L = 4$	5	—	5	—		
		$C_L = 5$	6	—	6	—		
I_{RCD}	RDA/WRA to LAL Command Input Delay (applicable to same bank)		1	1	1	1		
I_{RAS}	LAL to RDA/WRA Command Input Delay (applicable to same bank)	$C_L = 3$	4	—	4	—		
		$C_L = 4$	4	—	4	—		
		$C_L = 5$	5	—	5	—		
I_{RBD}	Random Bank Access Delay (applicable to other bank)		2	—	2	—		
I_{RWD}	LAL following RDA to WRA Delay (applicable to other bank)	$B_L = 2$	2	—	2	—		
		$B_L = 4$	3	—	3	—		
I_{WRD}	LAL following WRA to RDA Delay (applicable to other bank)		1	—	1	—		
I_{RSC}	Mode Register Set Cycle Time	$C_L = 3$	5	—	5	—	cycle	
		$C_L = 4$	5	—	5	—		
		$C_L = 5$	6	—	6	—		
I_{PD}	$\overline{PD}$ Low to Inactive State of Input Buffer		—	1	—	1		
I_{PDA}	$\overline{PD}$ High to Active State of Input Buffer		—	1	—	1		
I_{PDV}	Power down mode valid from REF command	$C_L = 3$	15	—	15	—		
		$C_L = 4$	18	—	18	—		
		$C_L = 5$	22	—	22	—		
I_{REFC}	Auto-Refresh Cycle Time	$C_L = 3$	15	—	15	—		
		$C_L = 4$	18	—	18	—		
		$C_L = 5$	22	—	22	—		
I_{CKD}	REF Command to Clock Input Disable at Self-Refresh Entry		I_{REFC}	—	I_{REFC}	—		
I_{LOCK}	DLL Lock-on Time (applicable to RDA command)		200	—	200	—		

AC TEST CONDITIONS

SYMBOL	PARAMETER	VALUE	UNIT	NOTES
$V_{IH\ (min)}$	Input High Voltage (minimum)	V_{REF} + 0.2	V	
$V_{IL\ (max)}$	Input Low Voltage (maximum)	V_{REF} – 0.2	V	
V_{REF}	Input Reference Voltage	$V_{DDQ}/2$	V	
V_{TT}	Termination Voltage	V_{REF}	V	
V_{SWING}	Input Signal Peak to Peak Swing	0.7	V	
Vr	Differential Clock Input Reference Level	V_X (AC)	V	
V_{ID} (AC)	Input Differential Voltage	1.0	V	
SLEW	Input Signal Minimum Slew Rate	2.5	V/ns	
V_{OTR}	Output Timing Measurement Reference Voltage	$V_{DDQ}/2$	V	9



SLEW = ($V_{IH\ min}$ (AC) – $V_{IL\ max}$ (AC))/ΔT



AC Test Load

Note:

(1) Transition times are measured between $V_{IH\ min}$ (DC) and $V_{IL\ max}$ (DC).
Transition (rise and fall) of input signals have a fixed slope.

(2) If the result of nominal calculation with regard to t_{CK} contains more than one decimal place, the result is rounded up to the nearest decimal place.
(i.e., $t_{DQSS} = 0.75 \times t_{CK}$, t_{CK} = 5 ns, 0.75 × 5 ns = 3.75 ns is rounded up to 3.8 ns.)

(3) These parameters are measured from the differential clock (CLK and $\overline{CLK}$) AC cross point.

(4) These parameters are measured from signal transition point of DQS crossing V_{REF} level.
In case of $\overline{DQS}$ enable mode, these parameters are measured from the crossing point of DQS and $\overline{DQS}$.

(5) The $t_{REFI\ (max)}$ applies to equally distributed refresh method.
The $t_{REFI\ (min)}$ applies to both burst refresh method and distributed refresh method.
In such case, the average interval of eight consecutive Auto-Refresh commands has to be more than 400 ns always. In other words, the number of Auto-Refresh cycles which can be performed within 3.2 μs (8 × 400 ns) is to 8 times in the maximum.

(6) Low Impedance State is specified at $V_{DDQ}/2 \pm 0.2$ V from steady state.

(7) High Impedance State is specified where output buffer is no longer driven.

(8) These parameters depend on the clock jitter. These parameters are measured at stable clock.

(9) Output timing is measured by using Normal driver strength at V_{DDQ} = 1.7V~1.9V.
Output timing is measured by using Strong driver strength at V_{DDQ} = 1.4V~1.6V.

(10) These parameters are measured at t_{CK} = minimum~6.0ns. When t_{CK} is longer than 6.0ns, these parameters are specified as below for all Speed version

t_{CKQS} (MIN/MAX) = –0.6ns / 0.6ns, t_{AC} (MIN/MAX) = –0.65ns / 0.65ns

POWER UP SEQUENCE

(1) As for $\overline{PD}$, being maintained by the low state (≤ 0.2 V) is desirable before a power-supply injection.

(2) Apply V_{DD} before or at the same time as V_{DDQ}.

(3) Apply V_{DDQ} before or at the same time as V_{REF}.

(4) Start clock (CLK, $\overline{CLK}$) and maintain stable condition for 200 μs (min).

(5) After stable power and clock, apply DESL and take $\overline{PD}$ =H.

(6) Issue EMRS to enable DLL and to define driver strength with OCD calibration mode exit command (A7~A9=0). (Note: 1, 2)

(7) Issue MRS for set $\overline{CAS}$ latency (CL), Burst Type (BT), and Burst Length (BL). (Note: 1)

(8) Issue two or more Auto-Refresh commands (Note: 1).

(9) Ready for normal operation after 200 clocks from Extended Mode Register programming.

(10) If OCD calibration (Off Chip Driver impedance adjustment) is used, execute OCD calibration sequence.

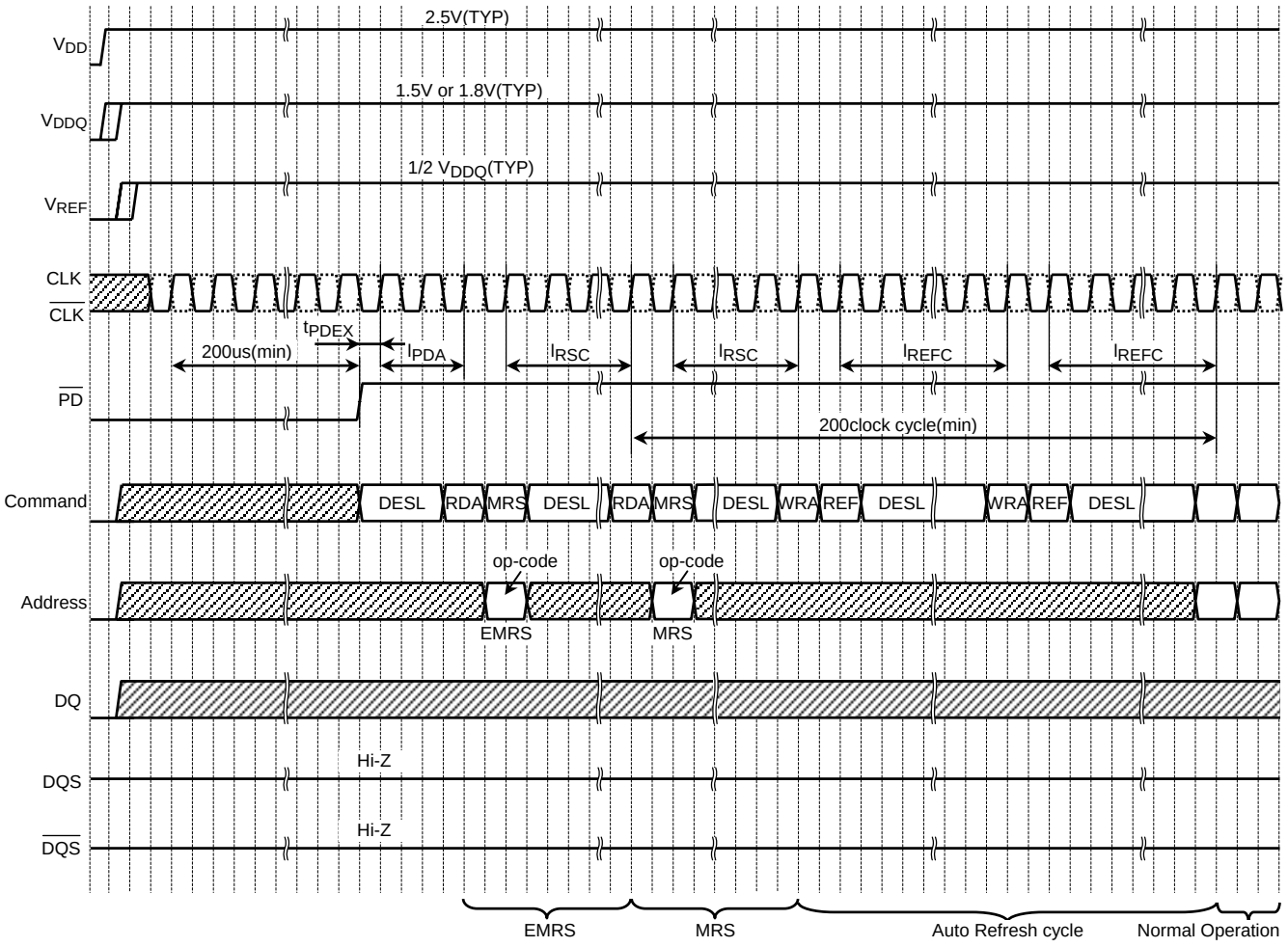
Notes:

(1) Sequence 6, 7 and 8 can be issued in random order.

(2) Set $\overline{DQS}$ mode for TC59LM906AMG.

(3) L = Logic Low, H = Logic High

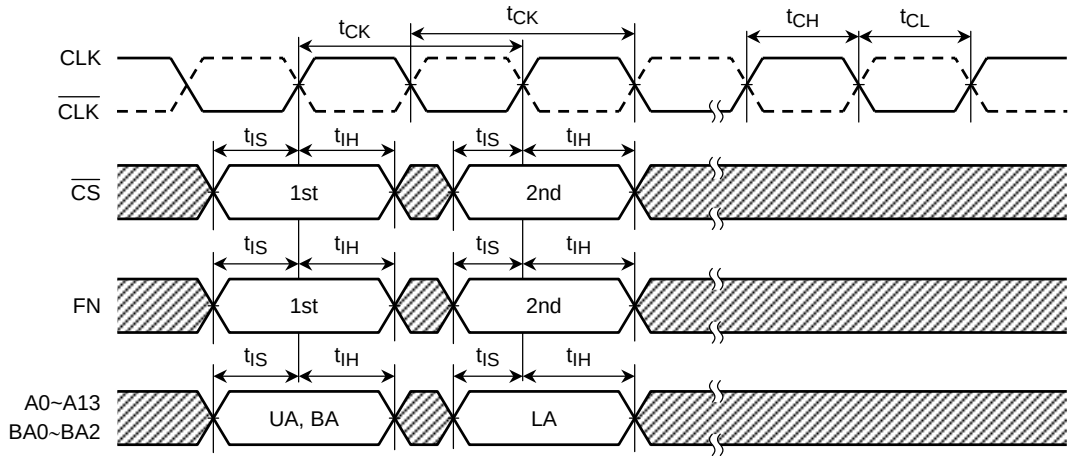
(4) All DQs output level are high impedance state during power up sequence.



TIMING DIAGRAMS

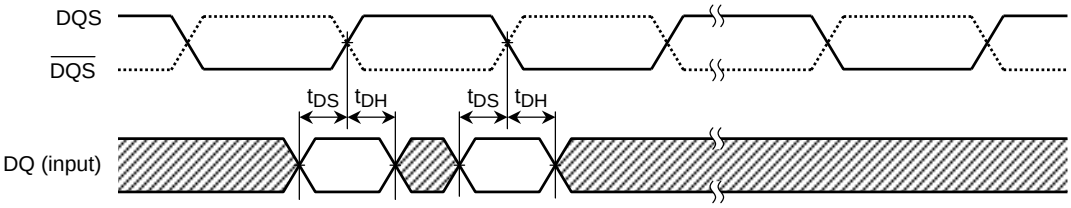
Input Timing

Command and Address



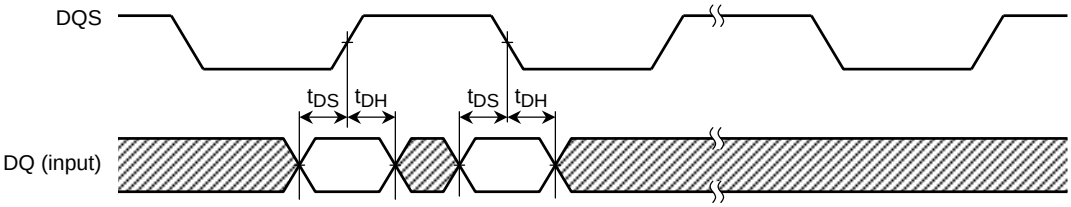
Data

- TC59LM906AMG $\overline{DQS}$ enable mode



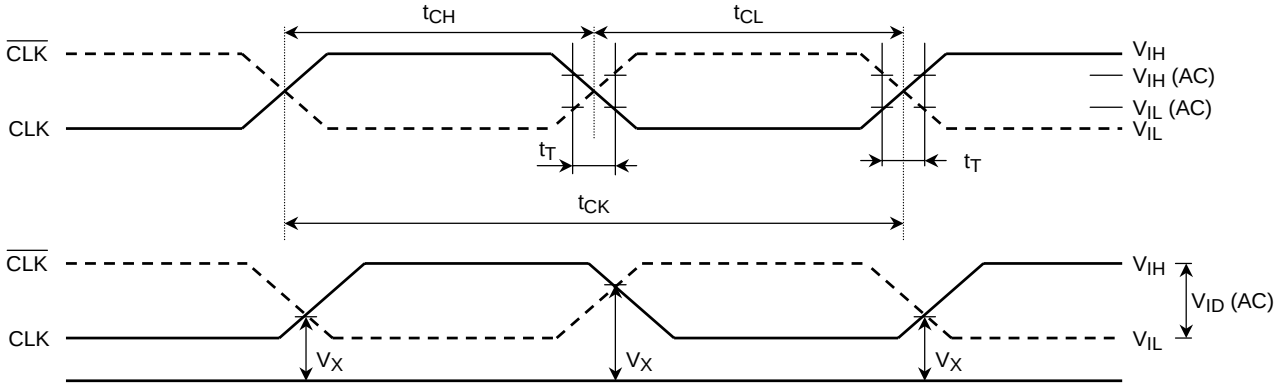
Data

- TC59LM906AMG $\overline{DQS}$ disable mode
- TC59LM914AMG

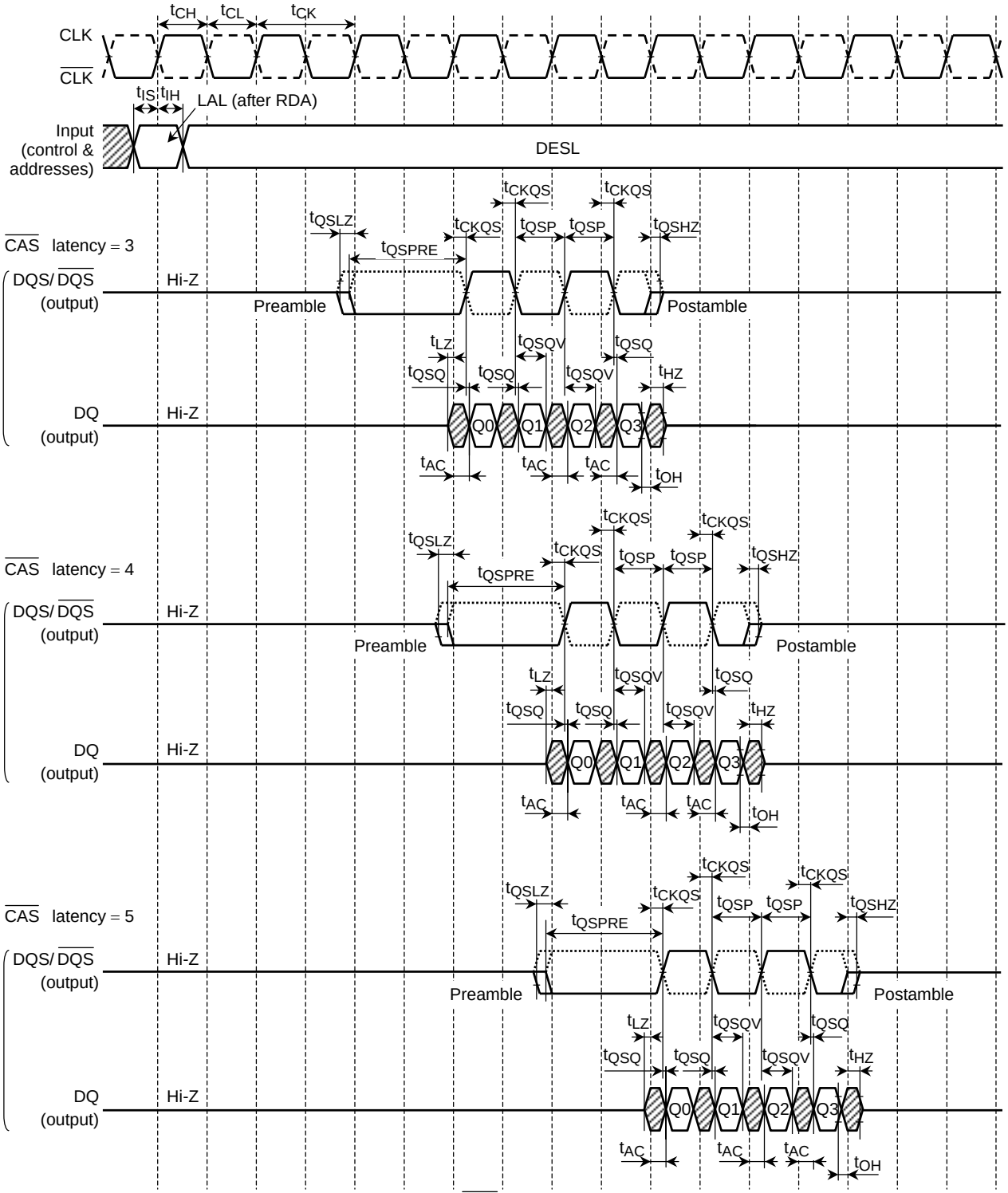


Refer to the Command Truth Table.

Timing of the CLK, $\overline{CLK}$



Read Timing (Burst Length = 4)



Note: TC59LM914AMG doesn't have $\overline{DQS}$.

The correspondence of LDQS, UDQS to DQ. (TC59LM914AMG)

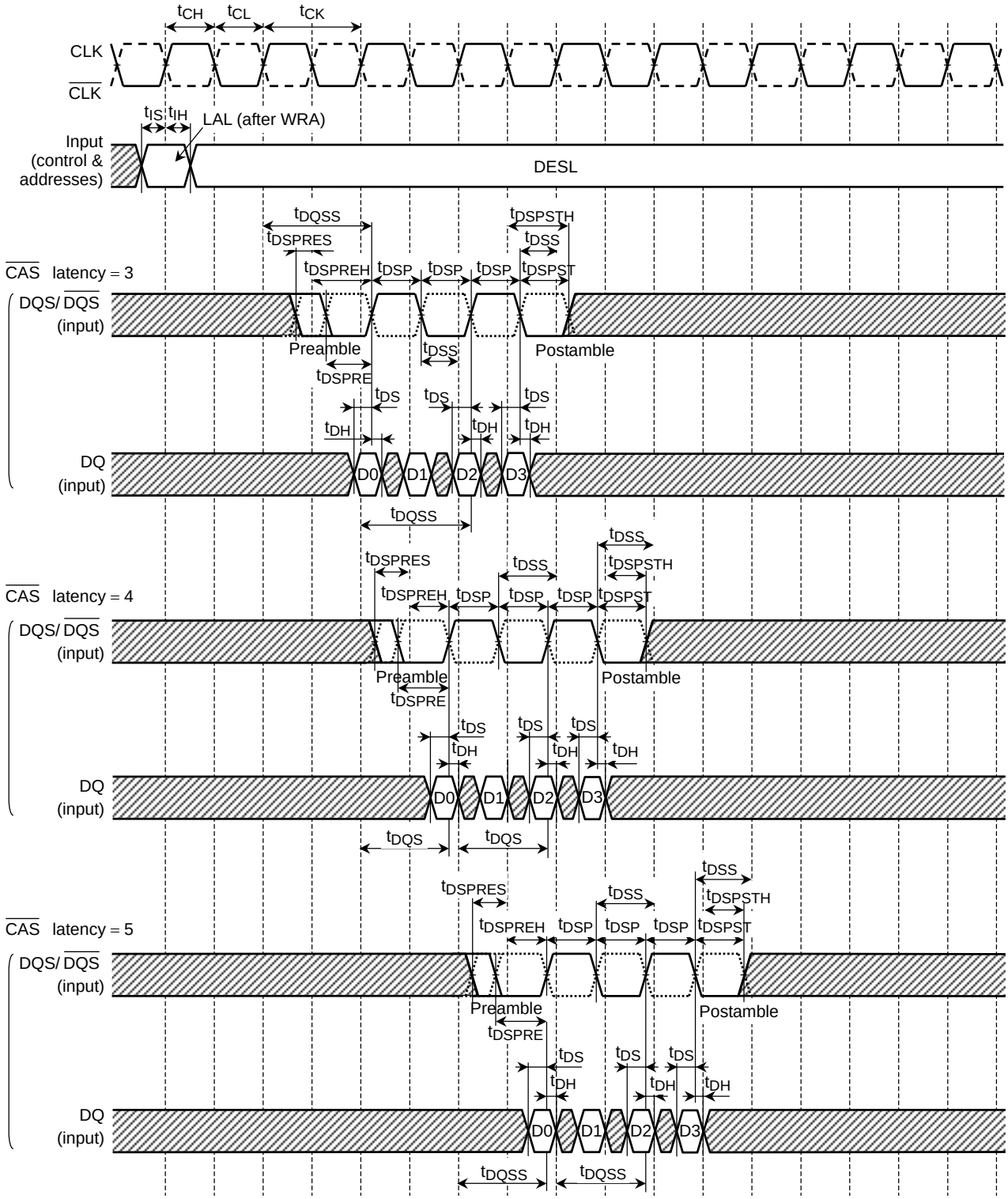
LDQS	DQ0~DQ7
UDQS	DQ8~DQ15

$\overline{DQS}$ is Hi-Z in $\overline{DQS}$ disable mode.

$\overline{DQS}$ mode is chosen by EMRS. (TC59LM906AMG)

When $\overline{DQS}$ is enable, the condition of $\overline{DQS}$ is changed from Hi-Z to "High at Preamble and the condition of $\overline{DQS}$ is changed from "High" to Hi-Z at Postamble.

Write Timing (Burst Length = 4)



Note: TC59LM914AMG doesn't have $\overline{DQS}$.

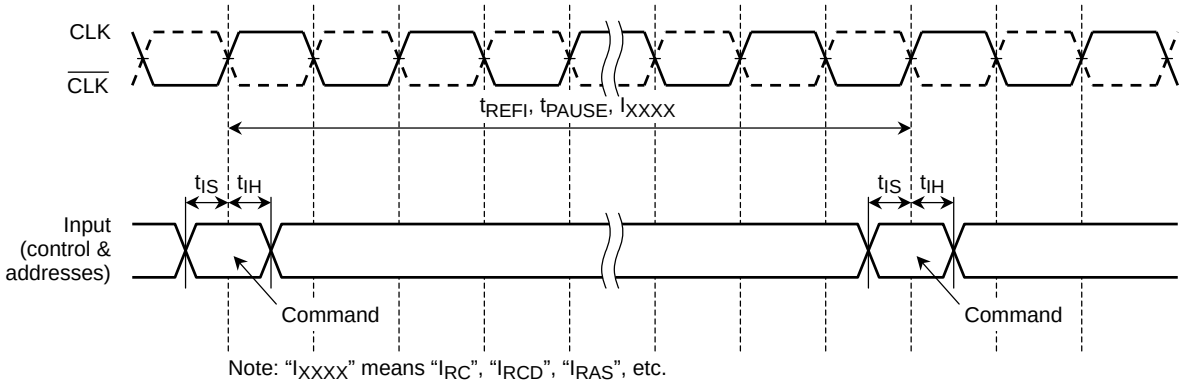
The correspondence of LDQS, UDQS to DQ. (TC59LM914AMG)

LDQS	DQ0~DQ7
UDQS	DQ8~DQ15

$\overline{DQS}$ is ignored in $\overline{DQS}$ disable mode.

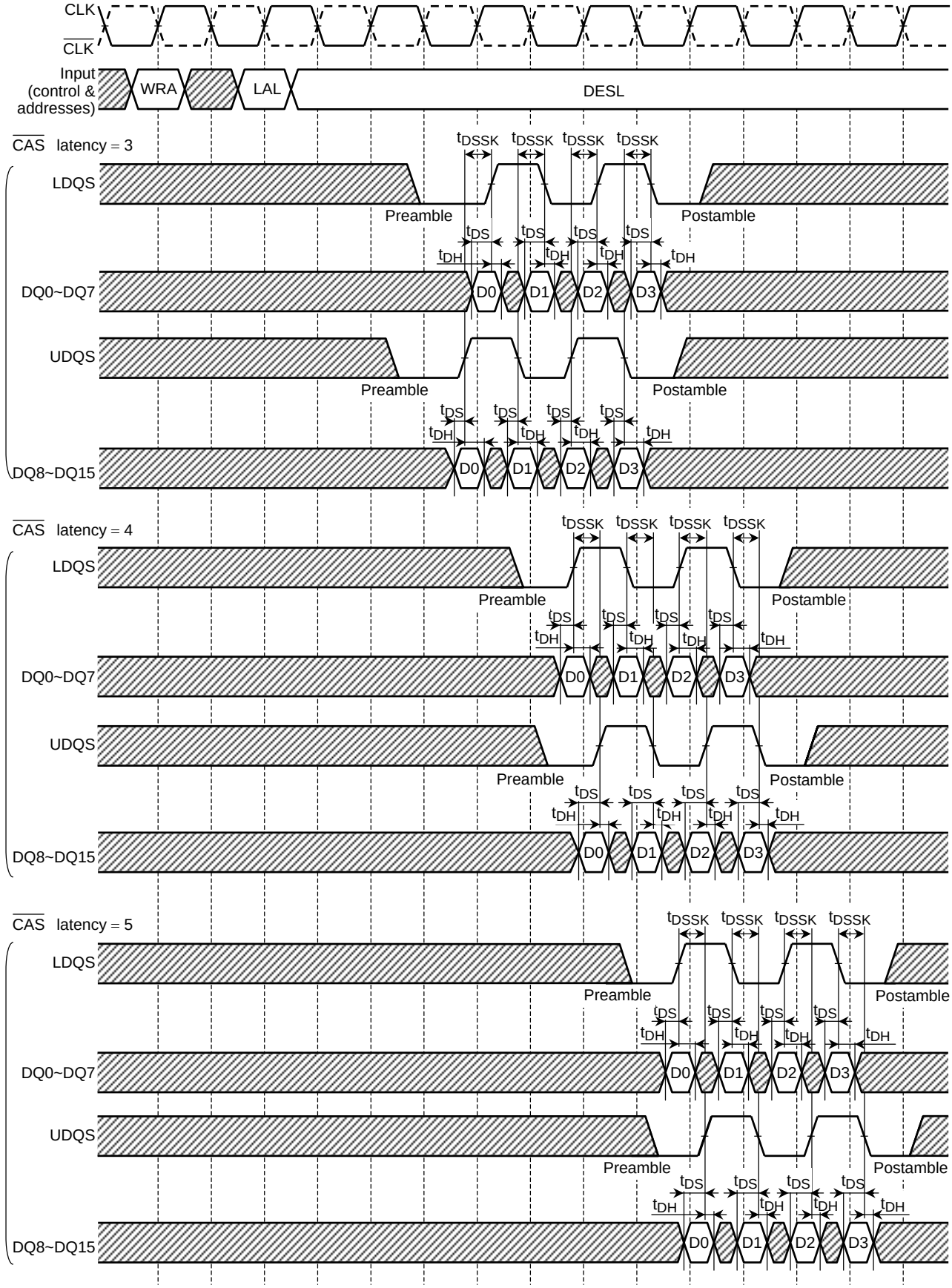
$\overline{DQS}$ mode is chosen by EMRS. (TC59LM906AMG)

t_{REFI}, t_{PAUSE}, Ixxxx Timing



Note: "I_{XXXX}" means "I_{RC}", "I_{RCD}", "I_{RAS}", etc.

Write Timing (x16 device) (Burst Length =4)



FUNCTION TRUTH TABLE (Notes: 1, 2, 3)

Command Truth Table (Notes: 4)

• The First Command

SYMBOL	FUNCTION	$\overline{CS}$	FN	BA2~BA0	A13~A9	A8	A7	A6~A0
DESL	Device Deselect	H	×	×	×	×	×	×
RDA	Read with Auto-close	L	H	BA	UA	UA	UA	UA
WRA	Write with Auto-close	L	L	BA	UA	UA	UA	UA

• The Second Command (The next clock of RDA or WRA command)

SYMBOL	FUNCTION	$\overline{CS}$	FN	BA1~ BA0	BA2	A13	A12~ A11	A10~A 9	A8	A7	A6~A0
LAL	Lower Address Latch (x16)	H	×	×	V	V	V	×	×	LA	LA
LAL	Lower Address Latch (x8)	H	×	×	V	V	×	×	LA	LA	LA
REF	Auto-Refresh	L	×	×	×	×	×	×	×	×	×
MRS	Mode Register Set	L	×	V	L	L	L	L	L	V	V

Notes: 1. L = Logic Low, H = Logic High, × = either L or H, V = Valid (specified value), BA = Bank Address, UA = Upper Address, LA = Lower Address
2. All commands are assumed to issue at a valid state.
3. All inputs for command (excluding SELFX and PDEX) are latched on the crossing point of differential clock input where CLK goes to High.
4. Operation mode is decided by the combination of 1st command and 2nd command. Refer to “STATE DIAGRAM” and the command table below.

Read Command Table

COMMAND (SYMBOL)	$\overline{CS}$	FN	BA2~BA0	A13~A9	A8	A7	A6~A0	NOTES
RDA (1st)	L	H	BA	UA	UA	UA	UA	
LAL (2nd)	H	×	×	×	LA	LA	LA	5

Note 5 : For x16 device, A8 is “X” (either L or H).

Write Command Table

• TC59LM914AMG

COMMAND(SYMBOL)	$\overline{CS}$	FN	BA1~ BA0	BA2	A13	A12	A11	A10~ A9	A8	A7	A6~A0
WRA (1st)	L	L	BA	UA	UA	UA	UA	UA	UA	UA	UA
LAL (2nd)	H	×	×	LVW0	LVW1	UVW0	UVW1	×	×	LA	LA

• TC59LM906AMG

COMMAND(SYMBOL)	$\overline{CS}$	FN	BA1~ BA0	BA2	A13	A12	A11	A10~ A9	A8	A7	A6~A0
WRA (1st)	L	L	BA	UA	UA	UA	UA	UA	UA	UA	UA
LAL (2nd)	H	×	×	VW0	VW1	×	×	×	LA	LA	LA

Notes: 6. BA2, A13 ~ A11 are used for Variable Write Length (VW) control at Write Operation.

FUNCTION TRUTH TABLE (continued)

VW Truth Table

Burst Length	Function	VW0	VW1
BL=2	Write All Words	L	×
	Write First One Word	H	×
BL=4	Reserved	L	L
	Write All Words	H	L
	Write First Two Words	L	H
	Write First One Word	H	H

Note 7 : For x16 device, LVW0 and LVW1 control DQ0~DQ7.
UVW0 and UVW1 control DQ8~DQ15.

Mode Register Set Command Table

COMMAND (SYMBOL)	$\overline{CS}$	FN	BA2~BA0	A13~A9	A8	A7	A6~A0	NOTES
RDA (1st)	L	H	×	×	×	×	×	
MRS (2nd)	L	×	V	V	V	V	V	8

Notes: 8. Refer to “MODE REGISTER TABLE”.

Auto-Refresh Command Table

FUNCTION	COMMAND (SYMBOL)	CURRENT STATE	$\overline{PD}$		$\overline{CS}$	FN	BA2~BA0	A13~A9	A8	A7	A6~A0	NOTES
			n – 1	n								
Active	WRA (1st)	Standby	H	H	L	L	×	×	×	×	×	
Auto-Refresh	REF (2nd)	Active	H	H	L	×	×	×	×	×	×	

Self-Refresh Command Table

FUNCTION	COMMAND (SYMBOL)	CURRENT STATE	$\overline{PD}$		$\overline{CS}$	FN	BA2~BA0	A13~A9	A8	A7	A6~A0	NOTES
			n – 1	n								
Active	WRA (1st)	Standby	H	H	L	L	×	×	×	×	×	
Self-Refresh Entry	REF (2nd)	Active	H	L	L	×	×	×	×	×	×	9, 10
Self-Refresh Continue	—	Self-Refresh	L	L	×	×	×	×	×	×	×	
Self-Refresh Exit	SELFX	Self-Refresh	L	H	H	×	×	×	×	×	×	11

Power Down Table

FUNCTION	COMMAND (SYMBOL)	CURRENT STATE	$\overline{PD}$		$\overline{CS}$	FN	BA2~BA0	A13~A9	A8	A7	A6~A0	NOTES
			n – 1	n								
Power Down Entry	PDEN	Standby	H	L	H	×	×	×	×	×	×	10
Power Down Continue	—	Power Down	L	L	×	×	×	×	×	×	×	
Power Down Exit	PDEX	Power Down	L	H	H	×	×	×	×	×	×	11

Notes: 9. $\overline{PD}$ has to be brought to Low within t_{FPDL} from REF command.
10. $\overline{PD}$ should be brought to Low after DQ’s state turned high impedance.
11. When $\overline{PD}$ is brought to High from Low, this function is executed asynchronously.

FUNCTION TRUTH TABLE (continued)

CURRENT STATE	$\overline{PD}$ n – 1	$\overline{PD}$ n	$\overline{CS}$	FN	ADDRESS	COMMAND	ACTION	NOTES
Idle	H	H	H	×	×	DESL	NOP	
	H	H	L	H	BA, UA	RDA	Row activate for Read	
	H	H	L	L	BA, UA	WRA	Row activate for Write	
	H	L	H	×	×	PDEN	Power Down Entry	12
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Refer to Power Down State	
Row Active for Read	H	H	H	×	LA	LAL	Begin Read	
	H	H	L	×	Op-code	MRS/EMRS	Access to Mode Register	
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	MRS/EMRS	Illegal	
	L	×	×	×	×	—	Invalid	
Row Active for Write	H	H	H	×	LA	LAL	Begin Write	
	H	H	L	×	×	REF	Auto-Refresh	
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	REF (self)	Self-Refresh Entry	
	L	×	×	×	×	—	Invalid	
Read	H	H	H	×	×	DESL	Continue Burst Read to End	
	H	H	L	H	BA, UA	RDA	Illegal	13
	H	H	L	L	BA, UA	WRA	Illegal	13
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Invalid	
Write	H	H	H	×	×	DESL	Data Write & Continue Burst Write to End	
	H	H	L	H	BA, UA	RDA	Illegal	13
	H	H	L	L	BA, UA	WRA	Illegal	13
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Invalid	
Auto-Refreshing	H	H	H	×	×	DESL	NOP → Idle after t_{REFC}	
	H	H	L	H	BA, UA	RDA	Illegal	
	H	H	L	L	BA, UA	WRA	Illegal	
	H	L	H	×	×	PDEN	Self-Refresh Entry	14
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Refer to Self-Refreshing State	
Mode Register Accessing	H	H	H	×	×	DESL	NOP → Idle after t_{RSC}	
	H	H	L	H	BA, UA	RDA	Illegal	
	H	H	L	L	BA, UA	WRA	Illegal	
	H	L	H	×	×	PDEN	Illegal	
	H	L	L	×	×	—	Illegal	
	L	×	×	×	×	—	Invalid	
Power Down	H	×	×	×	×	—	Invalid	
	L	L	×	×	×	—	Maintain Power Down Mode	
	L	H	H	×	×	PDEX	Exit Power Down Mode → Idle after t_{PDEX}	
	L	H	L	×	×	—	Illegal	
Self-Refreshing	H	×	×	×	×	—	Invalid	
	L	L	×	×	×	—	Maintain Self-Refresh	
	L	H	H	×	×	SELFX	Exit Self-Refresh → Idle after t_{REFC}	
	L	H	L	×	×	—	Illegal	

Notes: 12. Illegal if any bank is not idle.

13. Illegal to bank in specified states; Function may be legal in the bank inidicated by Bank Address (BA).

14. Illegal if t_{FPDL} is not satisfied.

MODE REGISTER TABLE

Regular Mode Register (Notes: 1)

ADDRESS	BA1 *1	BA0 *1	BA2, A13~A8	A7 *3	A6~A4	A3	A2~A0
Register	0	0	0	TE	CL	BT	BL

A7	TEST MODE (TE)
0	Regular (default)
1	Test Mode Entry

A3	BURST TYPE (BT)
0	Sequential
1	Interleave

A6	A5	A4	$\overline{CAS}$ LATENCY (CL)
0	0	×	Reserved *2
0	1	0	Reserved *2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved *2
1	1	1	Reserved *2

A2	A1	A0	BURST LENGTH (BL)
0	0	0	Reserved *2
0	0	1	2
0	1	0	4
0	1	1	Reserved *2
1	×	×	

Extended Mode Register (Notes: 4)

ADDRESS	BA1 *4	BA0 *4	BA2, A13~A12	A11 *6	A10 *7	A9~A7	A6	A5~A2	A1	A0 *5
Register	0	1	0	0	$\overline{DQS}$	OCD	DIC	0	DIC	DS

A9	A8	A7	Driver Impedance Adjustment
0	0	0	OCD Calibration mode exit
0	0	1	Drive (1)
0	1	0	Drive (0)
1	0	0	Adjust mode
1	1	1	OCD Calibration default

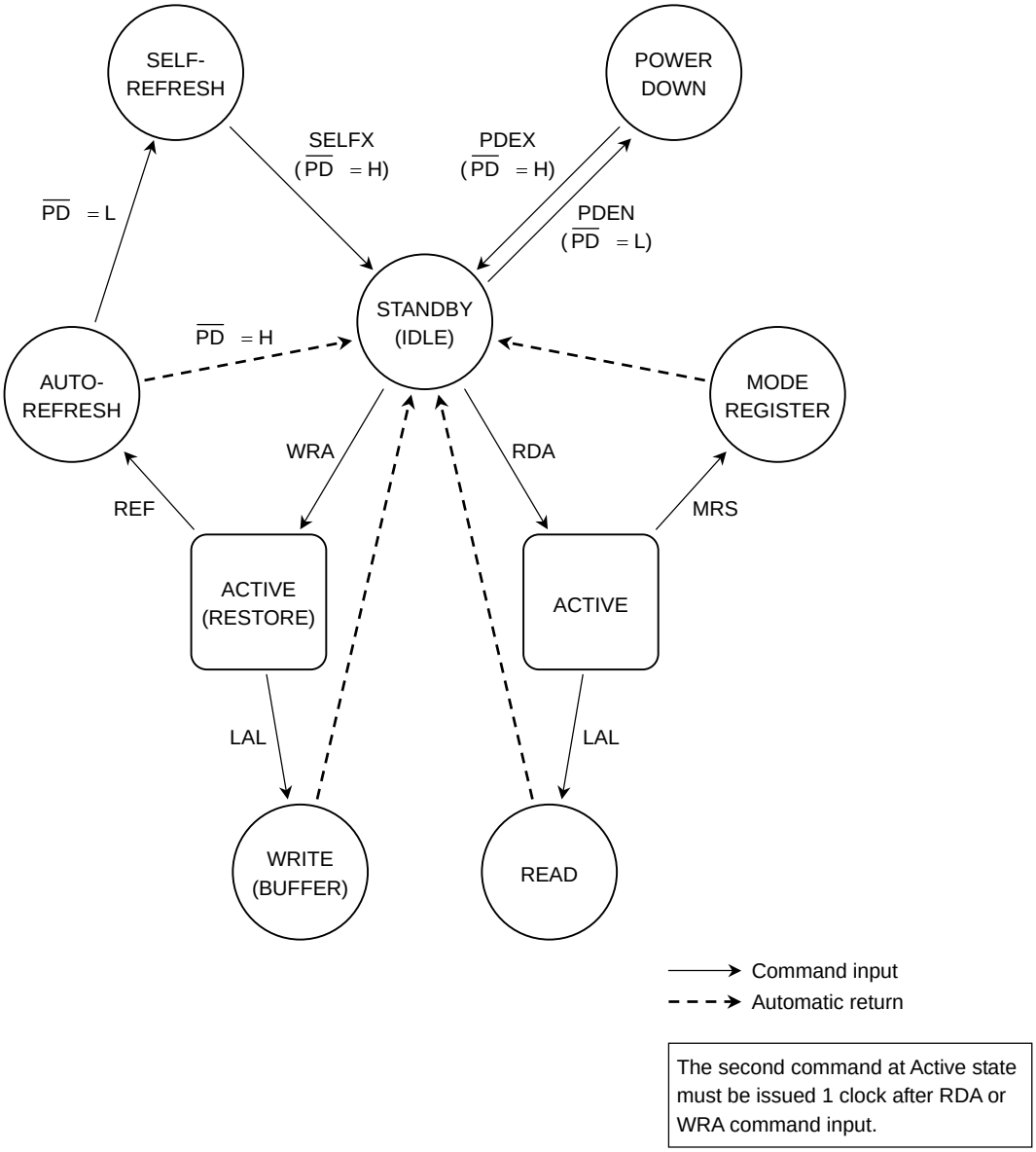
A6	A1	OUTPUT DRIVE IMPEDANCE CONTROL (DIC)
0	0	Normal Output Driver
0	1	Strong Output Driver
1	0	Weak Output Driver
1	1	Full strength Output Driver

A10	$\overline{DQS}$ Enable
0	Disable
1	Enable

A0	DLL SWITCH (DS)
0	DLL Enable
1	DLL Disable

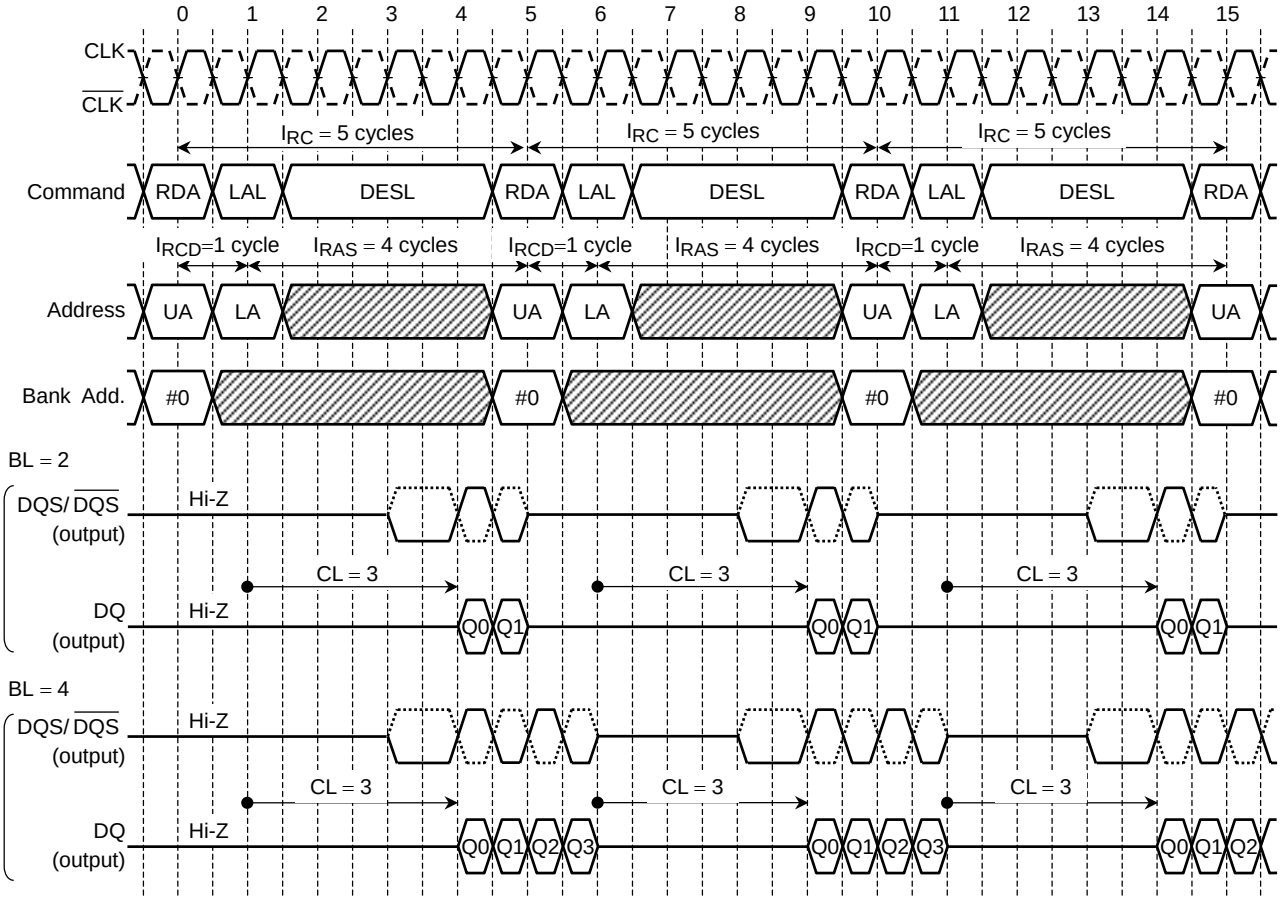
Notes: 1. Regular Mode Register is chosen using the combination of BA0 = 0 and BA1 = 0.
2. "Reserved" places in Regular Mode Register should not be set.
3. A7 in Regular Mode Register must be set to "0" (low state).
Because Test Mode is specific mode for supplier.
4. Extended Mode Register is chosen using the combination of BA0 = 1 and BA1 = 0.
5. A0 in Extended Mode Register must be set to "0" to enable DLL for normal operation.
6. A11 in Extended Mode Register must be set to "0".
7. TC59LM914AMG, A10 in Extended Mode Register is ignored. $\overline{DQS}$ is available only TC59LM906AMG.

STATE DIAGRAM



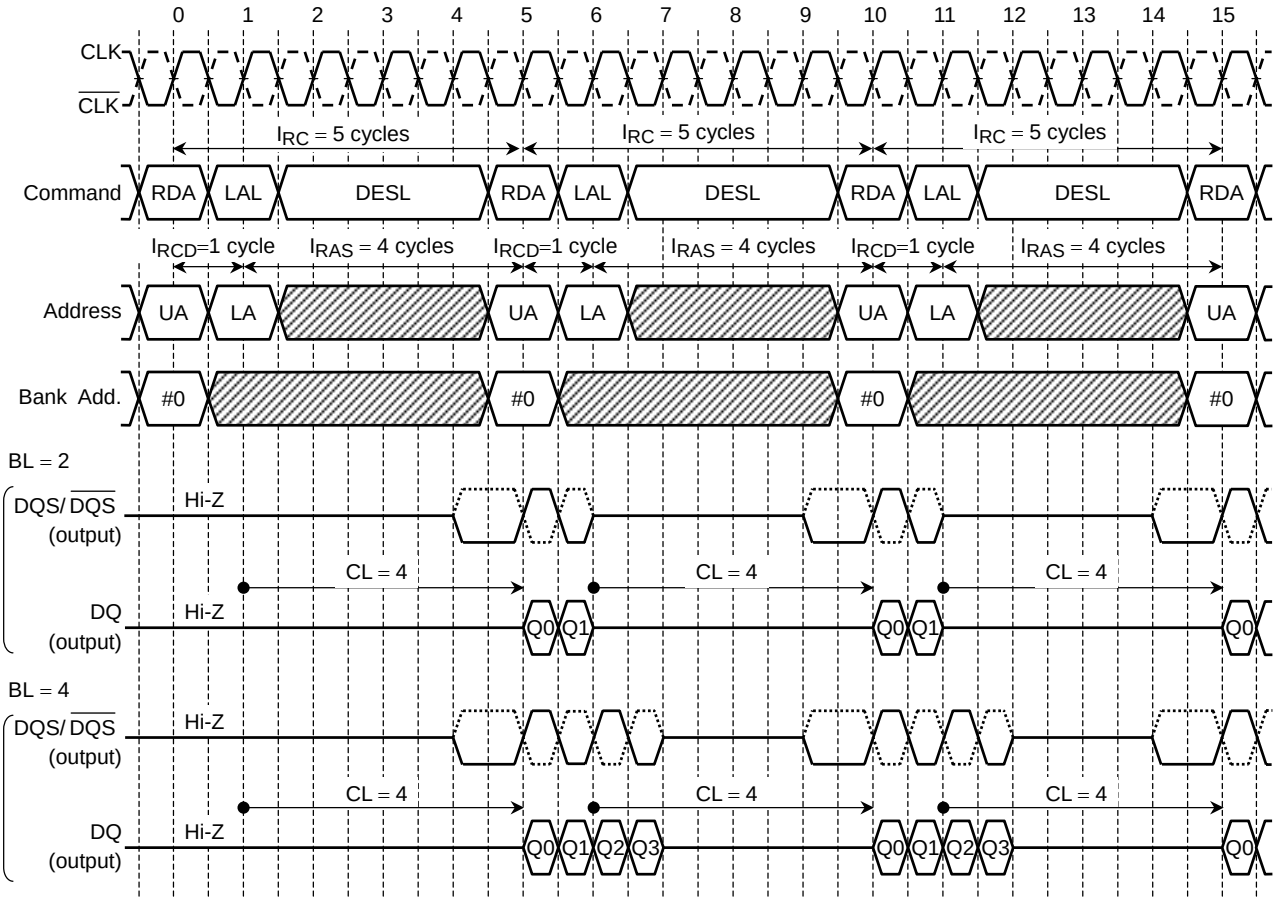
TIMING DIAGRAMS

SINGLE BANK READ TIMING (CL = 3)



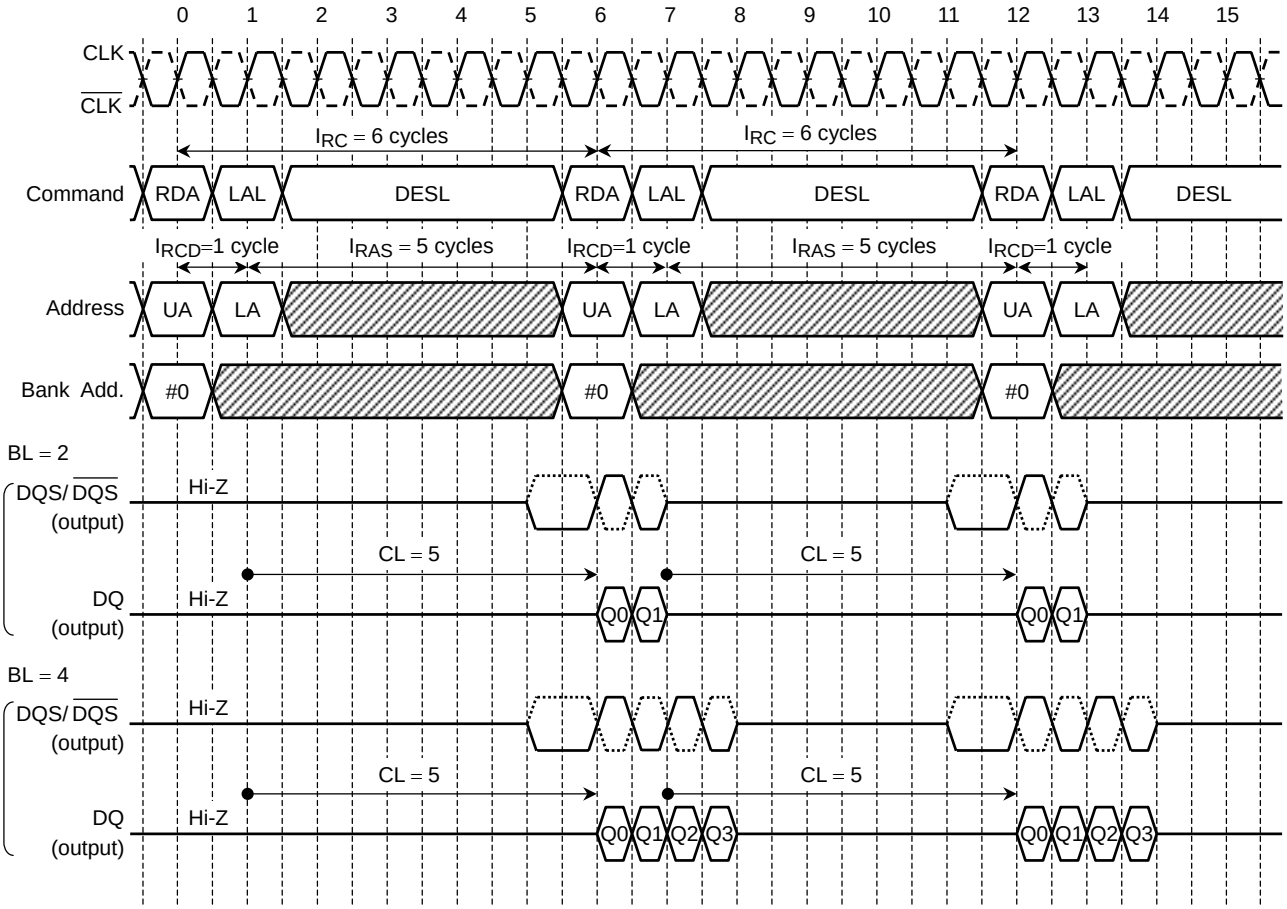
Note : TC59LM914AMG doesn't have $\overline{DQS}$.

SINGLE BANK READ TIMING (CL = 4)



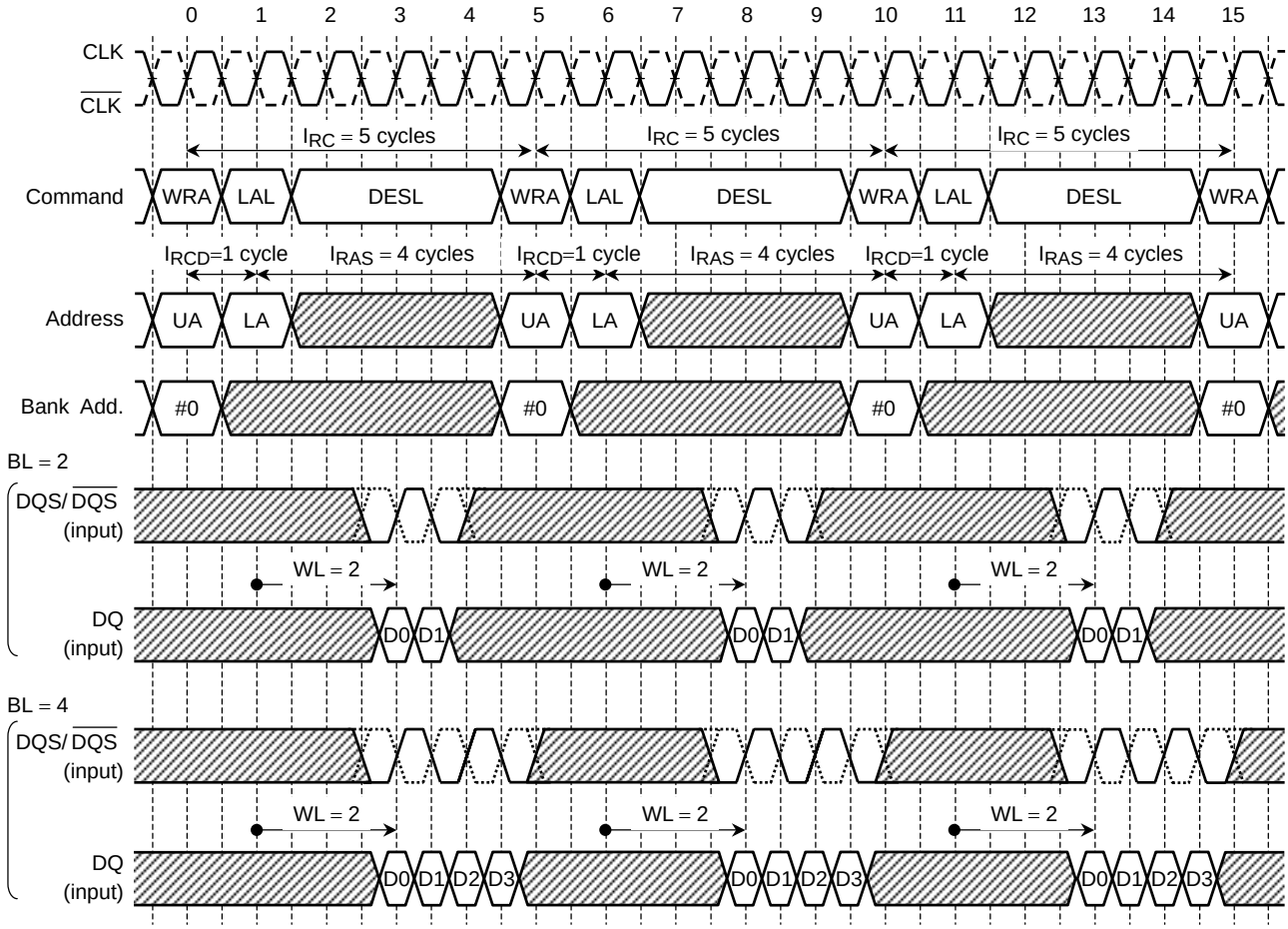
Note : TC59LM914AMG doesn't have $\overline{DQS}$.

SINGLE BANK READ TIMING (CL = 5)



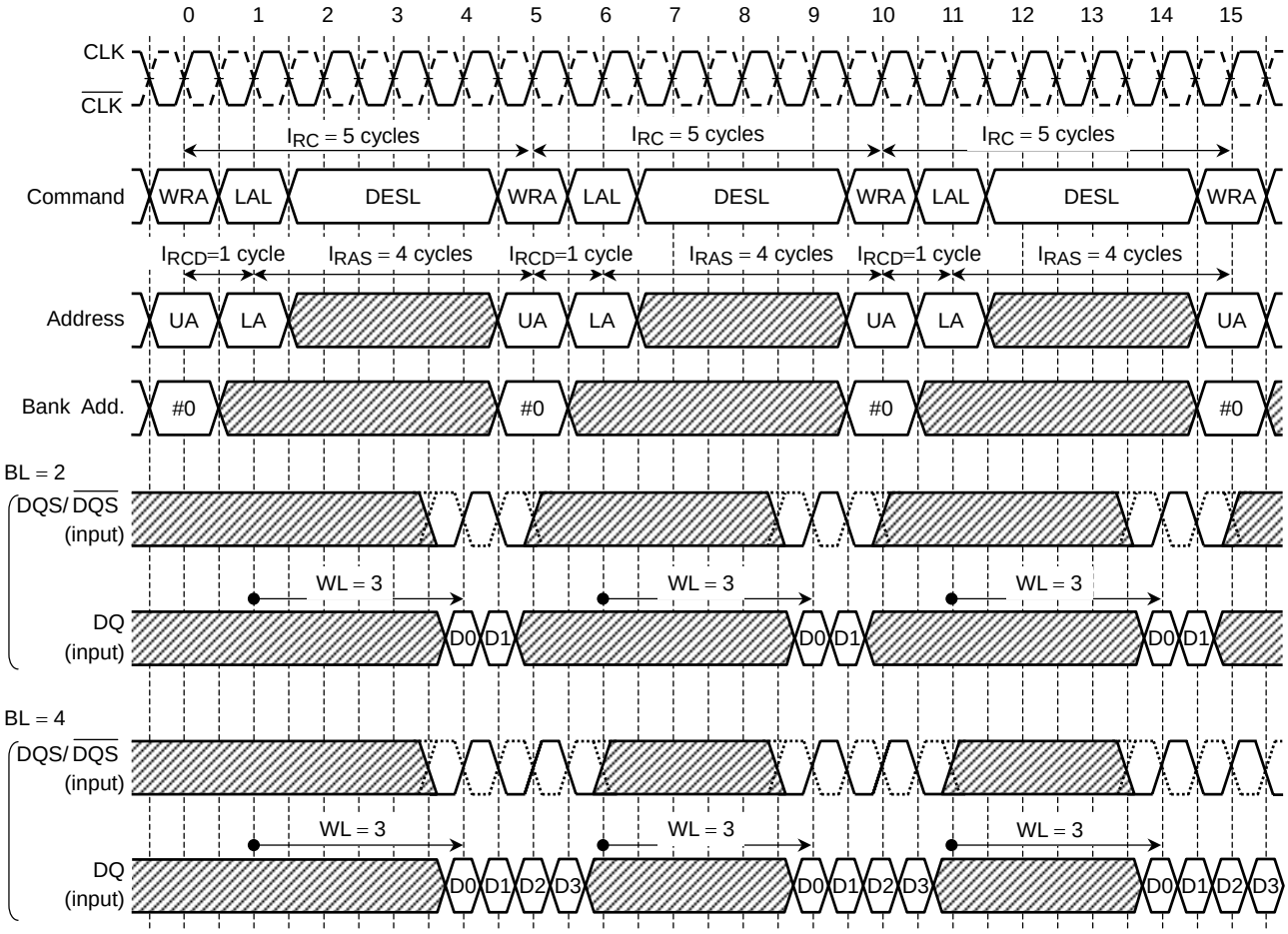
Note : TC59LM914AMG doesn't have $\overline{DQS}$.

SINGLE BANK WRITE TIMING (CL = 3)



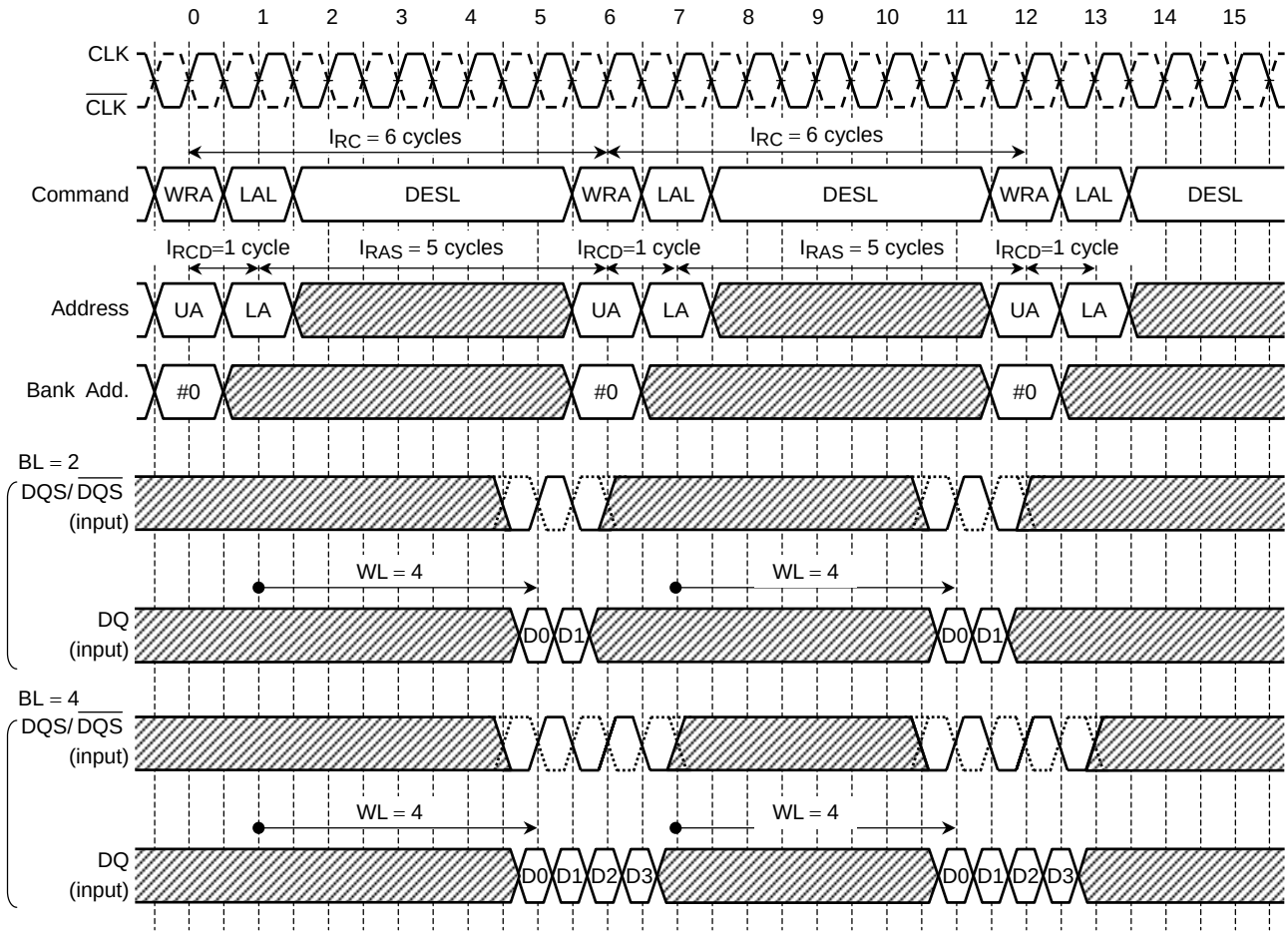
Note : TC59LM914AMG doesn't have $\overline{DQS}$.

SINGLE BANK WRITE TIMING (CL = 4)



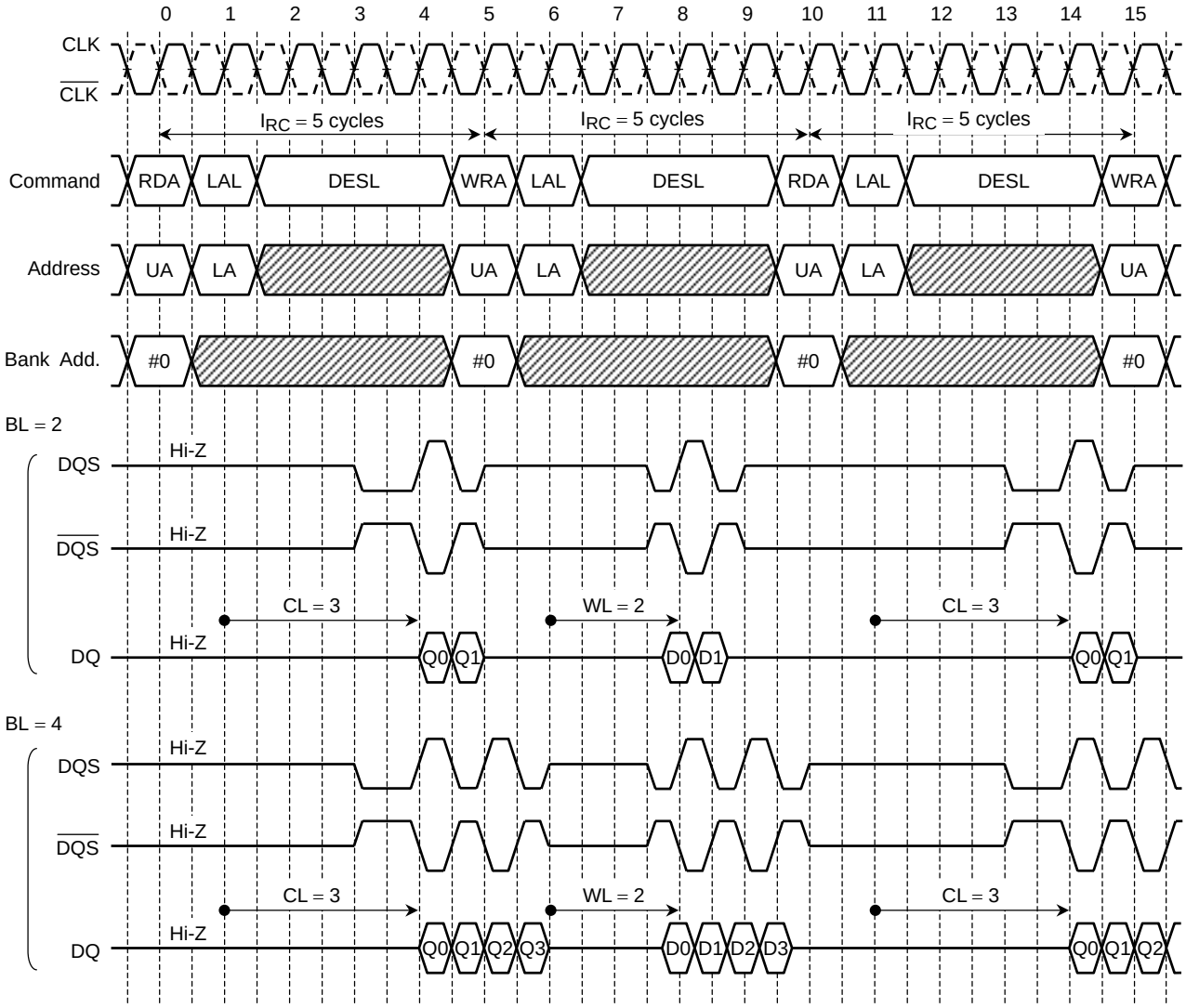
Note : TC59LM914AMG doesn't have $\overline{DQS}$.

SINGLE BANK WRITE TIMING (CL = 5)



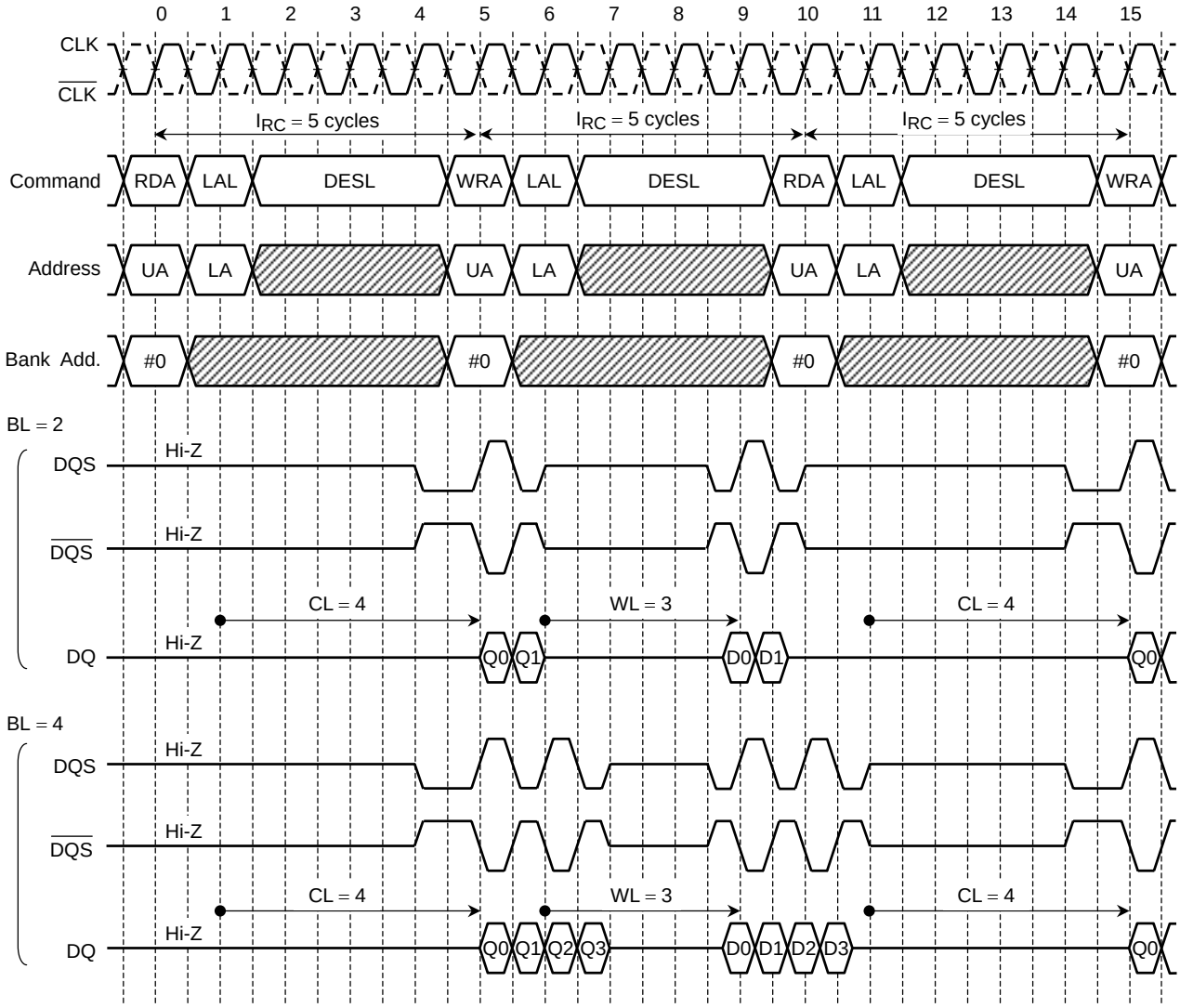
Note : TC59LM914AMG doesn't have $\overline{DQS}$.

SINGLE BANK READ-WRITE TIMING (CL = 3)



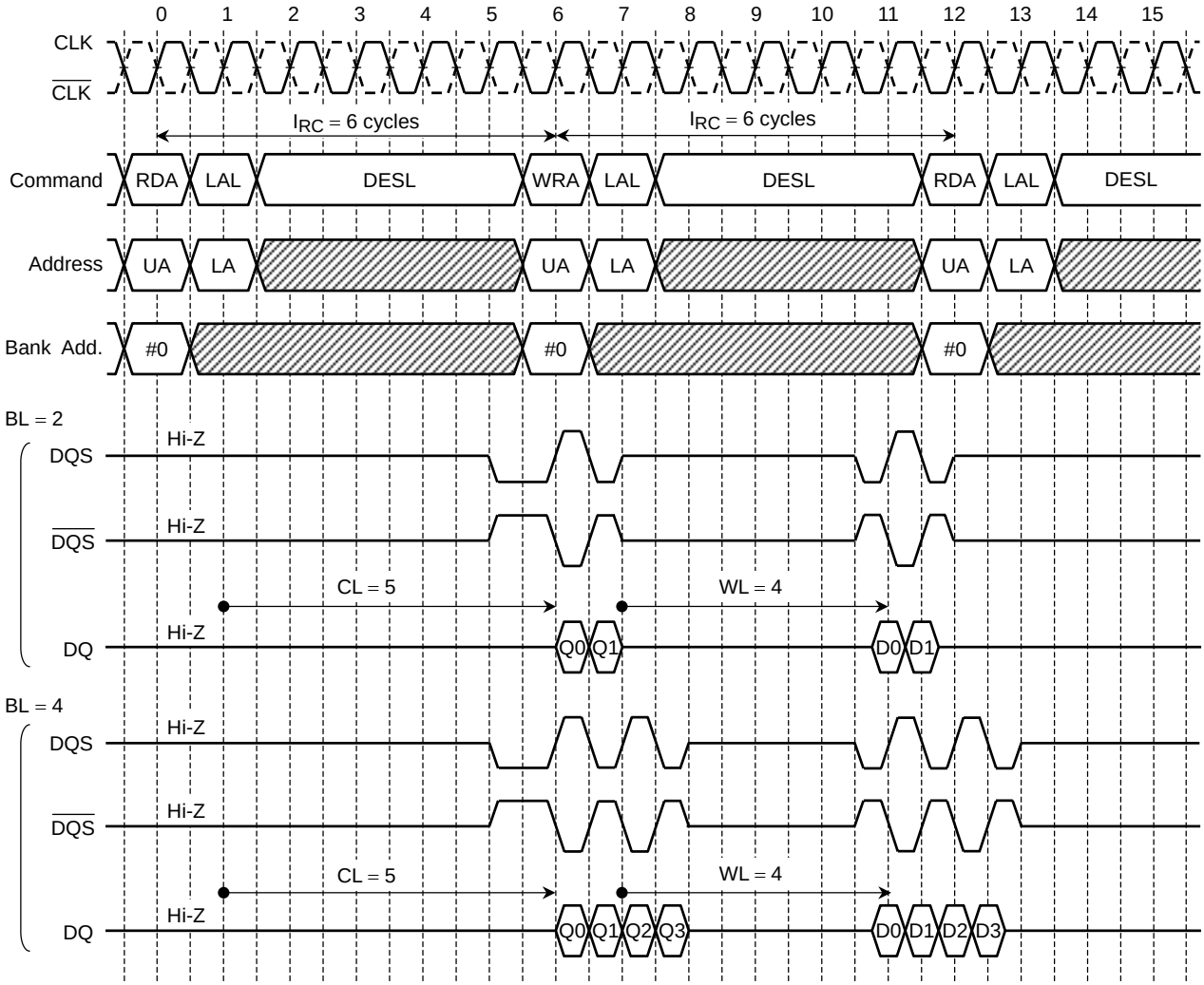
Note : TC59LM914AMG doesn't have $\overline{DQS}$.

SINGLE BANK READ-WRITE TIMING (CL = 4)



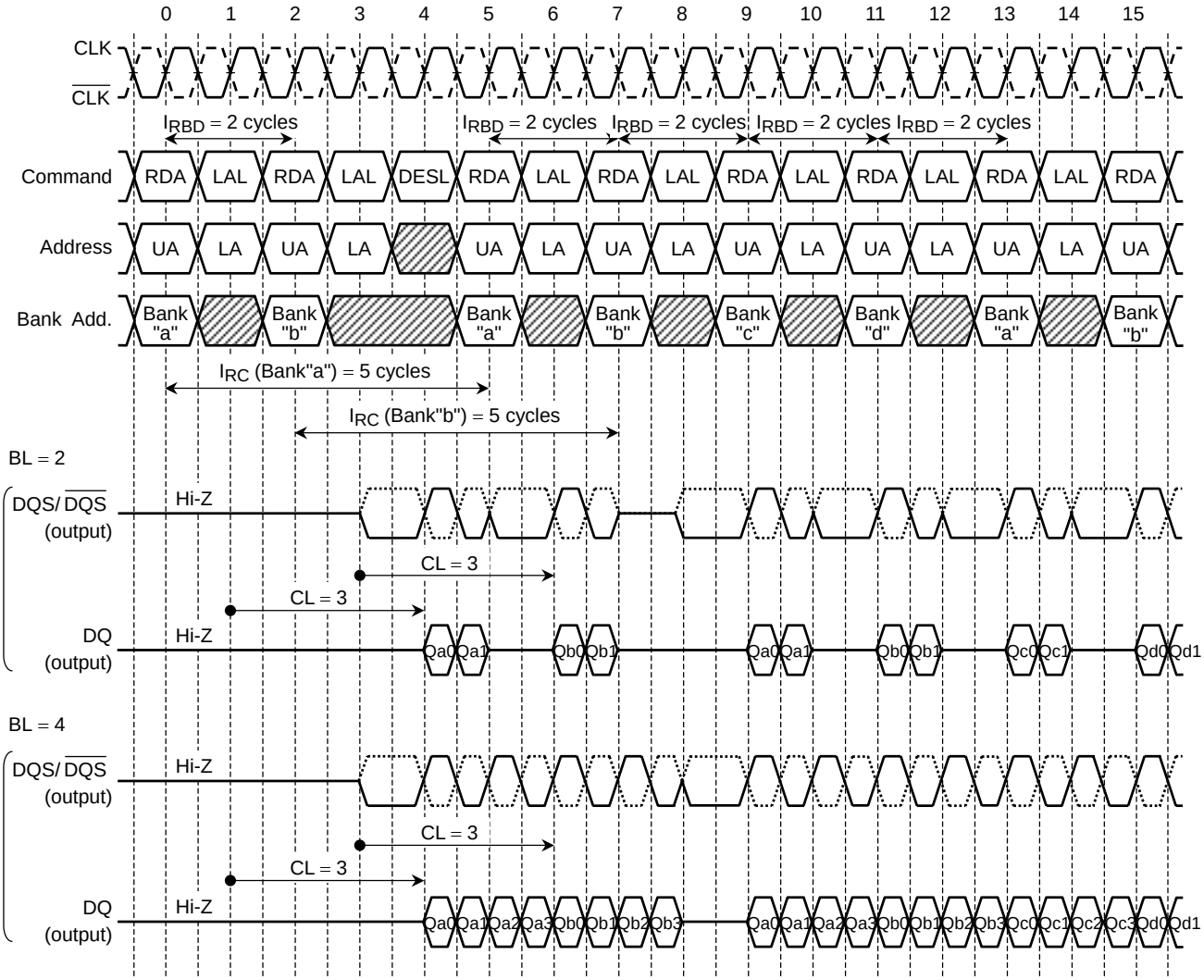
Note : TC59LM914AMG doesn't have $\overline{DQS}$.

SINGLE BANK READ-WRITE TIMING (CL = 5)



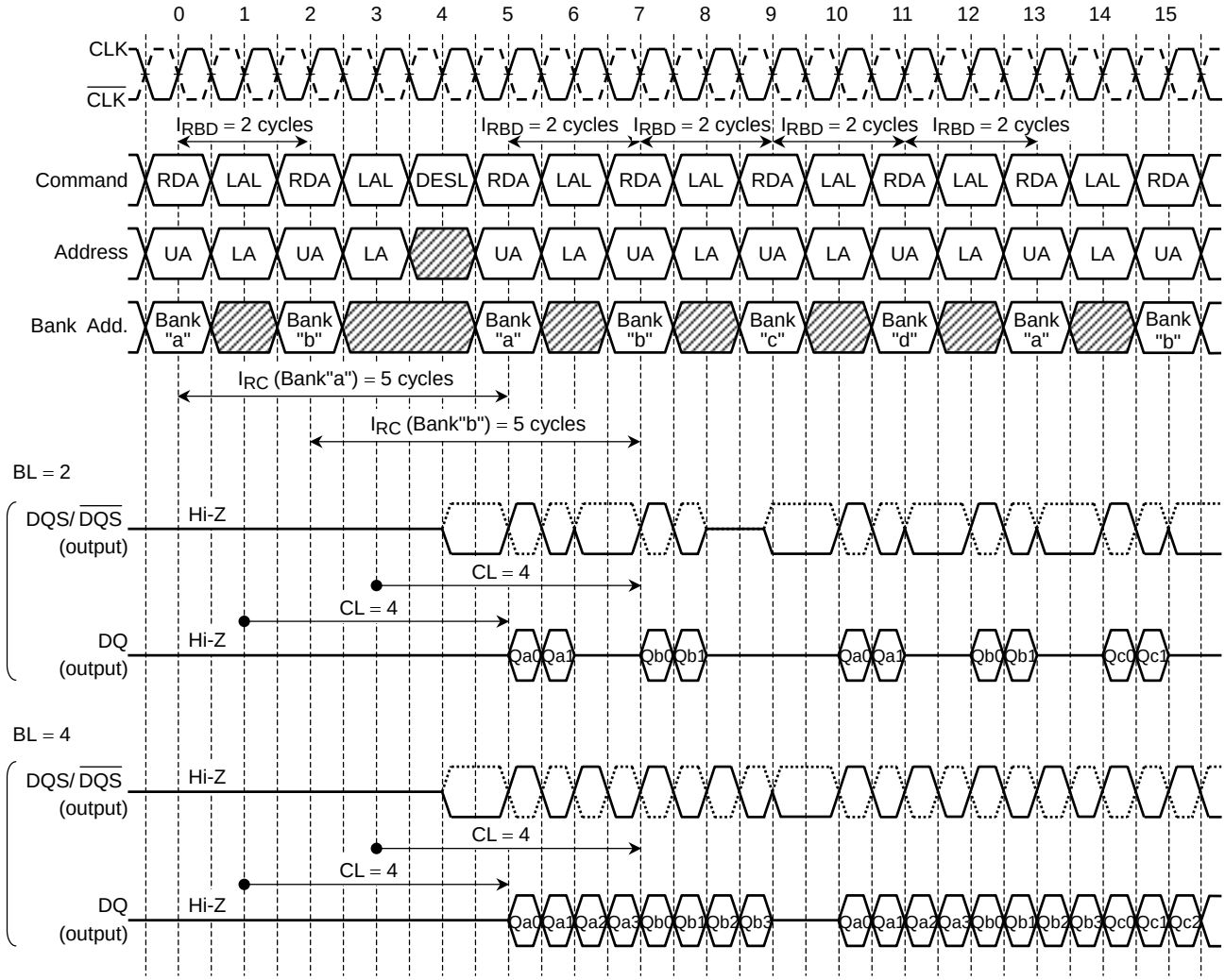
Note : TC59LM914AMG doesn't have $\overline{DQS}$.

MULTIPLE BANK READ TIMING (CL = 3)



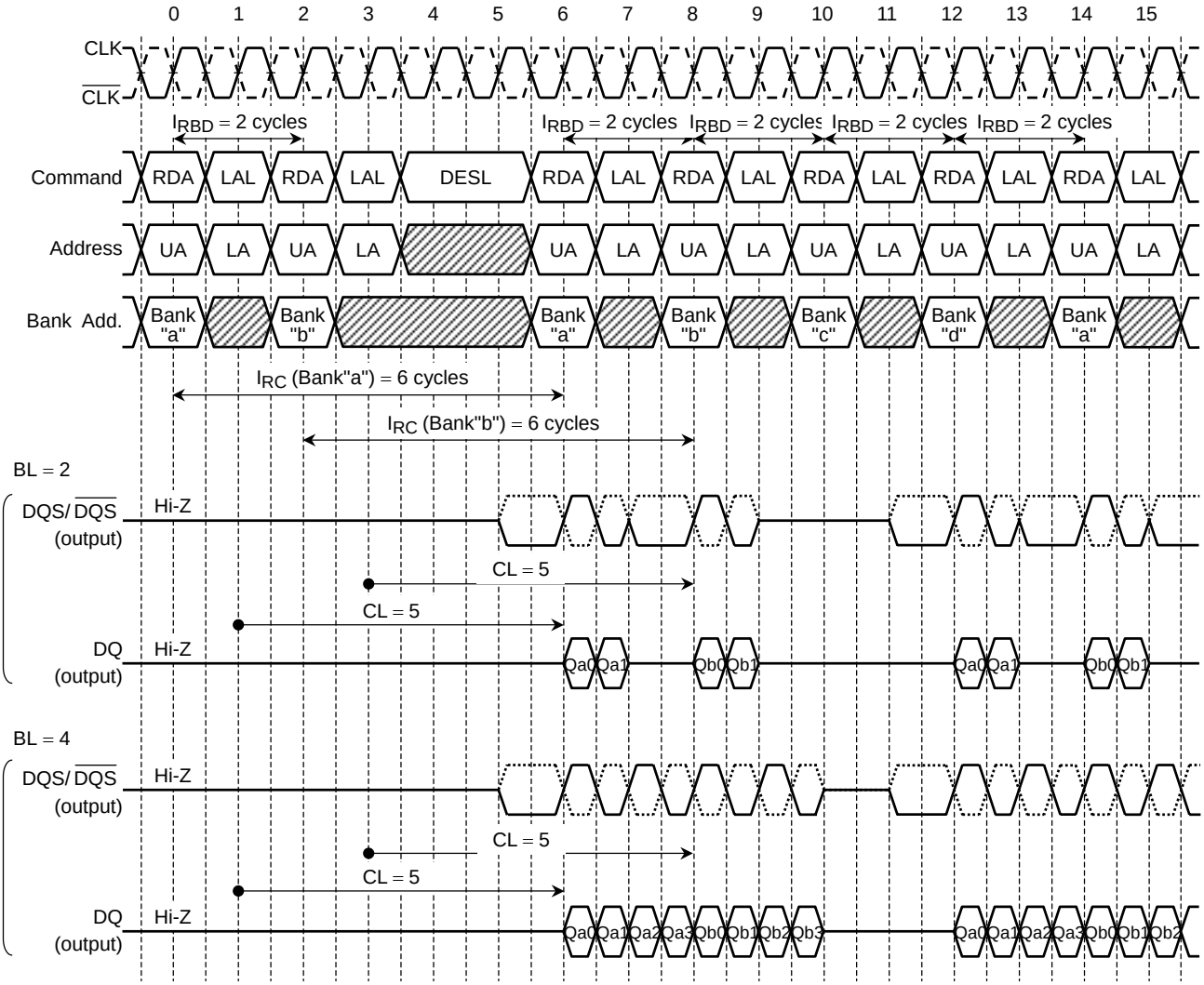
Note: I_{RC} to the same bank must be satisfied.
TC59LM914AMG doesn't have $\overline{DQS}$.

MULTIPLE BANK READ TIMING (CL = 4)



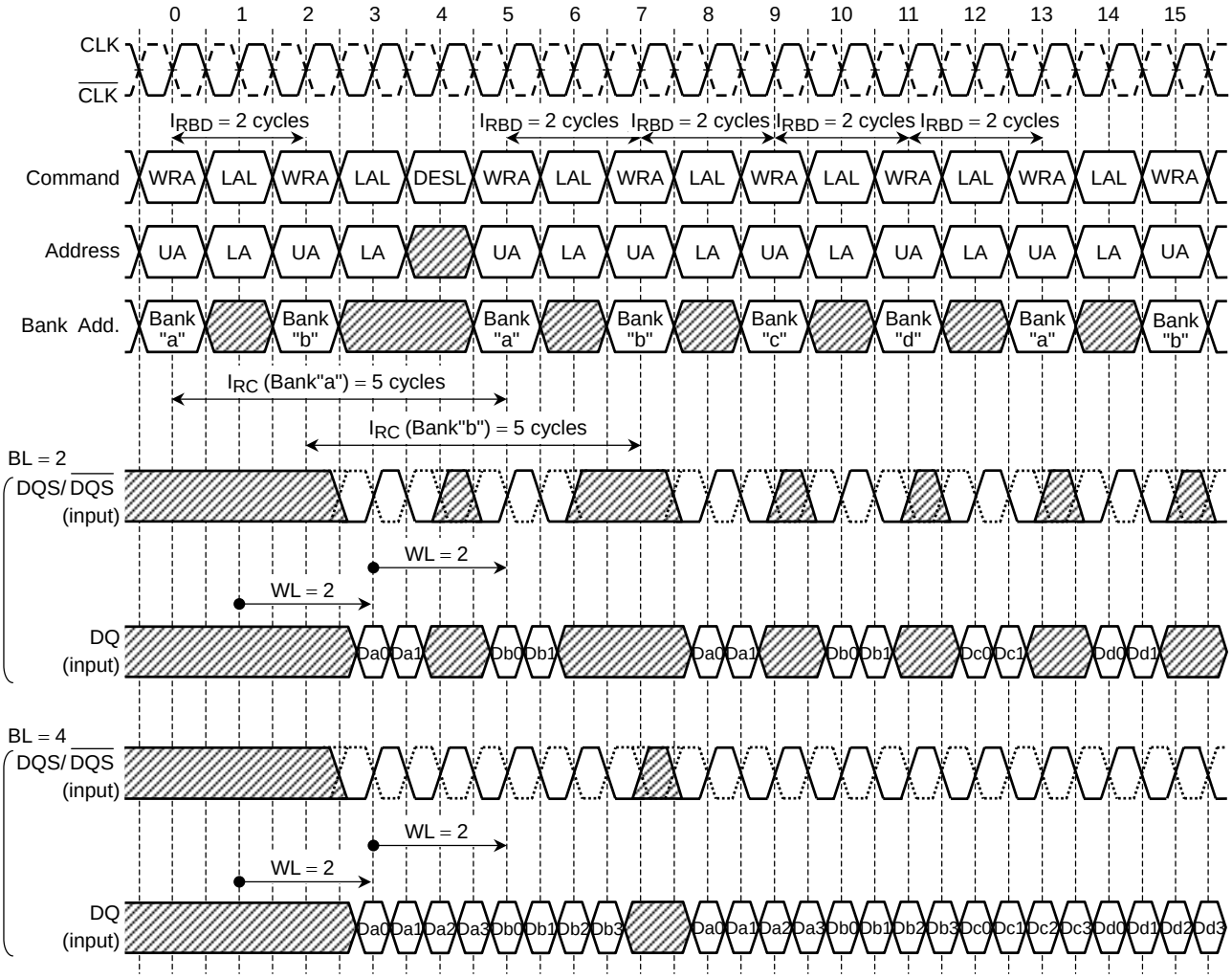
Note: I_{RC} to the same bank must be satisfied.
TC59LM914AMG doesn't have $\overline{DQS}$.

MULTIPLE BANK READ TIMING (CL = 5)



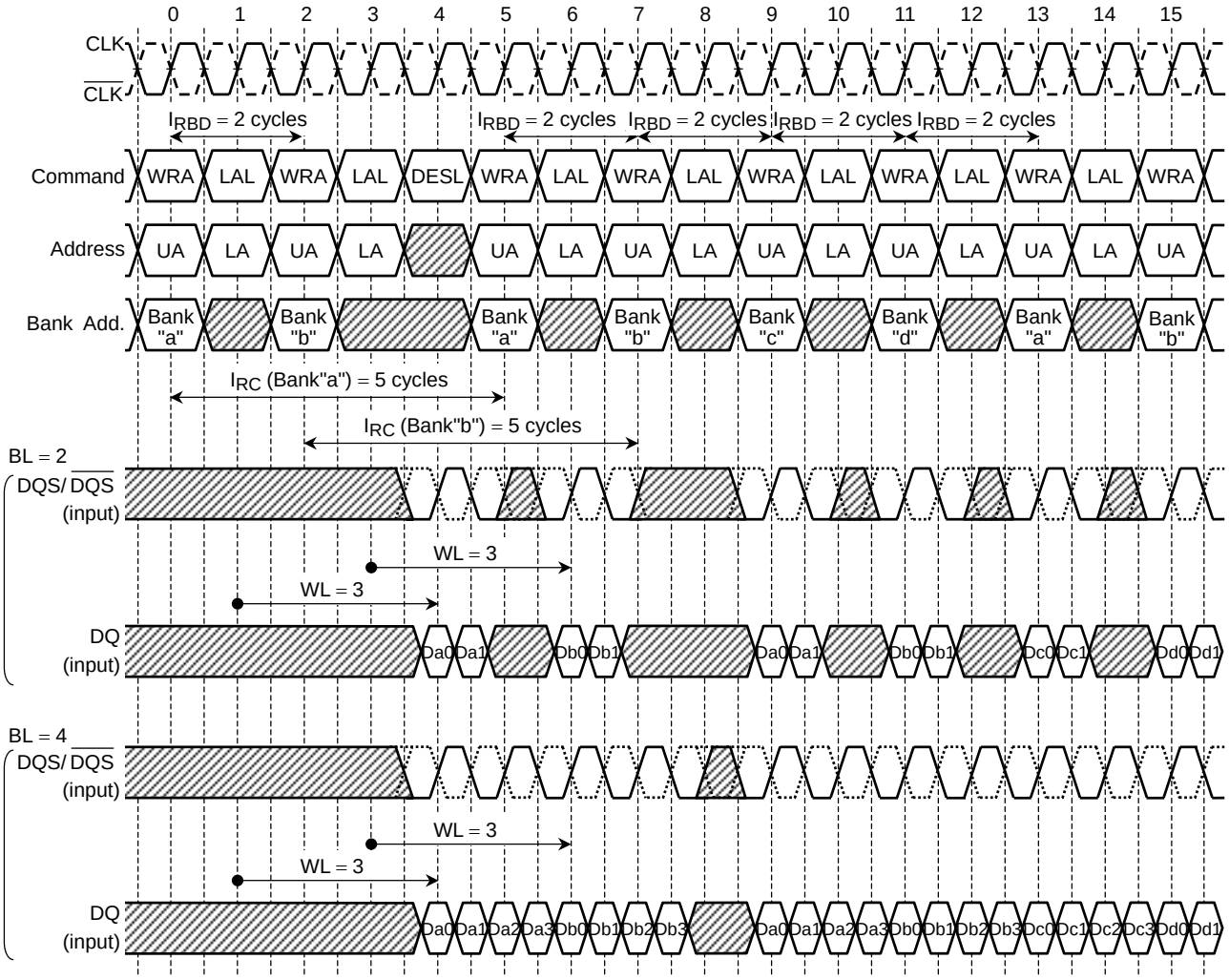
Note: I_{RC} to the same bank must be satisfied.
TC59LM914AMG doesn't have $\overline{DQS}$.

MULTIPLE BANK WRITE TIMING (CL = 3)



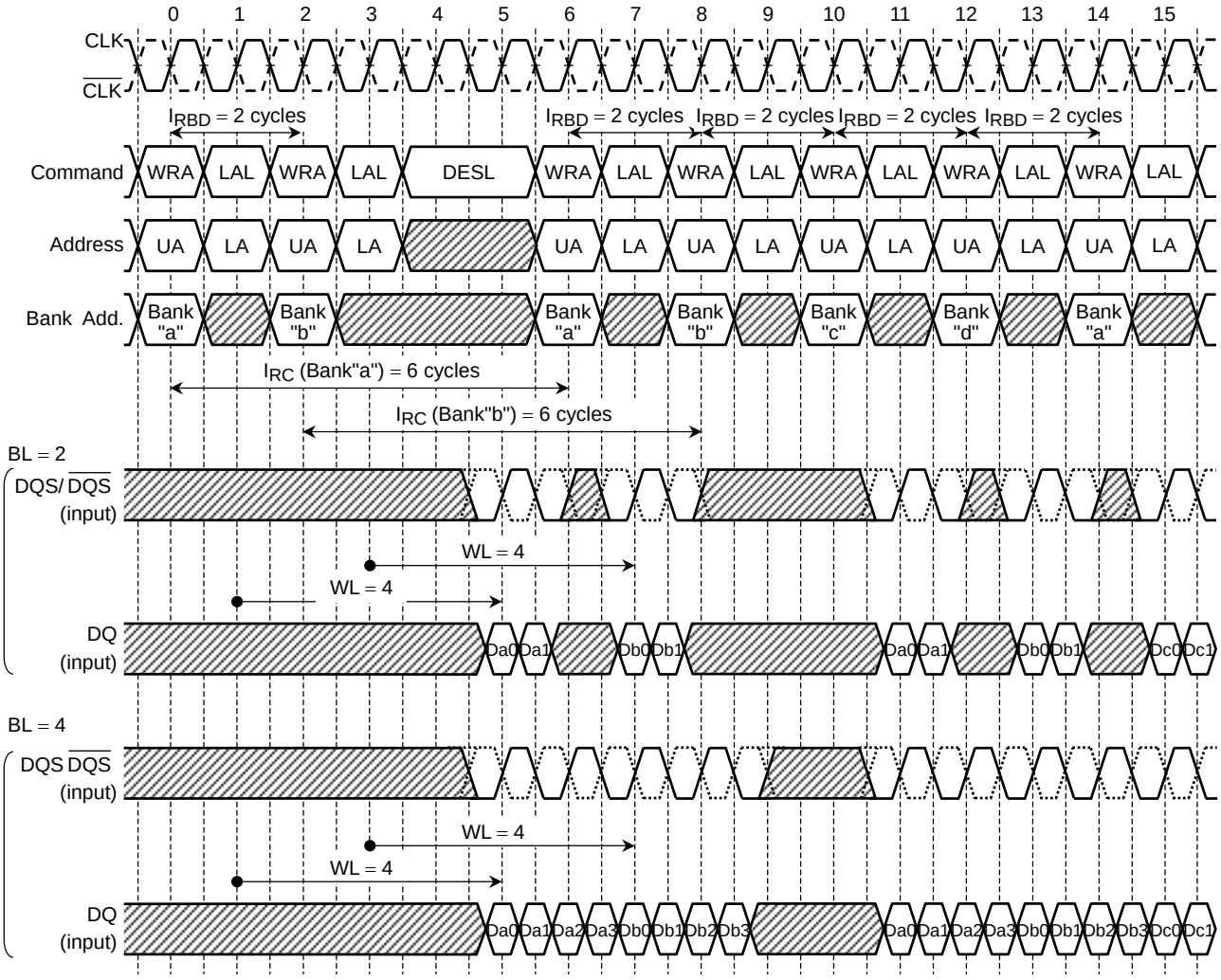
Note: I_{RC} to the same bank must be satisfied.
TC59LM914AMG doesn't have $\overline{DQS}$.

MULTIPLE BANK WRITE TIMING (CL = 4)



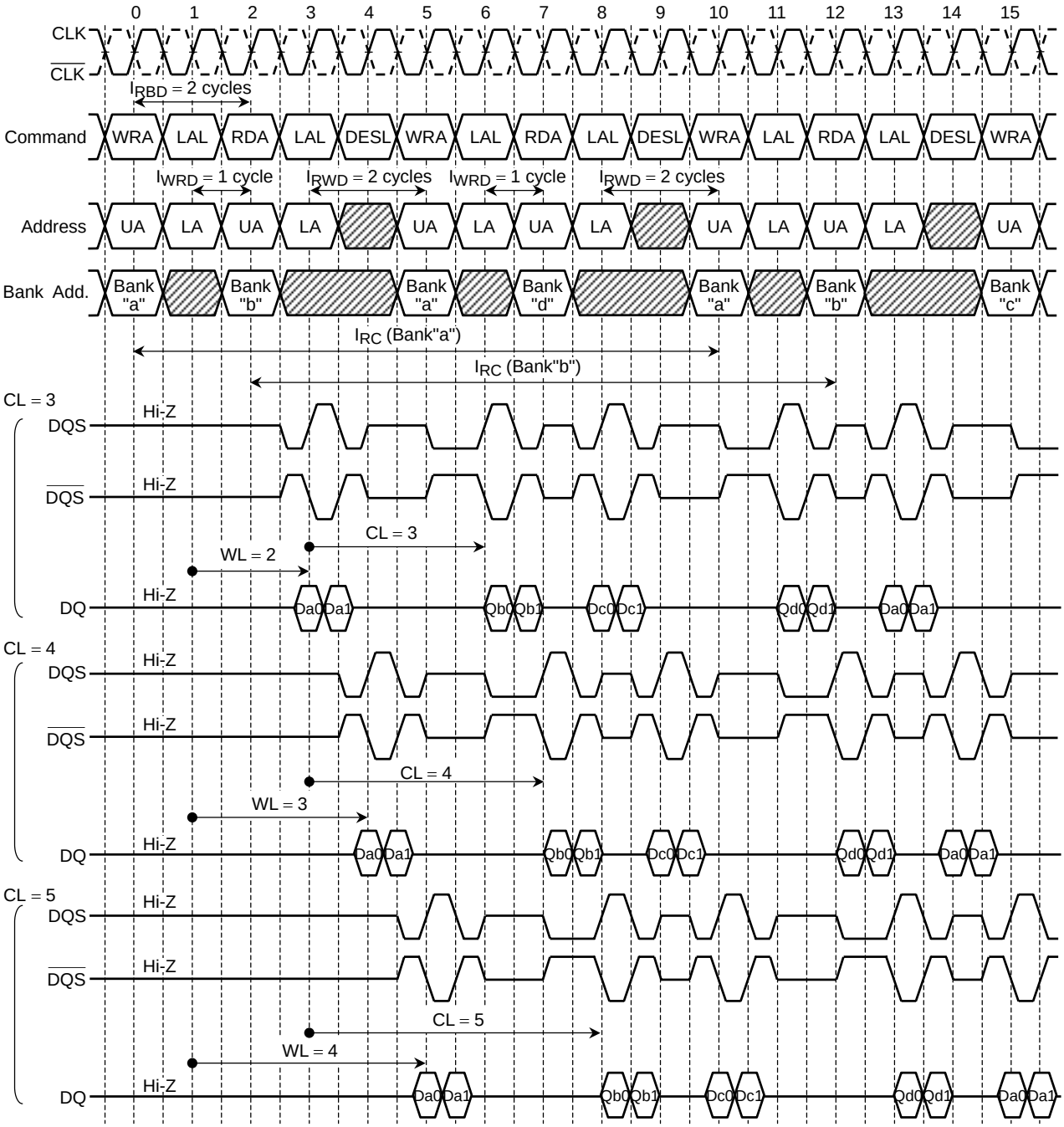
Note: I_{RC} to the same bank must be satisfied.
TC59LM914AMG doesn't have $\overline{DQS}$.

MULTIPLE BANK WRITE TIMING (CL = 5)



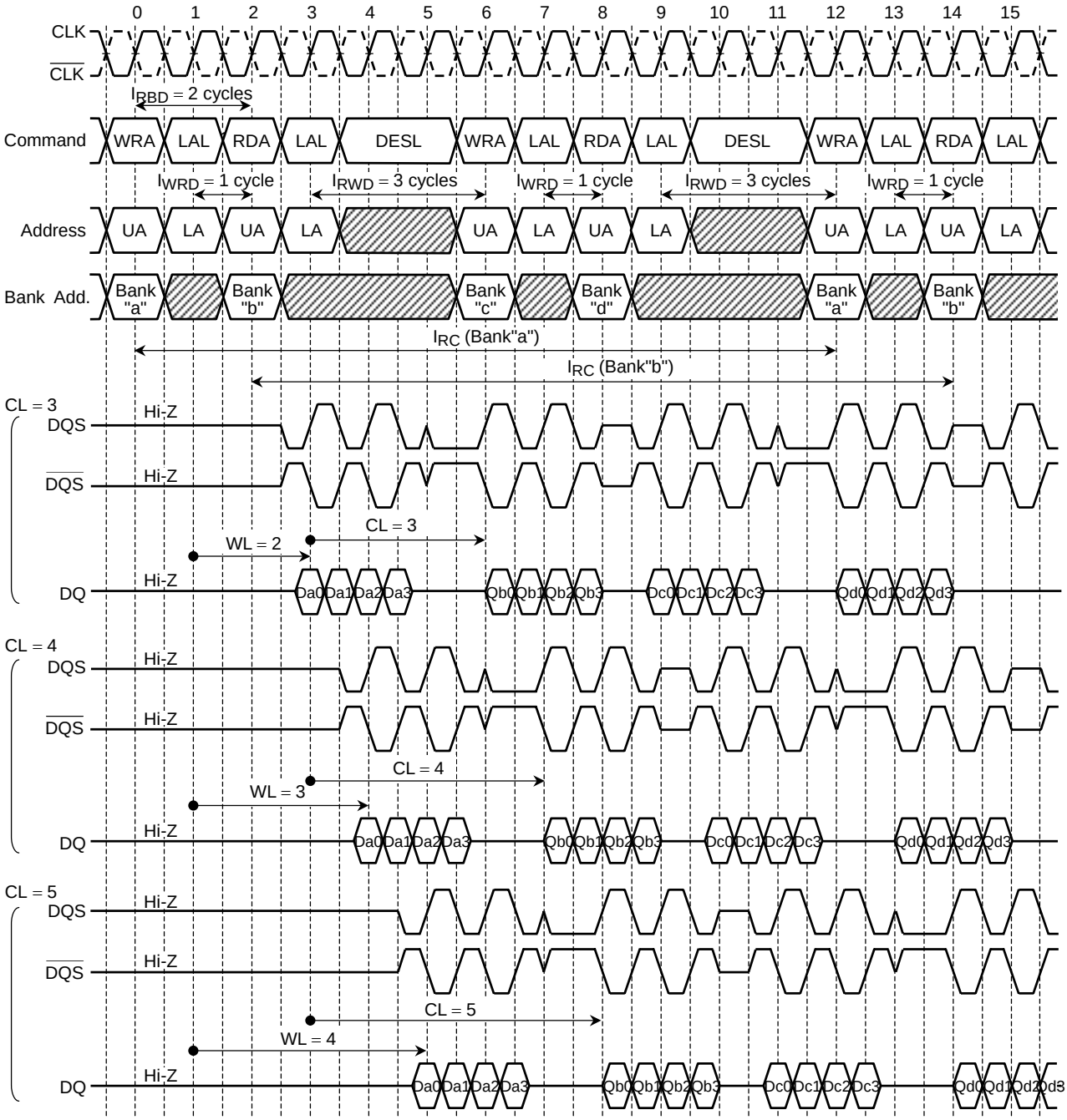
Note: I_{RC} to the same bank must be satisfied.
TC59LM914AMG doesn't have $\overline{DQS}$.

MULTIPLE BANK READ-WRITE TIMING (BL = 2)



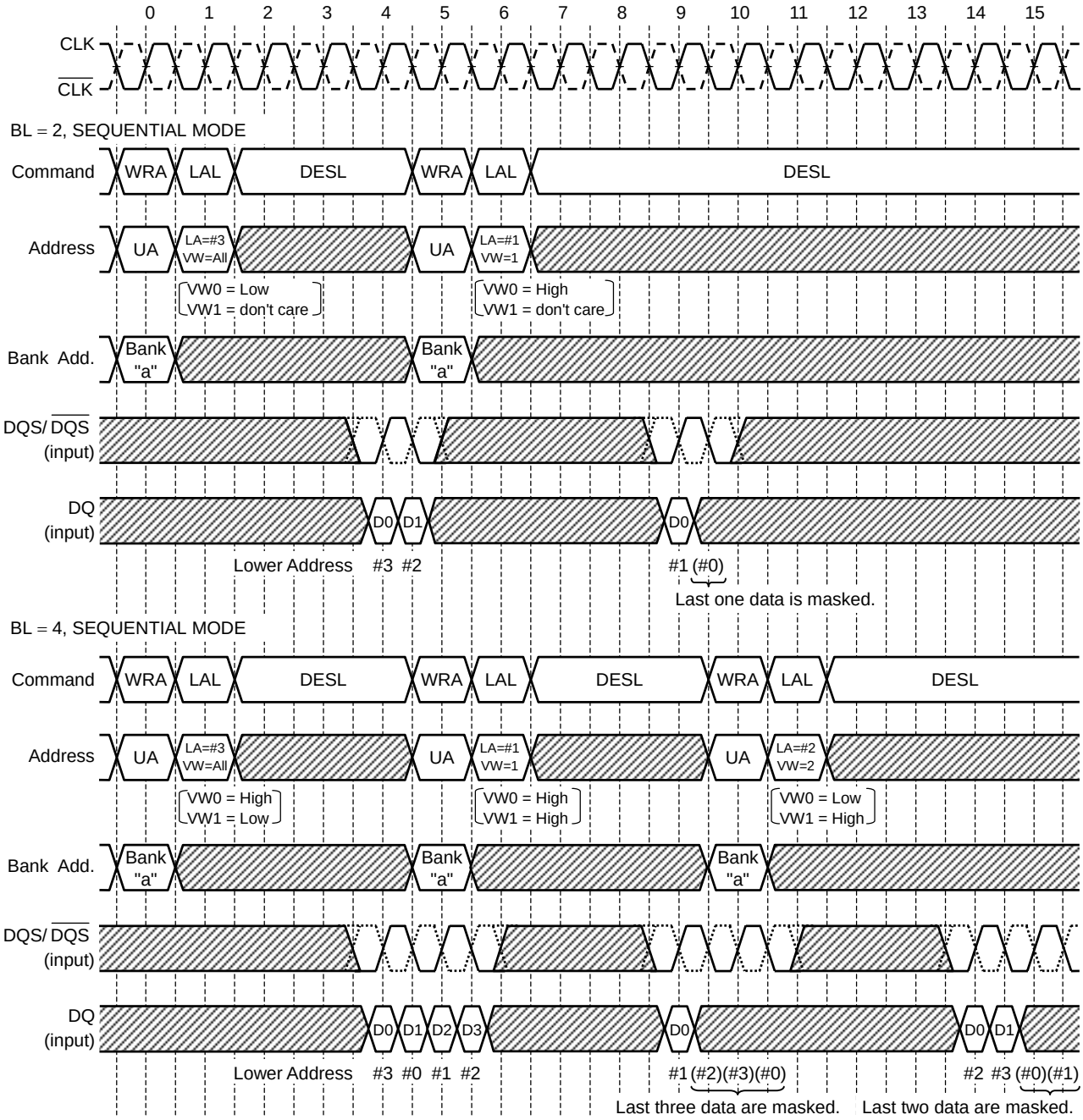
Note: t_{RC} to the same bank must be satisfied.
TC59LM914AMG doesn't have $\overline{DQS}$.

MULTIPLE BANK READ-WRITE TIMING (BL = 4)



Note: t_{RC} to the same bank must be satisfied.
TC59LM914AMG doesn't have $\overline{DQS}$.

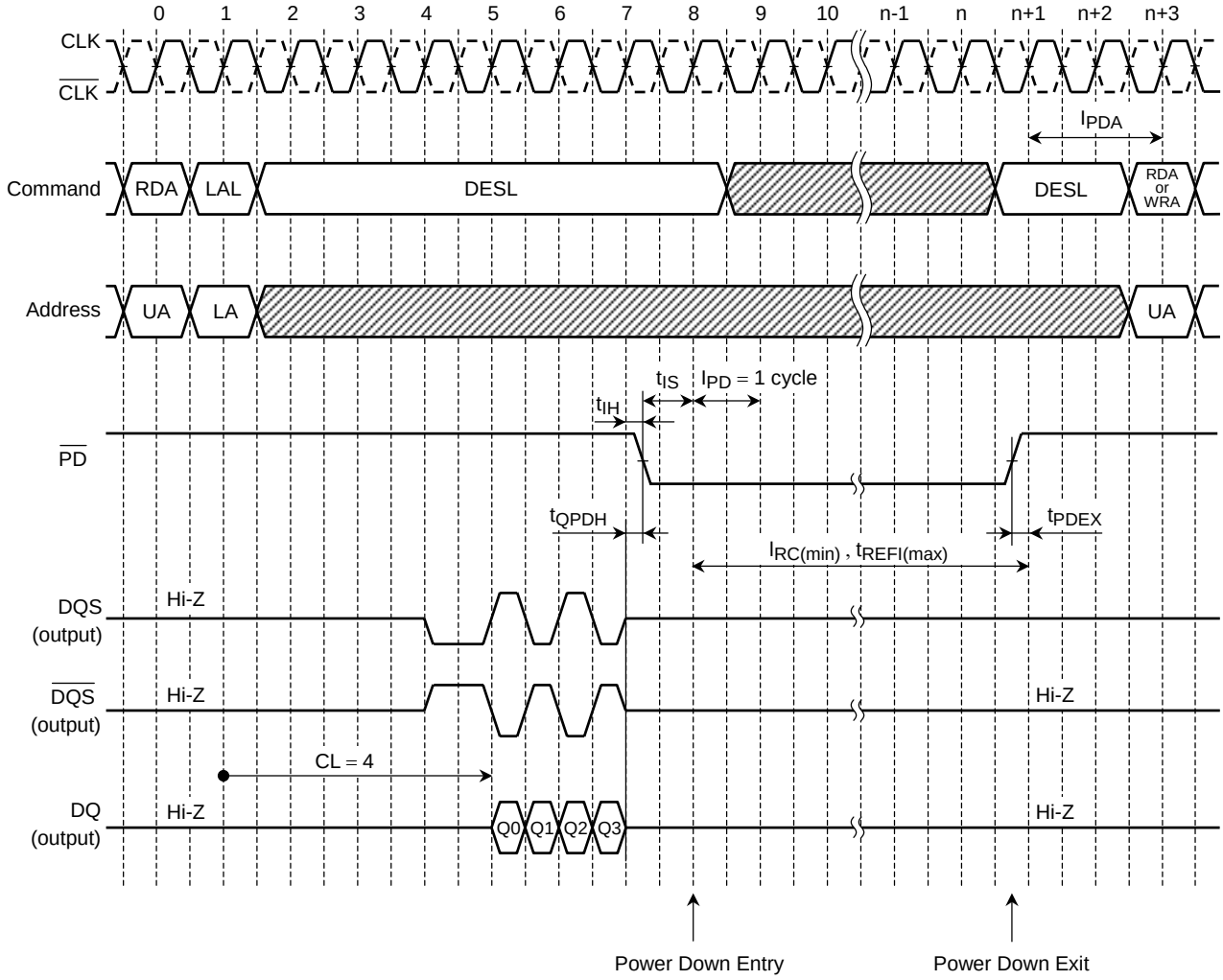
WRITE with VARIAVLE WRITE LENGTH (VW) CONTROL (CL = 4)



Note: DQS ($\overline{\text{DQS}}$) input must be continued till end of burst count even if some of laster data is masked.

POWER DOWN TIMING (CL = 4, BL = 4)

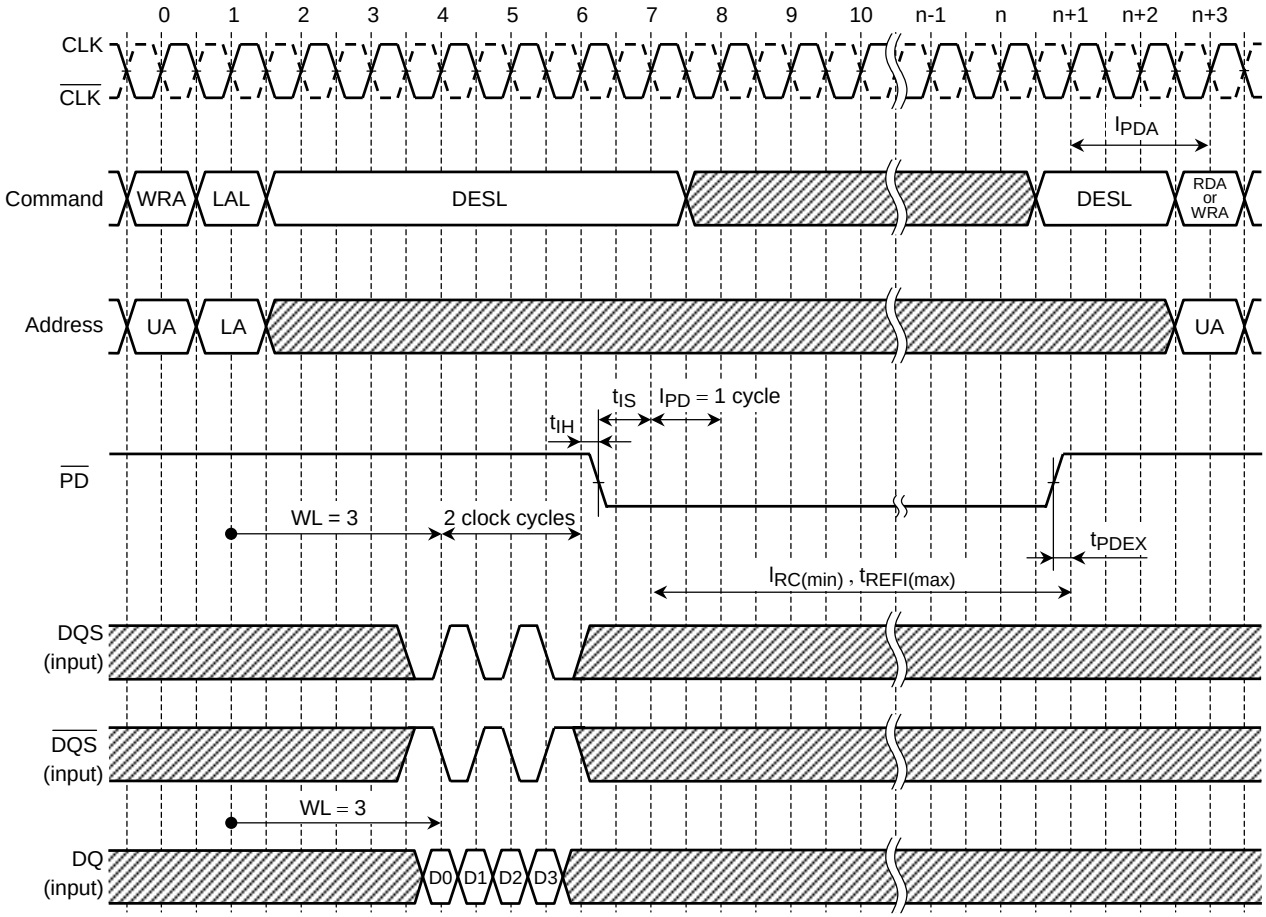
Read cycle to Power Down Mode



Note: $\overline{PD}$ must be kept "High" level until end of Burst data output.
$\overline{PD}$ should be brought to "High" within t_{REFI}(max.) to maintain the data written into cell.
In Power Down Mode, $\overline{PD}$ "Low" and a stable clock signal must be maintained.
When $\overline{PD}$ is brought to "High", a valid executable command may be applied I_{PDA} cycles later.
TC59LM914AMG doesn't have $\overline{DQS}$.

POWER DOWN TIMING (CL = 4, BL = 4)

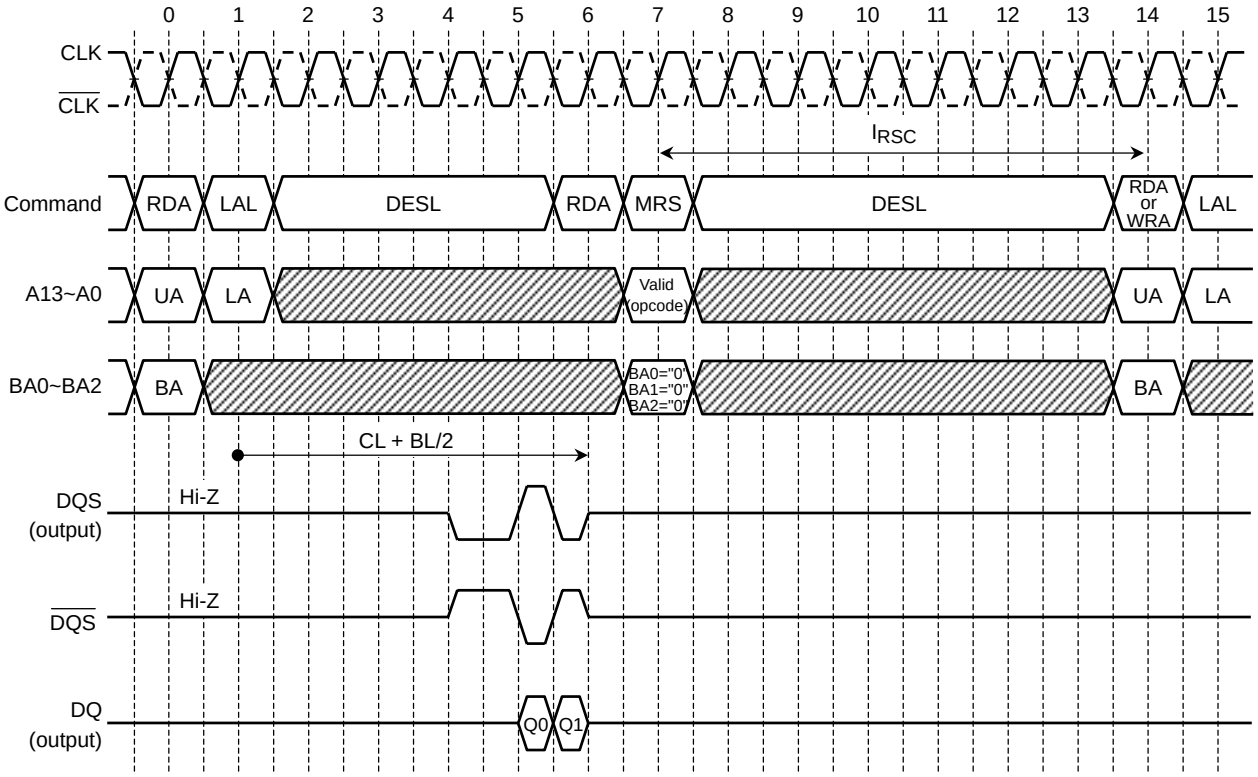
Write cycle to Power Down Mode



Note: $\overline{PD}$ must be kept "High" level until WL+2 clock cycles from LAL command.
$\overline{PD}$ should be brought to "High" within t_{REFI}(max.) to maintain the data written into cell.
In Power Down Mode, $\overline{PD}$ "Low" and a stable clock signal must be maintained.
When $\overline{PD}$ is brought to "High", a valid executable command may be applied I_{PDA} cycles later.
TC59LM914AMG doesn't have $\overline{DQS}$.

MODE REGISTER SET TIMING (CL = 4, BL = 2)

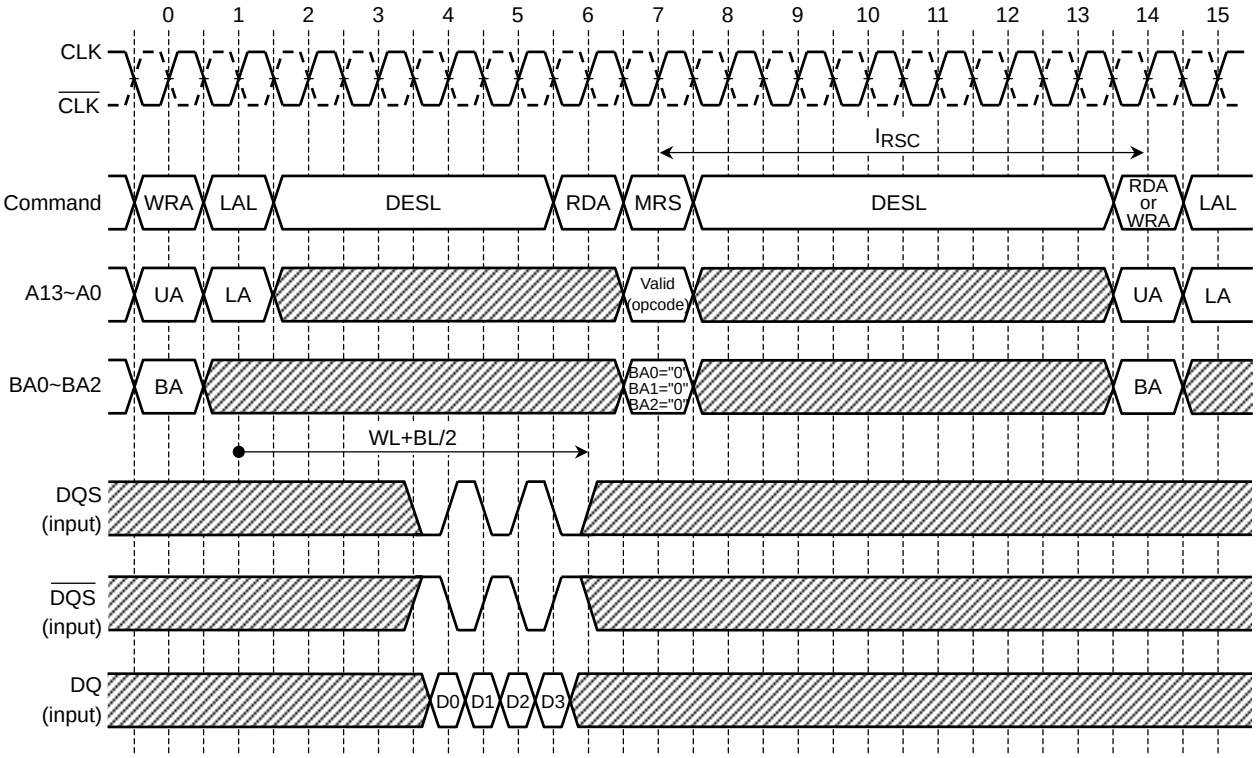
From Read operation to Mode Register Set operation.



Note: Minimum delay from LAL following RDA to RDA of MRS operation is CL+BL/2.
TC59LM914AMG doesn't have $\overline{DQS}$.

MODE REGISTER SET TIMING (CL = 4, BL = 4)

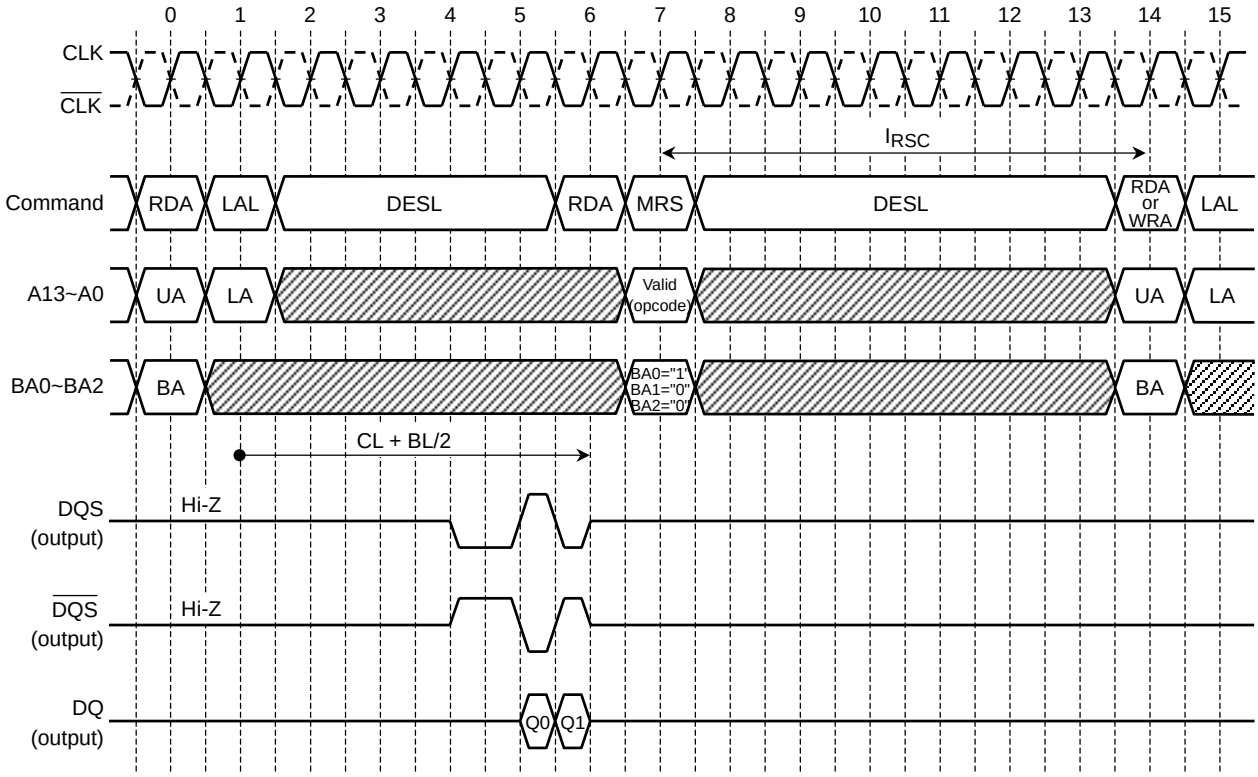
From Write operation to Mode Register Set operation.



Note: Minimum delay from LAL following WRA to RDA of MRS operation is WL+BL/2.
TC59LM914AMG doesn't have $\overline{DQS}$.

EXTENDED MODE REGISTER SET TIMING (CL = 4, BL = 2)

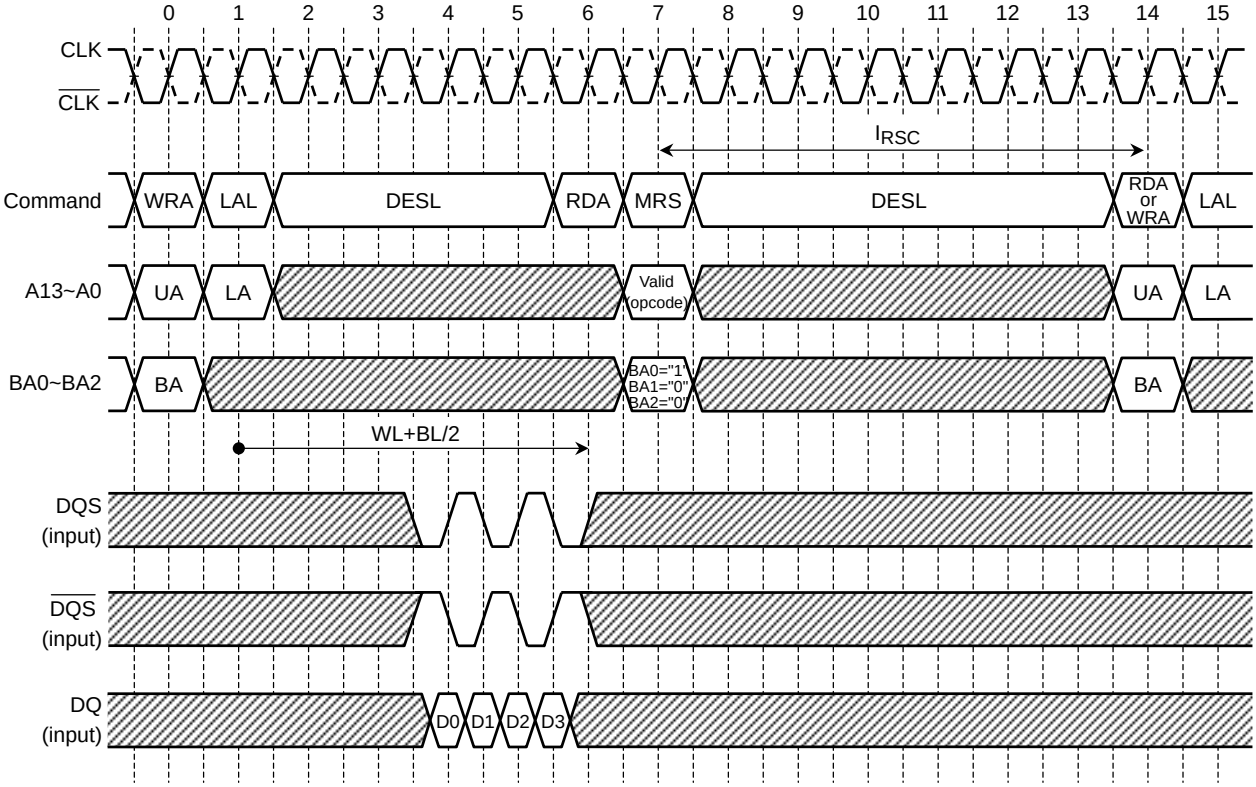
From Read operation to Extended Mode Register Set operation.



Note: Minimum delay from LAL following RDA to RDA of EMRS operation is CL+BL/2.
DLL switch in Extended Mode Register must be set to enable mode for normal operation.
DLL lock-on time is needed after initial EMRS operation. See Power Up Sequence.
TC59LM914AMG doesn't have $\overline{\text{DQS}}$.

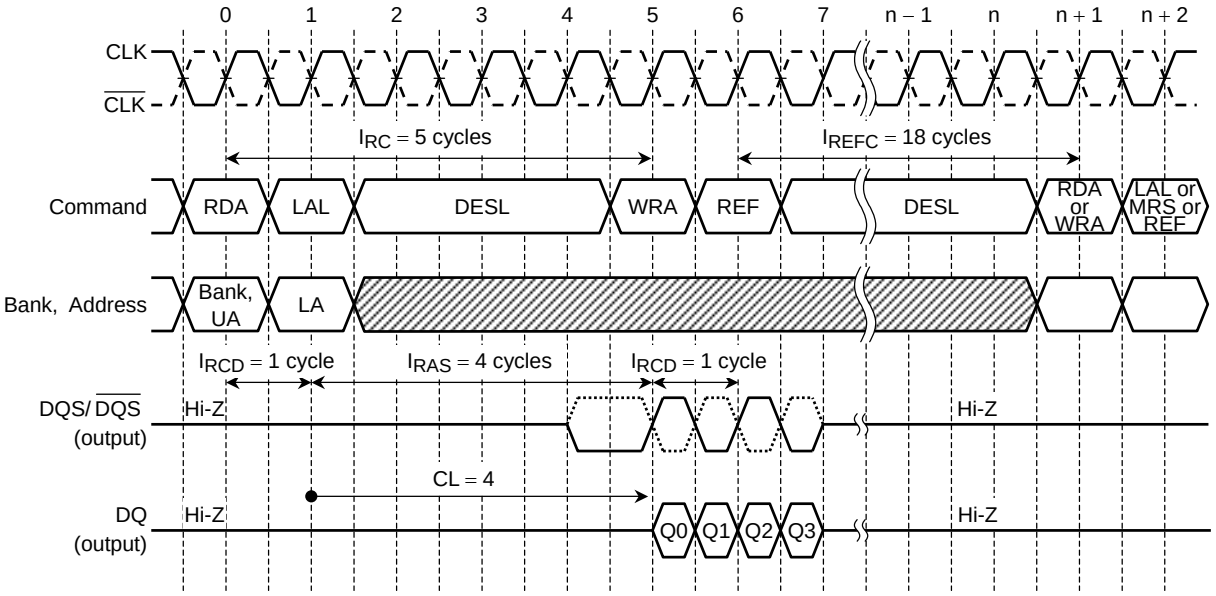
EXTENDED MODE REGISTER SET TIMING (CL = 4, BL = 4)

From Write operation to Extended Mode Register Set operation.

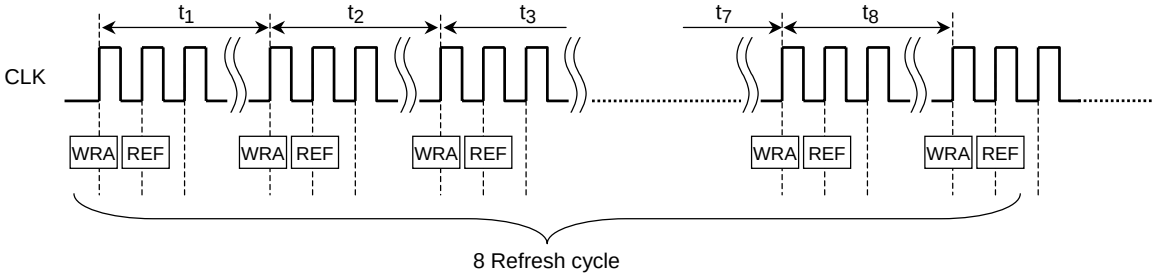


Note: DLL switch in Extended Mode Register must be set to enable mode for normal operation.
DLL lock-on time is needed after initial EMRS operation. See Power Up Sequence.
Minimum delay from LAL following WRA to RDA of EMRS operation is WL+BL/2.
TC59LM914AMG doesn't have $\overline{DQS}$.

AUTO-REFRESH TIMING (CL = 4, BL = 4)



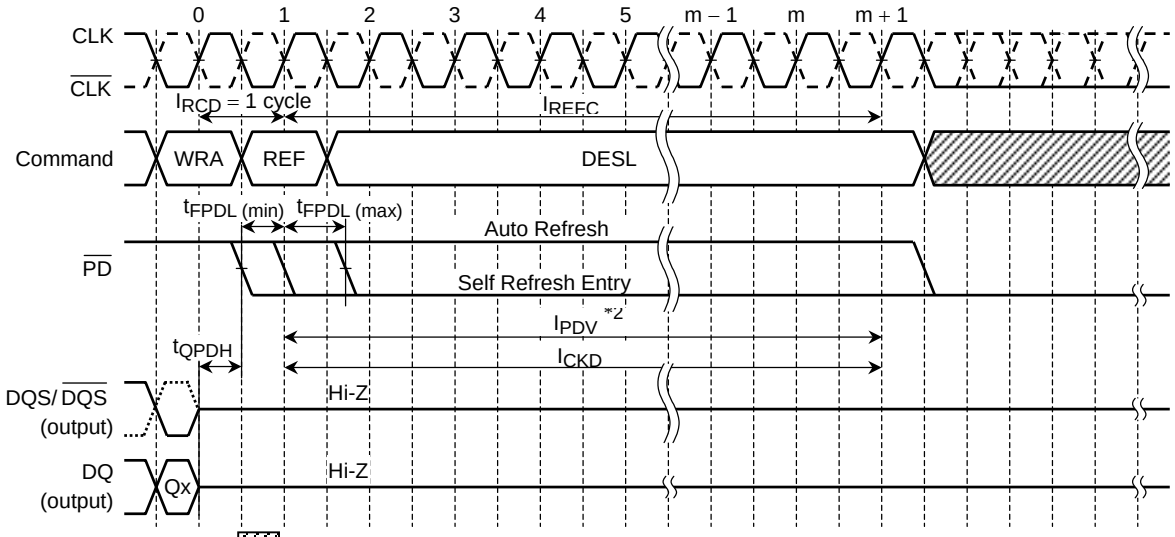
Note: In case of CL = 4, I_{REFC} must be meet 18 clock cycles.
When the Auto-Refresh operation is performed, the synthetic average interval of Auto-Refresh command specified by t_{REFI} must be satisfied.
t_{REFI} is average interval time in 8 Refresh cycles that is sampled randomly.
TC59LM914AMG doesn't have $\overline{DQS}$.



$$t_{REFI} = \frac{\text{Total time of 8 Refresh cycle}}{8} = \frac{t_1 + t_2 + t_3 + t_4 + t_5 + t_6 + t_7 + t_8}{8}$$

t_{REFI} is specified to avoid partly concentrated current of Refresh operation that is activated larger area than Read / Write operation.

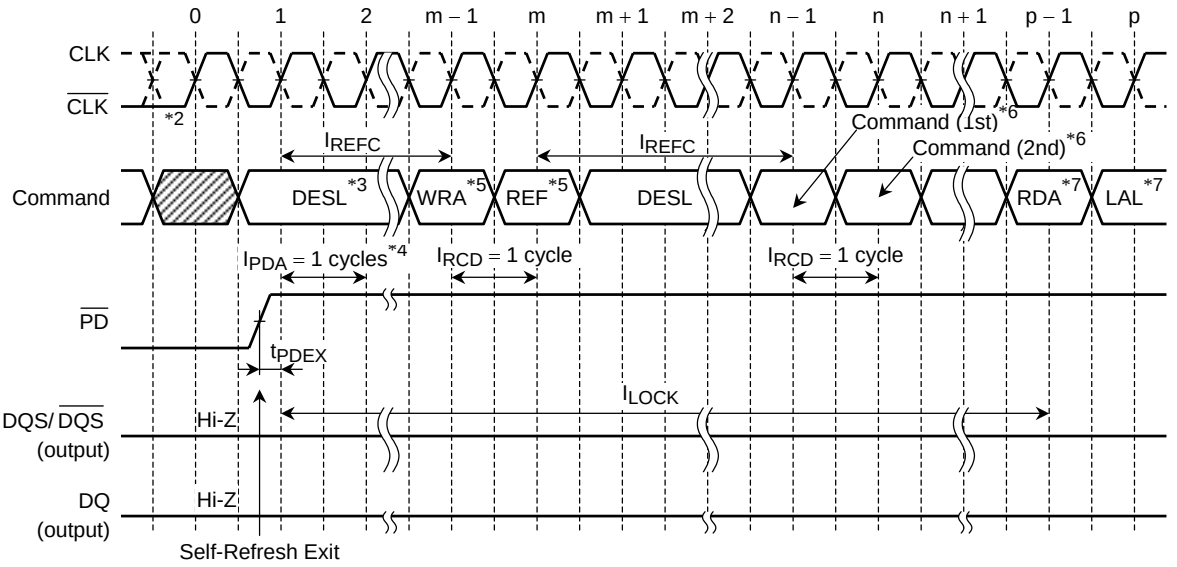
SELF-REFRESH ENTRY TIMING



Notes: 1. ▨ is don't care.

2. $\overline{PD}$ must be brought to "Low" within the timing between t_{FPDL}(min) and t_{FPDL}(max) to Self Refresh mode. When $\overline{PD}$ is brought to "Low" after t_{PDV}, FCRAM perform Auto Refresh and enter Power down mode. In case of $\overline{PD}$ fall between t_{FPDL}(max) and t_{PDV}, FCRAM will either entry Self-Refresh mode or Power down mode after Auto-Refresh operation. It can't be specified which mode FCRAM operates.
3. It is desirable that clock input is continued at least t_{CKD} from REF command even though $\overline{PD}$ is brought to "Low" for Self-Refresh Entry.
4. TC59LM914AMG doesn't have $\overline{DQS}$.
5. In the case of Self-Refresh entry after Write Operation, the delay time from the LAL command following WRA to the REF command is Write Latency (WL) +3 clock cycles minimum.

SELF-REFRESH EXIT TIMING



Notes: 1. ▨ is don't care.

2. Clock should be stable prior to $\overline{PD}$ = "High" if clock input is suspended in Self-Refresh mode.
3. DESL command must be asserted during t_{REFC} after $\overline{PD}$ is brought to "High".
4. t_{PDA} is defined from the first clock rising edge after $\overline{PD}$ is brought to "High".
5. It is desirable that one Auto-Refresh command is issued just after Self-Refresh Exit before any other operation.
6. Any command (except Read command) can be issued after t_{REFC}.
7. Read command (RDA + LAL) can be issued after t_{LOCK}.
8. TC59LM914AMG doesn't have $\overline{DQS}$.

FUNCTIONAL DESCRIPTION

Network FCRAM™

FCRAM™ is an acronym of Fast Cycle Random Access Memory. The Network FCRAM™ is competent to perform fast random core access, low latency and high-speed data transfer.

PIN FUNCTIONS

CLOCK INPUTS: CLK & $\overline{CLK}$

The CLK and $\overline{CLK}$ inputs are used as the reference for synchronous operation. CLK is master clock input. The $\overline{CS}$, FN and all address input signals are sampled on the crossing of the positive edge of CLK and the negative edge of $\overline{CLK}$. The DQS and DQ output are aligned to the crossing point of CLK and $\overline{CLK}$. The timing reference point for the differential clock is when the CLK and $\overline{CLK}$ signals cross during a transition.

POWER DOWN: $\overline{PD}$

The PD input controls the entry to the Power Down or Self-Refresh modes. The $\overline{PD}$ input does not have a Clock Suspend function like a CKE input of a standard SDRAMs, therefore it is illegal to bring $\overline{PD}$ pin into low state if any Read or Write operation is being performed.

CHIP SELECT & FUNCTION CONTROL: $\overline{CS}$ & FN

The $\overline{CS}$ and FN inputs are a control signal for forming the operation commands on FCRAM™. Each operation mode is decided by the combination of the two consecutive operation commands using the $\overline{CS}$ and FN inputs.

BANK ADDRESSES: BA0~BA2

The BA0 to BA2 inputs are latched at the time of assertion of the RDA or WRA command and are selected the bank to be used for the operation. BA0 and BA1 also define which mode register is loaded during the Mode Register Set command (MRS or EMRS).

	BA0	BA1	BA2
Bank #0	0	0	0
Bank #1	1	0	0
Bank #2	0	1	0
Bank #3	1	1	0
Bank #4	0	0	1
Bank #5	1	0	1
Bank #6	0	1	1
Bank #7	1	1	1

Also, when BA2 input assign to A14 input, TC59LM914/06AMG can function as 4 bank devices and can keep backward compatibility to 256Mb (4bank) Network FCRAM.

ADDRESS INPUTS: A0~A13

Address inputs are used to access the arbitrary address of the memory cell array within each bank. The Upper Addresses with Bank addresses are latched at the RDA or WRA command and the Lower Addresses are latched at the LAL command. The A0 to A13 inputs are also used for setting the data in the Regular or Extended Mode Register set cycle.

	I/O organization	UPPER ADDRESS	LOWER ADDRESS
8 bank operation	8 bits	A0~A13	A0~A8
	16 bits	A0~A13	A0~A7
4 bank operation	8 bits	A0~A13, BA2(A14)	A0~A8
	16 bits	A0~A13, BA2(A14)	A0~A7

DATA INPUT/OUTPUT: DQ0~DQ7 or DQ15

The input data of DQ0 to DQ15 are taken in synchronizing with the both edges of DQS input signal. The output data of DQ0 to DQ15 are outputted synchronizing with the both edges of DQS output signal.

DATA STROBE: DQS, $\overline{DQS}$

The DQS is bi-directional signal. Both edge of DQS are used as the reference of data input or output. In write operation, the DQS used as an input signal is utilized for a latch of write data. In read operation, the DQS is an output signal provides the read data strobe.

TC59LM906AMG has differential data strobe pin ($\overline{DQS}$). When $\overline{DQS}$ is enable mode, $\overline{DQS}$ is differential output signal for DQS in read operation, data input are latched at the crossing point of DQS and $\overline{DQS}$ in Write operation. When $\overline{DQS}$ is disable mode, $\overline{DQS}$ is always Hi-Z, and data input are latched at the crossing point of DQS and VREF level. $\overline{DQS}$ mode is set at Extended Mode Register Set Cycle.

TC59LM914AMG doesn't have $\overline{DQS}$ pin. Data input are latched at the crossing point of L/UDQS and VREF level in Write operation. LDQS is strobe signal for DQ0-DQ7. UDQS is strobe signal for DQ8-DQ15.

POWER SUPPLY: V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}

V_{DD} and V_{SS} are power supply pins for memory core and peripheral circuits.
V_{DDQ} and V_{SSQ} are power supply pins for the output buffer.

REFERENCE VOLTAGE: V_{REF}

V_{REF} is reference voltage for all input signals.

COMMAND FUNCTIONS and OPERATIONS

TC59LM914/06AMG are introduced the two consecutive command input method. Therefore, except for Power Down mode, each operation mode decided by the combination of the first command and the second command from stand-by states of the bank to be accessed.

Read Operation (1st command + 2nd command = RDA + LAL)

Issuing the RDA command with Bank Addresses and Upper Addresses to the idle bank puts the bank designated by Bank Address in a read mode. When the LAL command with Lower Addresses is issued at the next clock of the RDA command, the data is read out sequentially synchronizing with the both edges of DQS/$\overline{\text{DQS}}$ output signal (Burst Read Operation). The initial valid read data appears after $\overline{\text{CAS}}$ latency from the issuing of the LAL command. The valid data is outputted for a burst length. The $\overline{\text{CAS}}$ latency, the burst length of read data and the burst type must be set in the Mode Register beforehand. The read operated bank goes back automatically to the idle state after l_{RC}. $\overline{\text{DQS}}$ is differential data strobe signal supported TC59LM906AMG.

Write Operation (1st command + 2nd command = WRA + LAL)

Issuing the WRA command with Bank Addresses and Upper Addresses to the idle bank puts the bank designated by Bank Address in a write mode. When the LAL command with Lower Addresses is issued at the next clock of the WRA command, the input data is latched sequentially synchronizing with the both edges of DQS/$\overline{\text{DQS}}$ input signal (Burst Write Operation). The data and DQS/$\overline{\text{DQS}}$ inputs have to be asserted in keeping with clock input after $\overline{\text{CAS}}$ latency-1 from the issuing of the LAL command. The DQS/$\overline{\text{DQS}}$ has to be provided for a burst length. The $\overline{\text{CAS}}$ latency and the burst type must be set in the Mode Register beforehand. The write operated bank goes back automatically to the idle state after l_{RC}. Write Burst Length is controlled by VW0 and VW1 inputs with LAL command. See VW truth table. $\overline{\text{DQS}}$ is differential data strobe signal supported TC59LM906AMG.

Auto-Refresh Operation (1st command + 2nd command = WRA + REF)

TC59LM914/06AMG are required to refresh like a standard SDRAM. The Auto-Refresh operation is begun with the REF command following to the WRA command. The Auto-Refresh mode can be effective only when all banks are in the idle state. In a point to notice, the write mode started with the WRA command is canceled by the REF command having gone into the next clock of the WRA command instead of the LAL command. The minimum period between the Auto-Refresh command and the next command is specified by l_{REFC}. However, about a synthetic average interval of Auto-Refresh command, it must be careful. In case of equally distributed refresh, Auto-Refresh command has to be issued within once for every 3.9 μs by the maximum. In case of burst refresh or random distributed refresh, the average interval of eight consecutive Auto-Refresh command has to be more than 400 ns always. In other words, the number of Auto-Refresh cycles that be performed within 3.2 μs (8 × 400 ns) is to 8 times in the maximum.

Self-Refresh Operation (1st command + 2nd command = WRA + REF with $\overline{\text{PD}}$= "L")

In case of Self-Refresh operation, refresh operation can be performed automatically by using an internal timer. When all banks are in the idle state and all outputs are in Hi-Z states, the TC59LM914/06AMG become Self-Refresh mode by issuing the Self-Refresh command. $\overline{\text{PD}}$ has to be brought to "Low" within t_{FPDL} from the REF command following to the WRA command for a Self-Refresh mode entry. In order to satisfy the refresh period, the Self-Refresh entry command should be asserted within 3.9 μs after the latest Auto-Refresh command. Once the device enters Self-Refresh mode, the DESL command must be continued for l_{REFC} period. In addition, it is desirable that clock input is kept in l_{CKD} period. The device is in Self-Refresh mode as long as $\overline{\text{PD}}$ held "Low". During Self-Refresh mode, all input and output buffers are disabled except for $\overline{\text{PD}}$, therefore the power dissipation lowers. Regarding a Self-Refresh mode exit, $\overline{\text{PD}}$ has to be changed over from "Low" to "High" along with the DESL command, and the DESL command has to be continuously issued in the number of clocks specified by l_{REFC}. The Self-Refresh exit function is asynchronous operation. It is required that one Auto-Refresh command is issued to avoid the violation of the refresh period just after l_{REFC} from Self-Refresh exit.

Power Down Mode ($\overline{\text{PD}}$= "L")

When all banks are in the idle state and DQ outputs are in Hi-Z states, the TC59LM914/06AMG become Power Down Mode by asserting $\overline{\text{PD}}$ is "Low". When the device enters the Power Down Mode, all input and output buffers are disabled after specified time except for $\overline{\text{PD}}$. Therefore, the power dissipation lowers. To exit the Power Down Mode, $\overline{\text{PD}}$ has to be brought to "High" and the DESL command has to be issued for two clock cycle after $\overline{\text{PD}}$ goes high. The Power Down exit function is asynchronous operation.

Mode Register Set (MRS) and Extended Mode Register Set (EMRS)
(1st command + 2nd command = RDA + MRS)

When all banks are in the idle state, issuing the MRS command following to the RDA command can program the Mode Register. In a point to notice, the read mode started with the RDA command is canceled by the MRS command having gone into the next clock of the RDA command instead of the LAL command. The data to be set in the Mode Register is transferred using A0 to A13, BA0 to BA2 address inputs. The TC59LM914/06AMG have two mode registers. These are Regular and Extended Mode Register. The Regular or Extended Mode Register is chosen by BA0 and BA1 in the MRS command. The Regular Mode Register designates the operation mode for a read or write cycle. The Regular Mode Register has four function fields.

The four fields are as follows:
(R-1) Burst Length field to set the length of burst data
(R-2) Burst Type field to designate the lower address access sequence in a burst cycle
(R-3) $\overline{\text{CAS}}$ Latency field to set the access time in clock cycle
(R-4) Test Mode field to use for supplier only.

The Extended Mode Register has four function fields.
The five fields are as follows:
(E-1) DLL Switch field to choose either DLL enable or DLL disable.
(E-2) Output Driver Impedance Control field.
(E-3) Off-Chip Driver (OCD) Impedance Adjustment for full strength output driver.
(E-4) $\overline{\text{DQS}}$ enable field.

Once those fields in the Mode Register are set up, the register contents are maintained until the Mode Register is set up again by another MRS command or power supply is lost. The initial value of the Regular or Extended Mode Register after power-up is undefined, therefore the Mode Register Set command must be issued before proper operation.

- Regular Mode Register/Extended Mode Register change bits (BA0, BA1)
  These bits are used to choose either Regular MRS or Extended MRS

BA1	BA0	Mode Register Set
0	0	Regular MRS
0	1	Extended MRS
1	×	Reserved

Regular Mode Register Fields

(R-1) Burst Length field (A2 to A0), (BL)
This field specifies the data length for column access using the A2 to A0 pins and sets the Burst Length to be 2 or 4 words.

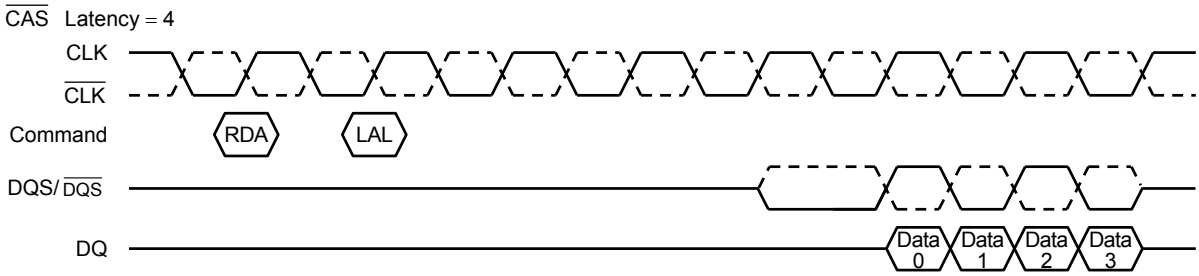
A2	A1	A0	BURST LENGTH
0	0	0	Reserved
0	0	1	2 words
0	1	0	4 words
0	1	1	Reserved
1	×	×	Reserved

(R-2) Burst Type field (A3), (BT)
The Burst Type can be chosen Interleave mode or Sequential mode. When the A3 bit is “0”, Sequential mode is selected. When the A3 bit is “1”, Interleave mode is selected. Both burst types support burst length of 2 and 4 words.

A3	BURST TYPE
0	Sequential
1	Interleave

- Addressing sequence of Sequential mode

  A column access is started from the inputted lower address and is performed by incrementing the lower address input to the device.



Addressing sequence for Sequential mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	n	2 words (address bits is LA0) not carried from LA0~LA1
Data 1	n + 1	
Data 2	n + 2	4 words (address bits is LA1, LA0) not carried from LA1~LA2
Data 3	n + 3	

- Addressing sequence of Interleave mode

  A column access is started from the inputted lower address and is performed by interleaving the address bits in the sequence shown as the following.

Addressing sequence for Interleave mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	···A8 A7 A6 A5 A4 A3 A2 A1 A0	2 words
Data 1	···A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data 2	···A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	4 words
Data 3	···A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	

(R-3) $\overline{CAS}$ Latency field (A6 to A4), (CL)

This field specifies the number of clock cycles from the assertion of the LAL command following the RDA command to the first data read. The minimum values of $\overline{CAS}$ Latency depends on the frequency of CLK. In a write mode, the place of clock that should input write data is $\overline{CAS}$ Latency cycles – 1.

A6	A5	A4	$\overline{CAS}$ LATENCY
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

(R-4) Test Mode field (A7), (TE)

This bit is used to enter Test Mode for supplier only and must be set to “0” for normal operation.

(R-5) Reserved field in the Regular Mode Register

- Reserved bits (A8 to A13, BA2)

  These bits are reserved for future operations. They must be set to “0” for normal operation.

Extended Mode Register fields

(E-1) DLL Switch field (A0), (DS)

This bit is used to enable DLL. When the A0 bit is set "0", DLL is enabled. This bit must set to "0" for normal operation.

(E-2) Output Driver Impedance Control field (A1, A6) (DIC)

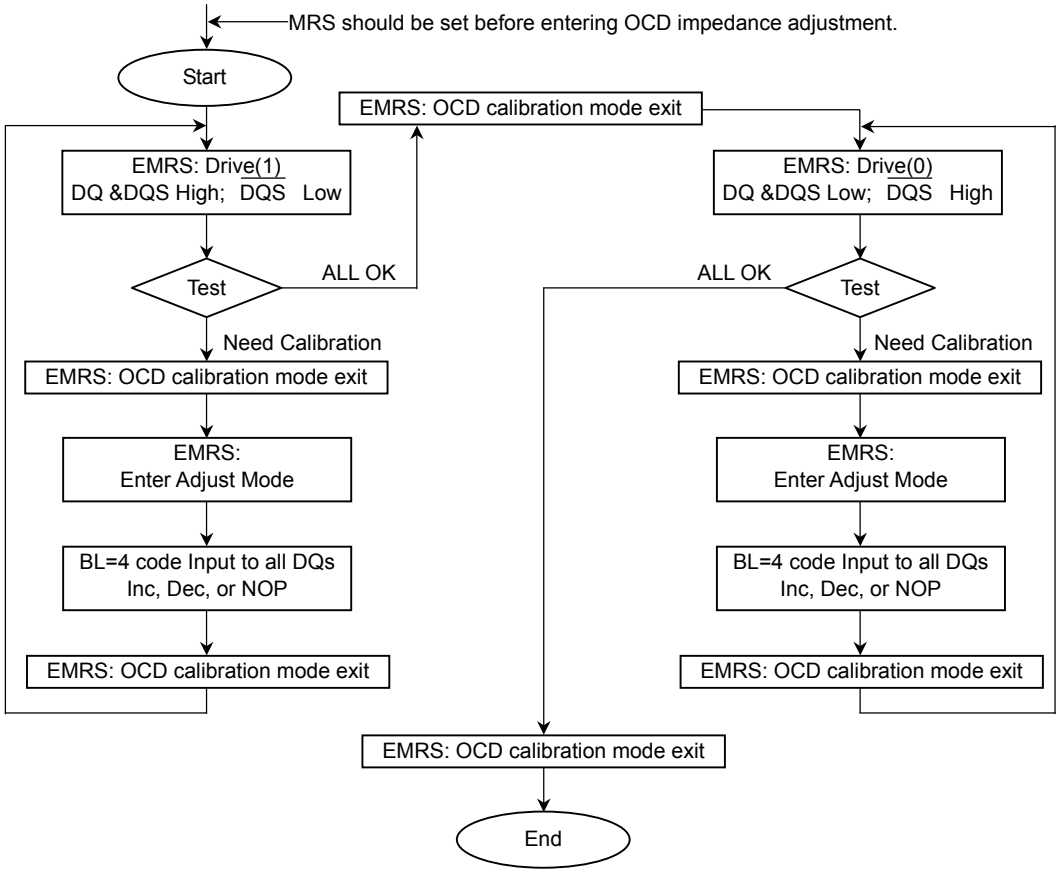
This field is used to choose Output Driver Strength. Four types of Driver Strength are supported. Output Driver Strength can be set by field in EMRS with OCD calibration default (A7~A9=1 at EMRS).

A6	A1	OUTPUT DRIVER IMPEDANCE CONTROL
0	0	Normal Output Driver
0	1	Strong Output Driver
1	0	Weak Output Driver
1	1	Full Strength Output Driver

(E-3) Off-Chip Driver (OCD) Impedance Adjustment for full strength output driver (A7 to A9) (OCD)

Output Driver Strength can be set by DIC field (E-2). In case of choosing Full strength Output Driver, OCD calibration is available. The driver strength set by DIC field is the initial driver level at OCD Impedance Adjustment. When OCD calibration is performed, A1 and A6 inputs at EMRS must be "1" for Full Strength Output Driver.

The Network FCRAM™ supports driver calibration feature and the flow chart below is an example of sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment.



Extended Mode Register Set for OCD Impedance adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by Network FCRAM. In drive (1) mode, all DQ, DQS signals are driven high and $\overline{DQS}$ signals are driven low. In drive (0) mode, all DQ, DQS signals are driven low and $\overline{DQS}$ signals are driven high. In adjust mode, BL=4 of operation code data must be used

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive (1) DQ, DQS high and $\overline{DQS}$ low
0	1	0	Drive (0) DQ, DQS low and $\overline{DQS}$ high
1	0	0	Adjust mode
1	1	1	OCD calibration default

OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to Network FCRAM. For this operation, Burst Length has to be set to BL=4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DQs simultaneously and after OCD calibration, all DQs of a given Network FCRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect.

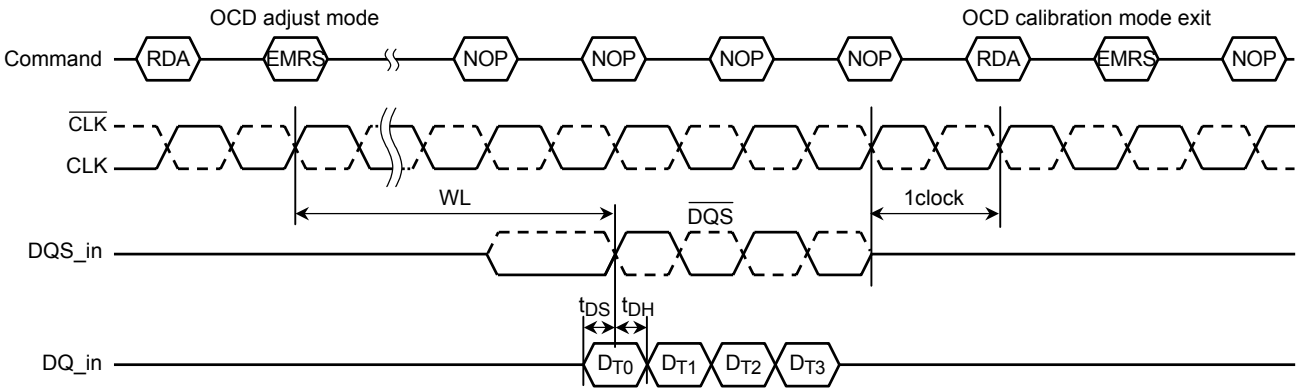
Off-Chip Driver Program

4bit burst code inputs to all DQs				Operation	
D_{T0}	D_{T1}	D_{T2}	D_{T3}	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

For proper operation of adjust mode, WL=CL-1 clocks and t_{DS} / t_{DH} should be met as the following timing diagram. For input data pattern for adjustment, DT0~DT3 is a fixed order and "not affected by MRS addressing mode (i.e. Sequential or interleave).

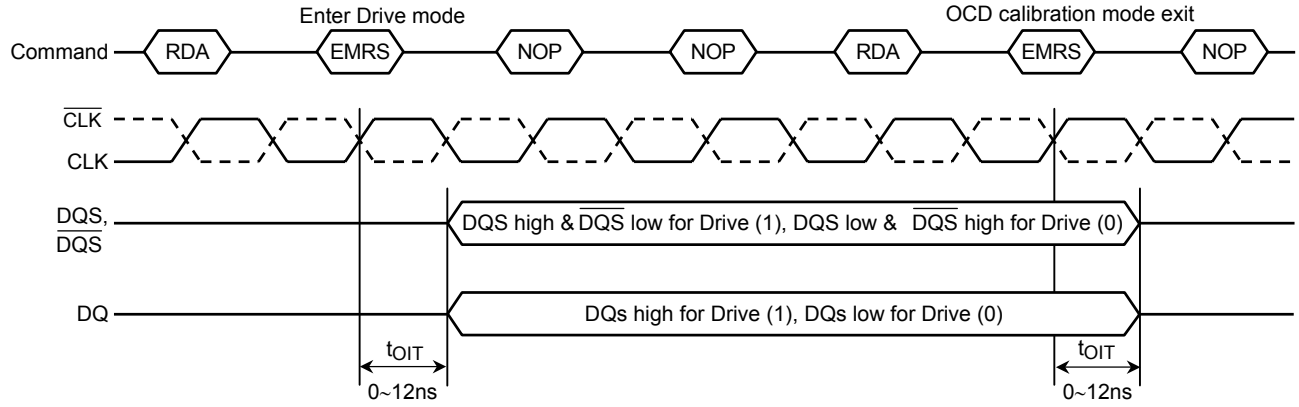
Driver strength is controlled within the following range by OCD impedance adjustment.

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
I_{OH} (DC)	Full Strength Output Driver	Output Source DC Current for $V_{DD}Q$ = 1.7V~1.9V $V_{DD}Q$ = 1.7V V_{OH} = 1.420V	−14.0	−18.7	mA	
I_{OL} (DC)		Output Sink DC Current for $V_{DD}Q$ = 1.7V~1.9V $V_{DD}Q$ = 1.7V V_{OL} = 0.280V	14.0	18.7		



Drive mode

Drive mode, both Drive (1) and Drive (0), is used for controllers to measure Network FCRAM Driver impedance. In this mode, all outputs are driven out t_{OIT} after "enter drive mode" command and all output drivers are turned-off t_{OIT} after "OCD calibration mode exit" command as the following timing diagram.



(E-4) $\overline{DQS}$ enable field (A10), ($\overline{DQS}$)

This bit is used to enable Differential Data strobe.

$\overline{DQS}$ is available on TC59LM906AMG. This field of TC59LM914AMG is ignored.

A10	$\overline{DQS}$ Enable
0	Disable
1	Enable

(E-5) Interface mode select (A11)

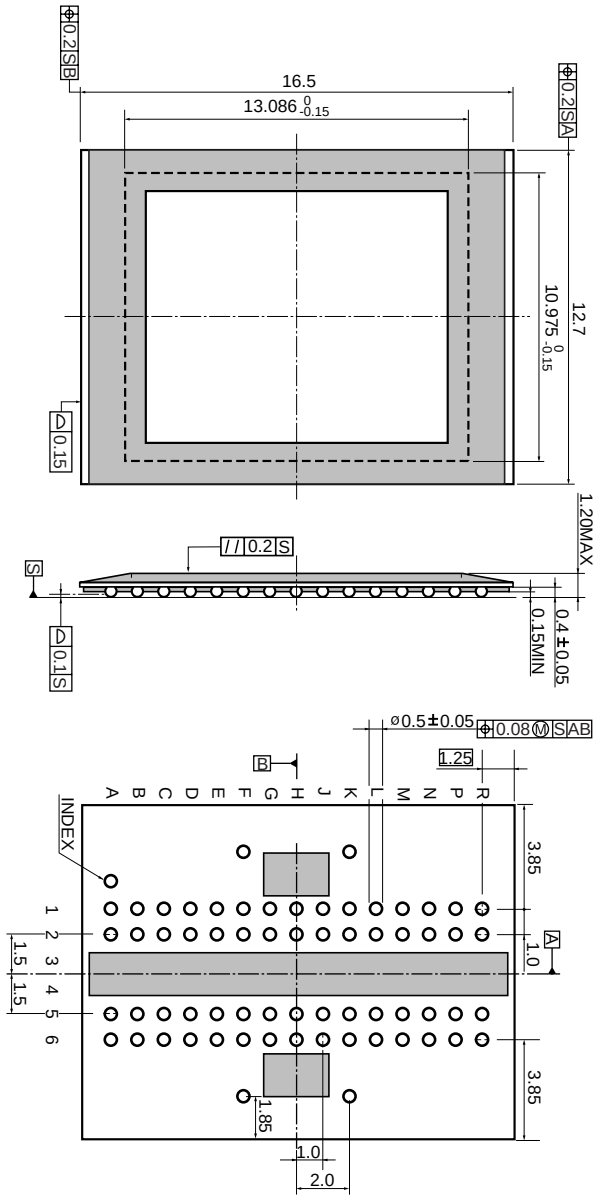
This bit must be always set "0".

(E-6) Reserved field (A2 to A5, A12 to A13, BA2)

These bits are reserved for future operations and must be set to "0" for normal operation.

PACKAGE DIMENSIONS

P-BGA64-1317-1.00AZ



Note: In order to support a package, four outer balls located on F and K row are required to assembly to board. These four ball is not connected to any electrical level.

Weight: 0.23g (typ.)

REVISION HISTORY

– Rev.0.9 (Feb. 27 '2004)

– Rev0.91 (Mar. 16 '2004)
- Corrected TYPO (page57). Pin name is changed from "Q" to "R".

– Rev0.92 (Apr. 21 '2004)
- Parameter definition in Recommended DC, AC Operating Conditions Table are changed (page 5).
  – V_{ICK}(DC): Differential ~~Clock~~ DC Input Voltage
  – V_{ID}(DC): Input DC Differential Voltage. ~~CLK and /CLK inputs (DC)~~
  – V_{ID}(AC): Input AC Differential Voltage. ~~CLK and /CLK inputs (AC)~~
  – V_{ID}(AC),min is changed from 0.55V to 0.5V.
  – V_{ISO}(AC): Differential ~~Clock~~ AC Middle Level.
- CLK is changed to V_{TR} and $\overline{CLK}$ is changed to V_{CP} (page 6).
- Below comment is added in Note(10) (page 6).
  VTR is the true input (such as CLK, DQS) level and VCP is the complementary input (such as $\overline{CLK}$, $\overline{DQS}$) level.

– Rev0.93 (Jun. 9 '2004)
- Package name (P–BGA64–1317–1.00AZ) added (page 1).
- t_{REFI} (Auto-Refresh Average Interval) spec changed from 7.8µs to 3.9µs (page 1, 10, 51).
- V_{DD} range changed from 2.5V ± 0.15V to 2.5V ± 0.125V.
- Corrected TYPO (page 9, 10, 14, 15, 17)
- t_{DSP} spec changed for all speed bin as below (page 9)
  $t_{DSP(min)} = 0.4 \times t_{CK} \rightarrow 0.35 \times t_{CK}$
  $t_{DSP(max)} = 0.6 \times t_{CK} \rightarrow 0.65 \times t_{CK}$
- t_{IS} and t_{IH} spec changed for all speed bin as below (page 9)
  "–37": $t_{IS} = 0.6ns \rightarrow 0.5ns$, $t_{IH} = 0.6ns \rightarrow 0.5ns$
  "–45": $t_{IS} = 0.7ns \rightarrow 0.6ns$, $t_{IH} = 0.7ns \rightarrow 0.6ns$
  "–50": $t_{IS} = 0.8ns \rightarrow 0.7ns$, $t_{IH} = 0.8ns \rightarrow 0.7ns$
- t_{DSH} (DQS Input Falling Edge Hold Time from CLK) added (page 9).
- t_{OIT} (OCD drive mode output delay time) added (page 10, 56).
- OCD definition at power up sequence added (page 12).
- Note (4) added at power up sequence (page 12).
- OCD setting on Extended Mode Register table changed as below (page 21, 54, 55)
  (A9, A8, A7) = (0, 0, 0): OCD Calibration default → OCD Calibration mode exit.
  (A9, A8, A7) = (1, 1, 1): OCD Calibration mode exit → OCD Calibration mode default.
- Full strength Output Driver added on DIC (page 21, 54).
  (A6, A1) = (1, 1): Reserved → Full Strength Output Driver.
- Note (5) added on Self-Refresh Entry Timing (page 48).
- Explanation for OCD Impedance Adjustment modified (page 54).
- I_{OH} / I_{OL} table added (page 55).

– Rev1.0 (Aug. 20 '2004)
- "-45" version dropped.
- Some notes in the page 8 moved to page 7 (page 7, 8).
- Note 2 changed as below (page 7).
  Before: These parameters depend on the output loading. The specified values are obtained with the output open
  After: These parameters define the current between V_{DD} and V_{SS}.
- Corrected TYPO (page 2, 3, 14, 15, 17).
- Package weight (0.23g) added (page 57).

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