TELEDYNE COMPONENTS

HIGH FREQUENCY, HYBRID VOLTAGE TO FREQUENCY CONVERTER

FEATURES

- Full Scale Output 10MHz
- Fully Differential Input
- Dynamic Range 100dB
- Linearity 11-Bit
- Supplies ..... ±14V to ±18V
- Easily Modified for Different I/O Signals

APPLICATIONS

- Two-Wire Digital Data Transmission
- Ratiometric Data Conversion
- Long Term Integrators
- Fiber Optic Data Links
- FM Modulation

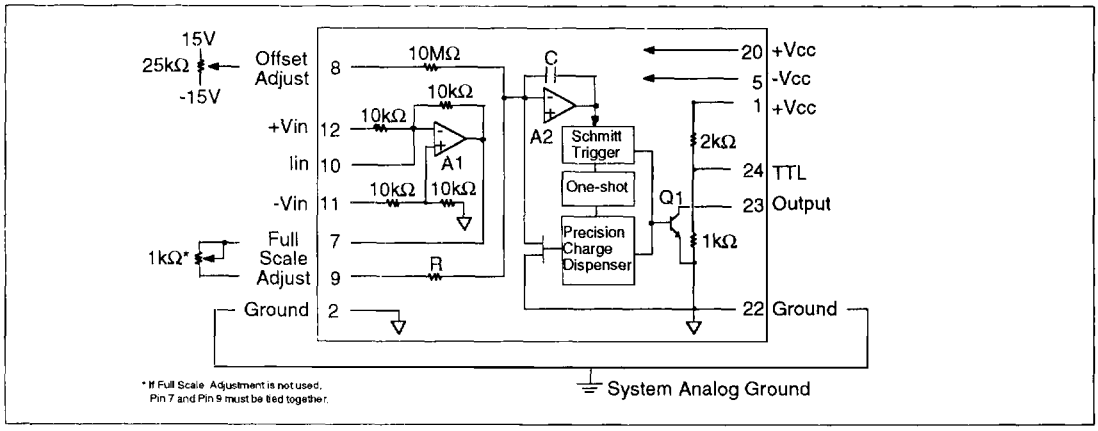
GENERAL DESCRIPTION

The 4743 hybrid voltage to frequency converter offers a full scale output of 10MHz, and can be externally trimmed to any value from its rated full scale output down to 2.5 MHz. The 4743 has full differential input and can be driven with positive voltage, negative voltage, or positive current. Common mode rejection ratio, with VCM = 10 volts, is 80 dB. With external resistors, the input is easily adapted to accept almost any input signal range. The output stage of the unit is a single uncommitted transistor that operates as a saturated switch. A pull-up resistor for TTL compatibility is internal to the 4743. An external resistor can be added to make the output CMOS compatible, and the output can drive 10 TTL loads.

The 4743 has quick response time, and settles to within ±0.01%FS of a new frequency in 15 µsec. Overload recovery time is approximately 10 output signal periods. Dynamic range is greater than 100 dB, and input/output linearity over a ±10 mV to ±10.5V input range is ±0.05%FS plus ±0.05% of signal. Initial zero offset error is ±8 mV (8 kHz). Zero Offset error is externally adjustable to zero. Initial full scale accuracy is ±50 kHz, and full scale error is also externally adjustable to zero. If full scale adjust is not employed, Pins 7 and 9 must be tied together.

The standard 4743 is specified for 0°C to +70°C operation. The -HR version is specified for -55°C to +125°C operation.

BLOCK DIAGRAM

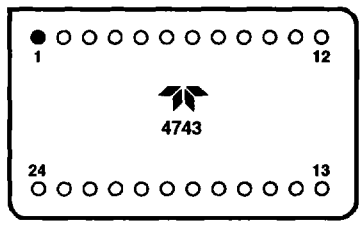


4743

PIN CONFIGURATION

Pin No.	Designation	Pin No.	Designation
1	$+V_{CC}$	24	TTL
2	GROUND	23	f_{OUT}
3	NC	22	GROUND
4	NC	21	NC
5	$-V_{CC}$	20	$+V_{CC}$
6	NC	19	NC
7	FULL SCALE ADJUST	18	NC
8	OFFSET ADJUST	17	NC
9	FULL SCALE ADJUST	16	NC
10	$+I_{IN}$	15	NC
11	$-V_{IN}$	14	NC
12	$+V_{IN}$	13	NC

NC = No internal connection



ABSOLUTE MAXIMUM RATINGS

V_{CC} Power Supplies ..... ±22V
$\pm V_{IN}$ Input Voltage (Note 1) ..... ±15V
V_{ID} Differential Input Voltage ..... V_{CC}
I_{IN} Current Input ..... 2.1 mA
T_C Specified Temperature Range, Case
4743 ..... 0°C to +70°C
4743-HR ..... -55°C to +125°C
T_{STG} Storage Temperature Range ..... –65°C to +150°C

ELECTRICAL CHARACTERISTICS: T_C = +25°C, $\pm V_{CC}$ = ±15V, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
$+V_{IN}$	Positive Input Range (Note 1)	For specified linearity	0.0001	—	10.5	V
$-V_{IN}$	Negative Input Range	For specified linearity	-0.0001	—	-10.5	V
V_{CM}	Common Mode Input Range		—	—	±10	V
CMRR	Common Mode Rejection Ratio		60	80	—	dB
V_{ID}	Differential Input Voltage	Referenced to $-V_{IN}$	10.5	12	—	V
I_{IN}	Current Input Range		0.0001	—	1.2	mA
	Input Dynamic Range		100	—	—	dB
V_{OS}	Input Offset Voltage	Adjustable to zero	—	±8	±20	mV
V_{OS} TC	Input Offset Drift		—	—	±100	µV/°C
$PSRR_1$	V_{OS} vs. Power Supplies	Constant voltage at Pin 8	—	—	±20	µV/%

ELECTRICAL CHARACTERISTICS: (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input (cont.)						
R_{+IN}	$+V_{IN}$ Input Impedance		—	10	—	kΩ
R_{-IN}	$-V_{IN}$ Input Impedance		—	20	—	kΩ
R_{IIN}	I_{IN} Input Impedance	Virtual Ground	—	<0.1	—	Ω
Output						
V_{OH}	Output High Voltage	I_{OH} = 400 µA	**2.4**	—	**5**	V
V_{OL}	Output Low Voltage	I_{OL} = -16 mA	—	—	**0.4**	V
R_O	Output Impedance		632	666	700	Ω
Dynamic						
ts	Settling Time to ±0.01% 10V step		—	15	—	µs
	Overload Recovery	ΔV_{IN} = +20V to +10V	—	—	10	Cycles
Transfer						
f_O	Output Frequency	ΔV_{IN} equals V_{IN} - ($-V_{IN}$)		$[\Delta V_{IN} \times f_A] \div 10V$ $[I_{IN} \times f_A] \div I_{FS}$		MHz MHz
f_A	Full Scale Frequency	@ V_{IN} = 10.0000V pins 7 & 9 shorted @ 25°C	**10**	**10.1**	**10.2**	MHz
I_{FS}	Full Scale Current		.75	1	1.25	mA
$f_A T_C$	f_A vs Temperature	$T_C = T_{MIN}$ to T_{MAX}	—	**±40**	**±100**	ppm/°C
$I_{FS} T_C$	I_{FS} vs Temperature		—	30	—	ppm/°C
±PSRR	f_A vs Power Supplies	@ 10 MHz, ±14 to ±18V	**-125**	—	**125**	ppm/%ΔV
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V, V_{dif} = .5V	**60**	—	**120**	dB
$+V_{INLE}$	$+V_{IN}$ Linearity Error (Note 2)	V_{IN} = 10 mV to 10V	**-.100**	**<.05**	**.100**	%FS
$-V_{INLE}$	$-V_{IN}$ Linearity Error (Note 2)		-.100	<.05	.100	%FS
I_{INLE}	I_{IN} Linearity Error (Note 2)		-.100	<.05	.100	%FS
t_{PW}	Output Pulse Width	@ 10 MHz	**20**	—	**65**	ns
Power Supplies						
V_{CC}	Voltage Range		±14	±15	±18	V
	Voltage Asymmetry	$\|V_{CC}\| - \|-V_{CC}\|$	—	—	±4	V
$+I_{CC}$	Positive Supply Quiescent Current		—	**75**	**90**	mA
$-I_{CC}$	Negative Supply Quiescent Current		—	**-25**	**-35**	mA
P_D	Power Dissipation		—	1500	1875	mW

NOTES:
1. $+V_{IN}$ has a 10kΩ internal resistor and a 2 mA maximum input current limit. The Voltage input, if current limited by a series input resistor, is virtually unlimited.
2. Linearity specifications apply only after offset and gain have been trimmed to nominal.
3. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested. HR product tested at +125°C, +25°C and -55°C unless otherwise noted. Standard parts tested at room temperature only.

APPLICATION INFORMATION

To take maximum advantage of the 4743's versatility, a functional block diagram and theory of operation are provided. With this information, input and output circuitry are easily understood and adapted to handle virtually any signal or load.

The 4743 is a free-running (astable) voltage controlled multivibrator. A true differential input amplifier, (A_1), allows the device to be driven by positive input voltage applied to Pin 12 (with Pin 11 open or grounded), by negative voltage applied to Pin 11 (with Pin 12 open or grounded), by differential voltages applied between Pins 12 and 11 (V_{IN} = $+V_{IN}$ - ($-V_{IN}$)), or by positive current applied to Pin 10. CMRR with VCM = 10V is typically 80 dB.

No combination of input signals that will drive the output of amplifier A_1 positive is permitted. The trigger circuit has a positive threshold level and will not respond to the negative signals that would result from a positive A_1 output.

Operating with any of the input conditions described above results in a negative voltage at the output of A_1. Resistor R, amplifier A_2, and capacitor C(100 pF) form an integrator. C charges as a precise linear function of the V/F's input signal. When the voltage (charge) impressed on C reaches a fixed precise threshold, the trigger circuit triggers the one-shot (monostable) multivibrator, which in turn produces a constant-width output pulse. This pulse performs two functions. Amplified by Q_1, it becomes the output of the V/F and at the same time, it activates the precision charge dispenser (PCD).

The PCD discharges C to the same "zero" level every time an output pulse is produced. Thus, capacitor C is repeatedly charged between two precise voltages at a rate which is a linear function of the V/F input signal. That is, the rate of charging C, the repetition rate of reaching the trigger threshold, and the output frequency are all functions of the V/F voltage and/or current inputs.

Offset and Full Scale Trim Theory

Offset and full scale trim are performed at the input circuit. Offset is adjusted with a 25 kΩ potentiometer between $+V_{CC}$ and $-V_{CC}$, with its wiper tied to Pin 8. The subsequent voltage applied to Pin 8 falls across a 10 MΩ resistor to become a constant positive or negative current directly injected into the integrator capacitor.Full scale is adjusted by varying the integrator's input resistance with a series 1 kΩ potentiometer connected between Pins 7 and 9. This adjustment can only lower the V/F's full scale output frequency, so units are laser trimmed at the factory to have initial full scale output errors that are always positive. By placing a fixed resistor in series with the adjusting potentiometer, the full scale output frequency can be lowered to 2.5 MHz. If full scale adjustment is not employed, Pins 7 and 9 must be tied together with as short a jumper as possible.

4743 Output Circuit

The TTL logic pulse train from the V/F is designed to drive 10 TTL loads with ±15V supplies. The output circuit is a single transistor (Q_1) connected as a saturated switch with an uncommitted 2 kΩ pull-up resistor. With Pins 23 and 24 connected together, the output is approximately zero volts when Q_1 is on. With Q_1 off, the output voltage is $+V_{CC}/3$ or +5V when $+V_{CC}$ = +15V. If Pin 23 is not connected to Pin 24, an external divider must be provided. The output circuit is easily adapted to drive CMOS logic by paralleling the 2 kΩ resistor with an external resistor large enough to bring the output up to the desired level. The additional pull-up resistor also decreases pulse rise time when driving larger capacitive loads.

The output (collector of Q_1) may be shorted to ground indefinitely without damage. However, since Q_1 is on most of the time, a short to $+V_{CC}$ will cause certain catastrophic failure in about 5 seconds.