



54F/74F350 4-Bit Shifter with TRI-STATE® Outputs

General Description

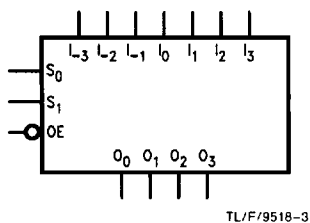
The 'F350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select (S_0 , S_1) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the TRI-STATE outputs of different packages and using the Output Enable (\overline{OE}) inputs as a third Select level. With appropriate interconnections, the 'F350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions.

Features

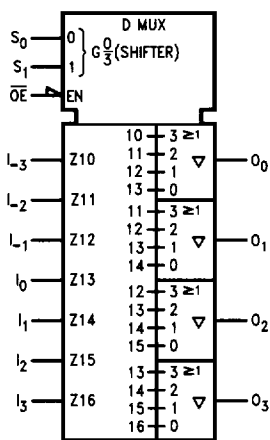
- Linking inputs for word expansion
- TRI-STATE outputs for extending shift range

Ordering Code: See Section 5

Logic Symbols

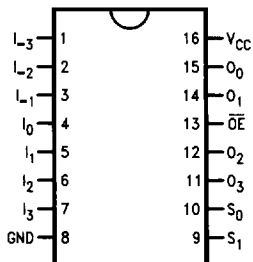


IEEE/IEC

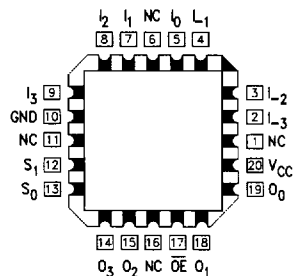


Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC and PCC



Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
S_0, S_1	Select Inputs	1.0/2.0	20 μ A/ -1.2 mA
$I_{-3}-I_2$	Data Inputs	1.0/2.0	20 μ A/ -1.2 mA
\overline{OE}	Output Enable Input (Active LOW)	1.0/2.0	20 μ A/ -1.2 mA
O_0-O_3	TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)

Functional Description

The 'F350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes successive one-bit shifts of the data word. This internal connection makes it possible to perform shifts of 0, 1, 2 or 3 places on words of any length.

A 4-bit data word is introduced at the I_n inputs and is shifted according to the code applied to the select inputs S_0, S_1 . Outputs O_0-O_3 are TRI-STATE, controlled by an active LOW output enable (\overline{OE}). When \overline{OE} is LOW, data outputs will follow selected data inputs; when HIGH, the data outputs will be forced to the high impedance state. This feature allows shifters to be cascaded on the same output lines or

to a common bus. The shift function can be logical, with zeros pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

Logic Equations

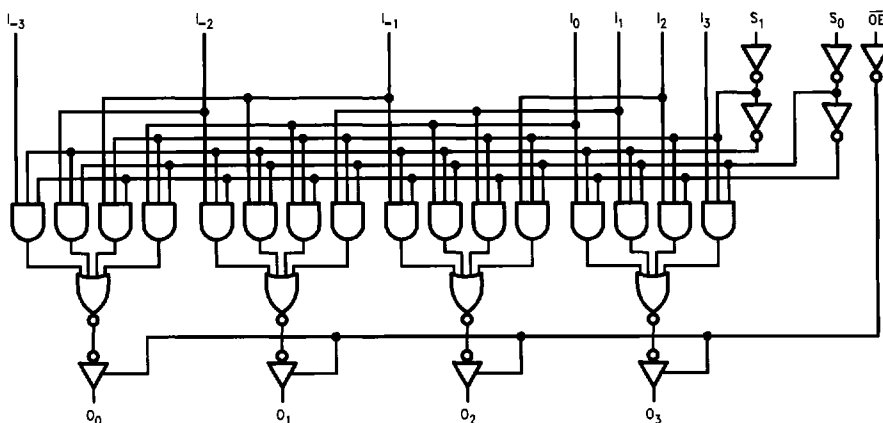
$$\begin{aligned} O_0 &= \overline{S_0}\overline{S_1}I_0 + S_0\overline{S_1}I_{-1} + \overline{S_0}S_1I_{-2} + S_0S_1I_{-3} \\ O_1 &= \overline{S_0}\overline{S_1}I_1 + S_0\overline{S_1}I_0 + \overline{S_0}S_1I_{-1} + S_0S_1I_{-2} \\ O_2 &= \overline{S_0}\overline{S_1}I_2 + S_0\overline{S_1}I_1 + \overline{S_0}S_1I_0 + S_0S_1I_{-1} \\ O_3 &= \overline{S_0}\overline{S_1}I_3 + S_0\overline{S_1}I_2 + \overline{S_0}S_1I_1 + S_0S_1I_0 \end{aligned}$$

Truth Table

Inputs			Outputs			
\overline{OE}	S_1	S_0	O_0	O_1	O_2	O_3
H	X	X	Z	Z	Z	Z
L	L	L	I_0	I_1	I_2	I_3
L	L	H	I_{-1}	I_0	I_1	I_2
L	H	L	I_{-2}	I_{-1}	I_0	I_1
L	H	H	I_{-3}	I_{-2}	I_{-1}	I_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram

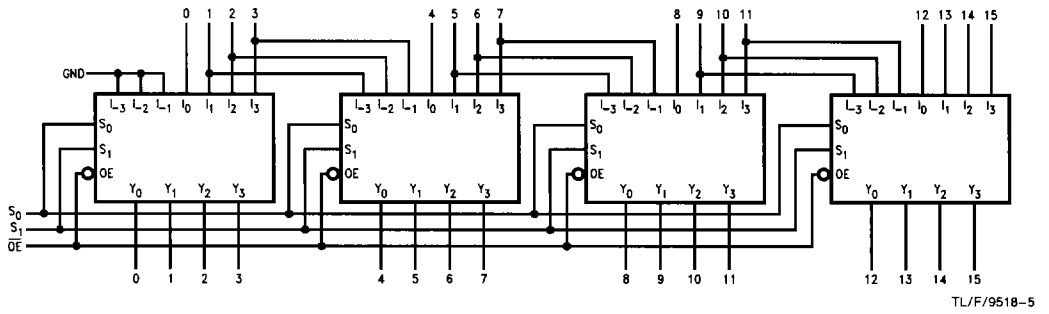


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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Applications

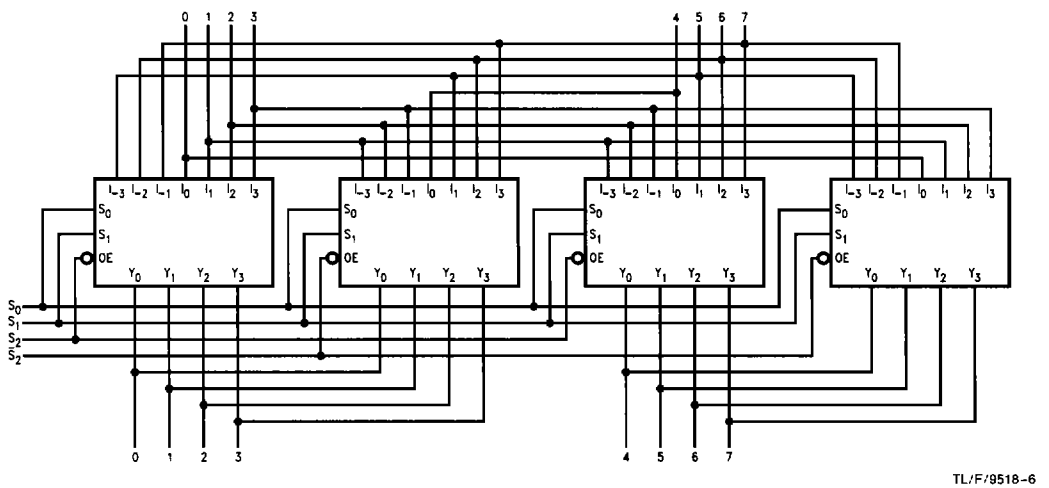
16-Bit Shift-Up 0 to 3 Places, Zero Backfill



Function Table

S ₁	S ₀	Shift Function
L	L	No Shift
L	H	Shift 1 Place
H	L	Shift 2 Places
H	H	Shift 3 Places

8-Bit End Around Shift 0 to 7 Places

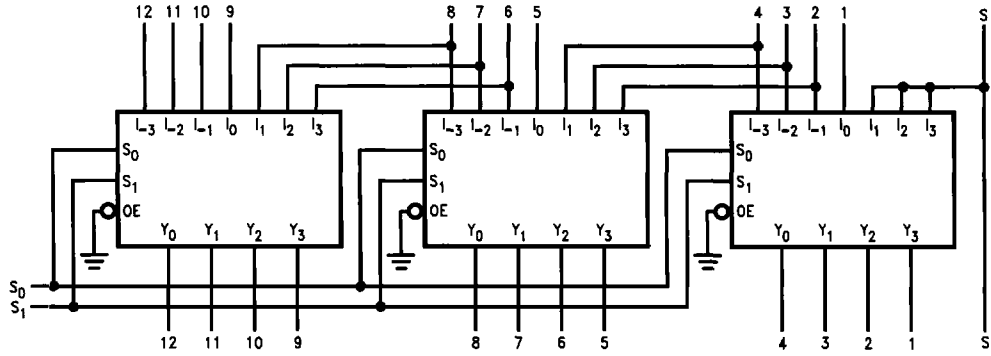


Applications (Continued)

Function Table

S ₂	S ₁	S ₀	Shift Function
L	L	L	No Shift
L	L	H	Shift End Around 1
L	H	L	Shift End Around 2
L	H	H	Shift End Around 3
H	L	L	Shift End Around 4
H	L	H	Shift End Around 5
H	H	L	Shift End Around 6
H	H	H	Shift End Around 7

13-Bit Twos Complement Scaler



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Function Table

S ₁	S ₀	Scale
L	L	$L \div 8$ $\frac{1}{8}$
L	H	$H \div 4$ $\frac{1}{4}$
H	L	$L \div 2$ $\frac{1}{2}$
H	H	H No Change 1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 10% V _{CC}	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 24 mA
I _{IH}	Input HIGH Current			20	μA	Max	V _{IN} = 2.7V
I _{BV}	Input HIGH Current Breakdown Test			100	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-1.2	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current			-60	mA	Max	V _{OUT} = 0V
I _{CEX}	Output HIGH Leakage Current			250	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = V _{CC}
I _{CCH}	Power Supply Current		34	42	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		40	57	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		40	57	mA	Max	V _O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig No
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay I _n to O _n	3.0 2.5	4.5 4.0	6.0 5.5			3.0 2.5	7.0 6.5	ns	2-3
t _{PLH} t _{PHL}	Propagation Delay S _n to O _n	4.0 3.0	7.8 6.5	10.0 8.5			4.0 3.0	13.5 9.5	ns	2-3
t _{PZH} t _{PZL}	Output Enable Time	2.5 4.0	5.0 7.0	7.0 9.0			2.5 4.0	8.0 10.0	ns	2-5
t _{PHZ} t _{PLZ}	Output Disable Time	2.0 2.0	3.9 4.0	5.5 5.5			2.0 2.0	6.5 7.5		