To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

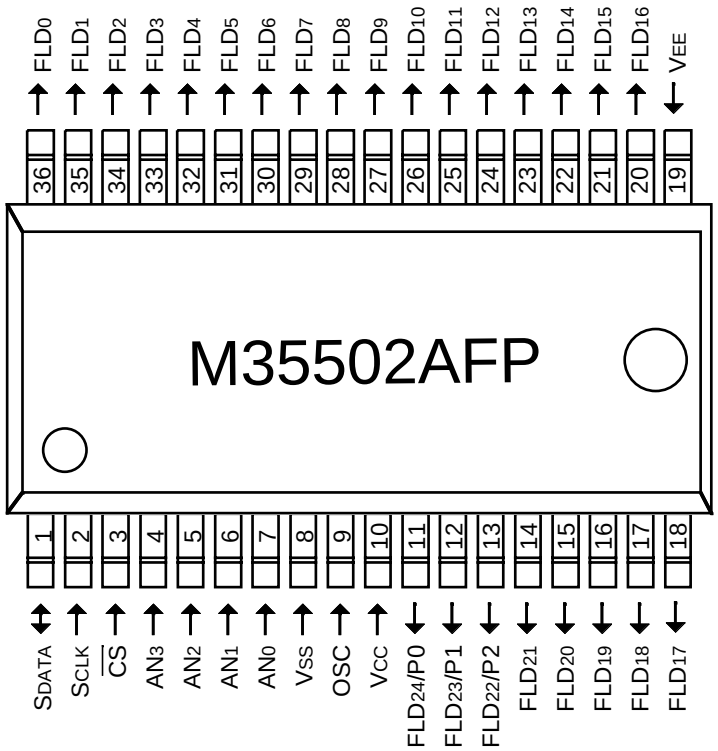
M35502AFP

FLD CONTROLLER

DESCRIPTION/FEATURES

- High-breakdown-voltage output port 25
  - Segment output ..... 8 to 20
  - Digit output ..... 5 to 16
    (Ports P0 to P2 are also used as normal output ports)
  - Output breakdown ..... Vcc – 45 V
  - Output current ..... –18 mA (at DIG selecting), –7 mA (at SEG selecting)
  - Pull-down resistor ..... built-in
  - Dimmer switch ..... 4 levels
- A-D converter ..... 8-bit × 4 channels
  - Absolute accuracy ..... ±3 LSB
- Serial I/O ..... 3 (CS controller, external clock)
  - Noise filter ..... built-in (in serial input pin and clock pin, 2 MHz sampling)
  - FLD display data ..... input
  - A-D conversion data ..... output
  - Command ..... input
- Package 36P2R-G
- Oscillation circuit ..... CR oscillation cirucit (external capacitor)
  - Oscillation frequency ..... 2 MHz
- Power source voltage ..... 4.0 to 5.5 V

PIN CONFIGURATION (TOP VIEW)



Package type: 36P2R-G

Fig.1 Pin configuration of M35502AFP

FUNCTIONAL BLOCK

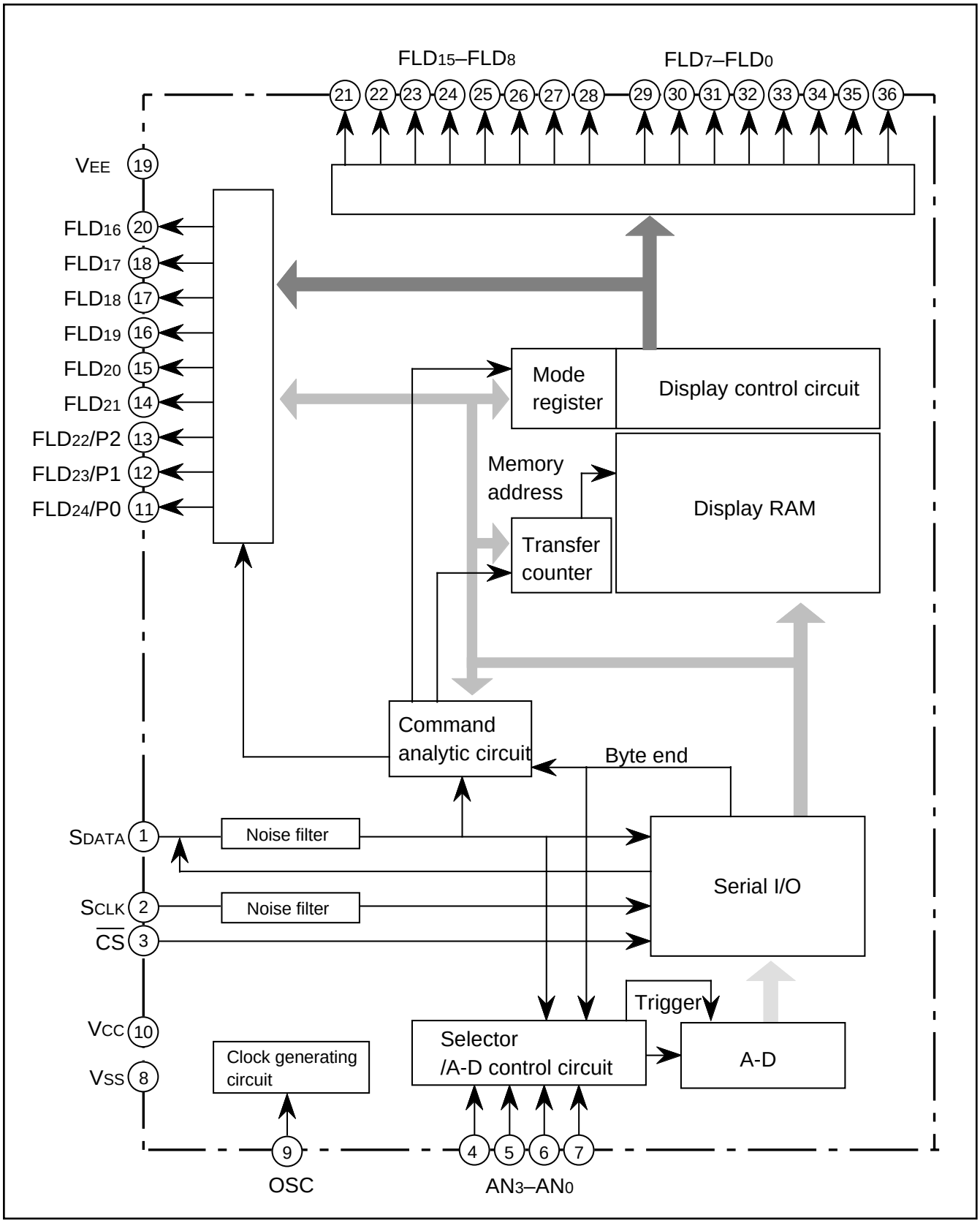


Fig.2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Input	Output	Function
V_{CC}, V_{SS}	Power source			• Apply voltage of 5 V to V_{CC}, and 0 V to V_{SS}.
V_{EE}	Pull-down power source			• Applies voltage supplied to pull-down resistors.
OSC	Clock input	Input		• Connect an external capacitor to this pin.
$\overline{CS}$	Chip select	CMOS input		• Serial transfer is possible by inputting "L" signal. • Pull-up resistor is built in.
SCLK	Serial clock	CMOS input Noise filter		• Clock for serial transfer is input. • Read a clock twice with 2 MHz sampling clock and judge if it is a noise or not.
SDATA	Serial input/ output	CMOS input Noise filter	N-channel open-drain	• Serial data is input/output. • In input mode, read a clock twice with 2 MHz sampling clock and judge if it is a noise or not.
FLD_{24}/P0 – FLD_{22}/P2	Digit/Port		P-channel open-drain	• Pin for ordinary output or digit output. • At reset this port is set to V_{EE} level through a pull-down resistor.
FLD_{21}– FLD_0	Segment/Digit		P-channel open-drain	• Pin for digit output or segment output. • At reset this port is set to V_{EE} level through a pull-down resistor.

PORT BLOCK

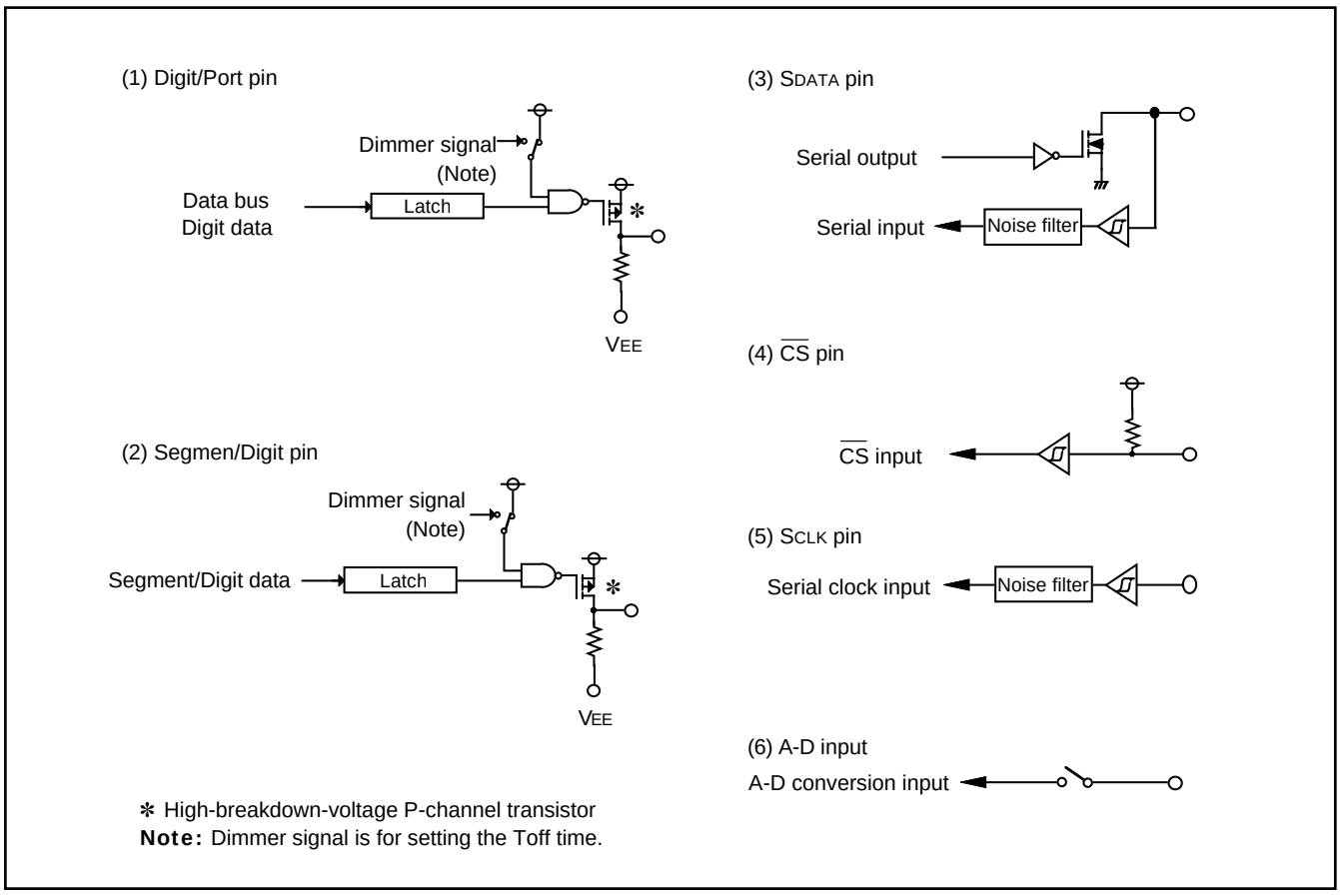
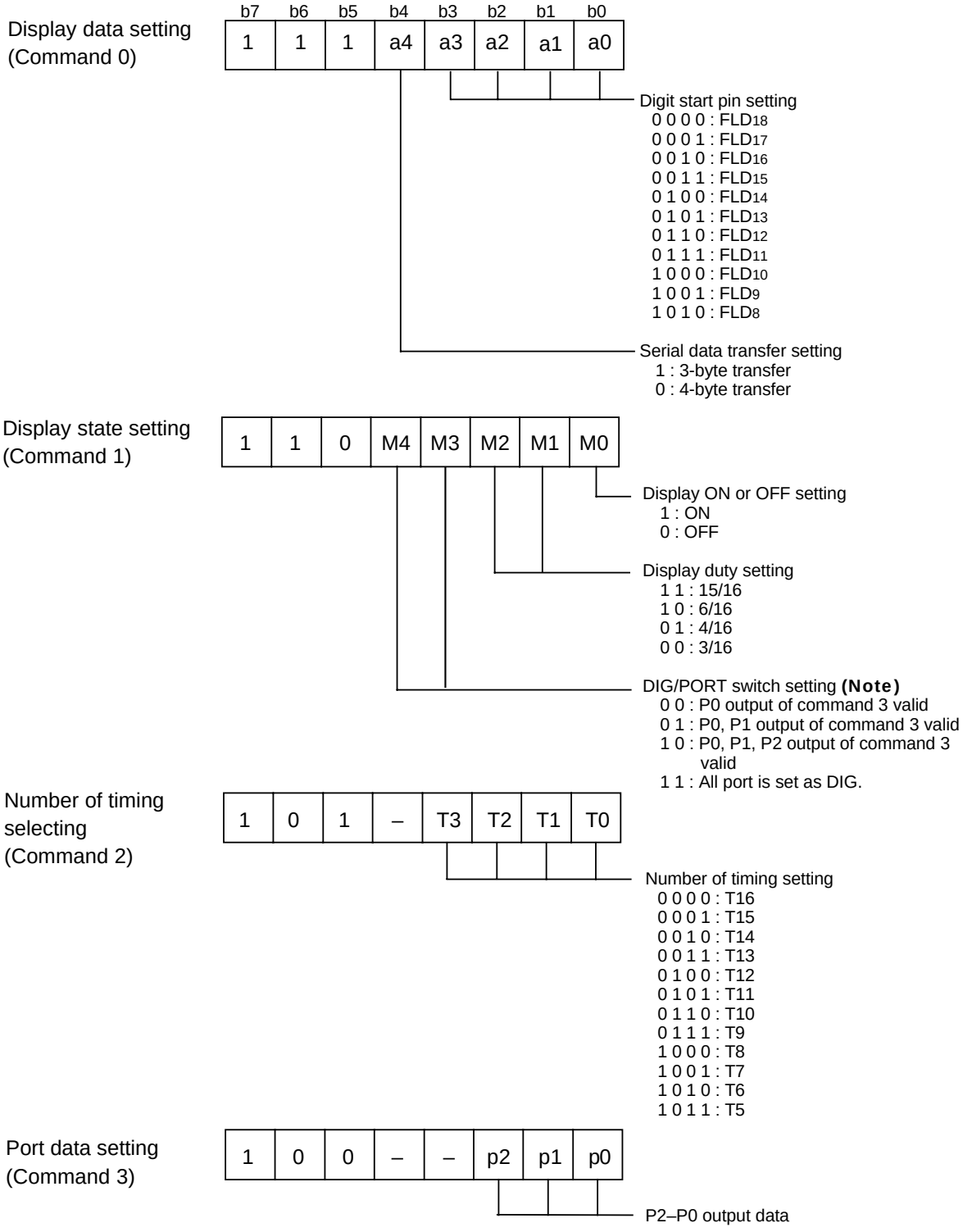


Fig.3 Port block diagram

COMMAND STYLE

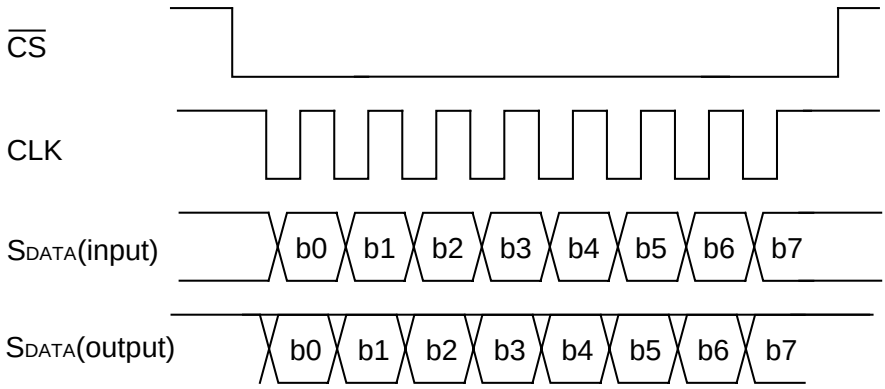


Note: DIG/PORT switch setting becomes valid when command 3 (port data setting) is accepted. When command 3 is not used, set "11_2" to these bits.

Fig.4 Command style

SERIAL I/O PROTOCOL

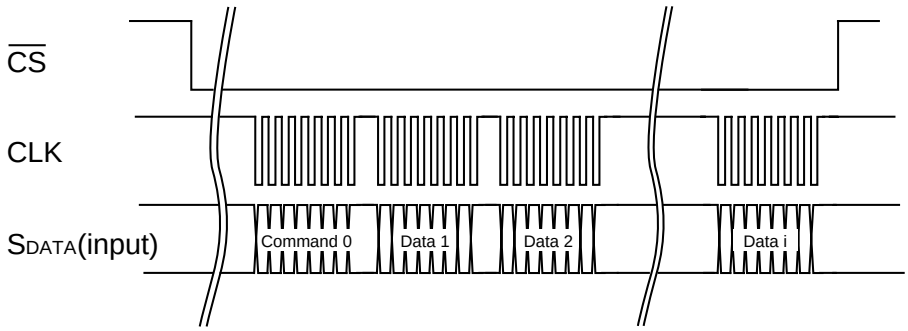
Byte protocol



Note: SDATA is in high-impedance state during CS signal is "H".

Command protocol

Display data setting
(Command 0)



Notes 1: The serial data which is transmitted after executing command 0 is recognized as a display data.
2: Set the CS signal to "H" level after transferring a display data.

Other setting except
display data setting
(Command 1 to 3)

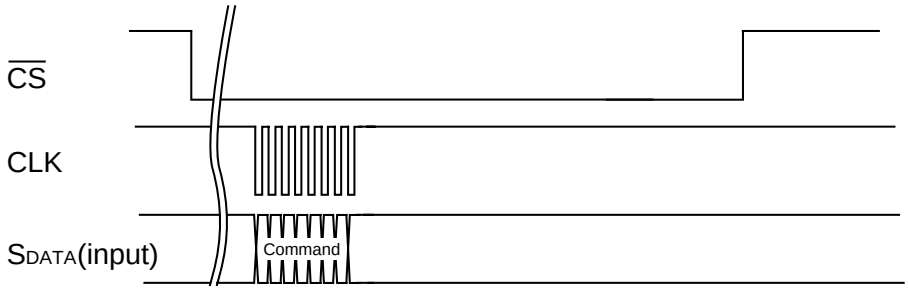
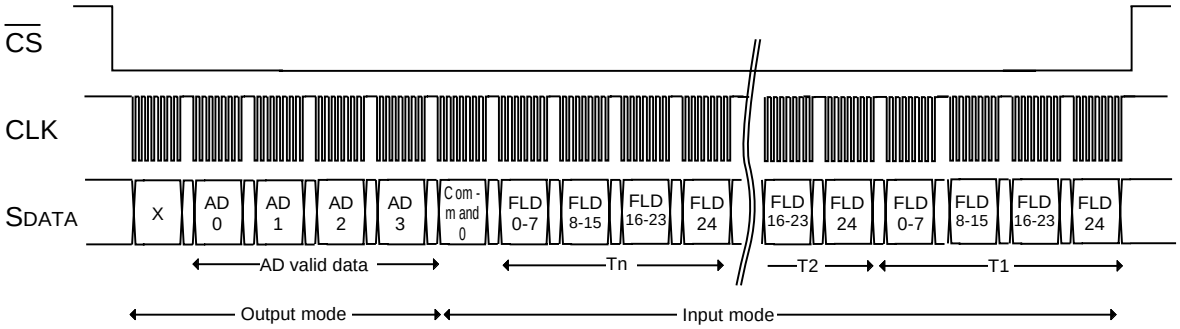


Fig.5 Serial I/O protocol

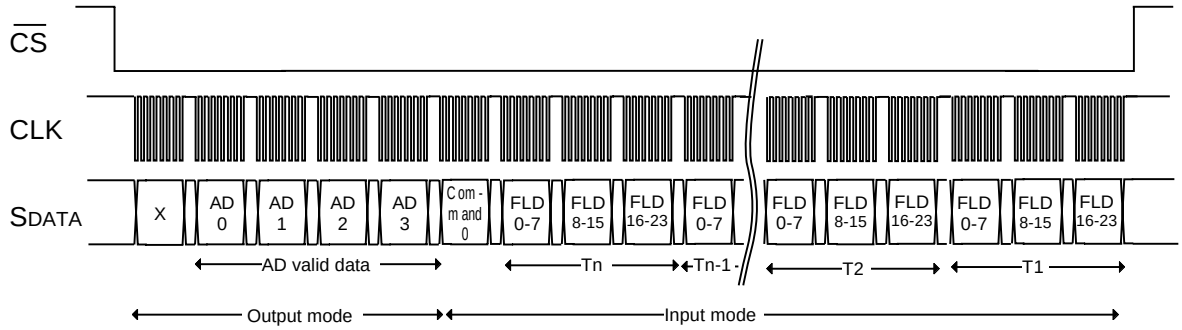
SERIAL COMMUNICATION FORMAT (DISPLAY DATA, A-D OUTPUT)

When using 25 high-breakdown-voltage ports (segment + grid) (4-byte transfer)



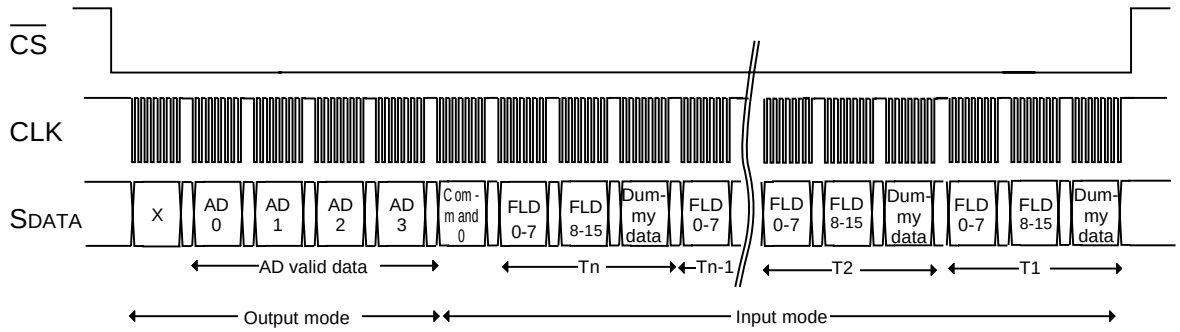
The SDATA pin becoms output mode from after the $\overline{CS}$ pin falling until the 5th byte of serial data.
The SDATA becomes command input mode from the 6th byte of serial data.

When using 24 high-breakdown-voltage ports (segment + grid) (3-byte transfer)



The SDATA pin becoms output mode from after the $\overline{CS}$ pin falling until the 5th byte of serial data.
The SDATA becomes command input mode from the 6th byte of serial data.

When using 16 high-breakdown-voltage ports (segment + grid) or less (3-byte transfer)



Transfer dummy data to the third byte of each timing.
The SDATA pin becoms output mode from after the $\overline{CS}$ pin falling until the 5th byte of serial data.
The SDATA becomes command input mode from the 6th byte of serial data.

Fig.6 Serial communication format

FLD DISPLAY TIMING

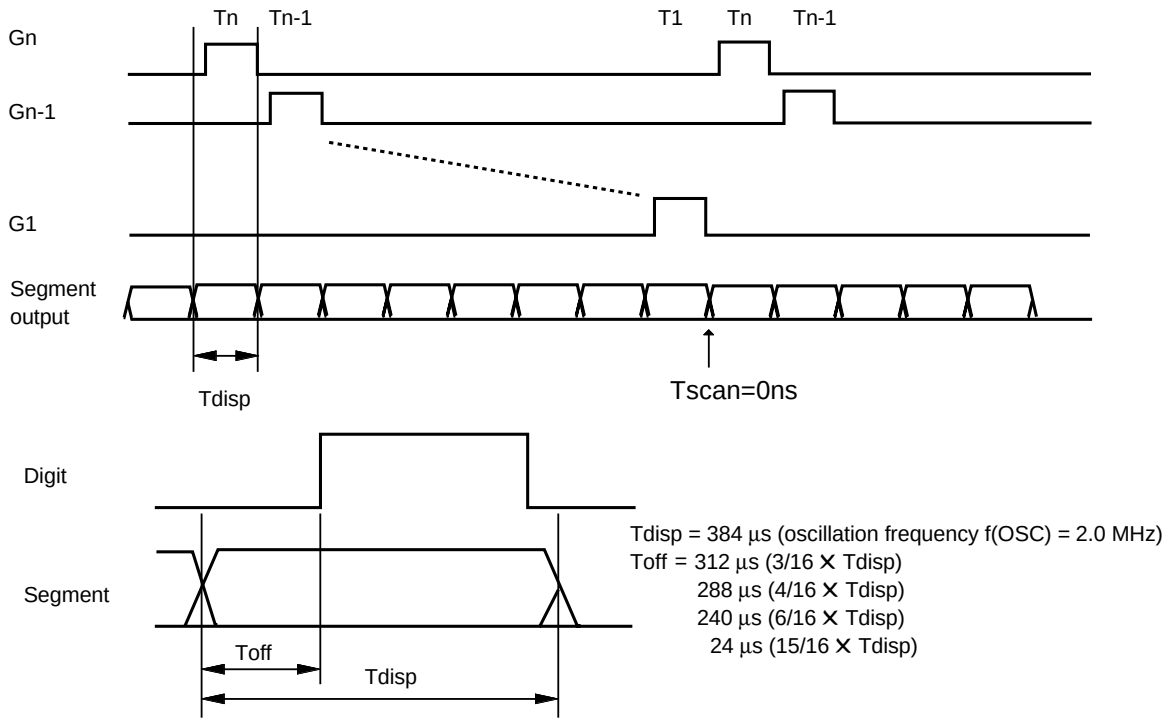


Fig.7 FLD display timing diagram

SEGMENT/DIGIT SETTING EXAMPLE

	PORT	FLD	Grid: 5 Segment: 8	Grid: 7 Segment: 8	Grid: 10 Segment: 8	Grid: 7 Segment 18
1		FLD_0	SEG1	SEG1	SEG1	SEG1
2		FLD_1	SEG2	SEG2	SEG2	SEG2
3		FLD_2	SEG3	SEG3	SEG3	SEG3
4		FLD_3	SEG4	SEG4	SEG4	SEG4
5		FLD_4	SEG5	SEG5	SEG5	SEG5
6		FLD_5	SEG6	SEG6	SEG6	SEG6
7		FLD_6	SEG7	SEG7	SEG7	SEG7
8		FLD_7	SEG8	SEG8	SEG8	SEG8
9		FLD_8	GRID5	GRID7	GRID10	SEG9
10		FLD_9	GRID4	GRID6	GRID9	SEG10
11		FLD_{10}	GRID3	GRID5	GRID8	SEG11
12		FLD_{11}	GRID2	GRID4	GRID7	SEG12
13		FLD_{12}	GRID1	GRID3	GRID6	SEG13
14		FLD_{13}		GRID2	GRID5	SEG14
15		FLD_{14}		GRID1	GRID4	SEG15
16		FLD_{15}			GRID3	SEG16
17		FLD_{16}			GRID2	SEG17
18		FLD_{17}			GRID1	SEG18
19		FLD_{18}				GRID7
20		FLD_{19}				GRID6
21		FLD_{20}				GRID5
22		FLD_{21}				GRID4
23	P2	FLD_{22}				GRID3
24	P1	FLD_{23}				GRID2
25	P0	FLD_{24}				GRID1

Fig.8 Segment/Digit setting example

BIT ALLOCATION FOR DISPLAY RAM

ADDRESS	b7							b0	
00_{16}								FLD 24	T1
01_{16}	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
02_{16}	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
03_{16}	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
04_{16}								FLD 24	T2
05_{16}	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
06_{16}	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
07_{16}	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
08_{16}								FLD 24	T3
09_{16}	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
$0A_{16}$	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
$0B_{16}$	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
$0C_{16}$								FLD 24	T4
$0D_{16}$	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
$0E_{16}$	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
$0F_{16}$	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
10_{16}								FLD 24	T5
11_{16}	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
12_{16}	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
13_{16}	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
14_{16}								FLD 24	T6
15_{16}	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
16_{16}	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
17_{16}	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
18_{16}								FLD 24	T7
19_{16}	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
$1A_{16}$	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
$1B_{16}$	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
$1C_{16}$								FLD 24	T8
$1D_{16}$	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
$1E_{16}$	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
$1F_{16}$	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	

	b7							b0	
20_{16}								FLD 24	T9
21_{16}	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
22_{16}	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
23_{16}	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
24_{16}								FLD 24	T10
25_{16}	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
26_{16}	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
27_{16}	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
28_{16}								FLD 24	T11
29_{16}	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
$2A_{16}$	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
$2B_{16}$	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
$2C_{16}$								FLD 24	T12
$2D_{16}$	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
$2E_{16}$	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
$2F_{16}$	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
30_{16}								FLD 24	T13
31_{16}	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
32_{16}	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
33_{16}	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
34_{16}								FLD 24	T14
35_{16}	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
36_{16}	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
37_{16}	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
38_{16}								FLD 24	T15
39_{16}	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
$3A_{16}$	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
$3B_{16}$	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	
$3C_{16}$								FLD 24	T16
$3D_{16}$	FLD 23	FLD 22	FLD 21	FLD 20	FLD 19	FLD 18	FLD 17	FLD 16	
$3E_{16}$	FLD 15	FLD 14	FLD 13	FLD 12	FLD 11	FLD 10	FLD 9	FLD 8	
$3F_{16}$	FLD 7	FLD 6	FLD 5	FLD 4	FLD 3	FLD 2	FLD 1	FLD 0	

Fig.9 Bit allocation for display RAM

CLOCK GENERATING CIRCUIT

Oscillating circuit is built up by connecting a capacitor between pins OSC and Vss.
When supplying a clock externally, input it to the OSC pin.

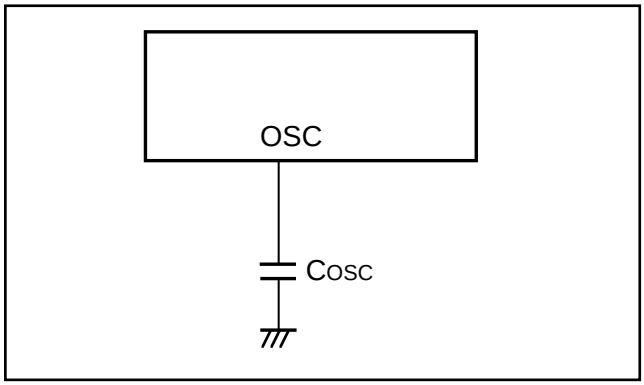


Fig.10 CR generating circuit

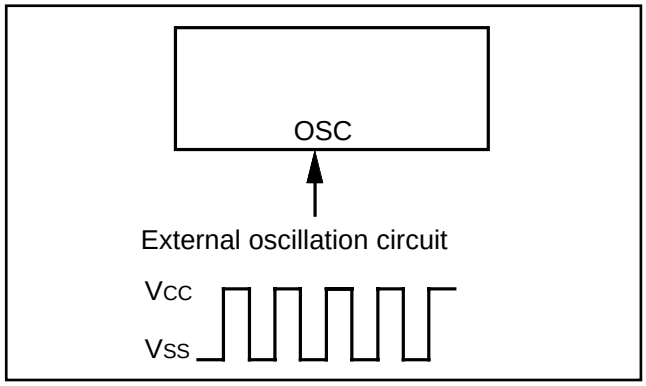


Fig.11 External clock input circuit

HANDLING OF UNUSED PINS

Handle unused pins as the follow.

Table 2 Handling of unused pins

Pin	Handling
Segment	Open
Digit	Open
Analog input	Connect to VCC or VSS through a resistor.

POWER-ON RESET

Reset can be performed automatically during power on (power-on reset) by the built-in power-on reset circuit.

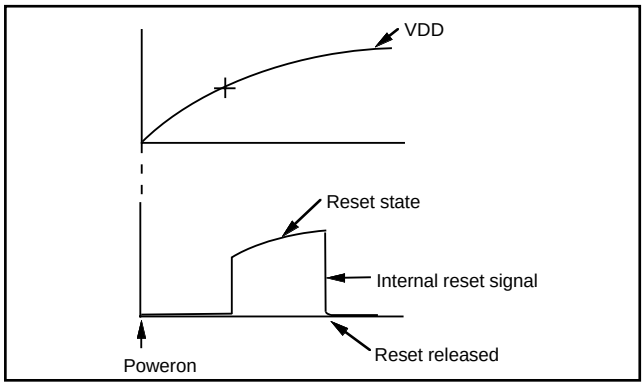


Fig.12 Power-on reset

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	• All voltage are based on V_{SS}. • Output transistors are cut off.	–0.3 to 6.5	V
V_{EE}	Pull-down power source voltage		V_{CC}–45 to V_{CC}+0.3	V
V_I	Input voltage AN_0 – AN_3		–0.3 to V_{CC}+0.3	V
V_I	Input voltage $\overline{CS}$, S_{DATA}, S_{CLK}		–0.3 to V_{CC}+0.3	V
V_O	Output voltage FLD_0 – FLD_{24}		V_{CC}–45 to V_{CC}+0.3	V
		• A waveform: 450 μs or more frequency and 30 μs or less pulse width. • Connect only capacitor load (C_L = 200pF).	V_{CC}–50 to V_{CC}+0.3	
V_O	Output voltage S_{DATA}	• All voltage are based on V_{SS}. • Output transistors are cut off.	–0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Ta = 25 °C	600	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Power source voltage	4.0	5.0	5.5	V
V_{SS}	Power source voltage		0		V
V_{EE}	Pull-down power source voltage	V_{CC}–38		V_{CC}	V
V_{IH}	"H" input voltage $\overline{CS}$, S_{CLK}, S_{DATA}	0.75V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $\overline{CS}$, S_{CLK}, S_{DATA}	0		0.25V_{CC}	V

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	FLD_0 – FLD_{24}	**(Note 1)**			–240	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	FLD_0 – FLD_{24}				–120	mA
$I_{OH(peak)}$	"H" peak output current	FLD_0 – FLD_{24} (at DIG selecting)	**(Note 2)**			–40	mA
$I_{OH(peak)}$	"H" peak output current	FLD_0 – FLD_{24} (at SEG selecting)	**(Note 2)**			–20	mA
$I_{OL(peak)}$	"L" peak output current	S_{DATA}				10	mA
$I_{OH(avg)}$	"H" peak output current	FLD_0 – FLD_{24} (at DIG selecting)	**(Note 3)**			–18	mA
$I_{OH(avg)}$	"H" average output current	FLD_0 – FLD_{24} (at SEG selecting)	**(Note 3)**			–7	mA
$I_{OL(avg)}$	"L" average output current	S_{DATA}				5.0	mA
f(OSC)	Clock input oscillation frequency		**(Note 4)**	1.4	2.0	2.6	MHz
f(S_{CLK})	Serial I/O external clock frequency				250		kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current is an average value measured over 100 ms.
4: When the oscillation frequency has a 50 % duty cycle.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	DIG output	I_{OH} = –18 mA	V_{CC}–2.0			V
		SEG output	I_{OH} = –7 mA	V_{CC}–2.0			V
V_{OL}	"L" output voltage	SDATA	I_{OL} = 5 mA			2.0	V
V_{T+} — V_{T-}	Hysteresis	SDATA, SCLK, $\overline{CS}$	V_{CC} = 5.0 V		0.5		V
I_{IH}	"H" input current	SDATA, SCLK, $\overline{CS}$	V_I = V_{CC}			5.0	μA
I_{IL}	"L" input current	SDATA, SCLK	V_I = V_{SS}			–5.0	μA
		$\overline{CS}$			–500		μA
		OSC			–4.0		μA
I_{LOAD}	Output load current	FLD_0 – FLD_{24}	V_{EE} = V_{CC}–36 V V_{OL} = V_{CC} Output transistors "off"	250	500	750	μA
I_{LEAK}	Output leakage current	FLD_0 – FLD_{24}	V_{EE} = V_{CC}–38 V V_{OL} = V_{CC}–38 V Output transistors "off"			–10	μA

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{RAM}	RAM hold voltage	When clock is stopped	2.0		5.5	V
I_{CC}	Power source current	V_{CC} = 5 V, f(X_{IN}) = 2.0 MHz Output transistors "off" at A-D converter operating		1.5	2.5	mA

A-D CONVERTER CHARACTERISTICS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)	V_{CC} = 5.12 V			±3	LSB
T_{conv}	Conversion time				100	tc(OSC)
V_{IA}	Analog input voltage		0		V_{CC}	V
I_{IA}	Analog port input current			0.5	5.0	μA
R_{LADDER}	Ladder resistor			35		kΩ

TIMING REQUIREMENTS (VCC = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tc(OSC)	Reset input "L" pulse width	384			ns
twH(OSC)	Clock input "H" pulse width	120			ns
twL(OSC)	Clock input "L" pulse width	120			ns
tc(SCLK)	Serial clock input cycle time **(Note)**	5			CLKs
twH(SCLK)	Serial clock input "H" pulse width **(Note)**	2			CLKs
twL(SCLK)	Serial clock input "L" pulse width **(Note)**	3			CLKs
tsu(SDATA-SCLK)	Serial input setup time **(Note)**	2			CLKs
th(SCLK-SDATA)	Serial input hold time **(Note)**	3			CLKs
tsu($\overline{CS}$)	Serial input setup time	50 tc(OSC)			ns
th($\overline{CS}$)	Serial input hold time	50 tc(OSC)			ns
tre(SCLK)	Serial clock interval time	50 tc(OSC)			ns

Note: The unit means a number of noise filter sampling clock (tc(OSC)).

SWITCHING CHARACTERISTICS (VCC = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
td(SCLK-SOUT)	Serial I/O output delay time **(Note 1)**				3	CLKs
tv(SCLK-SOUT)	Serial I/O output valid time		0			ns
tr(Pch)	High-breakdown-voltage P-channel open-drain output rising time	CL = 100pF VEE = VCC–36 V		1.8		μs
COSC	External capacitor size **(Note 2)**			18	80	pF

Note 1: The unit means a number of noise filter sampling clock (tc(OSC)).
2: An external capacitor size varies with a mounted condition.

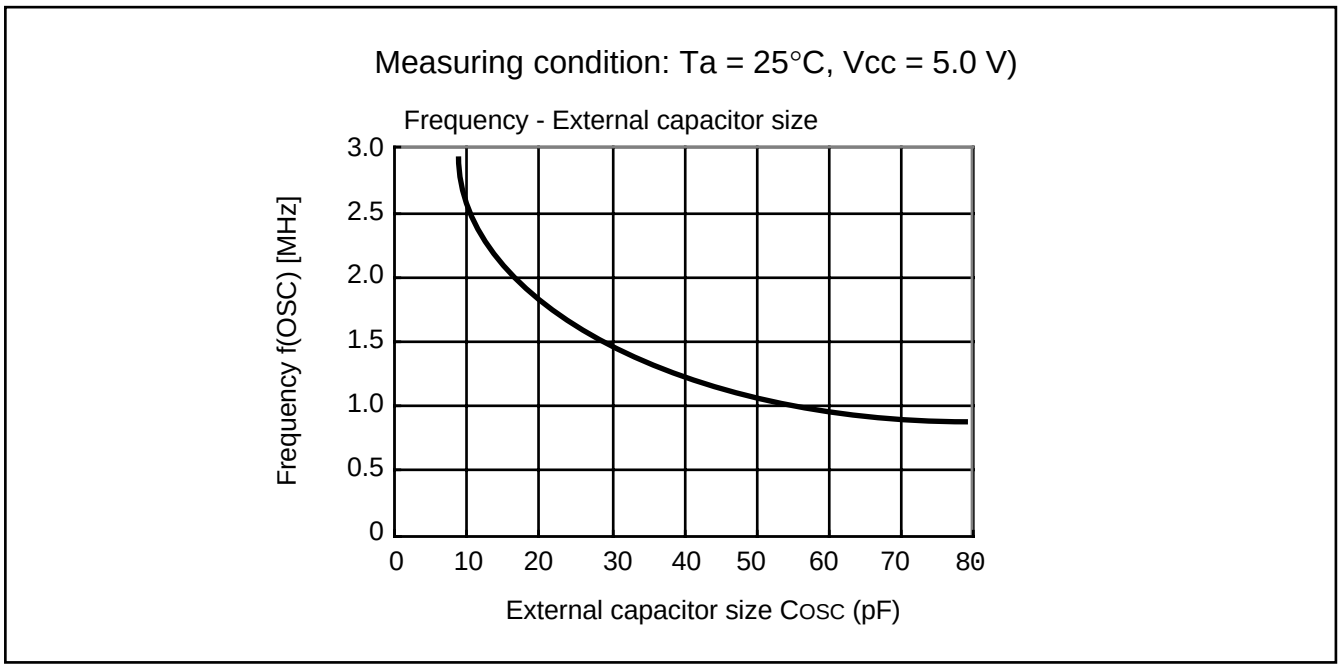


Fig. 13 Standard characteristic example of f(OSC)–Cosc

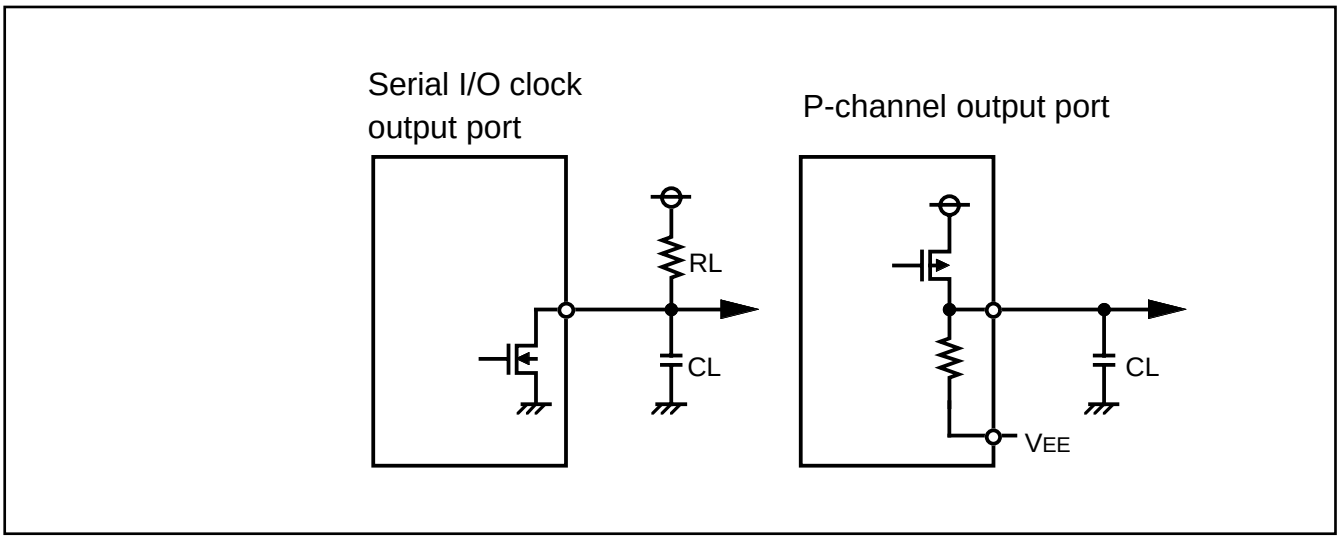


Fig.14 Output switching characteristics measurement circuit diagram

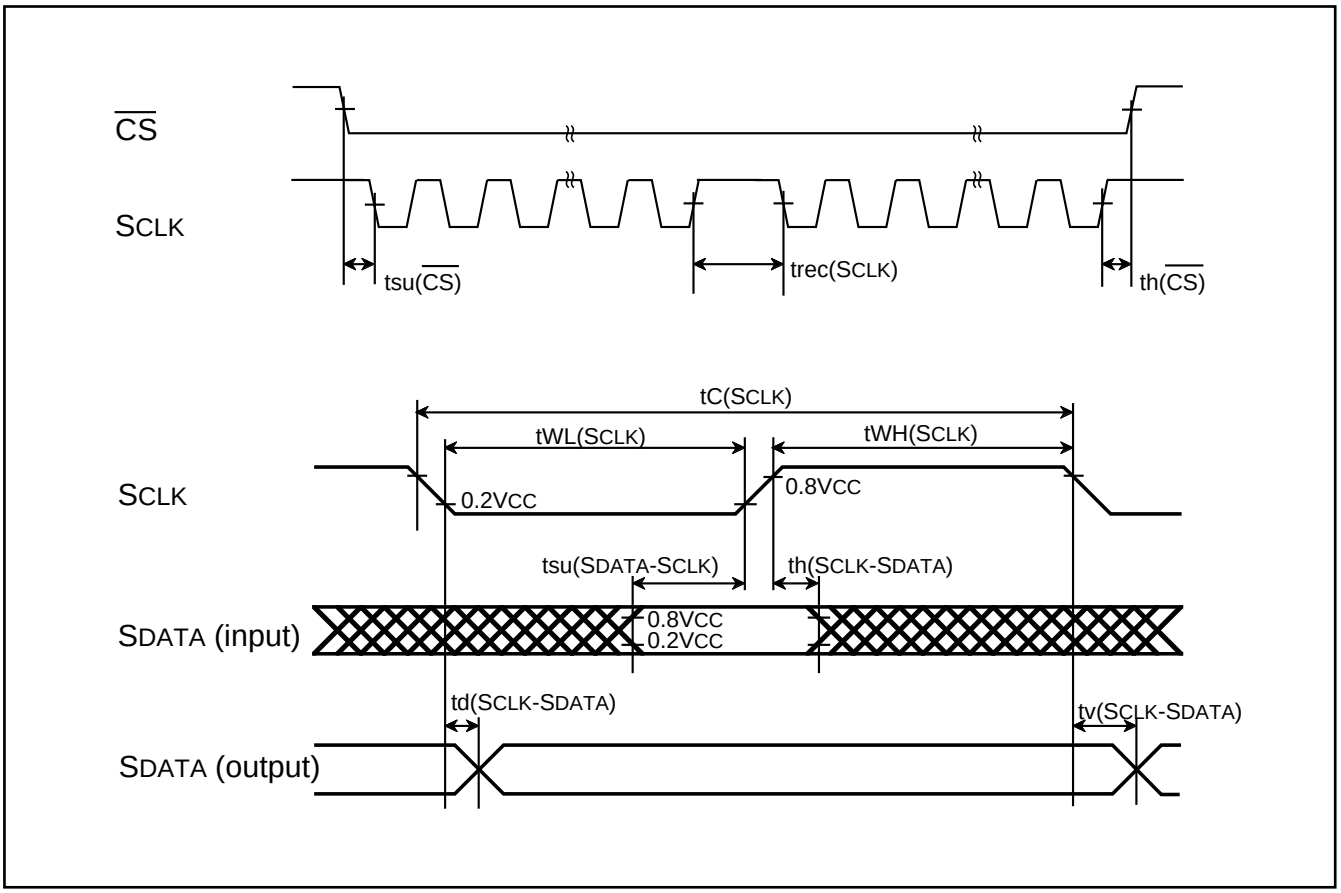


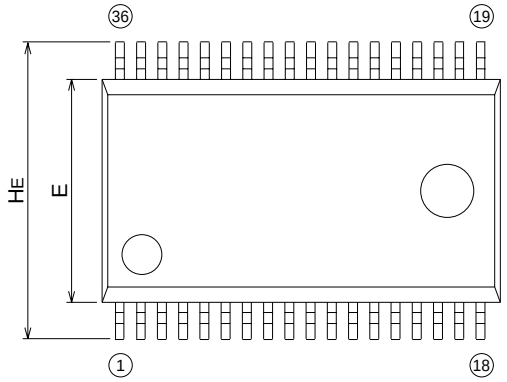
Fig.15 Timing diagram

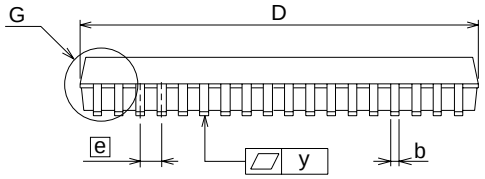
PACKAGE OUTLINE

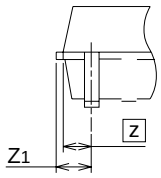
36P2R-G

Plastic 36pin 450mil SSOP

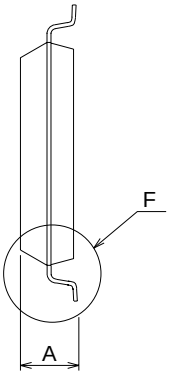
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP36-P-450-0.80	—	0.53	Alloy 42

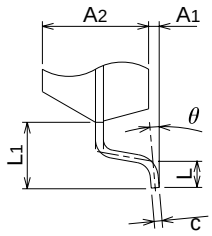




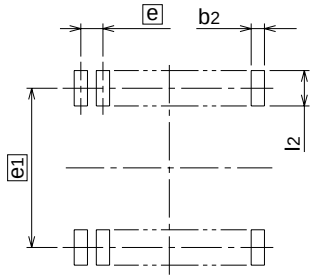


Detail G





Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.3
A1	0	0.1	0.2
A2	—	2.0	—
b	0.25	0.3	0.4
c	0.10	0.15	0.22
D	14.8	15.0	15.2
E	8.2	8.4	8.6
e	—	0.8	—
HE	10.1	10.4	10.7
L	0.3	0.5	0.7
L1	—	1.0	—
z	—	0.7	—
Z1	—	—	0.85
y	—	—	0.15
θ	0°	—	10°
b2	—	0.5	—
e1	—	11.43	—
l2	1.27	—	—

Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

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