SONET/SDH/ATM OC-48 16 : TRANSMITTER S3043

FEATURES

- Micro-power Bipolar supply
- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLL for clock generation
- Supports 2.4 GHz (OC-48)
- Reference frequency of 155.52 MHz
- Interface to both LVPECL and LVTTL logic
- 16-bit LVPECL data path
- Compact 80 PQFP/TEP package
- Diagnostic loopback mode
- Line loopback
- Lock detect
- Low jitter LVPECL interface
- Single 3.3V supply

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add drop multiplexors
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

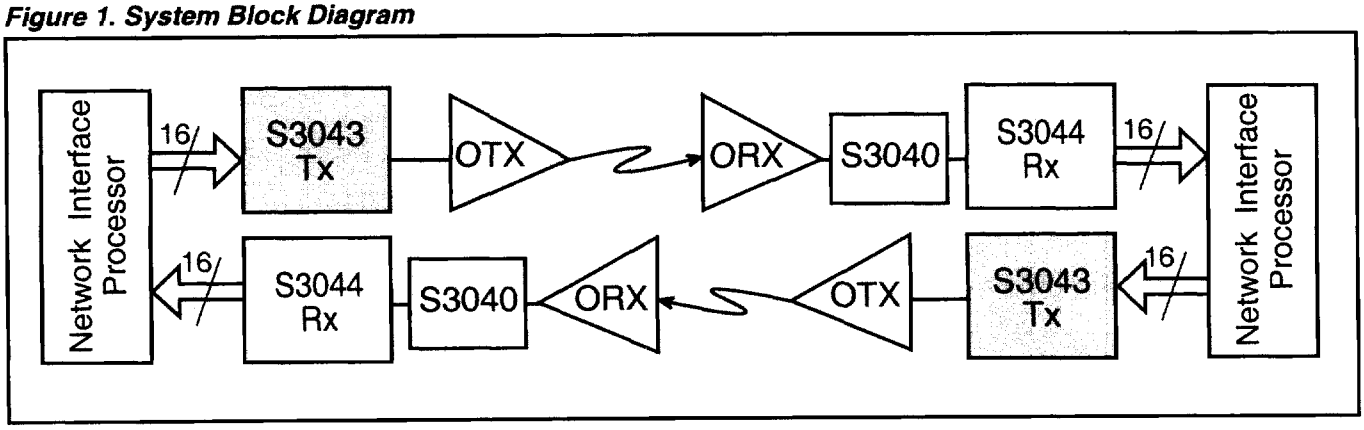
GENERAL DESCRIPTION

The S3043 SONET/SDH Mux chip is a fully integrated serialization SONET OC-48 (2.4 GHz) interface device. The chip performs all necessary parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis PLL components are contained in the S3043 Mux chip allowing the use of a slower external transmit clock reference. The chip can be used with 155.52 MHz reference clock, in support of existing system clocking schemes.

The low jitter LVPECL interface guarantees compliance with the bit-error rate requirements of the Bellcore, ANSI, and ITU-T standards. The S3043 is packaged in an 80 PQFP/TEP, offering designers a small package outline.

Figure 1. System Block Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3043 chip supports OC-48 rate (2.4 Gbps).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-48 consists of 144 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 144 overhead and 4176 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the ANSI SONET standard document.

Figure 2. SONET Structure

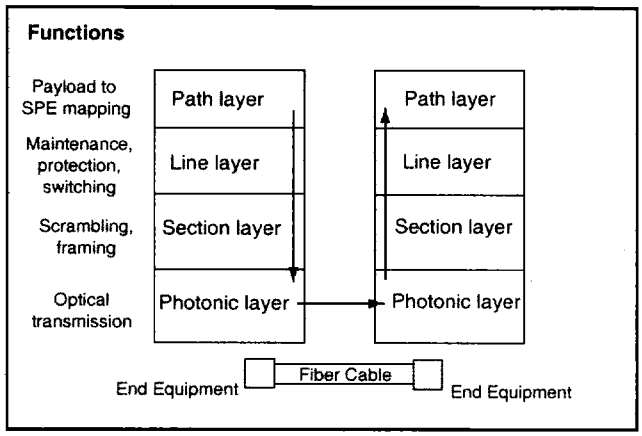
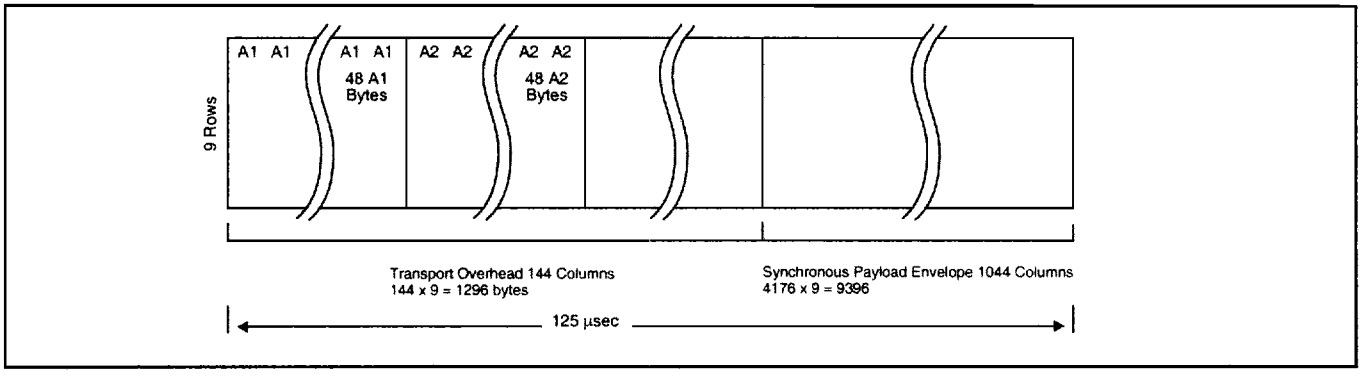


Table 1. SONET Signal Hierarchy

Elec.	CCITT	Optical	Data Rate (Mbps)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24	STM-8	OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 3. STS-48/OC-48 Frame Format



S3043 OVERVIEW

The S3043 transmitter implements SONET/SDH serialization and transmission functions. The block diagram in Figure 4 shows basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip includes parallel-to-serial conversion and system timing. The system timing circuitry consists of a high-speed phase detector, clock dividers, and clock distribution throughout the front end.

The sequence of operations is as follows:

Transmitter Operations:

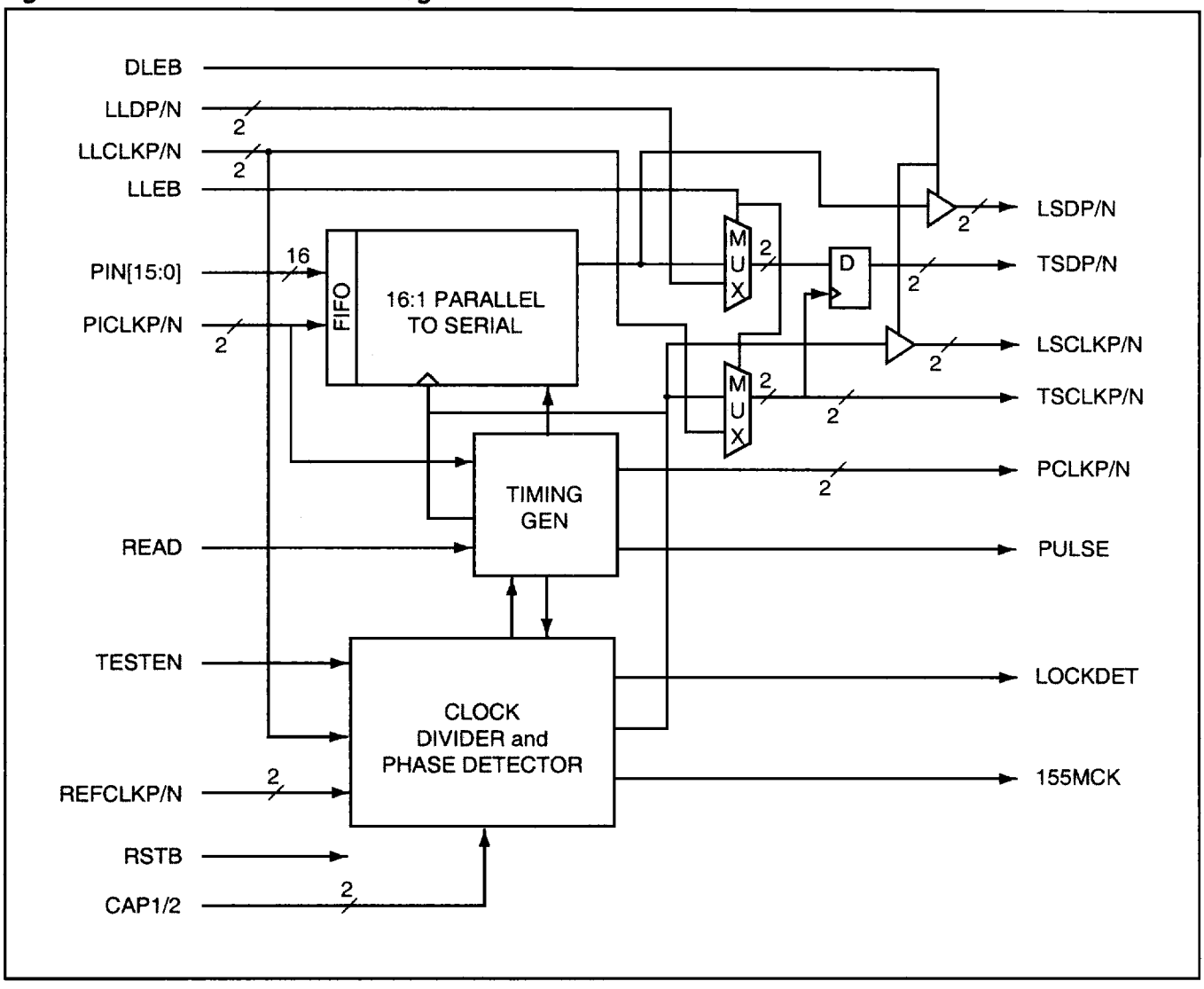
1. 16-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 7, 16 and 17.

Suggested Interface Devices

AMCC	S3040	OC-48 Clock Recovery Device
AMCC	S3044	OC-48 Receiver

Figure 4. S3043 Functional Block Diagram



S3043 ARCHITECTURE/FUNCTIONAL DESIGN

MUX OPERATION

The S3043 performs the serializing stage in the processing of a transmit SONET STS-48 bit serial data stream. It converts the byte serial 155 Mbyte/sec data stream to bit serial format at 2.4 Gbps. Diagnostic loopback is provided (transmitter to receiver), and Line Loopback is also provided (receiver to transmitter).

A high-frequency bit clock is generated from a 155 MHz frequency reference by using a frequency synthesizer consisting of an on-chip phase-locked loop circuit with a divider, VCO and loop filter.

Clock Divider and Phase Detector

The Clock Divider and Phase Detector, shown in the block diagram in Figure 4, contains monolithic PLL components that generate signals required to drive the loop filter.

The REFCLK input must be generated from a differential LVPECL crystal oscillator which has a frequency accuracy of better than 20 ppm in order for the VCOCLK frequency to have the same accuracy required for operation in a SONET system.

In order to meet the .01 UI SONET jitter specifications, the maximum reference clock jitter must be guaranteed over the 12KHz to 20 MHz bandwidth. For details of reference clock jitter requirements, see Table 2.

The on–chip phase detector, which compares the phase relationship between the VCO input and the REFCLK input, drives the loop filter.

Timing Generator

The Timing Generator function, seen in Figure 4, provides two separate functions. It provides a byte rate version of the TSCLK, and a mechanism for aligning the phase between the incoming byte clock and the clock which loads the parallel-to-serial shift register.

Table 2. Reference Jitter Limits

Maximum Reference Clock Jitter in 12 KHz to 20 MHz Band	Operating Mode
1 ps rms	STS-48

The PCLK output is a byte rate version of TSCLK. For STS-48, the PCLK frequency is 155 MHz. PCLK is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3043 device.

In the parallel-to-serial conversion process, the incoming data is passed from the PICLK byte clock timing domain to the internally generated byte clock timing domain, which is phase aligned to TSCLK.

The Timing Generator also produces a feedback reference clock to the Phase Detector. A counter divides the synthesized clock down to the same frequency as the reference clock REFCLK.

Parallel-to-Serial Converter

The Parallel-to-Serial converter shown in Figure 4 is comprised of two byte-wide registers. The first register latches the data from the PIN[15:0] bus on the rising edge of PICLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

An internally generated byte clock, which is phase aligned to the transmit serial clock as described in the Timing Generator description, activates the parallel data transfer between registers. The serial data is shifted out of the second register at the TSCLK rate.

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is low, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. The differential serial output data from the transmitter is routed to the receiver in place of the normal data stream (RSD).

Line Loopback

The Line Loopback circuitry consists of alternate clock and data output drivers. For the S3043, it selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable input (LLEB) is high, it selects data and clock from the Parallel to Serial Converter block. When LLEB is low, it forces the output data multiplexor to select data and clock from the LLD and LLCLK inputs, and a receive-to-transmit loopback can be established at the serial data rate.

Table 3. Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
PIN0 PIN1 PIN2 PIN3 PIN4 PIN5 PIN6 PIN7 PIN8 PIN9 PIN10 PIN11 PIN12 PIN13 PIN14 PIN15	Single-Ended LVPECL	I	25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40	Parallel Data Input. A 155 Mbyte/sec word, aligned to the PICLK parallel input clock. PIN<15> is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PIN<0> is the least significant bit (corresponding to bit 15 of each PCM word, the last bit transmitted). PIN<15:0> is sampled on the rising edge of PICLK.
PICLKP PICLKN	Diff. LVPECL	I	22 21	Parallel Input Clock. A 155 MHz nominally 50% duty cycle input clock, to which PIN<15:0> is aligned. PICLK is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLK samples PIN<15:0>.
LLDP LLDN	Externally Biased Diff. LVPECL	I	14 15	Line Loopback Data. Inputs normally provided from a companion S3044 device. Used to implement a line loopback function in which the receive serial bit serial data and clock signals are regenerated and passed through the S3043 transmitter. Internally terminated.
LLCLKP LLCLKN	Externally Biased Diff. LVPECL	I	11 12	Line Loopback Clock. Inputs normally provided from a companion S3044 device. Used to implement a line loopback function in which the receive serial bit serial data and clock signals are regenerated and passed through the S3043 transmitter. Internally terminated.
TESTEN	LVTTL	I	13	Test Clock Enable. Set High to provide access to the PLL during production tests.
REFCLKP REFCLKN	Internally Biased Diff. LVPECL	I	78 77	Reference Clock. Input used as the reference for the internal bit clock frequency synthesizer. Internally terminated and biased.
DLEB	LVTTL	I	8	Diagnostic Loopback Enable. Active Low. When active, selects diagnostic loopback. When DLEB is inactive, LSD and LSCLK are powered down and inactive. When active, the diagnostic loopback clock, (LSCLK), and data (LSD) outputs are active. TSD and TSCLK remain active in both states of DLEB.
RSTB	LVTTL	I	9	Master Reset. Reset input for the device, active Low. During reset, PCLK does not toggle.

Table 3. Input Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
LLEB	LVTTL	I	5	Line Loopback Enable. Selects Line Loopback. When LLEB is low, the S3043 will route the data from the LLD/LLCLK inputs to the TSD/TSCLK outputs.
CAP1 CAP2	Analog	I	67 66	Loop Filter Pins. Connections for external loop filter capacitor and resistors.
READ	Single-Ended LVPECL	I	45	Elastic Store Write Single-Ended Input. This input pin is clocked in using the rising edge of PICLK clock. This input is used to align the elastic store. The S3043 mux will monitor the READ input for a fault condition.

Table 4. Output Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
TSCLKP TSCLKN	Diff. CML	O	57 56	Transmit Clock Output. Transmit serial clock output that can be used to retime the TSD signal.
TSDP TSDN	Diff. CML	O	55 54	Transmit Serial Data. Serial data stream signals, normally connected to an optical transmitter module.
PCLKP PCLKN	Diff. LVPECL	O	23 24	Parallel Clock. A reference clock generated by dividing the internal bit clock by sixteen. It is normally used to coordinate byte-wide transfers between upstream logic and the S3043 device.
LSDP LSDN	Low Swing Diff. CML	O	6 7	Loopback Serial Data. Serial data stream signals normally connected to a companion S3044 device for diagnostic loopback purposes. The LSD outputs are updated on the falling edge of the LSCLK.
LSCLKP LSCLKN	Low Swing Diff. CML	O	1 2	Loopback Serial Clock. Serial clock signals normally connected to a companion S3044 device for diagnostic loopback purposes. The LSD outputs are updated on the falling edge of the LSCLK.
155MCK	Single- Ended LVPECL	O	20	155 MHz Clock Output. 155 MHz clock output from the clock synthesizer. This output should be connected to the reference clock input of the external clock recovery function (such as the S3040).
PULSE	Single- Ended LVPECL	O	43	Elastic Store Read Single-Ended Outputs. This output pulse is sychronized with the falling edge of PCLKP/N. This signal is used to align the elastic store. The PULSE output should be active for only one pulse every third 155 MHz clock cycle during the normal (no fault) operation.
LOCKDET	LVTTL	O	47	Lock Detect. Goes Low after the PLL has locked to the clock provided on the REFCLK pins. LOCKDET is an asynchronous output.

Table 5. Common Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
COREGND	GND		51, 61, 63, 65, 75	Core Ground
COREVCC	+3.3V		50, 60, 62, 64, 70	Core VCC
LVPECLVCC	+3.3V		3, 16, 17, 52, 59	LVPECL VCC
LVPECLGND	GND		4, 10, 18, 53, 58	LVPECL Ground
TTLVCC	+3.3V		48	TTL VCC
TTLGND	GND		19	TTL Ground
NC			44, 46, 49, 76	Not Connected
LVPECLVCC	+3.3V		41	LVPECL VCC
LVPECLGND	GND		42	LVPECL Ground
AVCC	+3.3V		69, 72, 74, 80	Analog VCC
AGND	GND		68, 71 73, 79	Analog Ground

Figure 5. S3043 Pinout

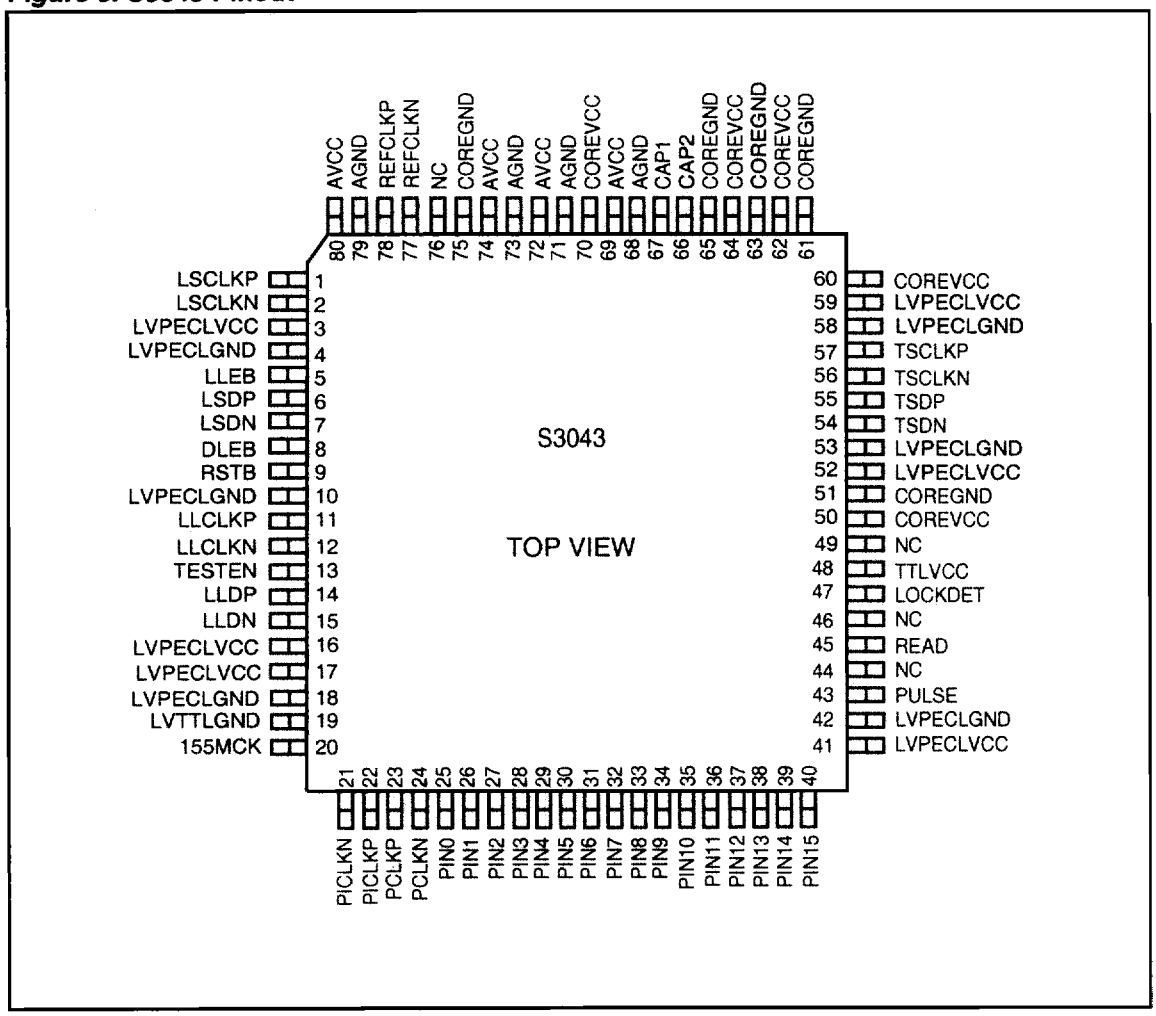
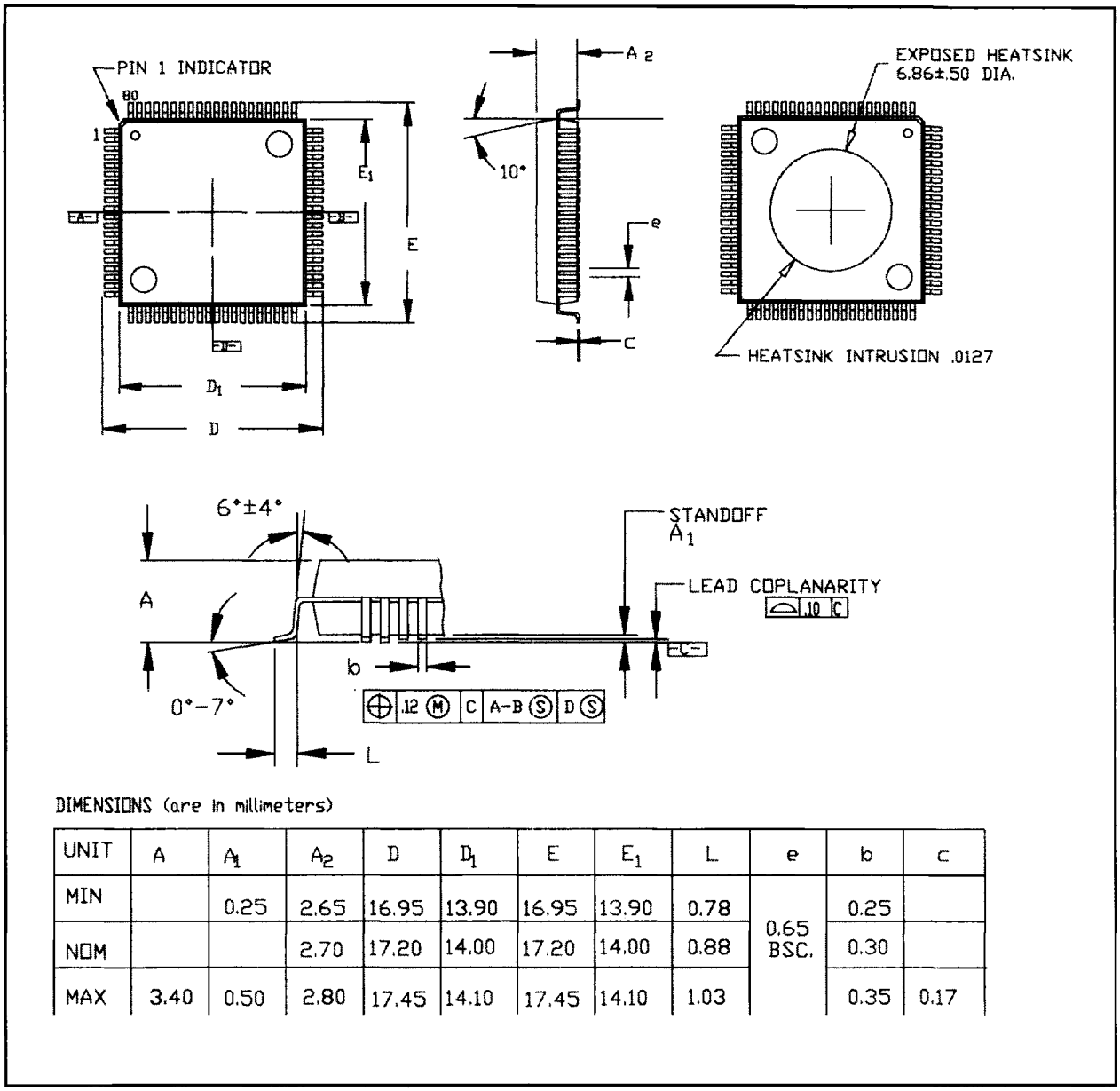


Figure 6. 80 PQFP/TEP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.25	2.65	16.95	13.90	16.95	13.90	0.78	0.65 BSC.	0.25	
NOM			2.70	17.20	14.00	17.20	14.00	0.88		0.30	
MAX	3.40	0.50	2.80	17.45	14.10	17.45	14.10	1.03		0.35	0.17

Note: The S3043 package is equipped with an embedded conductive heatsink on the bottom (board side). Active circuitry and vias should not appear in the area immediately under the package. This heatsink is electrically biased to the Vee potential of the S3043. For optimum thermal management, a foil surface at ground (or Vee if other than ground) is recommended immediately under the package, and connected with multiple vias to the internal plane(s) of similar potential. Thermally conductive epoxy or other conductive interposer can be used to establish a good thermal dissipation path.

Table 6. Thermal Management

Device	Max	Θjc
S3043	1.56 W	2.1°C/W

1. Add .24W for loopback active.

Table 7. Performance Specifications

Parameter	Min	Typ	Max	Units	Conditions
Nominal VCO Center Frequency		2.488 ±12%		GHz	
TSCLK Clock Output Jitter OC-48/STS-48			0.01	UI (rms)	
Data Output Jitter STS-48 155.52 MHz Ref. Clk.			0.01	UI (rms)	rms jitter, in lock.
Reference Clock Frequency Tolerance	-100		+100	ppm	± 20 ppm. Required to meet SONET output frequency specification.
Reference Clock Input Duty Cycle	30%		70%	%	
Reference Clock Rise & Fall Times			1.5	ns	20% to 80% of amplitude.

Table 8. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	-55		125	°C
Junction Temperature Under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on Vcc with Respect to GND	-0.5		+5.0	V
Voltage on any LVTTL Input Pin	-0.5		+5.5	V
Voltage on any LVPECL Input Pin	0		Vcc	V
LVTTL Output Sink Current			8	mA
LVTTL Output Source Current			8	mA
High Speed LVPECL Output Source Current			50	mA
Static Discharge Voltage[1]	500			V

1. Except CAP1, CAP2.

Table 9. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	-40		85	°C
Junction Temperature Under Bias			+130	°C
Voltage on Vcc with Respect to GND	3.13	3.3	3.46	V
Voltage on any LVPECL Input Pin	Vcc -2		Vcc	V

Table 10. Power Consumption

Parameter	Min	Typ	Max	Units
ICC[1]		383	450	mA

1. Add 70 mA for loopback active.

Table 11. LVTTL Input/Output DC Characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	TTL V_{CC} = Max	2.0		TTL V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	TTL V_{CC} = Max	0.0		0.8	V
I_{IH}	Input High Current	V_{IN} = 2.4 V			50	µA
I_{IL}	Input Low Current	V_{IN} = 0.5 V	-500			µA
V_{OH}	Output High Voltage	V_{IH} = Min. V_{IL} = Max. I_{OH} = -100 µA	2.1			V
V_{OL}	Output Low Voltage	V_{IH} = Min. V_{IL} = Max. I_{oL} = 4 mA			0.5	V

Table 12. Differential CML Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Condition
V_{OL}	CML Output LOW Voltage	Vcc -0.95		Vcc -0.55	V	100Ω line-to-line.
V_{OH}	CML Output HIGH Voltage	Vcc -0.35		Vcc -0.10	V	100Ω line-to-line.
$\Delta V_{OUTDIFF}$	CML Serial Output Differential Voltage Swing	560		1300	mV	100Ω line-to-line. See Figure 18.
$\Delta V_{OUTSINGLE}$	CML Serial Output Single-ended Voltage Swing	280		650	mV	100Ω line-to-line. See Figure 18.

Table 13. Low Swing Differential CML Output DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OL}	Loopback CML Output LOW Voltage	Vcc -0.50		Vcc -0.25	V	100Ω line-to-line.
V_{OH}	Loopback CML Output HIGH Voltage	Vcc -0.20		Vcc -0.05	V	100Ω line-to-line.
$\Delta V_{OUTDIFF}$	Loopback CML Serial Output Differential Voltage Swing	360		800	mV	100Ω line-to-line.
$\Delta V_{OUTSINGLE}$	Loopback CML Serial Output Single-ended Voltage Swing	180		400	mV	100Ω line-to-line.

Table 14. Internally Biased Differential LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	See Figure 18.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	150		600	mV	See Figure 18.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 15. Externally Biased Differential LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{BIAS}	LVPECL DC Bias Voltage	Vcc -1.2		Vcc -0.8	V	Inputs open.
V_{IL}	LVPECL Input LOW Voltage	Vcc -2.000		Vcc -0.25	V	
V_{IH}	LVPECL Input HIGH Voltage	Vcc -1.20		Vcc -0.05	V	
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	See Figure 18.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	150		600	mV	See Figure 18.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 16. Single Ended LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IL}	PECL Input Low Voltage	Vcc -2.30		Vcc -1.441	V	
V_{IH}	PECL Input High Voltage	Vcc -1.250		Vcc -0.570	V	

Table 17. Single Ended LVPECL Output DC Characteristics[1]

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OL}	PECL Output Low Voltage	Vcc -2.2		Vcc -1.75	V	400Ω to GND
V_{OH}	PECL Output High Voltage	Vcc -1.15		Vcc -0.65	V	400Ω to GND

1. For 155MCK and Pulse signals, externally terminate with 150Ω to ground. Maximum voltage swing = 500 mV for these two signals.

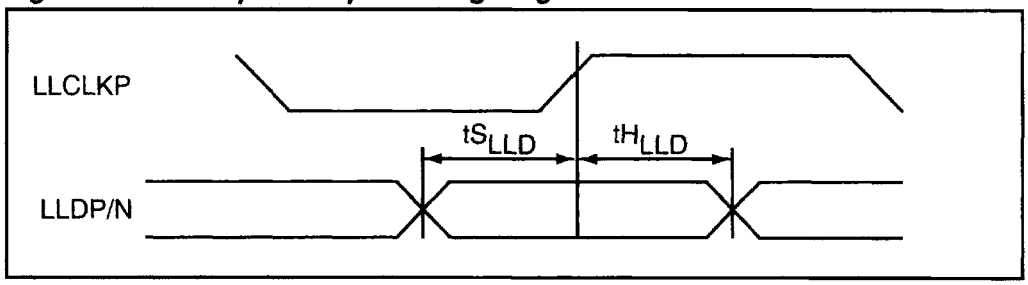
Table 18. Differential LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Comments
V_{IL}	LVPECL Input Low	Vcc -2.0		Vcc -0.5	V	
V_{IH}	LVPECL Input High	Vcc -1.2		Vcc -0.3	V	
ΔV_{INDIFF}	Diff. Input Voltage Swing	400		2000	mV	See Figure 18.
$\Delta V_{INSINGLE}$	Single Ended Input Voltage Swing	200		1000	mV	See Figure 18.

Table 19. Differential LVPECL Output DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Comments
$\Delta V_{OUTSINGLE}$	Single Ended Output Voltage Swing	700		950	mV	400 Ω to GND
$\Delta V_{OUTDIFF}$	Diff. Output Voltage Swing	1400		1900	mV	400 Ω to GND
V_{OH}	Output High Voltage	Vcc -1.15		Vcc -0.60	V	400 Ω to GND
V_{OL}	Output Low Voltage	Vcc -1.95		Vcc -1.50	V	400 Ω to GND

Figure 7. Line Loopback Input Timing Diagram



Notes on High-Speed LVPECL Input Timing:

1. Timing is measured from the cross-over point of the reference signal to the cross-over point of the input.

Table 20. AC Transmitter Timing Characteristics

Symbol	Description	Min	Max	Units
	TSCLK/LSCLK Frequency (nom. 2.48 GHz)		2.6	GHz
	TSCLK/LSCLK Duty Cycle	40	60	%
	PICLK Duty Cycle	40	60	%
tS_{PIN}	READ, PIN [15.0] Set-up Time w.r.t. PICLKP	1.5		ns
tH_{PIN}	READ, PIN [15.0] Hold Time w.r.t. PICLKP	0.5		ns
tP_{TSD}	TSCLK/LSCLK Low to TSD/LSD Valid Propagation Delay		200	ps
tS_{TSD}	TSD/LSD Set-up Time w.r.t. TSCLK/LSCLK	105		ps
tH_{TSD}	TSD/LSD Hold Time w.r.t. TSCLK/LSCLK	105		ps
tS_{LLD}	LLDP/N Set-up Time w.r.t. LLCLKP/N	100		ps
tH_{LLD}	LLDP/N Hold Time w.r.t. LLCLKP/N	100		ps
	PCLKP/N Duty Cycle	40	60	%
	CML Output Rise and Fall Time (20% - 80%)		170	ps
tP_{PICLK}	PICLK Delay from PCLK	0	13	ns
tP_{PRCLK}	READ Delay from PULSE	0	13	ns
tS_{PULSE}	PULSE Set-up Time w.r.t. PCLK	1.8		ns
tH_{PULSE}	PULSE Hold Time w.r.t. PCLK	2.0		ns
tP_{REFCLK}	PCLK Delay from REFCLK		6.5	ns

Figure 8. External Loop Filter

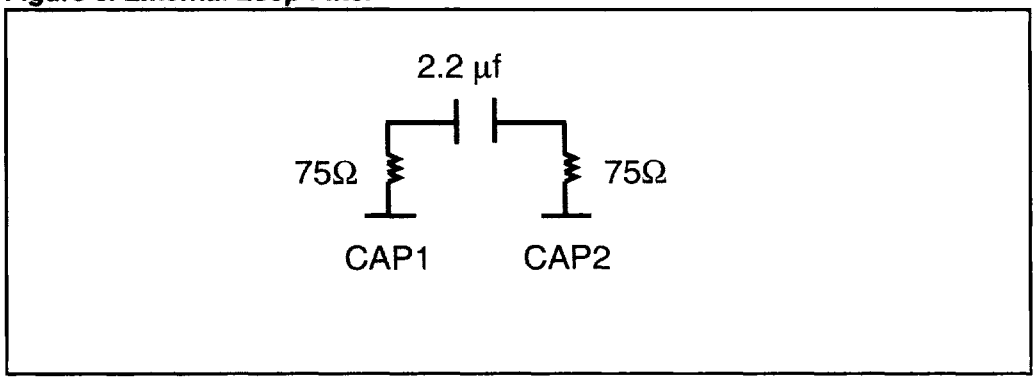


Figure 9. CML Output to +5V PECL Input AC Coupled Termination

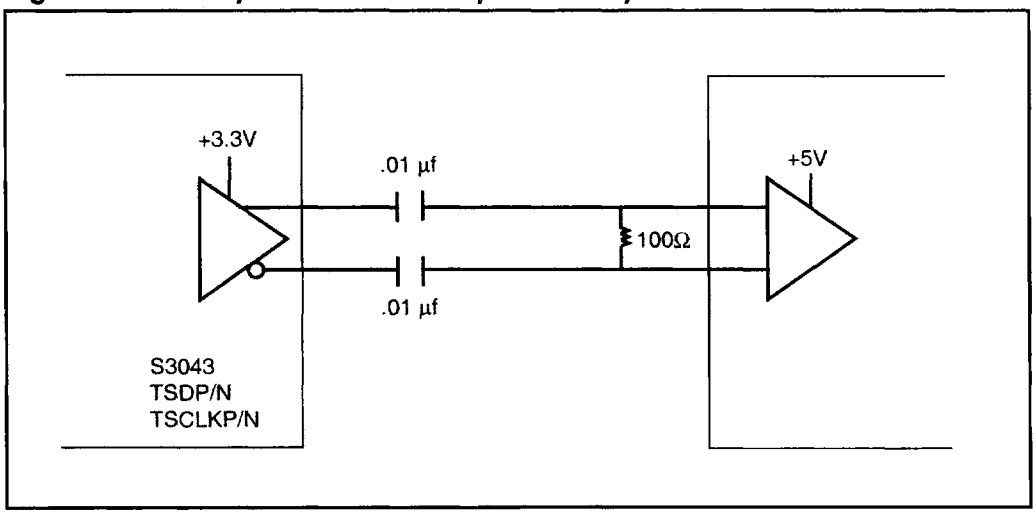


Figure 10. -5V Single Ended ECL Driver to S3043 Input AC Coupled Termination

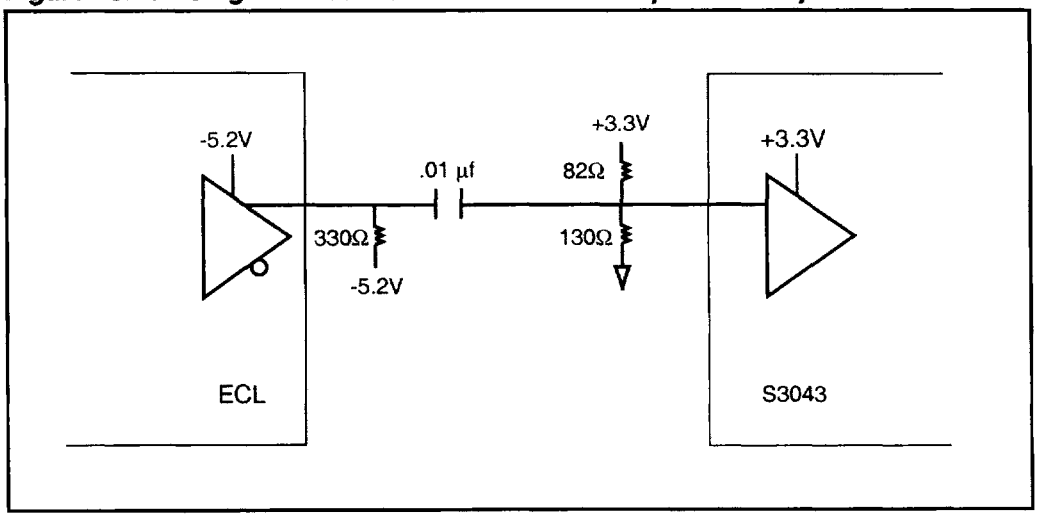


Figure 11. +5V Differential PECL Driver to S3043 Input AC Coupled Termination

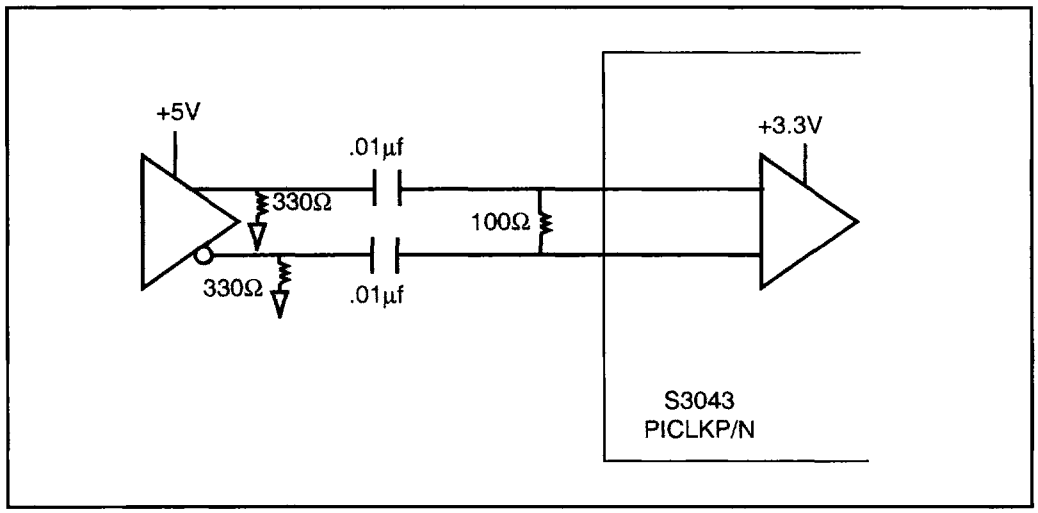


Figure 12. S3043 to S3043 Terminations

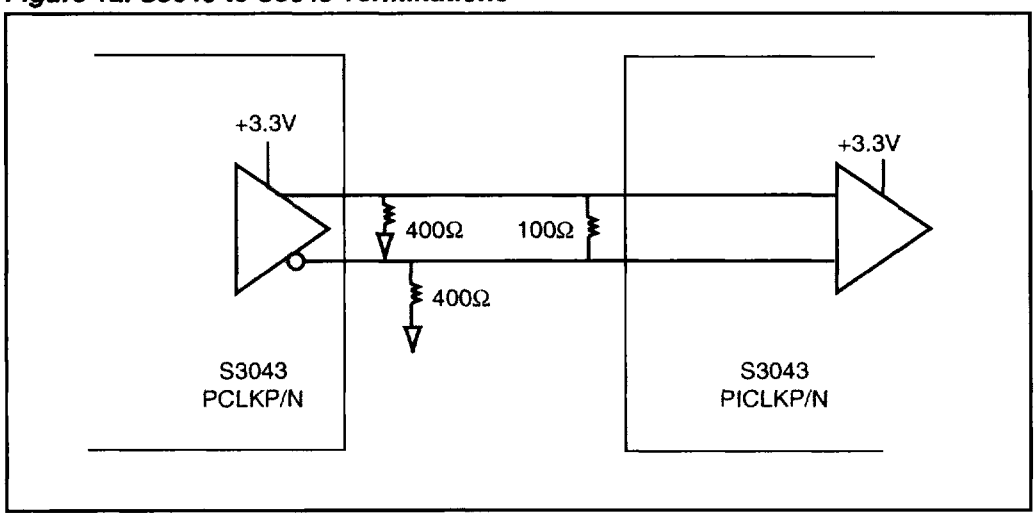


Figure 13. Single-Ended PECL Output Termination

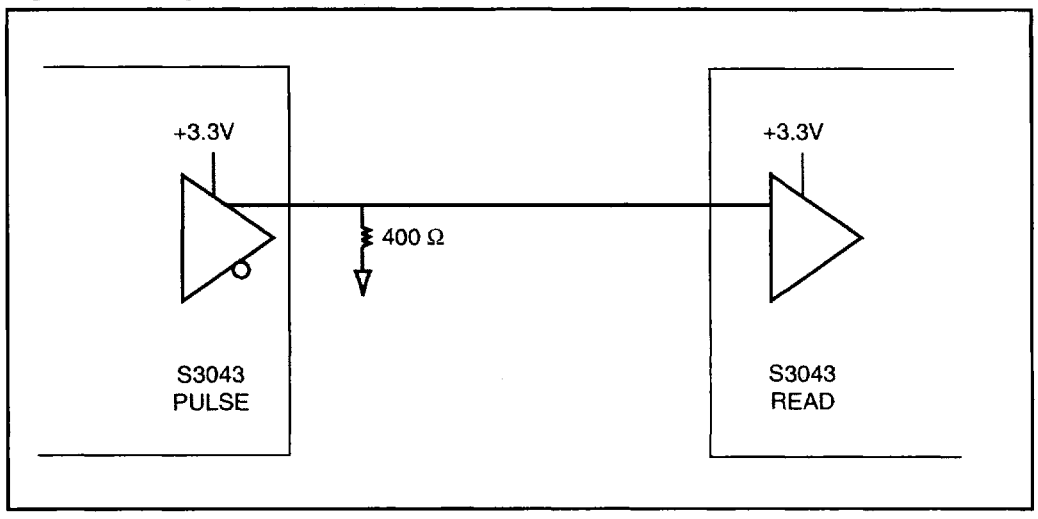


Figure 14. S3043 to S3044 for Diagnostic Loopback

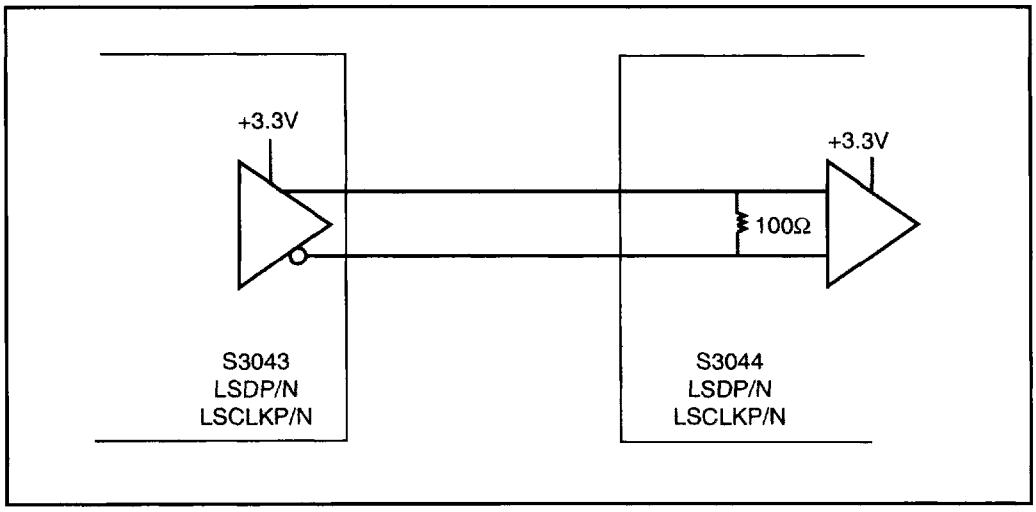


Figure 15. Single-Ended LVPECL Driver to S3043 Input AC Coupled Termination

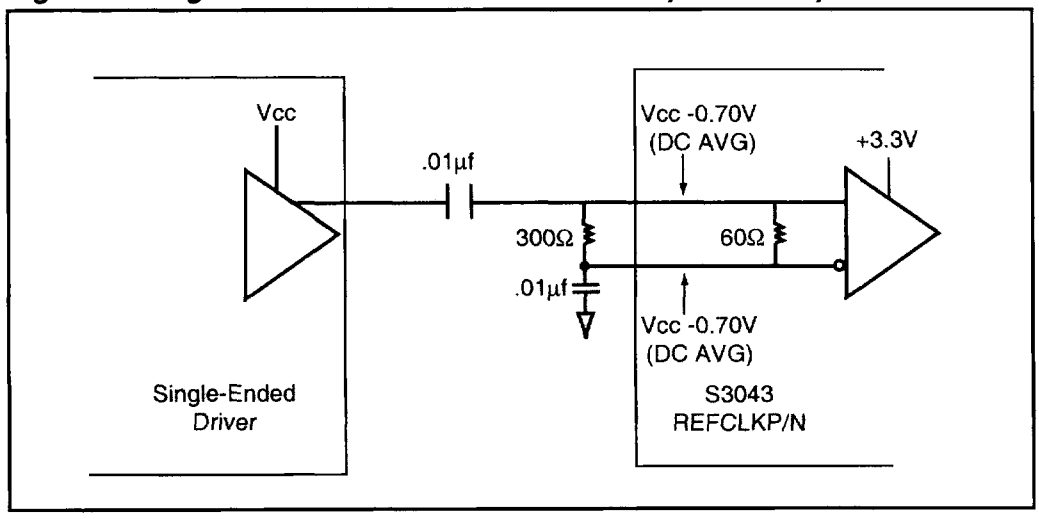
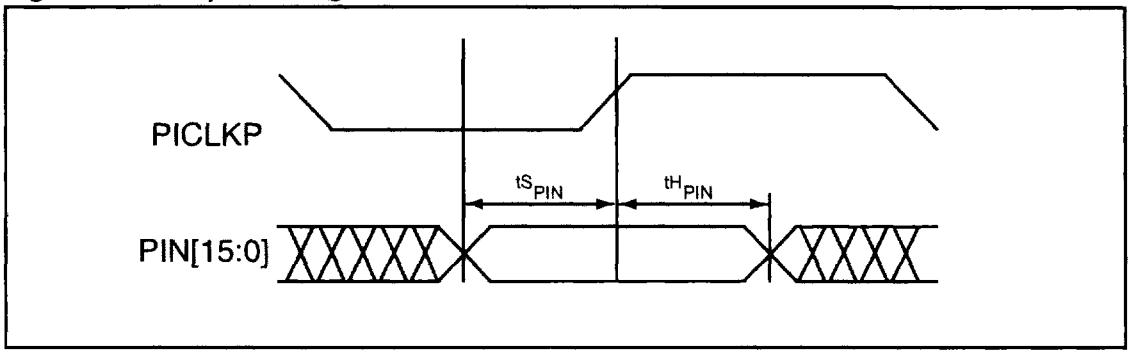
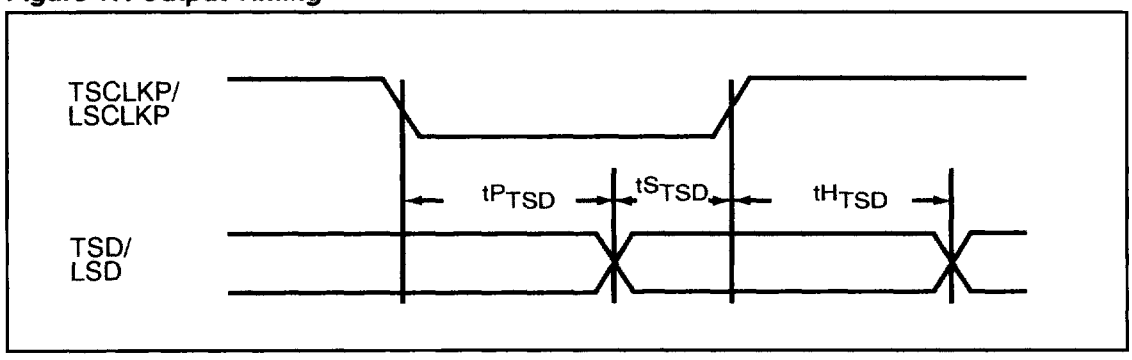


Figure 16. AC Input Timing



1. When a set-up time is specified on LVPECL signals between an input and a clock, the set-up time is the time in picoseconds from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on LVPECL signals between an input and a clock, the hold time is the time in picoseconds from the 50% point of the clock to the 50% point of the input.

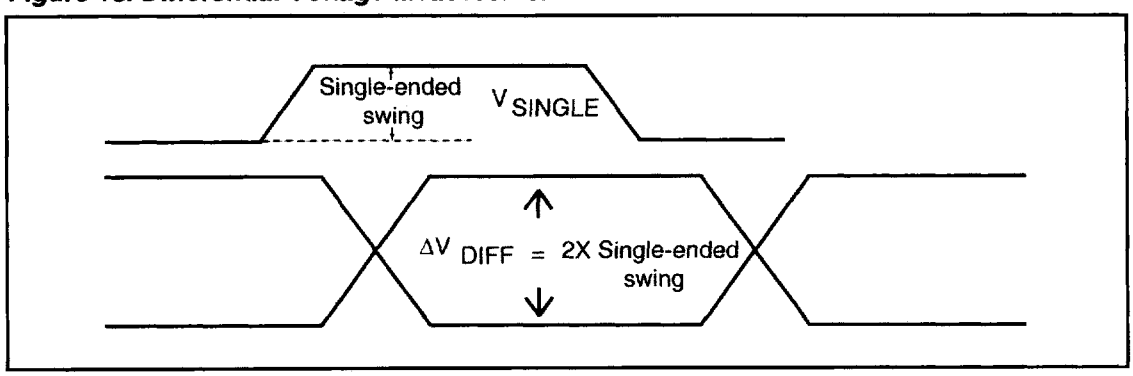
Figure 17. Output Timing



Notes on High-Speed PECL Output Timing

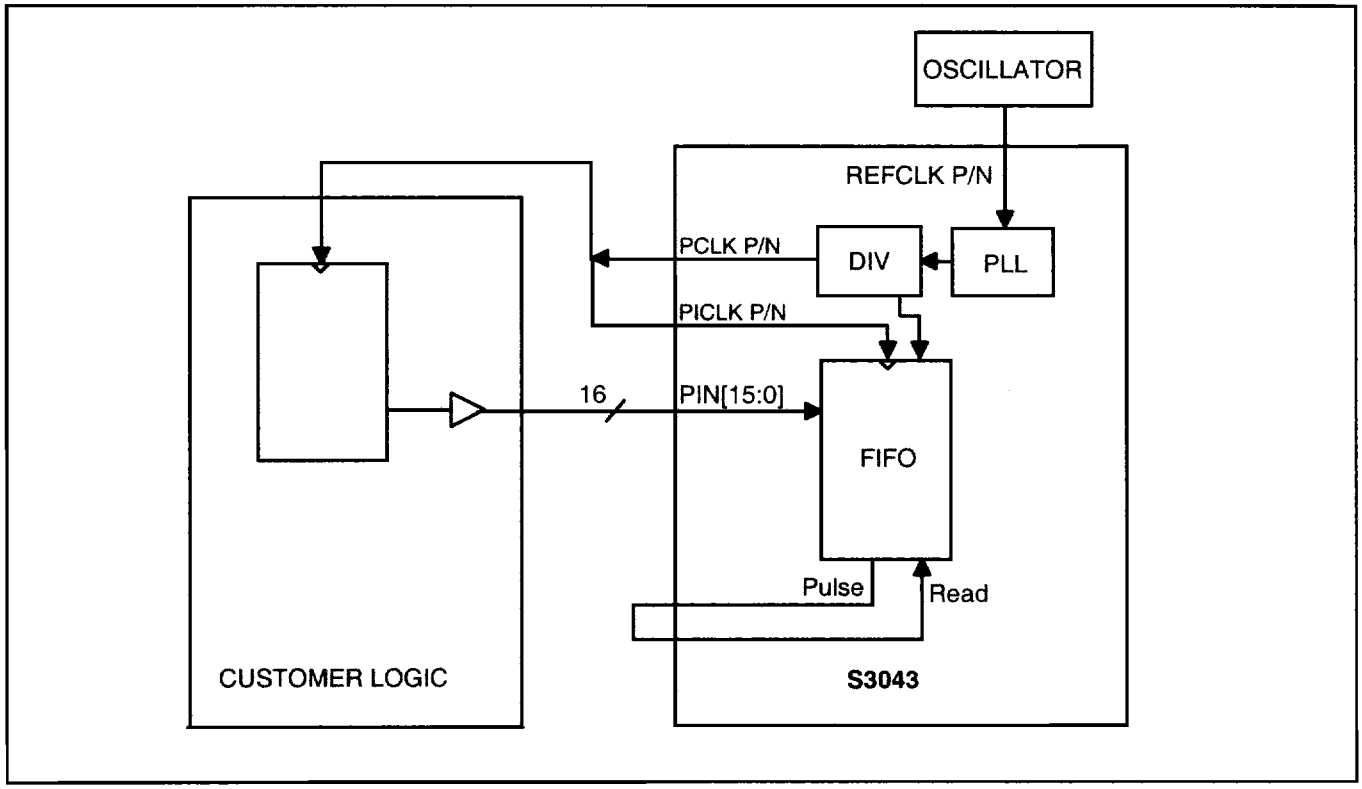
1. Output propagation delay time is the time in nanoseconds from thecross-over point of the reference signal to the cross-over point of the output.
2. When a set-up time is specified on differential LVPECL signals between an input and a clock, the set-up time is the time in picoseconds from the cross-over point of the input to the cross-over point of the clock.
3. When a hold time is specified on differential LVPECL signals between an input and a clock, the hold time is the time in picoseconds from the cross-over point of the clock to the cross-over point of the input.

Figure 18. Differential Voltage Measurement



The S3043 utilizes a unique elastic store buffer which can be set in two different configurations allowing the system designer to be flexible in the way a system is to be layed out. The configuration of the elastic store buffer is dependent upon the I/O pins which comprise the Synch Timing loop. This loop is formed from PULSE(I/P) to READ(O/P) and PCLK(I/P) to PICLK(O/P). The elastic store buffer can be thought of as a memory stack with a read pointer. The PULSE signal is the read pointer which announces that it has read a register and when fed back to READ input, it synchronizes the write operation of the buffer so as not to simultaneously write over the same register that it has read previously.

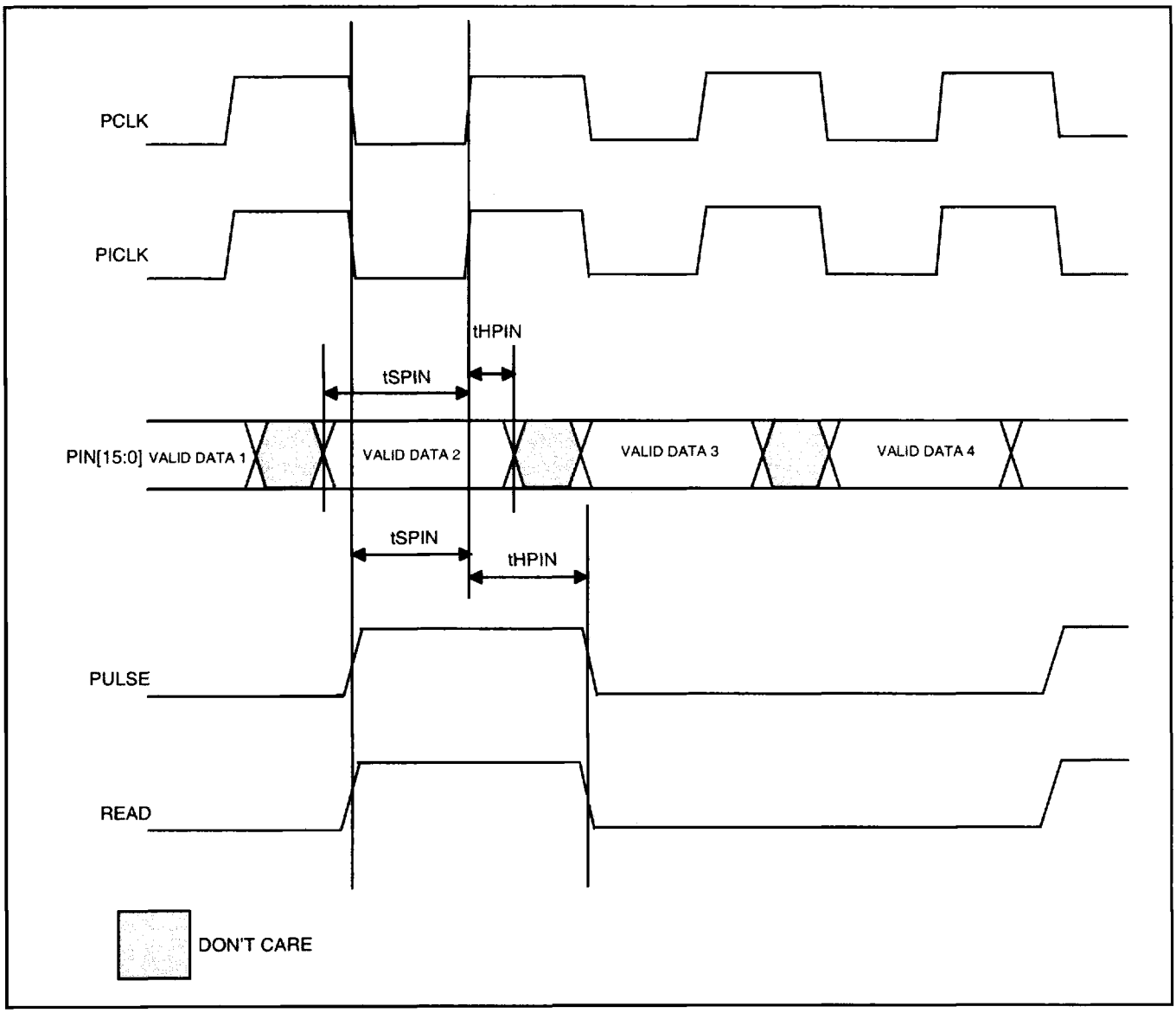
Figure 19. Block Diagram



Block Diagram

In the configuration shown above, both the loops (PCLK to PICLK) and (Pulse to Read) have 0 delay (they are shorted). S3043 is clocking data out of the customer logic. The oscillator frequency REFCLK is given to the PLL. The output of the PLL is given to the multiplier and divider circuits. The output of the chip PCLK, is used to clock data out of the customer logic. The PICLK is in phase and has the same frequency as PCLK .It used to clock in data to the register in S3043. The data will have the same frequency as PICLK, but it may not be in phase with PICLK. It is important to meet the set-up and hold time constraints in this case.

Figure 20.


PCLK
PICLK
tHPIN
tSPIN
PIN[15:0]
VALID DATA 1
VALID DATA 2
VALID DATA 3
VALID DATA 4
tSPIN
tHPIN
PULSE
READ
DON'T CARE

In the figure shown below, we are using the 2nd configuration of the elastic store buffer. This configuration fully utilizes the elastic store buffer and allows the user a delay accommodation of 0 to 14ns. The PULSE delay must follow the PCLK delay. It is very important that the relationship between these two signals be kept all the way through the loop. Otherwise it is possible to under or over spill the buffer. It is important to insure that the PULSE signal is retimed along with the outgoing data to the S3043.

Figure 21.

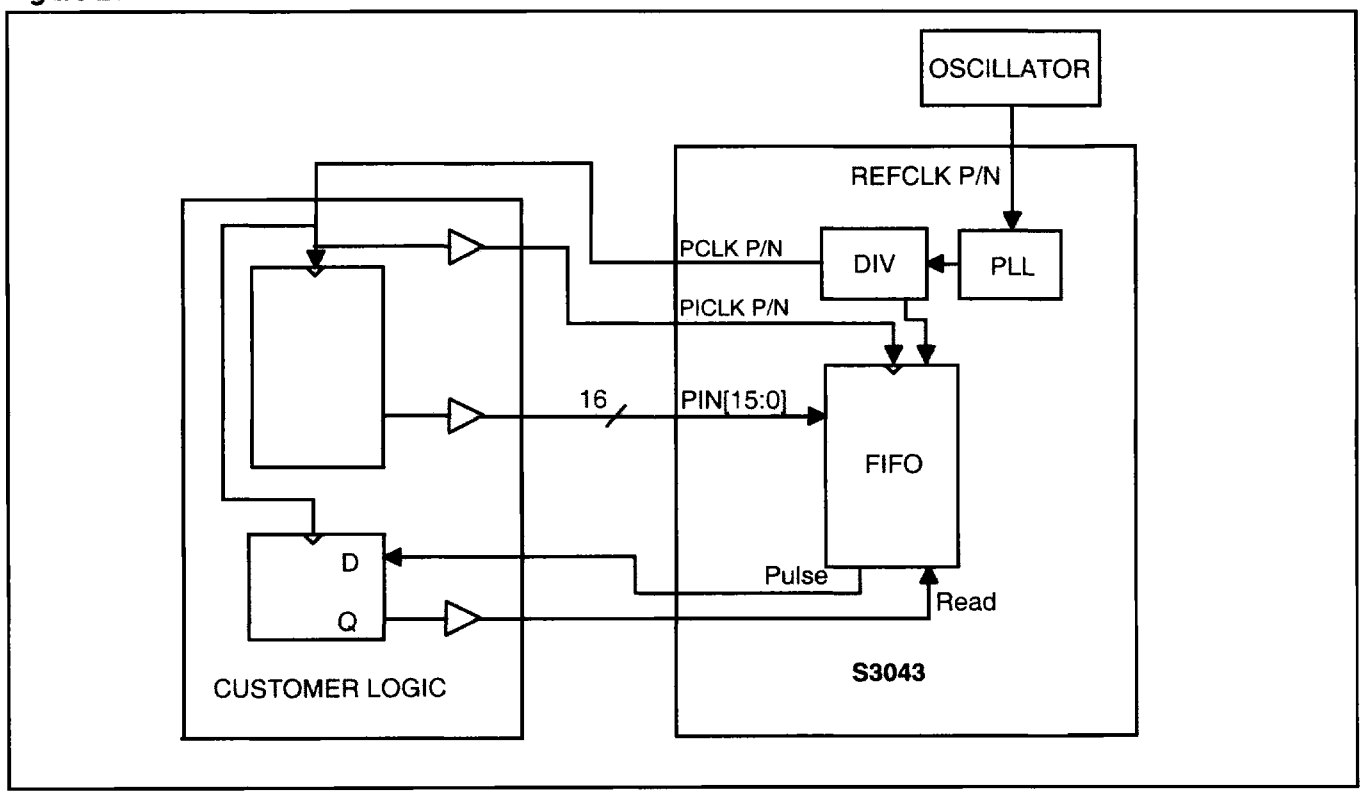


Figure 22.

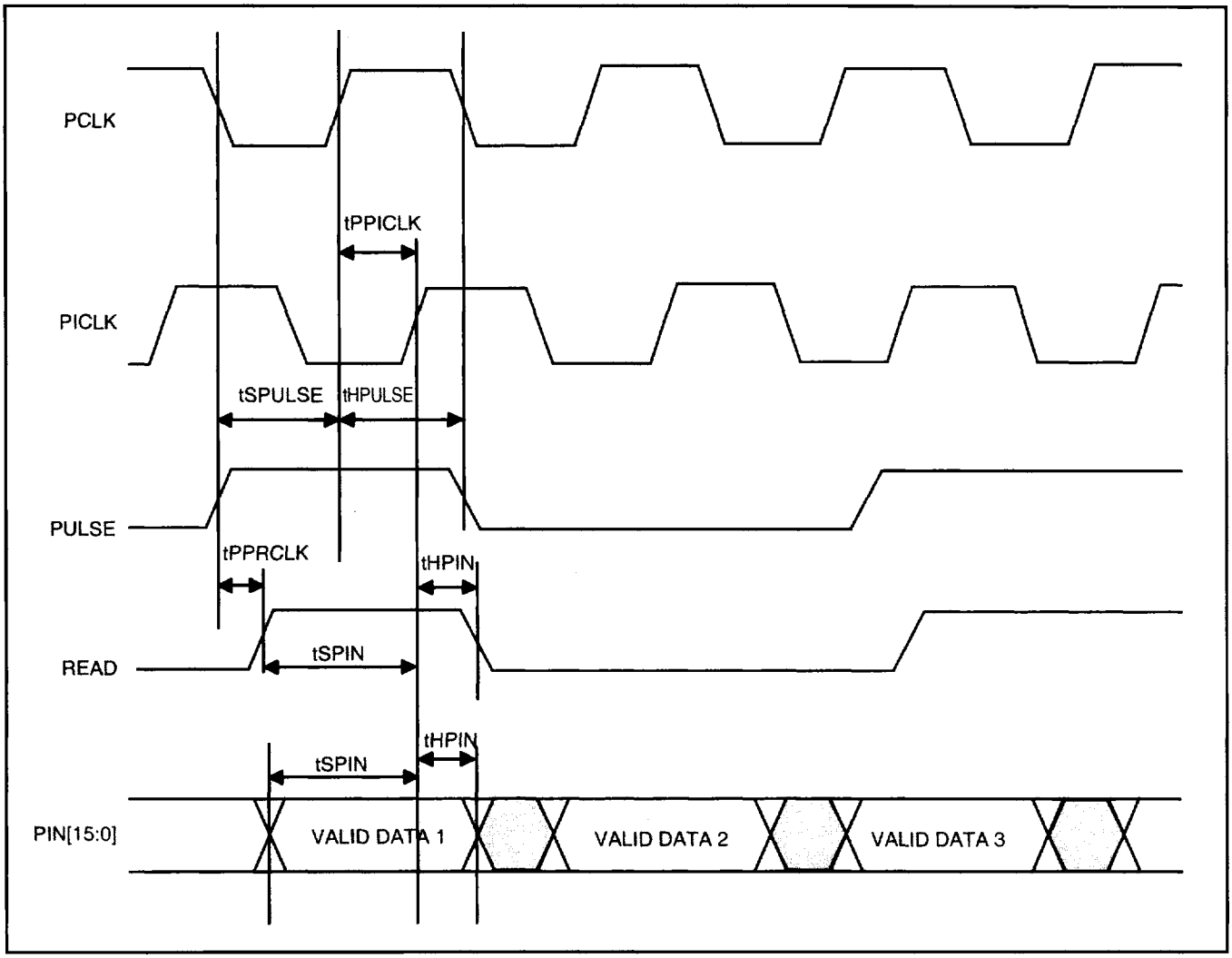
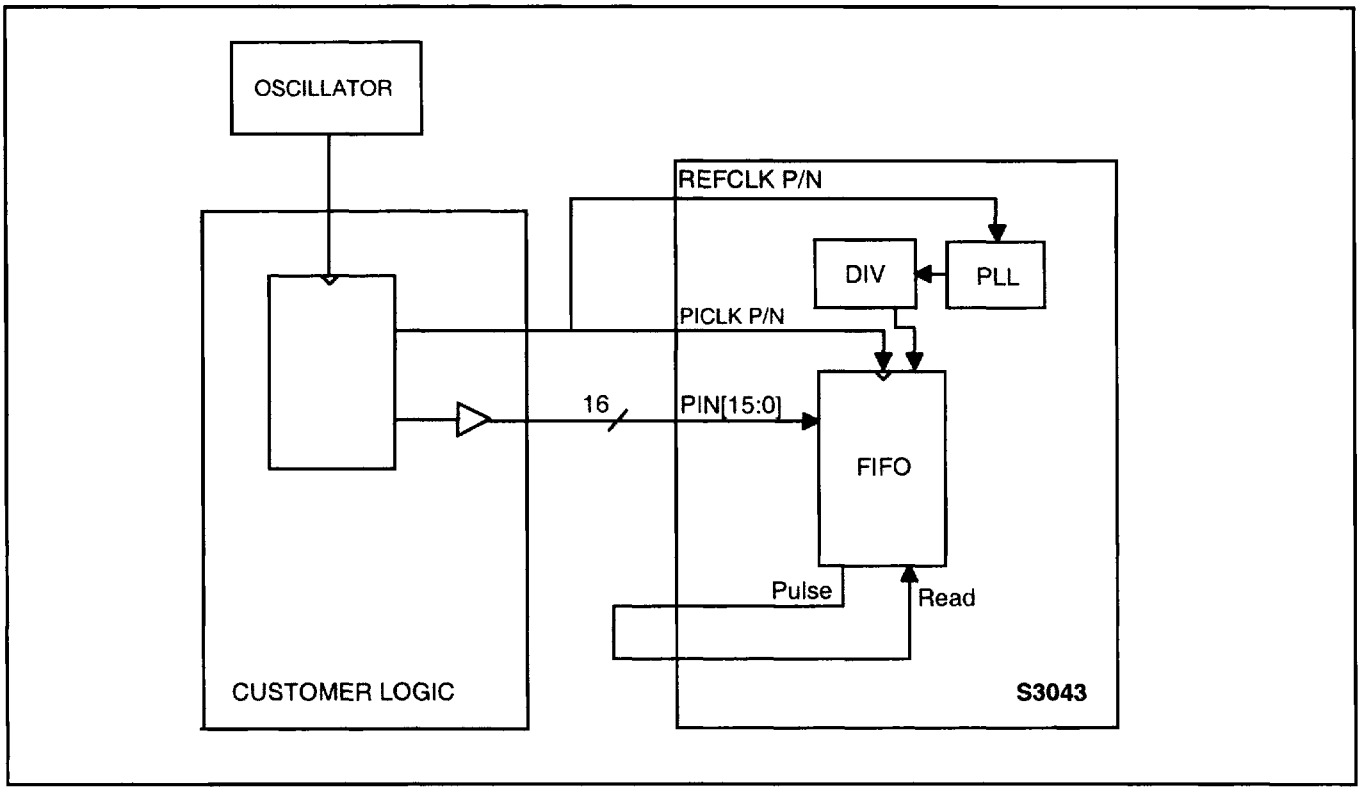

PCLK
tPPICLK
PICLK
tSPULSE
tHPULSE
PULSE
tPPRCLK
tHPIN
READ
tSPIN
tHPIN
tSPIN
PIN[15:0]
VALID DATA 1
VALID DATA 2
VALID DATA 3

Figure 23.

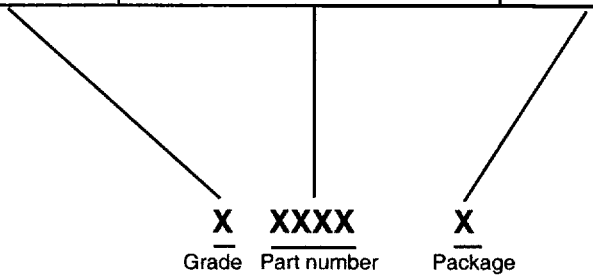


In some applications it is necessary to "forward clock" the data in a SONET/SDH system. In this application the reference clock from which the high speed serial clock is synthesized and the parallel data clock both originate from the same clock source. The timing control logic in the S3043 automatically generates an internal load signal which has the fixed relationship to the reference clock. The logic takes in to account the variation of the reference clock to the internal load signal over temperature and voltage. The connections required to implement the design are shown in the above figure. The setup and hold times for the PICLK to the data must be met by the customer logic. For timing diagram refer to Figure 16.

Possible Problems: In order to meet the jitter generation specifications required by SONET, the jitter of the reference clock must be minimized. It may be difficult to meet the SONET jitter generation specifications using a reference clock generated from the customer logic.

Ordering Information

GRADE	TRANSMITTER	PACKAGE
S – Industrial/Commercial	3043	A – 80 PQFP/TEP



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