FEATURES
18-Bit Dynamic Range
  12-Bit Significand
  6-Bit Normalization
100 kHz Conversion Rate
Sample-and-Hold Included
Status Word

APPLICATIONS
Sonar Signal Processing
Vibration Analysis
PC Data Acquisition
Medical Instrumentation
General Purpose DSP

AD1330 FUNCTIONAL BLOCK DIAGRAM

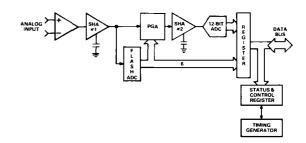
PRODUCT DESCRIPTION

The AD1330 is an 18-bit Floating Point Data Acquisition System. The device will digitize signals up to 50 kHz, at conversion rates up to 100 kHz. The output word format consists of an 18-bit word expressed as a 12-bit 2s complement significand and a 6-bit normalization term. The device offers 12-bits of resolution and 18-bits of dynamic range.

The AD1330 incorporates all of the necessary circuitry to acquire, hold and digitize the input signal, and output a digital representation. A complete AD1330 consists of two hybrids, one a 32-pin and the other a 48-pin. The 32-pin hybrid contains the "front end" or Analog Input Section (AIS), while the 48-pin package contains the "back-end" or Conversion & Control Section (CCS).

The analog input section consists of: differential amplifier, sample-and-hold and programmable gain amplifier. The differential amplifier and sample-and-hold have been optimized for low noise, low harmonic distortion and wide dynamic range. The differential amplifier provides optional ground sensing. Ground sensing is enabled by connecting the sense input to analog ground at the signal source. In addition, the user may select whether to bypass the differential amplifier since the input and output connections are made available at the package pins. Operation of the sample-and-hold is via the SHA1H-L and SHA1S-L signals which are internally generated by the control logic. The SHA is compensated for droop, distortion and feedthrough. The PGA incorporates an auto-zero loop to remove dc offsets. The auto-zero loop is enabled by connecting the auto-zero out to PGA in. All control signals to the PGA-AUTOZ-L, SHORT-L and GAIN-L through GAIN64-L are generated by the control logic.

The CCS contains a 7-bit flash ADC, a second SHA, 12-bit ADC, control logic and bus interface logic. The flash ADC generates the first conversion product (normalization constant) which in turn is used to set the gain of the PGA. The SHA is used to pipeline the analog input and to hold it for conversion by the successive approximation 12-bit ADC. The control logic generates all of the required timing and control signals to the AIS and CCS. The bus interface circuitry (BI) provides a high speed interface to a 16-bit data bus. The AD1330 generates an interrupt signal which may be used to initiate a read cycle. Reading of output data clears the interrupt; otherwise the interrupt is automatically cleared and output data is updated after 4.8 microseconds.

On each conversion cycle there are three output words available from the AD1330. The first two contain the ADC and normalization outputs; the third contains the status world. A complete result is obtained by multiplying (or scaling) the ADC result by the normalization constant.

The AD1330 has four operating modes: auto gain, fixed gain, forced gain and autocalibrate. In auto gain mode the PGA gain is set during each conversion cycle according to the result from the flash ADC. This process maximizes the amplitude of the signal presented to the 12-bit ADC thereby optimizing the resolution and accuracy of the conversion process. The fixed gain mode holds the last gain setting and inhibits any further updates to the PGA. The forced gain mode allows the user to set a specific gain via the data bus. In autocalibrate, the AD1330 corrects for any offset voltages in the second SHA and 12-bit ADC. Mode selection should be made immediately after reading the previous result. Changing modes before readback may overwrite the output data and is not recommended. Autocalibrate takes 10 microseconds, and one such cycle is initiated on powerup and at any time RST-L is asserted.