Commercial and Industrial DDR4 4Gb SDRAM

Features

- **Data Integrity**
  - Auto Self Refresh (ASR) by DRAM built-in TS
  - Auto Refresh and Self Refresh Modes
- **DRAM access bandwidth**
  - Separated IO gating structures by Bank Groups
  - Self Refresh Abort
  - Fine Granularity Refresh
- **Signal Synchronization**
  - Write Leveling via MR settings[1]
  - Read Leveling via MPR
- **Reliability & Error Handling**
  - Command/Address Parity
  - Databus Write CRC
  - MPR readout
  - Boundary Scan (X16)
- **Signal Integrity**
  - Internal VREFDQ Training
  - Read Preamble Training
  - Gear Down Mode
  - Per DRAM Addressability
  - Configurable DS for system compatibility
  - Configurable On-Die Termination
  - Data bus inversion (DBI)
  - ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240 Ω ± 1%)
- **Power Saving and efficiency**
  - POD with VDDQ termination
  - Command/Address Latency (CAL)
  - Maximum Power Saving
  - Low-power Auto Self Refresh (LPASR)

Options

- **Speed Grade (CL-TRCD-TRP)** [2]
  - 2133 Mbps / 15-15-15
  - 2400 Mbps / 16-16-16
  - 2666 Mbps / 18-18-18
- **Temperature Range (T_c)** [3]
  - Commercial Grade = 0℃~95℃
  - Industrial Grade = -40℃~95℃
- **VDD/VDDQ/VPP** [5]
  - 1.2V / 1.2V / 2.5V
  - 1.35V / 1.35V / 2.5V

Programmable Functions

- **Output Driver Impedance (34/48)**
- **CAS Write Latency (9/10/11/12/14/16/18)**
- **Additive Latency (0/CL-1/CL-2)**
- **$\overline{CS}$ to Command Address Latency(3/4/5/6/8)**
- **Command Address Parity Latency(4/5/6)**
- **Write Recovery Time (10/12/14/16/18/20/24)**
- **Burst Type (Sequential/Interleaved)**
- **RTT_PARK(34/40/48/60/80/120/240)**
- **RTT_NOM(34/40/48/60/80/120/240)**
- **RTT_WR(80/120/240)**
- **Read Preamble (1T/2T)**
- **Write Preamble (1T/2T)**
- **Burst Length (BL8/BC4/BC4 or 8 on the fly)**
- **LPASR(Manual:Normal/Reduced/Extended, Auto:TS)**

Packages / Density Information

Lead-free RoHS compliance and Halogen-free

4Gb (Org. / Package)		Dimension (mm)	Ball pitch (mm)
512Mbx8	78-ball TFBGA	9.00 x 11.00	0.80
256Mbx16	96-ball TFBGA	9.00 x 13.00	0.80

Density and Addressing

Organization	512Mb x 8	256Mb x 16
Banks	4 (BA[1:0])	4 (BA[1:0])
Bank Groups	4 (BG[1:0])	2 (BG[0])
Row Address	32K (A[14:0])	32K (A[14:0])
Column Address	1K (A[9:0])	1K (A[9:0])
Page Size	1KB	2KB
tREFI [3]	Tc≦85℃:7.8μs, Tc>85℃:3.9μs	
tRFC [4]	260ns	

NOTE 1 Write Leveling feedback should be given on all data bits in parallel.
NOTE 2 For the same organization and voltage, the timing specification of high speed bin is backward compatible with low speed bin.
NOTE 3 Violating tREFI is not guaranteed.
NOTE 4 Violating tRFC is not guaranteed.
NOTE 5 1.2V parts are not backward compatible with 1.35V parts.

Ordering Information

Organization	Part Number	Package	VDD/VDDQ/VPP[2]	Speed[3]		
				Clock (MHz)	Data Rate (Mb/s)	CL-TRCD-TRP
Commercial Grade						
512M x 8	NT5AD512M8B1-FM[1]	78-Ball	1.2V/1.2V/2.5V	1066	DDR4-2133	15-15-15
	NT5AD512M8B1-GN[1]			1200	DDR4-2400	16-16-16
	NT5AD512M8B1-HP[1]			1333	DDR4-2666	18-18-18
	NT5AE512M8B1-FM[1]		1.35V/1.35V/2.5V	1066	DDR4-2133	15-15-15
	NT5AE512M8B1-GN[1]			1200	DDR4-2400	16-16-16
	NT5AE512M8B1-HP[1]			1333	DDR4-2666	18-18-18
256M x 16	NT5AD256M16B2-FM	96-Ball	1.2V/1.2V/2.5V	1066	DDR4-2133	15-15-15
	NT5AD256M16B2-GN			1200	DDR4-2400	16-16-16
	NT5AD256M16B2-HP[1]			1333	DDR4-2666	18-18-18
	NT5AE256M16B2-FM[1]		1.35V/1.35V/2.5V	1066	DDR4-2133	15-15-15
	NT5AE256M16B2-GN[1]			1200	DDR4-2400	16-16-16
	NT5AE256M16B2-HP[1]			1333	DDR4-2666	18-18-18
Organization	**Part Number**	**Package**	**VDD/VDDQ/VPP[2]**	**Speed[3]**		
				Clock (MHz)	**Data Rate (Mb/s)**	**CL-TRCD-TRP**
Industrial Grade						
512M x 8	NT5AD512M8B1-FMI[1]	78-Ball	1.2V/1.2V/2.5V	1066	DDR4-2133	15-15-15
	NT5AD512M8B1-GNI[1]			1200	DDR4-2400	16-16-16
	NT5AD512M8B1-HPI[1]			1333	DDR4-2666	18-18-18
256M x 16	NT5AD256M16B2-FMI[1]	96-Ball	1.2V/1.2V/2.5V	1066	DDR4-2133	15-15-15
	NT5AD256M16B2-GNI[1]			1200	DDR4-2400	16-16-16
	NT5AD256M16B2-HPI[1]			1333	DDR4-2666	18-18-18

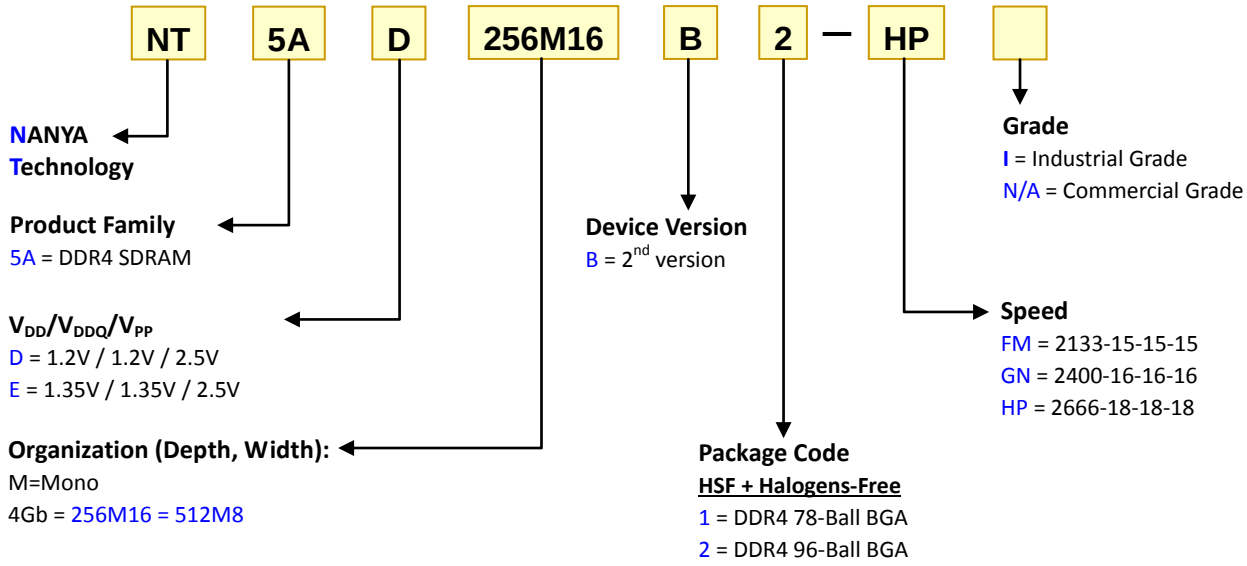
NOTE 1 Please confirm with NTC for the available schedule.

NOTE 2 1.2V parts are not backward compatible with 1.35V parts.

NOTE 3 For the same organization and voltage, the timing specification of high speed bin is backward compatible with low speed bin. For instance:

- DDR4-2666 18-18-18 is compatible with DDR4-2400 16-16-16 and DDR4-2133 15-15-15.

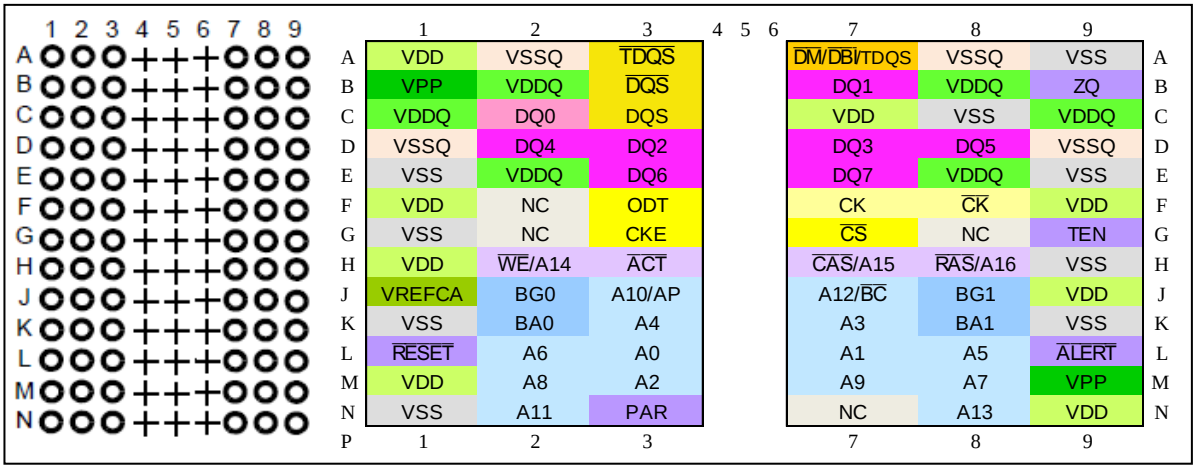
NANYA Consumer Component Part Numbering Guide



78 Ball (X8) Ball Assignment

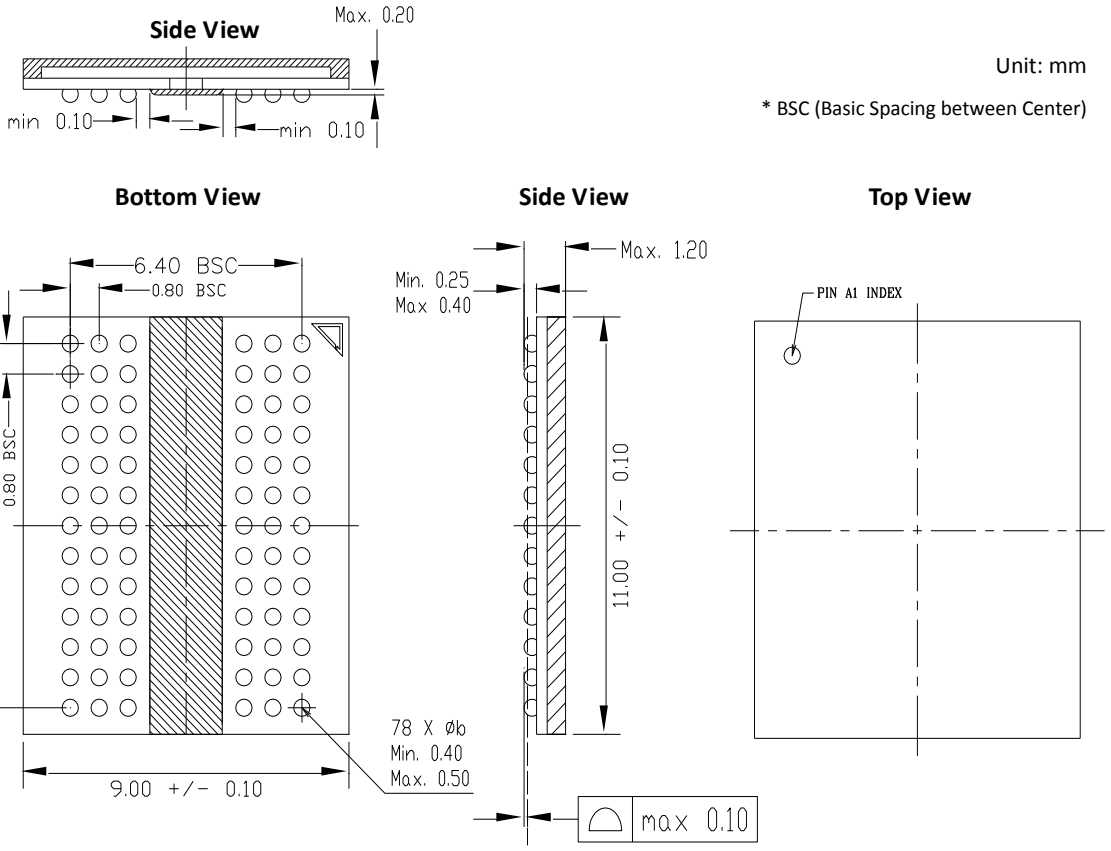
<TOP View>

See the balls through the package



	1	2	3	4 5 6	7	8	9	
A	VDD	VSSQ	$\overline{TDQS}$		$\overline{DM}/\overline{DBI}$/TDQS	VSSQ	VSS	A
B	VPP	VDDQ	$\overline{DQS}$		DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS		VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2		DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6		DQ7	VDDQ	VSS	E
F	VDD	NC	ODT		CK	$\overline{CK}$	VDD	F
G	VSS	NC	CKE		$\overline{CS}$	NC	TEN	G
H	VDD	$\overline{WE}$/A14	$\overline{ACT}$		$\overline{CAS}$/A15	$\overline{RAS}$/A16	VSS	H
J	VREFCA	BG0	A10/AP		A12/$\overline{BC}$	BG1	VDD	J
K	VSS	BA0	A4		A3	BA1	VSS	K
L	$\overline{RESET}$	A6	A0		A1	A5	$\overline{ALERT}$	L
M	VDD	A8	A2		A9	A7	VPP	M
N	VSS	A11	PAR		NC	A13	VDD	N
P	1	2	3		7	8	9	

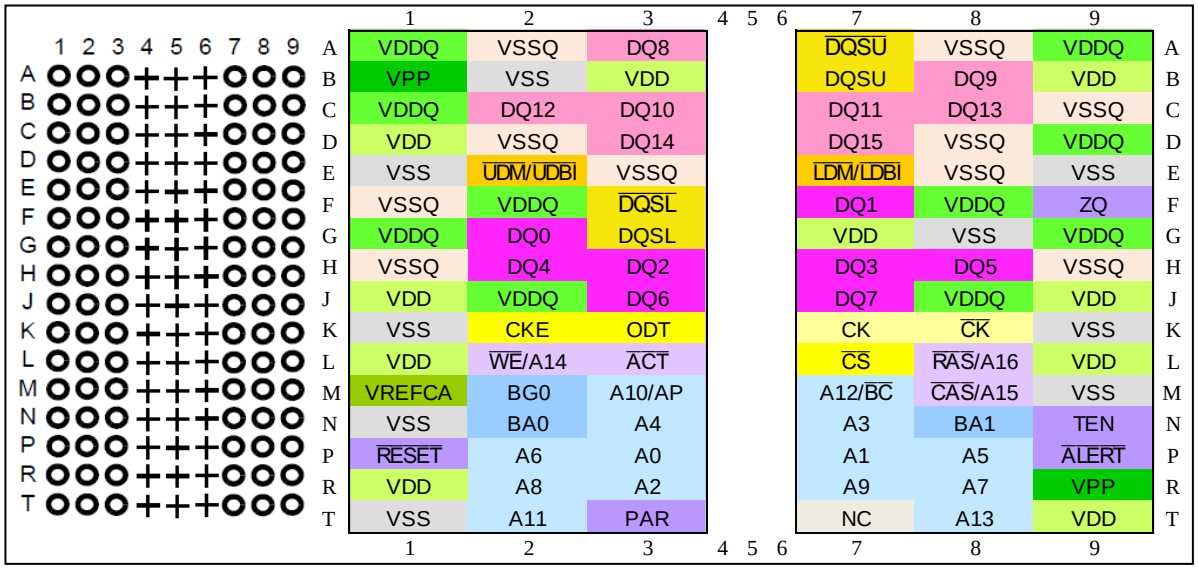
Package Outline Drawing



96 Ball (X16) Ball Assignment

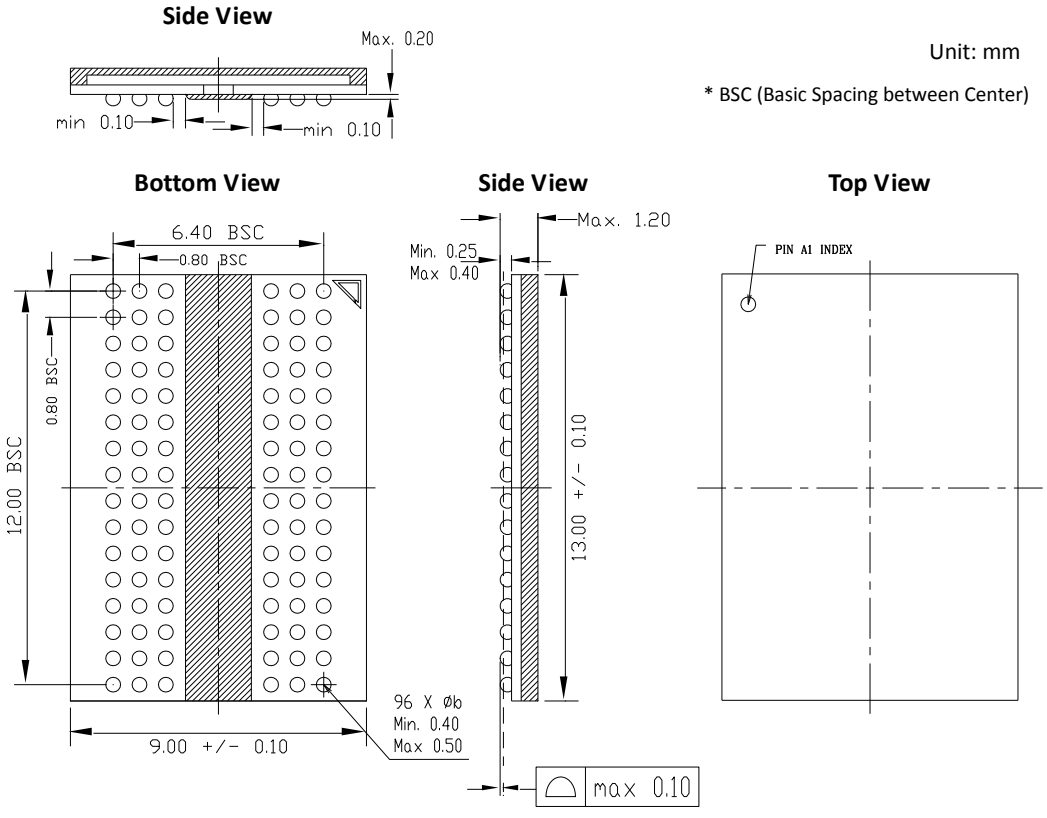
<TOP View>

See the balls through the package



	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQ8				$\overline{DQSU}$	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU	DQ9	VDD	B
C	VDDQ	DQ12	DQ10				DQ11	DQ13	VSSQ	C
D	VDD	VSSQ	DQ14				DQ15	VSSQ	VDDQ	D
E	VSS	$\overline{UDM}$/UDBI	VSSQ				$\overline{LDM}$/LDBI	VSSQ	VSS	E
F	VSSQ	VDDQ	$\overline{DQSL}$				DQ1	VDDQ	ZQ	F
G	VDDQ	DQ0	DQSL				VDD	VSS	VDDQ	G
H	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	H
J	VDD	VDDQ	DQ6				DQ7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK	$\overline{CK}$	VSS	K
L	VDD	$\overline{WE}$/A14	$\overline{ACT}$				$\overline{CS}$	$\overline{RAS}$/A16	VDD	L
M	VREFCA	BG0	A10/AP				A12/$\overline{BC}$	$\overline{CAS}$/A15	VSS	M
N	VSS	BA0	A4				A3	BA1	$\overline{TEN}$	N
P	$\overline{RESET}$	A6	A0				A1	A5	$\overline{ALERT}$	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T
	1	2	3	4	5	6	7	8	9	

Package Outline Drawing



Ball Descriptions

Symbol	Type	Description
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When ODT is enabled, on-die termination (RTT) is applied only to each DQ, DQS, $\overline{DQS}$, $\overline{DM}$/$\overline{DBI}$/TDQS, and $\overline{TDQS}$ signal for x4, x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, RTT is applied to each DQ, DQSU, $\overline{DQSU}$, DQSL, $\overline{DQSL}$, $\overline{UDM}$, and $\overline{LDM}$ signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
BA[1:0]	Input	**Bank Address Inputs:** Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MRS cycle.
BG[1:0]	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0.
$\overline{ACT}$	Input	**Command input:** $\overline{ACT}$ defines the Activation command being entered along with $\overline{CS}$. The input into $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 will be considered as Row Address A16, A15 and A14
$\overline{RAS}$/A16 $\overline{CAS}$/A15 $\overline{WE}$/A14	Input	**Command Inputs:** $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 (along with $\overline{CS}$) define the command being entered. Those pins have multi function. For example, for activation with $\overline{ACT}$ Low, those are Addressing like A16,A15 and A14 but for non-activation command with $\overline{ACT}$ High, those are Command pins for Read, Write and other command defined in command truth table.
A10/AP	Input	**Auto precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/$\overline{BC}$	Input	**Burst Chop:** Burst chop: A12/$\overline{BC}$ is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst-chopped).
A[17:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/$\overline{BC}$, $\overline{WE}$/A14, $\overline{CAS}$/A15, $\overline{RAS}$/A16 , have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts while A17 is only used on some 16Gb parts.

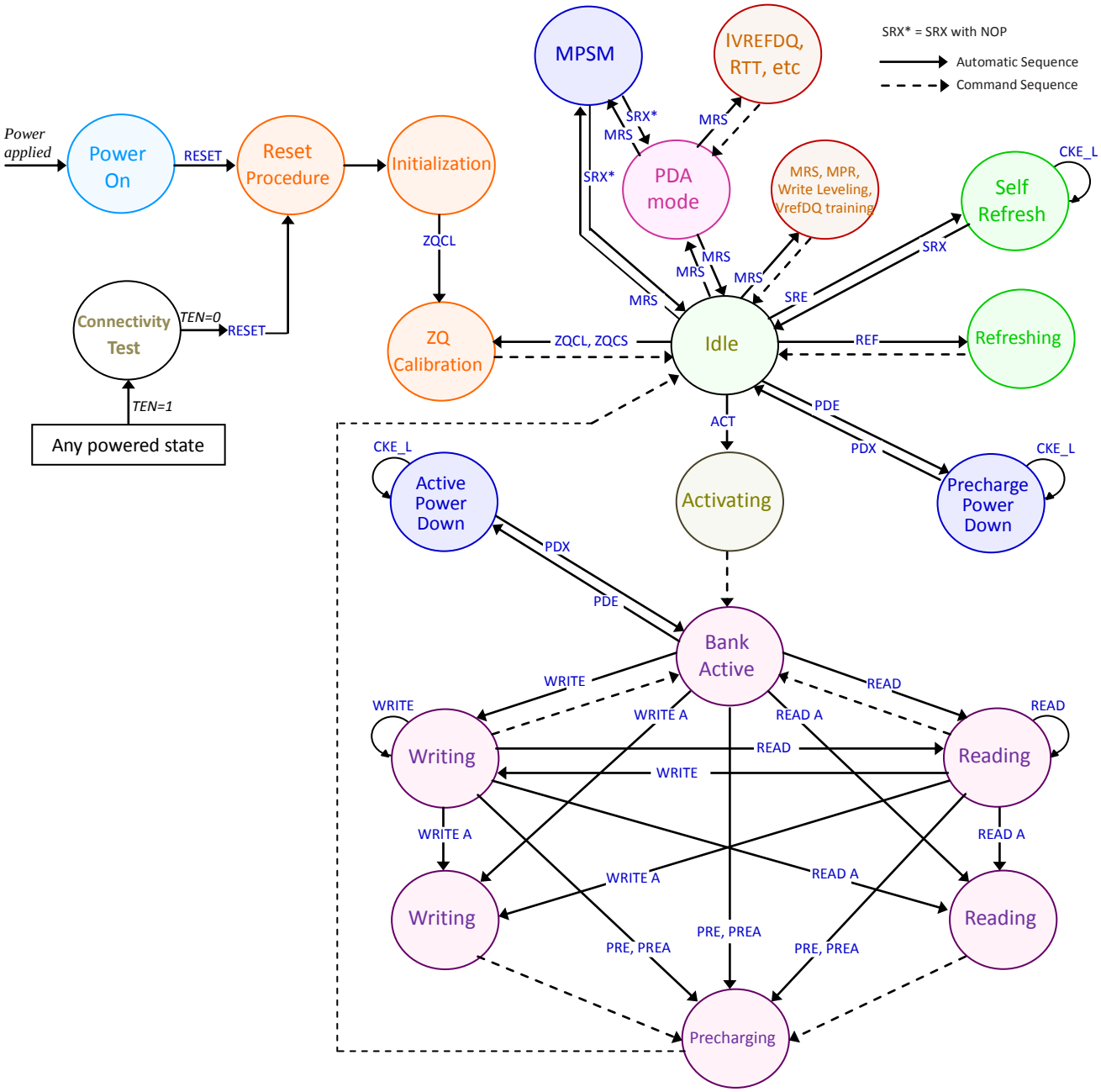
Symbol	Type	Description
PAR	Input	**Parity for command and address:** DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with $\overline{ACT}$,$\overline{RAS}$/A16,$\overline{CAS}$/A15,$\overline{WE}$/A14, A12/$\overline{BC}$, A10/AP, A17-A0, BA0-BA1, and BG0-BG1. Input parity should maintain at the rising edge of the clock and at the same time with command & address with $\overline{CS}$ LOW. Control pins NOT covered by the PARITY signal are $\overline{CS}$, CKE, and ODT. Unused address pins that are density and configuration specific should be treated internally as 0s by the DRAM parity logic.
DQ	Input/output	**Data input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If Write CRC is enabled via Mode register then the Write CRC code is added at the end of Data Burst. Either anyone or all DQ0, DQ1, DQ2, and DQ3 is used as monitoring of internal Vref level during test via Mode Register Setting MR4[4]=High, training times change when enabled. During this mode, RTT value should be set to Hi-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DQS/$\overline{DQS}$ DQSL/$\overline{DQSL}$ DQSU/$\overline{DQSU}$	Input/output	**Data Strobe:** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, DQSL corresponds to the data on DQ[7:0]; DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0] respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
TDQS/$\overline{TDQS}$	Output	**Termination Data Strobe:** TDQS/$\overline{TDQS}$ is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same R_{TT} termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When the TDQS function is disabled via the mode register, the $\overline{DM}$/$\overline{DBI}$/TDQS pin will provide the data mask ($\overline{DM}$) function or Data Bus Inversion ($\overline{DBI}$) depending on MR5, and the $\overline{TDQS}$ pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations.
$\overline{DM}$ $\overline{LDM}$, $\overline{UDM}$	Input	**Input data mask:** $\overline{DM}$ is an input mask signal for write data. Input data is masked when $\overline{DM}$ is sampled LOW coincident with that input data during a write access. $\overline{DM}$ is sampled on both edges of DQS. $\overline{DM}$ is muxed with $\overline{DBI}$ function by Mode Register A[12:10] setting in MR5. For x8 device, the function of $\overline{DM}$ or TDQS is enabled by Mode Register A11 setting in MR1. $\overline{DBI}$ is an input/output identifing whether to store/output the true or inverted data. If $\overline{DBI}$ is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if $\overline{DBI}$ is HIGH. DM is not supported in X4.
$\overline{DBI}$ $\overline{UDBI}$, $\overline{LDBI}$	Input/output	**DBI input/output:** Data bus inversion. $\overline{DBI}$ is an input/output signal used for data bus inversion in the x8 configuration. $\overline{UDBI}$ and $\overline{LDBI}$ are used in the x16 configuration; $\overline{UDBI}$ is associated with DQ[15:8], and $\overline{LDBI}$ is associated with DQ[7:0]. The DBI feature is not supported on x4 configurations. $\overline{DBI}$ can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See Data Bus Inversion (DBI).
$\overline{ALERT}$	Output	**Alert output:** It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then $\overline{ALERT}$ goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then $\overline{ALERT}$ goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, open-drain $\overline{ALERT}$ Pin must be bounded to VDD on board.
TEN	Input	**Connectivity test mode:** Connectivity Test Mode is active when TEN is HIGH, and inactive when TEN is LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with AC HIGH and LOW at 80% and 20% of VDD (960mV for DC HIGH and 240mV for DC LOW). Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
ZQ	Reference	**Reference pin for ZQ calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.

Symbol	Type	Description
$\overline{\text{RESET}}$	Input	**Active Low Asynchronous Reset:** Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V.
VPP	Supply	**DRAM activating power supply:** 2.5V (2.375V min , 2.75V max)
VDD	Supply	**Power Supply:** 1.2V ± 0.060V or 1.35V -0.067V/+0.1V
VDDQ	Supply	**DQ Power Supply:** 1.2V ± 0.060V or 1.35V -0.067V/+0.1V
VSS	Supply	**Ground**
VSSQ	Supply	**DQ Ground**
VREFCA	Supply	**Reference voltage for CA**
NC	-	**No Connect:** No internal electrical connection is present.
NF	-	**No function:** May have internal connection present, but has no function.
RFU	-	Reserved for future use.

Notes:

1. Input only pins (BG0-BG1,BA0-BA1, A0-A17, $\overline{\text{ACT}}$, $\overline{\text{RAS}}$/A16, $\overline{\text{CAS}}$/A15, $\overline{\text{WE}}$/A14, $\overline{\text{CS}}$, CKE, ODT, and $\overline{\text{RESET}}$) do not supply termination.
2. The signal may show up in a different symbol but it indicates the same thing. e.g., /CK = CK# = #CK = $\overline{\text{CK}}$ = CKb = CK_n, /DQS = DQS# = #DQS = $\overline{\text{DQS}}$ = DQSb = DQS_n, /CS = CS# = #CS = $\overline{\text{CS}}$ = CSb = CS_n.

Simplified State Diagram



Abbr.	Function	Abbr.	Function	Abbr.	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
ZQCS	ZQ Calibration Short	Write A	WRA, WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
RESET	Start RESET Procedure	TEN	Boundary Scan Mode Enable	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	REF	Refresh, Fine granularity Refresh	MRS	Mode Register Set

Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally conured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a ‘chopped’ burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A14 select the row; refer to Addressing section for more details. The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode ‘on the fly’ (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

RESET and Initialization Procedure

RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values for the following MR settings are defined:

Default MR settings for power-up and reset initialization

MR functions	MR bits	Value
Gear-down mode	MR3 A[3]	1/2 Rate
Per DRAM Addressability	MR3 A[4]	Disable
Max Power Saving Mode	MR4 A[1]	Disable
$\overline{CS}$ to Command/Address Latency	MR4 A[8:6]	Disable
CA Parity Latency Mode	MR5 A[2:0]	Disable

Power-Up and Initialization Sequence

The following sequence (Step 1-15) is required for power-up and initialization:

1) Apply power ($\overline{RESET}$ is recommended to be maintained below 0.2 × VDD; all other inputs may be undefined). $\overline{RESET}$ needs to be maintained for minimum 200µs with stable power. CKE is pulled LOW anytime before $\overline{RESET}$ is being deasserted (MIN time 10ns). The power voltage ramp time between 300mV to VDD, min must be no greater than 200ms, and, during the ramp, VDD must be greater than or equal to VDDQ and (VDD - VDDQ) < 0.3V. VPP must ramp at the same time or earlier than VDD, and VPP must be equal to or higher than VDD at all times.

   During power-up, either of the following conditions may exist and must be met:

   • Condition A
   - VDD and VDDQ are driven from a single-power converter output.
   - The voltage levels on all balls other than VDD, VDDQ, VSS, and VSSQ must be less than or equal to VDDQ, and VDD on one side and must be greater than or equal to VSSQ and VSS on the other side.
   - VTT is limited to 0.76V MAX when the power ramp is complete.
   - VREFCA tracks VDD/2.

   • Condition B
   - Apply VDD without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT and VREFCA.
   - Apply VPP without any slope reversal before or at the same time as VDD.
   - The voltage levels on all pins other than VPP, VDD, VDDQ, VSS, and VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2) After $\overline{RESET}$ is de-asserted, wait for another 500µs until CKE becomes active.
   During this time, the DRAM will start internal state initialization; this will be done independently of external clocks. A reasonable attempt was made in the design to have the DRAM power up with the following default MR settings (Refer to the table: default MR settings for power-up and reset initialization).

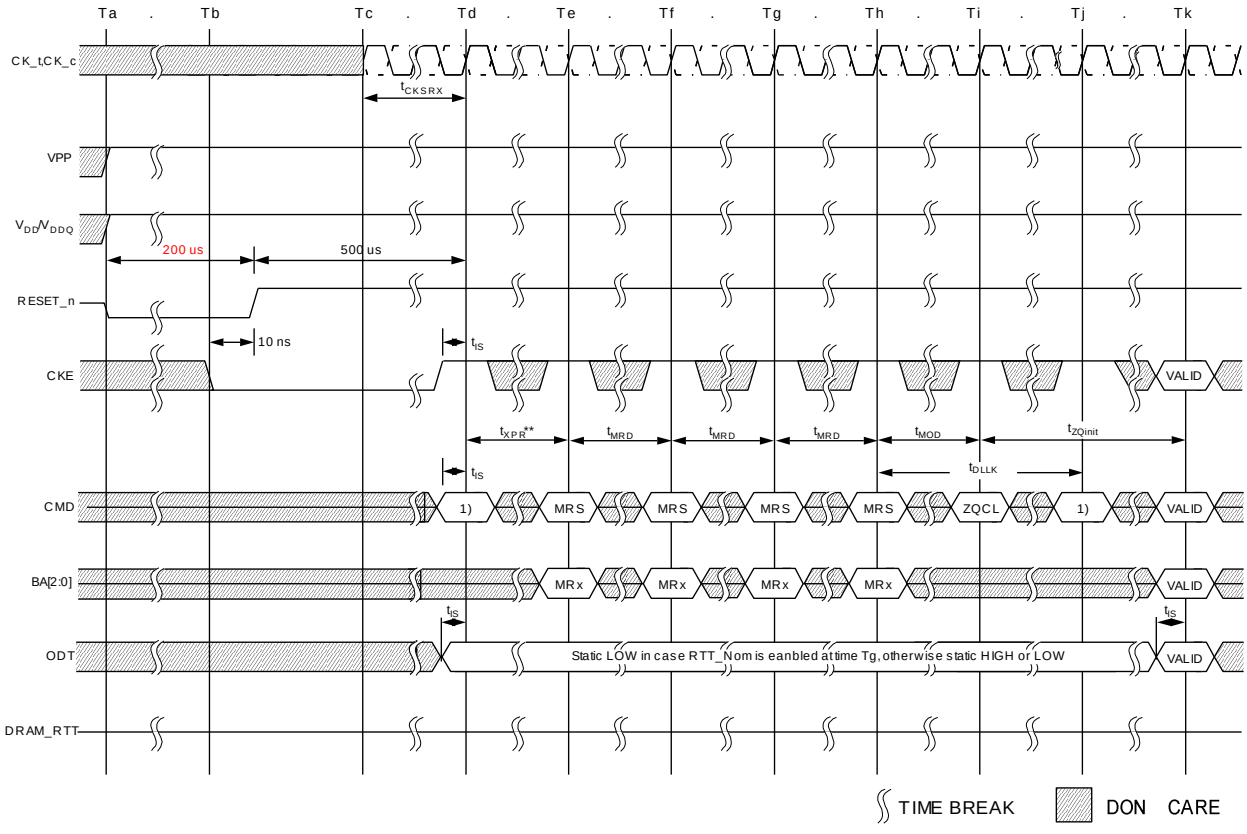
3) Clocks (CK, $\overline{CK}$) need to be started and stabilized for at least 10ns or 5 tCK Clocks (CK, $\overline{CK}$) need to be started and stabilized for at least 10ns or 5 tCK (whichever is larger) before CKE goes active. Because CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also, a DESELECT command must be registered (with tIS setup time to clock) at clock edge Td. After the CKE is registered HIGH after RESET, CKE needs to be continuously registered HIGH until the initialization sequence is finished, including expiration of tDLLK and tZQINIT.

4) The DDR4 SDRAM keeps its ODT in High-Z state as long as $\overline{RESET}$ is asserted. Further, the SDRAM keeps its ODT in

High-Z state after RESET de-assertion until CKE is registered HIGH. The ODT input signal may be in an undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power-up initialization sequence is finished, including the expiration of tDLLK and tZQINIT.

5) After CKE is registered HIGH, wait a minimum of RESET CKE EXIT time, tXPR, before issuing the first MRS command to load mode register (tXPR = MAX (tXS; 5 × tCK).
6) Issue MRS command to load MR3 with all application settings, wait tMRD.
7) Issue MRS command to load MR6 with all application settings, wait tMRD.
8) Issue MRS command to load MR5 with all application settings, wait tMRD.
9) Issue MRS command to load MR4 with all application settings, wait tMRD.
10) Issue MRS command to load MR2 with all application settings, wait tMRD.
11) Issue MRS command to load MR1 with all application settings, wait tMRD.
12) Issue MRS command to load MR0 with all application settings, wait tMOD.
13) Issue a ZQCL command to start ZQ calibration.
14) Wait for tDLLK and tZQINIT to complete.
15) The DDR4 SDRAM will be ready for normal operation.

RESET and Initialization Sequence at Power-On Ramping



NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2 MRS commands must be issued to all mode registers that have defined settings.
NOTE 3 In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
NOTE 4 TEN is not shown; however, it is assumed to be held LOW.

VDD Slew Rate

Symbol	Min	Max	Units	NOTE
VDD_sl	0.004	600	V/ms	1,2
VDD_on		200	ms	3

NOTE 1 Measurement made between 300mV and 80% VDD (minimum level).

NOTE 2 The DC bandwidth is limited to 20MHz

NOTE 3 Maximum time to ramp VDD from 300 mV to VDD minimum.

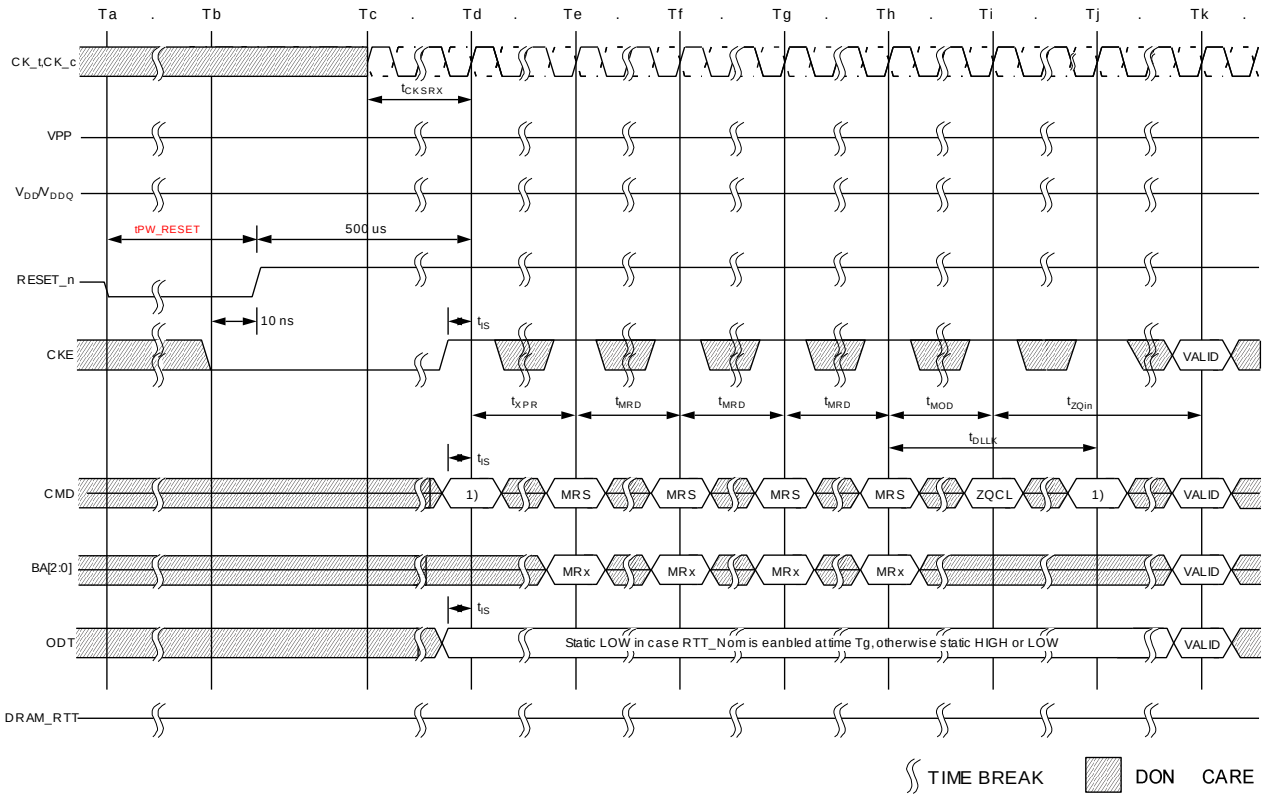
RESET Initialization with Stable Power Sequence

The following sequence is required for $\overline{\text{RESET}}$ at no power interruption initialization:

1. Assert $\overline{\text{RESET}}$ below 0.2 × VDD any time when reset is needed (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 100ns. CKE is pulled LOW before $\overline{\text{RESET}}$ is de-asserted (MIN time 10ns).
2. Follow Steps 2 to 7 in the Reset and Initialization Sequence at Power-on Ramping procedure.

When the reset sequence is complete, the DDR4 SDRAM is ready for normal operation.

RESET Procedure at Power Stable Condition



NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.

NOTE 2 MRS commands must be issued to all mode registers that have defined settings.

NOTE 3 In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0,for example).

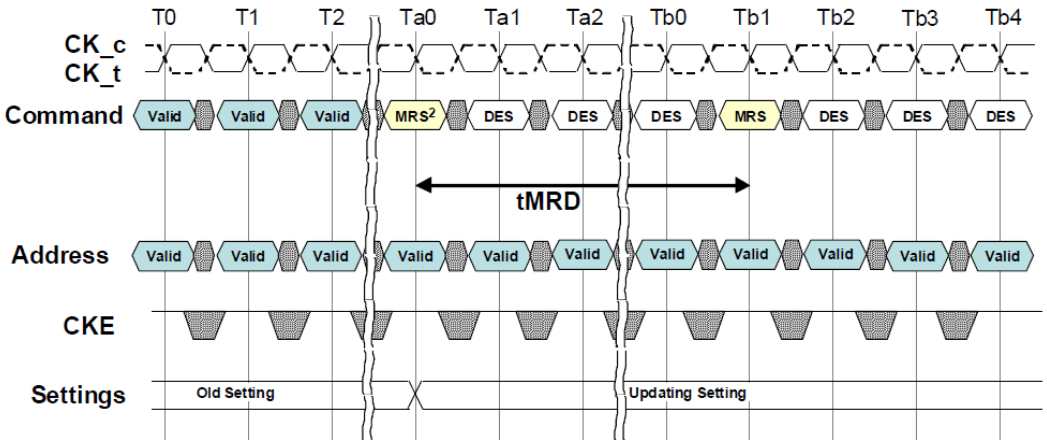
NOTE 4 TEN is not shown; however, it is assumed to be held LOW.

Programming Mode Registers

Mode Register Set (MRS)

MRS	Descriptions
Purpose	For application flexibility, various functions, features, and modes.
Range	Seven Mode Registers. They are divided into various fields depending on functionality and modes.
Regulations	1. As the default values of the Mode Registers (MRn) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation, as user defined variables and they must be programmed. 2. MRS command and DLL Reset do not affect array contents, which mean these commands can be executed any time after power-up without affecting the array contents. 3. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. 4. The contents of the Mode Registers can be altered by re-executing the MRS command during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If the RTT_NOM Feature is enabled in the Mode Register prior and/or after an MRS Command, the ODT Signal must continuously be registered LOW ensuring RTT is in an off State prior to the MRS command. The ODT Signal may be registered high after tMOD has expired. If the RTT_NOM feature is disabled in the Mode Register prior and after an MRS command, the ODT signal can be registered either LOW or HIGH before, during and after the MRS command. 5. The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands. 6. The most MRS command to Non-MRS command delay, tMOD, is required for the DRAM to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding DES. 7. Some of the Mode Register settings affect address/command/control input functionality. In these cases, function updating takes longer than tMOD so the next MRS command only can be allowed when the function updating by current MRS command completed. These MRS commands do not apply tMRD timing to next MRS command. These MRS command input cases have unique a MR setting procedure, so refer to individual function description: • Gear-down mode • Per DRAM Addressability • Max Power Saving Mode • $\overline{CS}$ to Command/Address Latency • CA Parity Latency Mode • VrefDQ training Value • VrefDQ Training mode • VrefDQ training Range

tMRD Timing



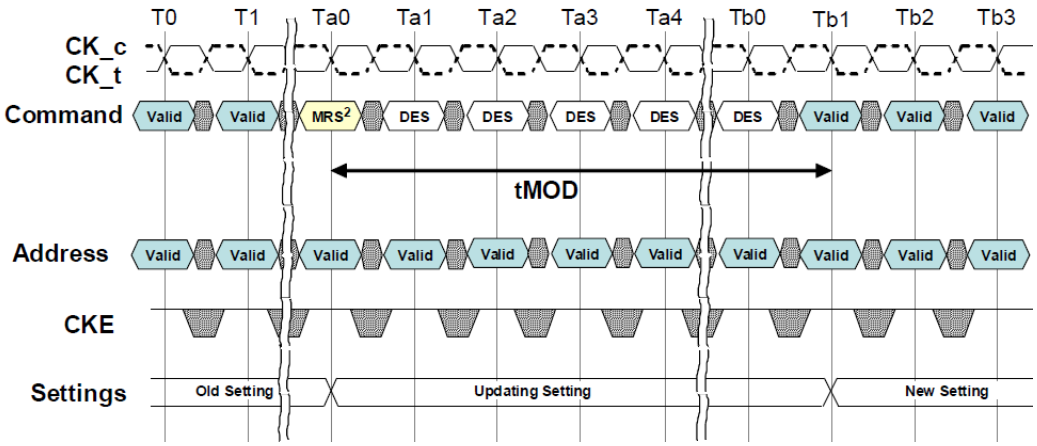
NOTE 1 This timing diagram depicts C/A Parity Mode "Disabled" case.

NOTE 2 tMRD applies to all MRS commands with the following exceptions:

- Geardown Mode
- C/A Parity Mode
- CAL Mode
- Per DRAM addressability Mode
- VrefDQ training value, VreDQ training mode, and VrefDQ Training Range

tMOD Timing

The MRS command to nonMRS command delay, tMOD, is required for the DRAM to update features, except DLL RESET, and is the minimum time required from an MRS command to a nonMRS command, excluding DES.



NOTE 1 This timing diagram depicts C/A Parity Mode "Disabled" case.

NOTE 2 tMOD applies to all MRS commands with the following exceptions:

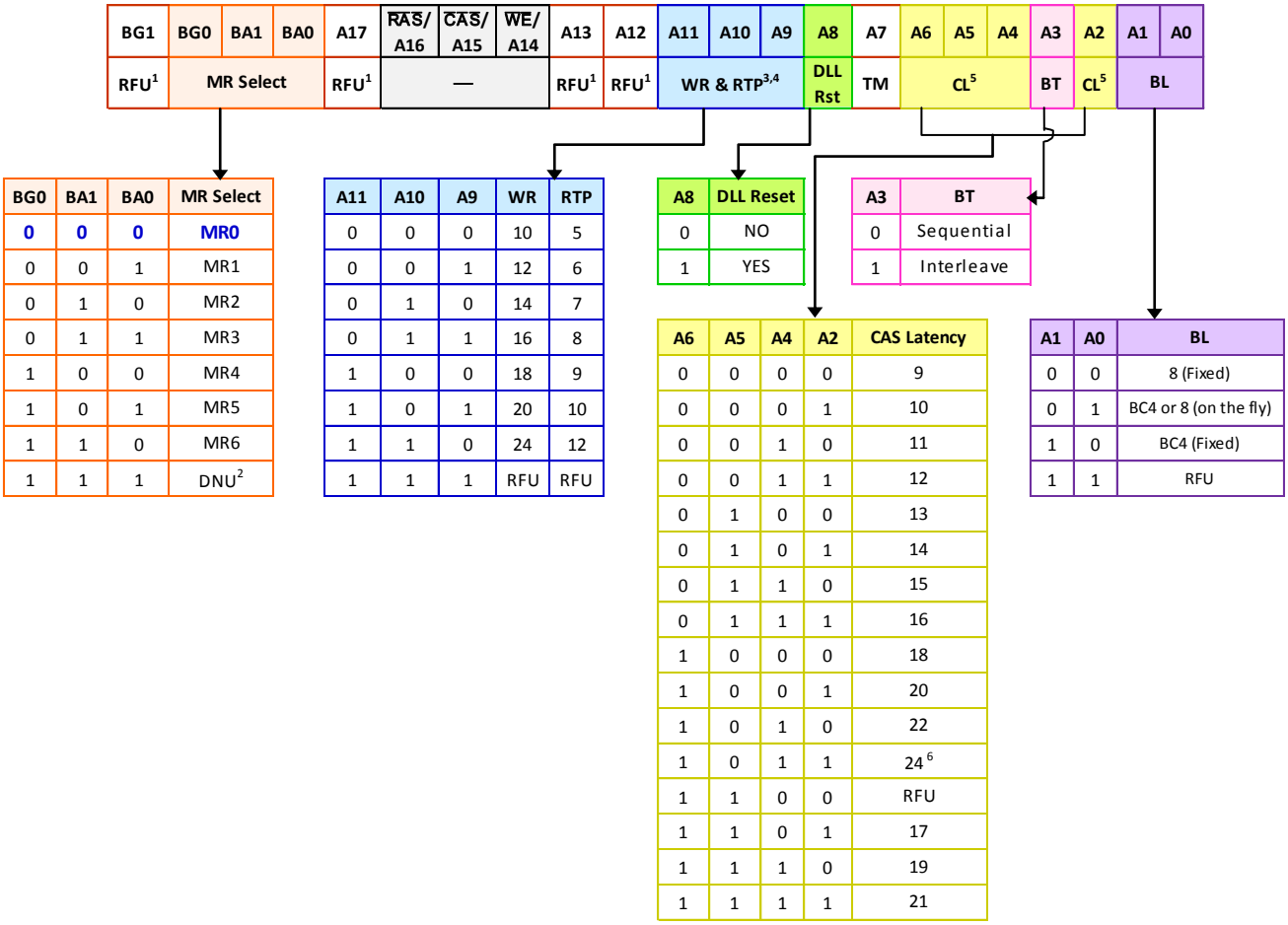
- DLL Enable
- Geardown Mode
- CA Parity Mode
- Maximum Power Savings Mode
- Per DRAM addressability Mode
- VrefDQ training value, internal Vref monitor, VreDQ training mode, and VrefDQ Training Range

MRS Overview

Detail options are described on the following pages.

	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
MR0	RFU[1]	RFU[1]	WR & RTP[3,4]			DLL Rst	TM	CL[5]			BT	CL[5]	BL	
MR1	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	RFU[1]	Qoff[2]	TDQS	RTT_NOM			Wlev	RFU[1]		AL		ODI		DLL
MR2	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	RFU[1]	Write CRC	RTT_WR			RFU[1]	LPASR		CWL			RFU[1]		
MR3	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	RFU[1]	MPR Read Format		Write CMD Latency		Fine Granularity Refresh Mode			TS	PDA	Geardown	MPR Operation	MPR Page Selection	
MR4	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	RFU[1]	tWPRE	tRPRE	tRPRE training	SRF abort	$\overline{CS}$ to CMD/ADDR Latency Mode			RFU[1]	Internal Vref	TCRM	TCRR	MPS	RFU[1]
MR5	A13	A12	A11	A10	A9	A8	A7	A6	A5[3]	A4	A3	A2	A1	A0
	RFU[1]	RDBI	WDBI	DM	CAP Persist	RTT_Park			ODT IB for PD	CAP error	CRC error	CA Parity Latency[4]		
MR6	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	RFU[1]	tCCD_L			RFU[1]		VrefDQ Training	VrefDQ Range	VrefDQ Training Value					
MR7	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	RFU[1]													

Mode Register 0 (MR0)



BG0	BA1	BA0	MR Select
0	**0**	**0**	**MR0**
0	0	1	MR1
0	1	0	MR2
0	1	1	MR3
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU[2]

A11	A10	A9	WR	RTP
0	0	0	10	5
0	0	1	12	6
0	1	0	14	7
0	1	1	16	8
1	0	0	18	9
1	0	1	20	10
1	1	0	24	12
1	1	1	RFU	RFU

A8	DLL Reset
0	NO
1	YES

A3	BT
0	Sequential
1	Interleave

A6	A5	A4	A2	CAS Latency
0	0	0	0	9
0	0	0	1	10
0	0	1	0	11
0	0	1	1	12
0	1	0	0	13
0	1	0	1	14
0	1	1	0	15
0	1	1	1	16
1	0	0	0	18
1	0	0	1	20
1	0	1	0	22
1	0	1	1	24[6]
1	1	0	0	RFU
1	1	0	1	17
1	1	1	0	19
1	1	1	1	21

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	RFU

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS

NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 3 WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer:WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

NOTE 4 The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.

NOTE 5 The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency.

NOTE 6 When CL is equal to 24 or more than 24, AL does not support CL-1.

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following Burst Type and Burst Order table. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selected coincident with the registration of a READ or WRITE command via A12/$\overline{BC}$.

Burst Length	READ/ WRITE	Starting Column Address			Burst Type (Decimal)																Notes
					Sequential								Interleaved								
		A2	A1	A0	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
BC4	READ	0	0	0	0	1	2	3	T	T	T	T	0	1	2	3	T	T	T	T	1,3
		0	0	1	1	2	3	0	T	T	T	T	1	0	3	2	T	T	T	T	1,2,3
		0	1	0	2	3	0	1	T	T	T	T	2	3	0	1	T	T	T	T	1,2,3
		0	1	1	3	0	1	2	T	T	T	T	3	2	1	0	T	T	T	T	1,2,3
		1	0	0	4	5	6	7	T	T	T	T	4	5	6	7	T	T	T	T	1,2,3
		1	0	1	5	6	7	4	T	T	T	T	5	4	7	6	T	T	T	T	1,2,3
		1	1	0	6	7	4	5	T	T	T	T	6	7	4	5	T	T	T	T	1,2,3
		1	1	1	7	4	5	6	T	T	T	T	7	6	5	4	T	T	T	T	1,2,3
	WRITE	0	V	V	0	1	2	3	X	X	X	X	0	1	2	3	X	X	X	X	1,2,4,5
		1	V	V	4	5	6	7	X	X	X	X	4	5	6	7	X	X	X	X	1,2,4,5
BL8	READ	0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	2
		0	0	1	1	2	3	0	5	6	7	4	1	0	3	2	5	4	7	6	2
		0	1	0	2	3	0	1	6	7	4	5	2	3	0	1	6	7	4	5	2
		0	1	1	3	0	1	2	7	4	5	6	3	2	1	0	7	6	5	4	2
		1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	2
		1	0	1	5	6	7	4	1	2	3	0	5	4	7	6	1	0	3	2	2
		1	1	0	6	7	4	5	2	3	0	1	6	7	4	5	2	3	0	1	2
		1	1	1	7	4	5	6	3	0	1	2	7	6	5	4	3	2	1	0	2
	WRITE	V	V	V	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	2,4

NOTE 1 In the case of setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In the case of setting burst length to on-the-fly in MR0, the internal WRITE operation starts at the same point in time as a BL8 (even if BC4 was selected during column time using A12/$\overline{BC4}$). This means that if the on-the-fly MR0 setting is used, the starting point for tWR and tWTR will not be pulled in by two clocks as described in the BC4 (fixed) case.

NOTE 2 Bit number(B0…B7) is the value of CA[2:0] that causes this bit to be the first READ during a burst.

NOTE 3 T = Output driver for data and strobes are in High-Z.

NOTE 4 V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins.

NOTE 5 X = "Don't Care."

CAS Latency (CL)

The CAS latency setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. DDR4 SDRAM does not support any half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL); **RL = AL + CL**.

Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a 1 places the DDR4 SDRAM into a DRAM manufacturer defined test mode that is to be used only by the DRAM manufacturer; and should not be used by the end user. No operations or functionality is specified if MR0[7] = 1.

Write Recovery/Read to Precharge

The programmed WR value MR0[11:9] is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto precharge) MIN in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer:

WRmin[cycles] = roundup (tWR[ns]/tCK[ns])

The WR must be programmed to be equal to or larger than tWR(MIN). When both DM and Write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array; tWR values will change when enabled. If there is a CRC error, the DRAM blocks the write operation and discards the data.

RTP (internal READ command to PRECHARGE command delay for auto precharge) min in clock cycles is calculated by dividing tRTP (in ns) by tCK (in ns) and rounding up to the next integer:

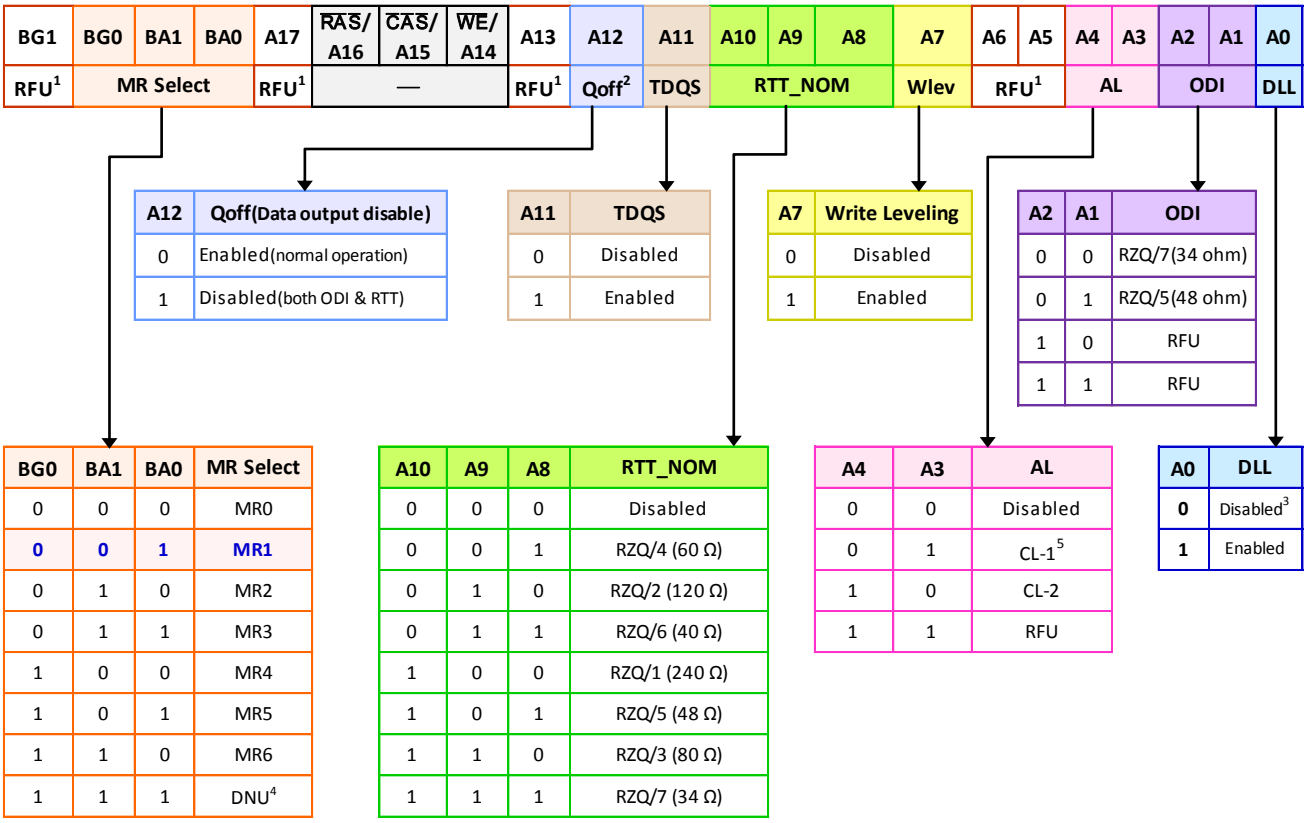
RTPmin[cycles] = roundup (tRTP[ns]/tCK[ns])

The RTP value in the mode register must be programmed to be equal or larger than RTPmin. The programmed RTP value is used with tRP to determine the act timing to the same bank.

DLL Reset

The DLL reset bit is self-clearing, meaning that it returns back to the value of 0 after the DLL reset function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (for example, READ commands or ODT synchronous operations).

Mode Register 1 (MR1)



BG1	BG0	BA1	BA0	A17	RAS/ A16	CAS/ A15	WE/ A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RFU[1]	MR Select			RFU[1]	—			RFU[1]	Qoff[2]	TDQS	RTT_NOM			Wlev	RFU[1]		AL		ODI		DLL

A12	Qoff(Data output disable)
0	Enabled(normal operation)
1	Disabled(both ODI & RTT)

A11	TDQS
0	Disabled
1	Enabled

A7	Write Leveling
0	Disabled
1	Enabled

A2	A1	ODI
0	0	RZQ/7(34 ohm)
0	1	RZQ/5(48 ohm)
1	0	RFU
1	1	RFU

BG0	BA1	BA0	MR Select
0	0	0	MR0
0	**0**	**1**	**MR1**
0	1	0	MR2
0	1	1	MR3
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU[4]

A10	A9	A8	RTT_NOM
0	0	0	Disabled
0	0	1	RZQ/4 (60 Ω)
0	1	0	RZQ/2 (120 Ω)
0	1	1	RZQ/6 (40 Ω)
1	0	0	RZQ/1 (240 Ω)
1	0	1	RZQ/5 (48 Ω)
1	1	0	RZQ/3 (80 Ω)
1	1	1	RZQ/7 (34 Ω)

A4	A3	AL
0	0	Disabled
0	1	CL-1[5]
1	0	CL-2
1	1	RFU

A0	DLL
0	Disabled[3]
1	Enabled

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS

NOTE 2 Outputs disabled - DQs, DQSs, $\overline{DQS}$s.

NOTE 3 States reversed to “0 as Disable” with respect to DDR4.

NOTE 4 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn’t respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 5 Not allowed when 1⁄4 rate geardown mode is enabled.

DLL Enable/DLL Disable

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation, (DLL-enabled) with MR1[0], the DLL is automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled upon exit of the SELF REFRESH operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a READ or SYNCHRONOUS ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON, or tAOF parameters.

During tDLLK, CKE must continuously be registered HIGH. DDR4 SDRAM does not require DLL for any WRITE operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL-off mode. The ODT resistors must be disabled by continuously registering the ODT pin LOW and/or by programming the RTT_NOM bits MR1[9,6,2] = 000 via a MODE REGISTER SET command during DLL-off mode.

The dynamic ODT feature is not supported in DLL-off mode; to disable dynamic ODT externally, use the MRS command to set RTT_WR, MR2[10:9] = 00.

Output Driver Impedance Control

The output driver impedance of the DDR4 SDRAM device is selected by MR1[2,1].

ODT RTT_NOM Values

DDR4 SDRAM is capable of providing three different termination values: RTT_Static, RTT_NOM, and RTT_WR. The nominal termination value, RTT_NOM, is programmed in MR1. A separate value (RTT_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during WRITEs. The RTT_WR value can be applied during WRITEs even when RTT_NOM is disabled. A third RTT value, RTT_Static, is programed in MR5. RTT_Static provides a termination value when the ODT signal is LOW.

Additive Latency (AL)

The additive latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR4 SDRAM. In this operation, the DDR4 SDRAM allows a READ or WRITE command (either with or without AUTO PRECHARGE) to be issued immediately after the ACTIVE command. The command is held for the time of AL before it is issued inside the device. The read latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. Write latency (WL) is controlled by the sum of the AL and CAS write latency (CWL) register settings.

Write Leveling

For better signal integrity, DDR4 memory modules use fly-by topology for the commands,addresses, control signals, and clocks. Fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain tDQSS, tDSS, and tDSH specifications. Therefore, the DDR4 SDRAM supports a write-leveling feature, which allows the controller to compensate for skew.

Output Disable

The DDR4 SDRAM outputs may be enabled/disabled by MR1[12]. When MR1[12] = 1 is enabled, all output pins (such as DQ, DQS, and $\overline{DQS}$) are disconnected from the device, which removes any loading of the output drivers. This feature may be useful when measuring module power, for example.For normal operation, set MR1[12] = 0.

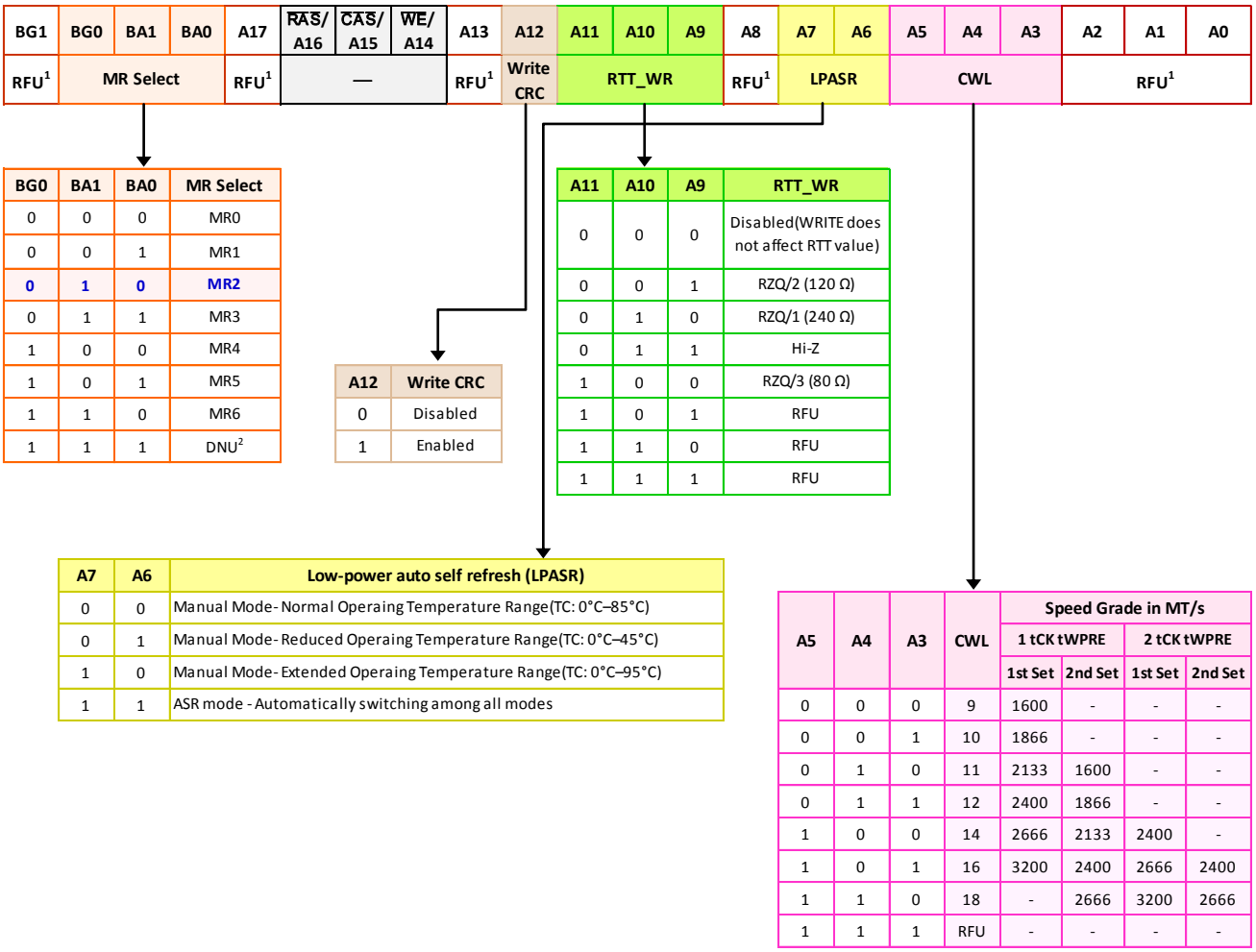
Termination Data Strobe (TDQS)

Termination data strobe (TDQS) is a feature of x8 DDR4 SDRAM and provides additional termination resistance outputs that may be useful in some system configurations. Because the TDQS function is available only in x8 DDR4 SDRAM, it must be disabled for x4 and x16 configurations. TDQS is not supported in x4 or x16 configurations. When enabled via the mode register, the same termination resistance function that is applied to the TDQS and $\overline{TDQS}$ pins is applied to the DQS and $\overline{DQS}$ pins.

The TDQS, DBI, and data mask functions share the same pin. When the TDQS function is enabled via the mode register, the data mask and DBI functions are not supported. When the TDQS function is disabled, the data mask and DBI functions can be enabled separately.

TDQS	Data Mask (DM)	WRITE DBI	READ DBI
Disabled	Enabled	Disabled	Enabled or disabled
	Disabled	Enabled	Enabled or disabled
	Disabled	Disabled	Enabled or disabled
Enabled	Disabled	Disabled	Disabled

Mode Register 2 (MR2)



BG1	BG0	BA1	BA0	A17	RAS/ A16	CAS/ A15	WE/ A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RFU[1]	MR Select			RFU[1]	—			RFU[1]	Write CRC	RTT_WR			RFU[1]	LPASR		CWL			RFU[1]		

BG0	BA1	BA0	MR Select
0	0	0	MR0
0	0	1	MR1
0	1	0	MR2
0	1	1	MR3
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU[2]

A12	Write CRC
0	Disabled
1	Enabled

A11	A10	A9	RTT_WR
0	0	0	Disabled(WRITE does not affect RTT value)
0	0	1	RZQ/2 (120 Ω)
0	1	0	RZQ/1 (240 Ω)
0	1	1	Hi-Z
1	0	0	RZQ/3 (80 Ω)
1	0	1	RFU
1	1	0	RFU
1	1	1	RFU

A7	A6	Low-power auto self refresh (LPASR)
0	0	Manual Mode- Normal Operaing Temperature Range(TC: 0°C–85°C)
0	1	Manual Mode- Reduced Operaing Temperature Range(TC: 0°C–45°C)
1	0	Manual Mode- Extended Operaing Temperature Range(TC: 0°C–95°C)
1	1	ASR mode - Automatically switching among all modes

A5	A4	A3	CWL	Speed Grade in MT/s			
				1 tCK tWPRE		2 tCK tWPRE	
				1st Set	2nd Set	1st Set	2nd Set
0	0	0	9	1600	-	-	-
0	0	1	10	1866	-	-	-
0	1	0	11	2133	1600	-	-
0	1	1	12	2400	1866	-	-
1	0	0	14	2666	2133	2400	-
1	0	1	16	3200	2400	2666	2400
1	1	0	18	-	2666	3200	2666
1	1	1	RFU	-	-	-	-

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS

NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

CAS Write Latency (CWL)

CAS write latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. DDR4 SDRAM does not support any half-clock latencies. The overall write latency (WL) is defined as additive latency (AL) + CAS write latency (CWL); **WL = AL + CWL**.

Low-Power Auto Self Refresh (LPASR)

Low-power auto self refresh (LPASR) is supported in DDR4 SDRAM. Applications requiring SELF REFRESH operation over different temperature ranges can use this feature to optimize the IDD6 current for a given temperature range as specified in the MR2 Register Definition table.

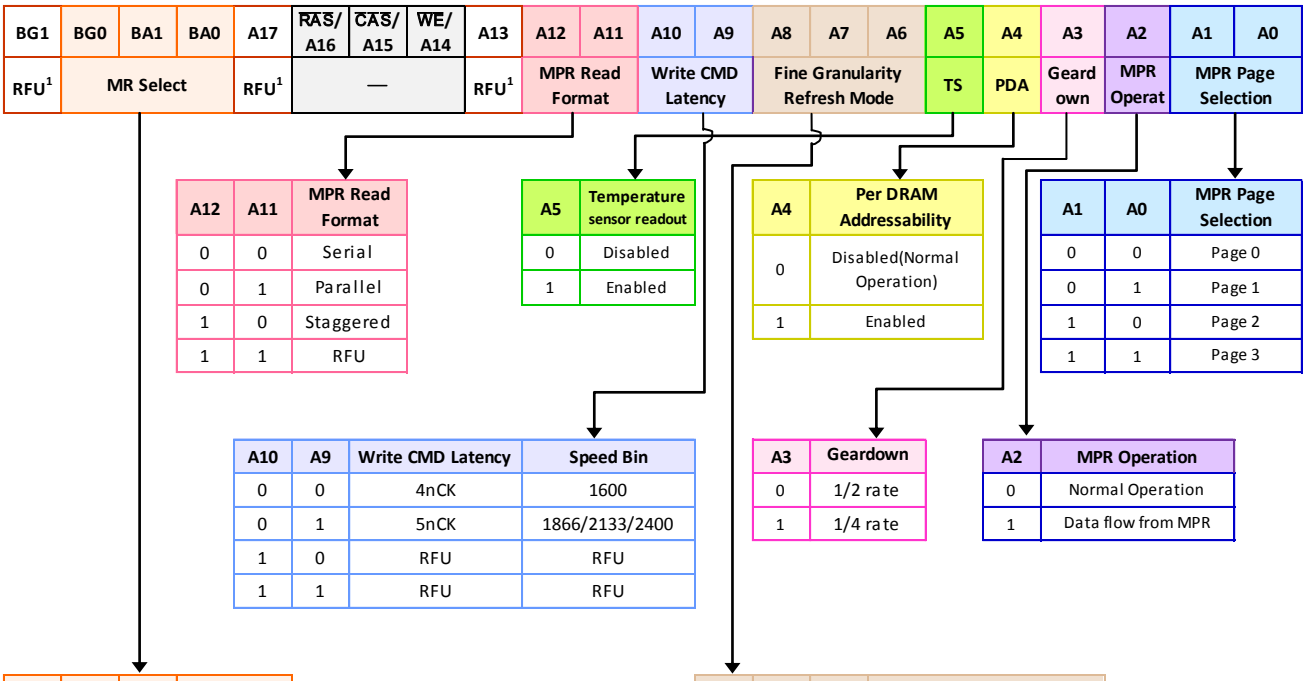
Dynamic ODT (RTT_WR)

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the DDR4 SDRAM without issuing an MRS command. Configure the Dynamic ODT settings in MR2[11:9]. In write-leveling mode, only RTT_NOM is available.

Write Cyclic Redundancy Check (CRC) Data Bus

The Write cyclic redundancy check (CRC) data bus feature during Writes has been added to DDR4 SDRAM. When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra 2UIs are used for the CRC information.

Mode Register 3 (MR3)



A12	A11	MPR Read Format
0	0	Serial
0	1	Parallel
1	0	Staggered
1	1	RFU

A5	Temperature sensor readout
0	Disabled
1	Enabled

A4	Per DRAM Addressability
0	Disabled(Normal Operation)
1	Enabled

A1	A0	MPR Page Selection
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

A10	A9	Write CMD Latency	Speed Bin
0	0	4nCK	1600
0	1	5nCK	1866/2133/2400
1	0	RFU	RFU
1	1	RFU	RFU

A3	Geardown
0	1/2 rate
1	1/4 rate

A2	MPR Operation
0	Normal Operation
1	Data flow from MPR

BG0	BA1	BA0	MR Select
0	0	0	MR0
0	0	1	MR1
0	1	0	MR2
0	**1**	**1**	**MR3**
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU[2]

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	RFU
1	0	0	RFU
1	0	1	On-the-fly 1x/2x
1	1	0	On-the-fly 1x/4x
1	1	1	RFU

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS

NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

WRITE CMD latency when CRC/DM enabled

The Write Command Latency (WCL) must be set when both Write CRC and DM are enabled for Write CRC persistent mode. This provides the extra time required when completing a Write burst when Write CRC and DM are enabled.

Fine Granularity Refresh Mode

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening tRFC and increasing cycle time allows more accesses to the chip and can produce higher bandwidth.

Temp Sensor Status

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; at the time of MPR Read of the Temperature Sensor Status bits, the temperature sensor status should be no older than 32ms.

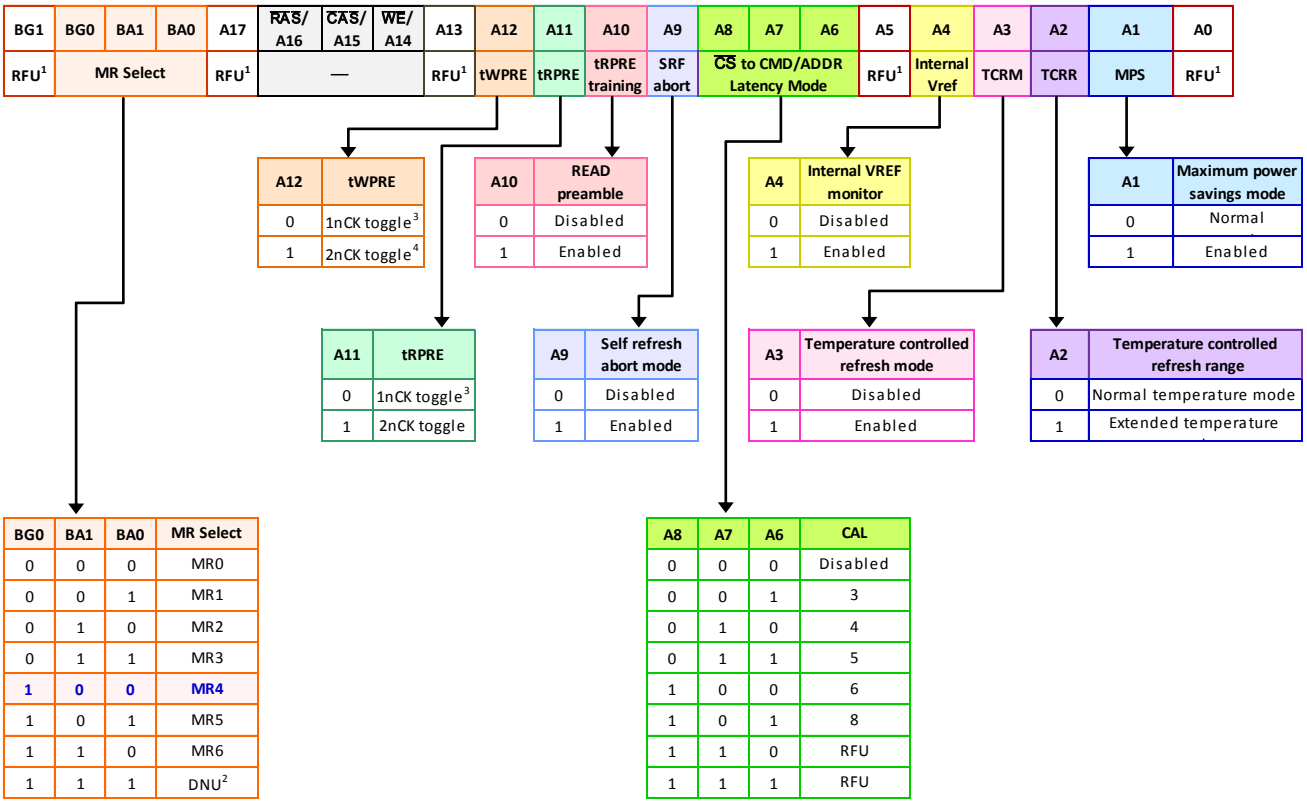
Per-DRAM Addressability

The MRS command mask allows programmability of a given device that may be in the same rank (devices sharing the same command and address signals). As an example, this feature can be used to program different ODT or VREF values on DRAM devices within a given rank.

Gear-down Mode

The DDR4 SDRAM defaults in half-rate (1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines $\overline{CS}$, CKE, and ODT when in quarter-rate (2N) mode. For operation in half-rate mode, no MRS command or sync pulse is required.

Mode Register 4 (MR4)



NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS

NOTE 2 Reserved for Register control word setting .DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 3 Not allowed when 1/4 rate Gear-down mode is enabled.

NOTE 4 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.

WRITE Preamble

DDR4 SDRAM introduces a programmable WRITE preamble tWPRE that can either be set to 1tCK or 2 tCK via the MR3 register. Note the 1tCK setting is similar to DDR3; however, the 2tCK setting is different. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. Check the table of CWL Selection for details.

READ Preamble

DDR4 SDRAM introduces a programmable READ preamble tRPRE that can be set to either 1tCK or 2tCK via the MR3 register. Note that both the 1tCK and 2tCK DDR4 preamble settings are different from what DDR3 SDRAM defined. Both of these READ preamble settings may require the memory controller to train (or READ-level) its data strobe receivers using the READ preamble training.

READ Preamble Training

DDR4 supports programmable READ preamble settings (1tCK or 2tCK). This mode can be used by the memory controller to train or READ level its data strobe receivers.

Temperature-Controlled Refresh (MR4[3] = 1 & MR2[6:7]=11)

When temperature-controlled refresh mode is enabled, the DDR4 SDRAM may adjust the internal refresh period to be longer than tREFI of the normal temperature range by skipping external refresh commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45°C. Normal temperature mode covers the range of 0°C to 85°C, while the extended temperature range covers 0°C to 95°C.

Command Address Latency (CAL)

DDR4 supports the command address latency (CAL) function as a power savings feature. This feature can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles (tCAL) between a $\overline{CS}$ registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register and is based on the roundup (in clocks) of [tCK(ns)/tCAL(ns)].

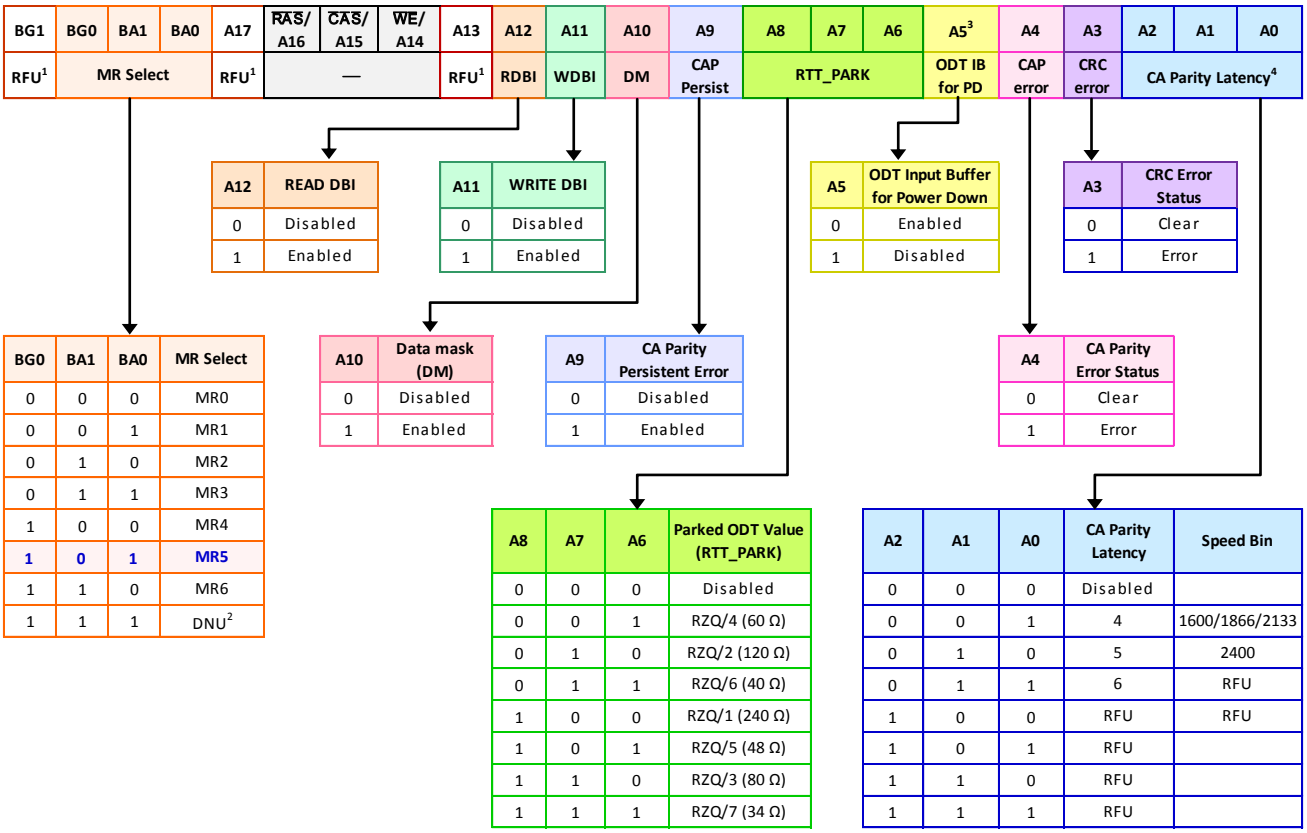
Internal Vref Monitor

DDR4 generates its own internal VrefDQ. This mode is allowed to be enabled during VrefDQ training and when enabled, Vref_time-short and Vref_time-long need to be increased by 10ns if DQ0, or DQ1, or DQ2, or DQ3 have 0pF loading; and add an additional 15ns per pF of added loading.

Maximum Power Savings Mode

This mode provides the lowest power mode where data retention is not required. When DDR4 SDRAM is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except maximum power saving mode exit command and during the assertion of $\overline{\text{RESET}}$ signal LOW).

Mode Register 5 (MR5)



NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS

NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 3 When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

NOTE 4 Parity latency must be programmed according to timing parameters by speed grade table.

Data Bus Inversion (DBI)

The data bus inversion (DBI) function has been added to DDR4 SDRAM and is supported for x8 and x16 configurations only (x4 is not supported). The DBI function shares a common pin with the DM and TDQS functions. The DBI function applies to both READ and WRITE operations and cannot be enabled at the same time the DM function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

Data Mask (DM)

The data mask (DM) function, also described as a partial write, has been added to DDR4 SDRAM and is supported for x8 and x16 configurations only (x4 is not supported). The DM function shares a common pin with the DBI and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the DBI function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

CA Parity Persistent Error Mode

Normal CA Parity Mode (CA Parity Persistent Mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA Parity Persistent Mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

ODT Input Buffer for Power Down

Determines whether the ODT input buffer is on or off during Power Down. If the ODT input buffer is configured to be on (enabled during power down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power down), the ODT input signal may be floating and the DRAM does not provide RTT_NOM termination. The DRAM may, however, provide Rtt_Park termination depending on the MR settings. This is primarily for additional power savings.

CA Parity Error Status

DRAM will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the DRAM Controller clears it explicitly using an MRS command.

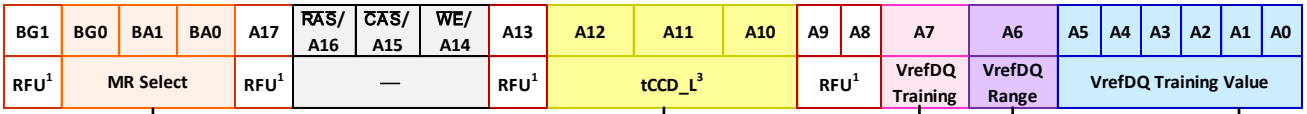
CRC Error Status

DRAM will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the DRAM controller clears it explicitly using an MRS command.

C/A Parity Latency Mode

CA Parity is enabled when a latency value, dependent on tCK, is programmed; this accounts for parity calculation delay internal to the DRAM. The normal state of CA Parity is to be disabled. If CA parity is enabled, the DRAM has to ensure that there are no parity errors before executing the command. CA Parity signal (PAR) covers $\overline{ACT}$, $\overline{RAS}$/A16 , $\overline{CAS}$/A15, $\overline{WE}$/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT and $\overline{CS}$ are not included in the parity calculation.

Mode Register 6 (MR6)



BG0	BA1	BA0	MR Select
0	0	0	MR0
0	0	1	MR1
0	1	0	MR2
0	1	1	MR3
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU[2]

A12	A11	A10	tCCD_L.min(nCK)	Remark [4]
0	0	0	4	≦2400Mbps
0	0	1	5	TBD
0	1	0	6	TBD
0	1	1	7	TBD
1	0	0	8	TBD
1	0	1	RFU	
1	1	0	RFU	
1	1	1	RFU	

A7	VrefDQ Training Enable
0	Disabled
1	Enabled

A6	VrefDQ Range
0	Range 1
1	Range 2

MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)	MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)	MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)	MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)
00 0000	60.00%	45.00%	00 1101	68.45%	53.45%	01 1010	76.90%	61.90%	10 0111	85.35%	70.35%
00 0001	60.65%	45.65%	00 1110	69.10%	54.10%	01 1011	77.55%	62.55%	10 1000	86.00%	71.00%
00 0010	61.30%	46.30%	00 1111	69.75%	54.75%	01 1100	78.20%	63.20%	10 1001	86.65%	71.65%
00 0011	61.95%	46.95%	01 0000	70.40%	55.40%	01 1101	78.85%	63.85%	10 1010	87.30%	72.30%
00 0100	62.60%	47.60%	01 0001	71.05%	56.05%	01 1110	79.50%	64.50%	10 1011	87.95%	72.95%
00 0101	63.25%	48.25%	01 0010	71.70%	56.70%	01 1111	80.15%	65.15%	10 1100	88.60%	73.60%
00 0110	63.90%	48.90%	01 0011	72.35%	57.35%	10 0000	80.80%	65.80%	10 1101	89.25%	74.25%
00 0111	64.55%	49.55%	01 0100	73.00%	58.00%	10 0001	81.45%	66.45%	10 1110	89.90%	74.90%
00 1000	65.20%	50.20%	01 0101	73.65%	58.65%	10 0010	82.10%	67.10%	10 1111	90.55%	75.55%
00 1001	65.85%	50.85%	01 0110	74.30%	59.30%	10 0011	82.75%	67.75%	11 0000	91.20%	76.20%
00 1010	66.50%	51.50%	01 0111	74.95%	59.95%	10 0100	83.40%	68.40%	11 0001	91.85%	76.85%
00 1011	67.15%	52.15%	01 1000	75.60%	60.60%	10 0101	84.05%	69.05%	11 0010	92.50%	77.50%
00 1100	67.80%	52.80%	01 1001	76.25%	61.25%	10 0110	84.70%	69.70%	11 0011 to 111111	Reserved	Reserved

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS

NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 3 tCCD_L should be programmed according to the value defined in AC parameter table per operating frequency.

NOTE 4 It's not finalized. Might be changed.

tCCD_L Programming

The DRAM Controller must program the correct tCCD_L value. tCCD_L will be programmed according to the value defined in the AC parameter table per operating frequency.

VREFDQ Training Enable

VREFDQ Training is where the DRAM internally generates it's own VREFDQ used by the DQ input receivers. The DRAM controller must use a MRS protocol (adjust up, adjust down, etc.) for setting and calibrating the internal VREFDQ level. The procedure is a series of Writes and Reads in conduction with VREFDQ adjustments to optimize and verify the data eye. Enabling VREFDQ Training should be used whenever MR6[6:0] register values are being written to.

VREFDQ Training Range

DDR4 defines two VREFDQ training ranges - Range 1 and Range 2. Range 1 supports VREFDQ between 60% and 92% of VDDQ while Range 2 supports VREFDQ between 45% and 77% of VDDQ. Range 1 is targeted for module based designs and Range 2 is added targeting point-to point designs.

VREFDQ Training Value

Fifty settings provided 0.65% of granularity steps sizes for both Range 1 and Range 2 of VREFDQ.

Mode Register 7 (MR7)

DRAM MR7 Ignore

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM.Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

BG1	BG0	BA1	BA0	A17	RAS/ A16	CAS/ A15	WE/ A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RFU[1]	MR Select			RFU[1]	—			RFU[1]													

BG0	BA1	BA0	MR Select
0	0	0	MR0
0	0	1	MR1
0	1	0	MR2
0	1	1	MR3
1	0	0	MR4
1	0	1	MR5
1	1	0	MR6
1	1	1	DNU[2]

NOTE 1 Please refer to addressing table. If the address is available, it must be programmed to 0 during MRS

NOTE 2 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Truth Table

Command Truth Table

Note 1,2,3 and 4 apply to the entire Command truth table.

Note 5 applies to all Read/Write commands.

[BG = Bank group address;BA = Bank address; RA =Row address; CA = Column address; $\overline{BC}$ = Burst chop; X = Don't Care; V = H or L]

Symbol	Function		CKE		$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG [1:0]	BA [1:0]	C [2:0]	A12 /$\overline{BC}$	A [13,11]	A10 /AP	A [9:0]	Notes
			Prev.	Pres.													
MRS	MODE REGISTER SET		H	H	L	H	L	L	L	BG	BA	V	OP code				12
REF	REFRESH		H	H	L	H	L	L	H	V	V	V	V	V	V	V	
SRE	Self refresh entry		H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
SRX	Self refresh exit		L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9,10
					L	H	H	H	H	V	V	V	V	V	V	V	
PRE	Single-bank PRECHARGE		H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
PREA	PRECHARGE all banks		H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	Reserved for future use		H	H	L	H	L	H	H	RFU							
ACT	Bank ACTIVATE		H	H	L	L	Row Address(RA)			BG	BA	V	Row Address(RA)				
WR	WRITE	Fixed BL8 or BC4	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
WRS4		BC4OTF	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
WRS8		BL8OTF	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
WRA	WRITE with auto precharge	Fixed BL8 or BC4	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
WRAS4		BC4OTF	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
WRAS8		BL8OTF	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
RD	READ	Fixed BL8 or BC4	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
RDS4		BC4OTF	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
RDS8		BL8OTF	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
RDA	READ with auto precharge	Fixed BL8 or BC4	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
RDAS4		BC4OTF	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
RDAS8		BL8OTF	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
NOP	NO OPERATION		H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
DES	Device DESELECTED		H	H	H	X	X	X	X	X	X	X	X	X	X	X	
PDE	Power-down entry		H	L	L	H	H	H	H	V	V	V	V	V	V	V	6
					H	X	X	X	X	X	X	X	X	X	X	X	6
PDX	Power-down exit		L	H	L	H	H	H	H	V	V	V	V	V	V	V	
					H	X	X	X	X	X	X	X	X	X	X	X	
ZQCL	ZQ CALIBRATION LONG		H	H	L	H	H	H	L	X	X	X	X	X	H	X	
ZQCS	ZQ CALIBRATION SHORT		H	H	L	H	H	H	L	X	X	X	X	X	L	X	

NOTE 1 All DDR4 SDRAM commands are defined by states of $\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and conuration dependant. When $\overline{ACT}$ = H; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as command pins $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ respectively. When $\overline{ACT}$= L; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as address pins A16, A15, and A14 respectively.

NOTE 2 $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

NOTE 3 Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.

NOTE 4 "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".

NOTE 5 Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

NOTE 6 The Power Down Mode does not perform any refresh operation.

NOTE 7 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

NOTE 8 Controller guarantees self refresh exit to be synchronous.

NOTE 9 VPP and VREF(VrefCA) must be maintained during Self Refresh operation.

NOTE 10 The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit

NOTE 11 Refer to the CKE Truth Table for more detail with CKE transition.

CKE Truth Table

Current State[2]	CKE		Command (N)[3]	Action(N)[3]	Notes
	Previous Cycle[1] (N-1)	Present Cycle[1] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power Down	L	L	X	Maintain power down	14, 15
	L	H	DESELECT	Power down exit	11, 14
Self Refresh	L	L	X	Maintain self refresh	15, 16
	L	H	DESELECT	Self refresh exit	8, 12, 16
Bank(s) Active	H	L	DESELECT	Active power down entry	11, 13, 14
Reading	H	L	DESELECT	Power down entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power down entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power down entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge power down entry	11
All banks idle	H	L	DESELECT	Precharge power down entry	11,13, 14, 18
	H	L	REFRESH	Self refresh	9, 13, 18
For more details with all signals See “Command Truth Table”.					10

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.

NOTE 2 Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N),ODT is not included here.

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

NOTE 6 During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

NOTE 7 DESELECT and NOP are defined in the Command Truth Table.

NOTE 8 On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

NOTE 9 Self-Refresh mode can only be entered from the All Banks Idle state.

NOTE 10 Must be a legal command as defined in the Command Truth Table.

NOTE 11 Valid commands for Power-Down Entry and Exit are DESELECT only.

NOTE 12 Valid commands for Self-Refresh Exit are DESELECT only except for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.

NOTE 13 Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions, see “Self-Refresh Operation” and “Power-Down Modes”.

NOTE 14 The Power-Down does not perform any refresh operations.

NOTE 15 “X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

NOTE 16 VPP and VREF(VrefCA) must be maintained during Self-Refresh operation.

NOTE 17 If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

NOTE 18 ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP,etc).

NOTE 19 Self refresh mode can be entered only from the all banks idle state.

NOTE 20 For more details about all signals, see the Command truth table; must be a legal command as defined in the table.

NOP Command

The NO OPERATION (NOP) command was originally used to instruct the selected DDR4 SDRAM to perform a NOP ($\overline{CS}$ = LOW and $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 = HIGH). This prevented unwanted commands from being registered during idle or wait states. The NOP command general support has been removed and should not be used unless specifically allowed; which is when exiting Max Power Saving Mode or when entering Gear-down Mode.

DESELECT Command

The DESELECT function ($\overline{CS}$ HIGH) prevents new commands from being executed by the DDR4 SDRAM. The DDR4 SDRAM is effectively deselected. Operations already in progress are not affected.

DLL On/Off

DLL-Off Mode

DLL-off mode is entered by setting MR1 bit A0 to 0, which will disable the DLL for subsequent operations until the A0 bit is set back to 1. The MR1 A0 bit for DLL control can be switched either during initialization or during self refresh mode. Refer to Input Clock Frequency Change for more details.

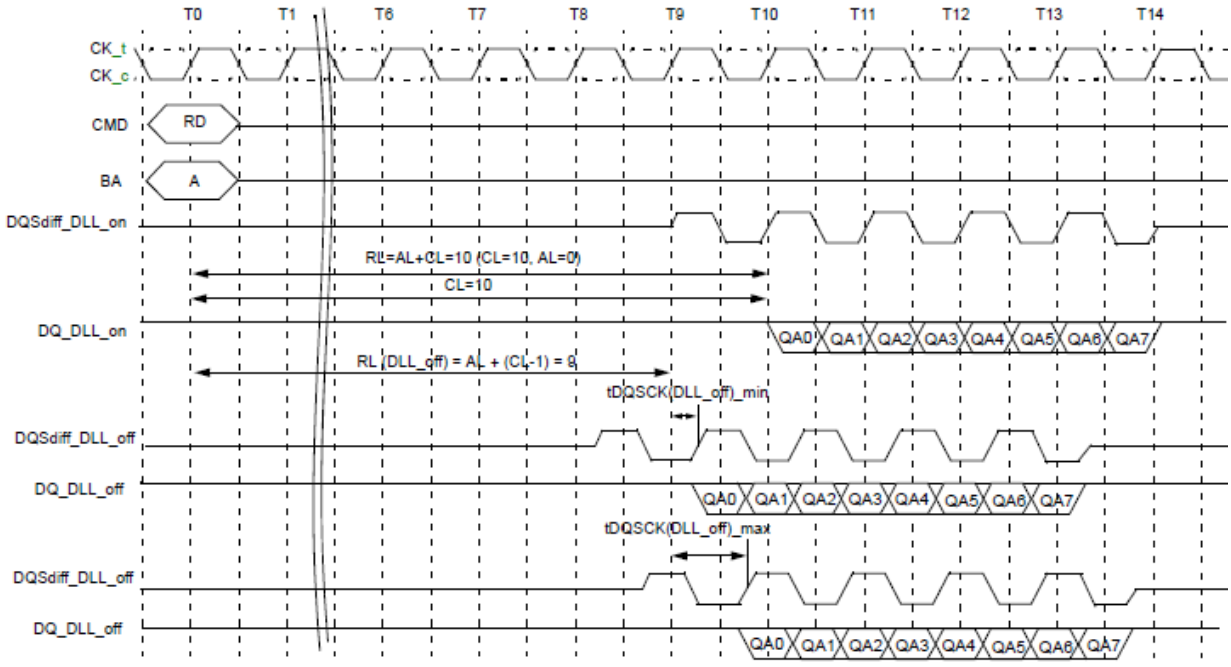
The maximum clock frequency for DLL-off mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one CL value in MR0 and CWL in MR2 is supported. The DLL-off mode is only required to support setting both CL = 10 and CWL = 9.

DLL-off mode will affect the read data clock-to-data strobe relationship (tDQSCK), but not the data strobe-to-data relationship (tDQSQ, tQH). Special attention is needed to line up read data to the controller time domain.

Compared with DLL-on mode, where tDQSCK starts from the rising clock edge (AL + CL) cycles after the READ command, the DLL-off mode tDQSCK starts (AL + CL - 1) cycles after the READ command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK), and the difference between tDQSCK MIN and tDQSCK MAX is significantly larger than in DLL-on mode. The tDQSCK (DLL_off) values are vendor-specific.

DLL-Off Mode Read Timing Operation

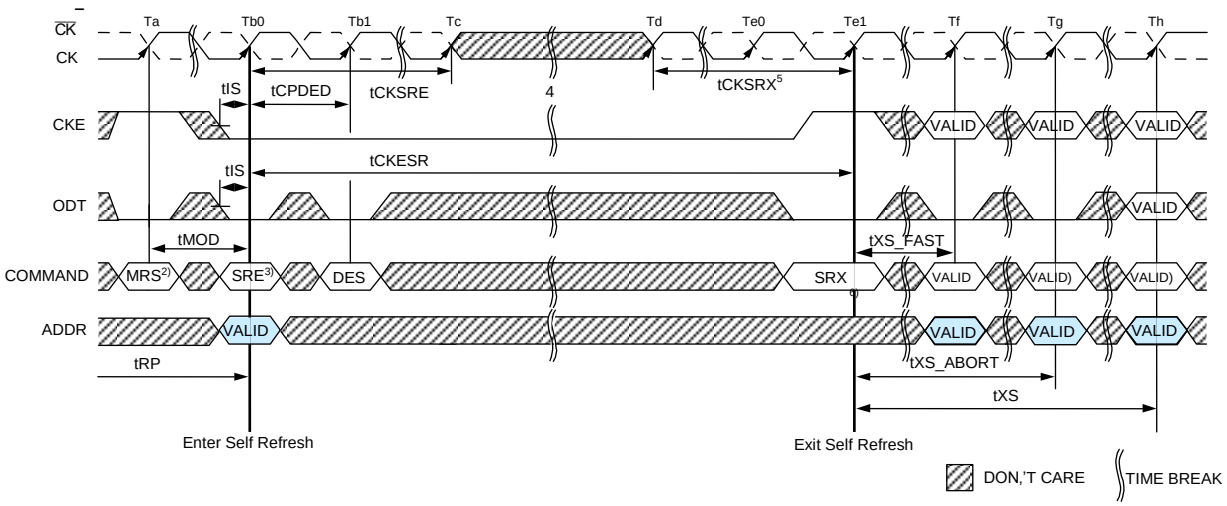


DLL On/Off Switching Procedure

DDR4 DLL-off mode is entered by setting MR1 bit A0 to 1; this will disable the DLL for subsequent operations until the A0 bit is set back to 0. To switch from DLL on to DLL off requires the frequency to be changed during self refresh, as outlined in the following procedure:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and DRAM on-die termination resistors, RTT_NOM, must be in the high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 bit A0 to 1 to disable the DLL.
3. Wait tMOD.
4. Enter self refresh mode; wait until (tCKSRE) is satisfied.
5. Change frequency, following the guidelines in the Input Clock Frequency Change section.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the SELF REFRESH EXIT command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If RTT_NOM was disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
8. Wait tXS_FAST, tXS_ABORT, or tXS, and then set mode registers with appropriate values (an update of CL, CWL, and WR may be necessary; aZQCL command can also be issued after tXS_FAST).
   - tXS: ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, RDAS8
   - tXS_FAST: ZQCL, ZQCS, MRS commands. For MRS commands, only CL and WR/RTP registers in MR0, the CWL register in MR2, and geardown mode in MR3 are allowed to be accessed provided the device is not in per-device addressability mode. Access to other device mode registers must satisfy tXS timing.
   - tXS_ABORT: If the bit is enabled, then the device aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of tXS_ABORT. Upon exiting from self refresh, the DDR4 SDRAM requires a minimum of one extra REFRESH command before it is put back into self refresh mode. This requirement remains the same regardless of the setting of the MRS bit for self refresh abort.
9. Wait for tMOD, and then the DRAM is ready for the next command.

DLL Switch Sequence from DLL On to DLL Off



NOTE 1 Starting in the idle state. RTT in stable state.

NOTE 2 Disable DLL by setting MR1 bit A0 to 0.

NOTE 3 Enter SR.

NOTE 4 Change frequency.

NOTE 5 Clock must be stable tCKSRX.

NOTE 6 Exit SR.

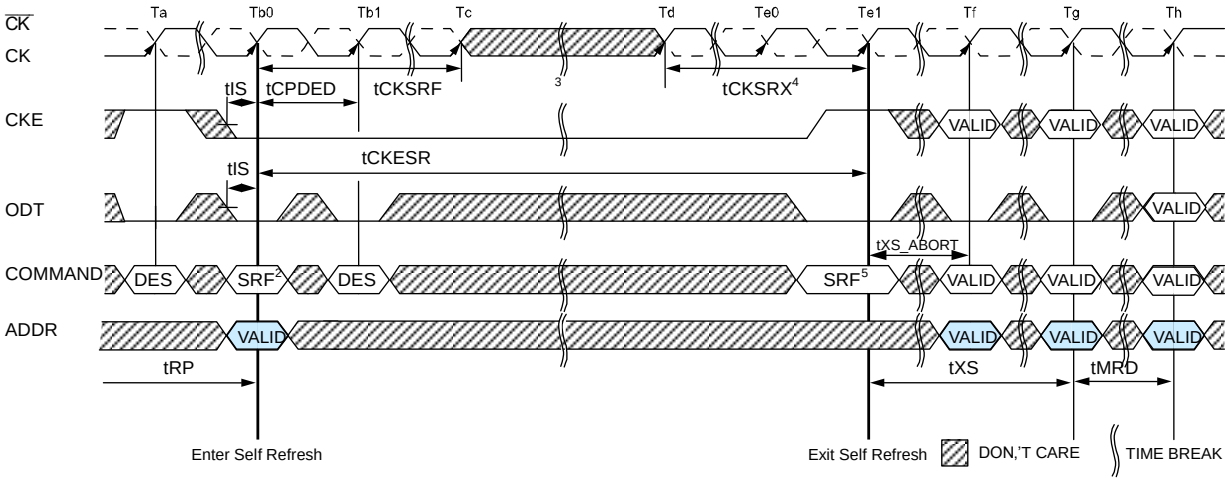
NOTE 7 Update mode registers allowed with DLL_off settings met.

DLL Off to DLL On Procedure

To switch from DLL off to DLL on (with required frequency change) during self refresh:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and DRAM on-die termination resistors (RTT) must be in the high impedance state before self refresh mode is entered.)
2. Enter self refresh mode; wait until tCKSRE satisfied.
3. Change frequency, following the guidelines in the Input Clock Frequency Change section.
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the SELF REFRESH EXIT command, CKE must continuously be registered HIGH until tDLLK timing from the subsequent DLL RESET command is satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW or HIGH until tDLLK timings from the subsequent DLL RESET command is satisfied. If RTT_NOM disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
6. Wait tXS or tXS_ABORT, depending on bit x in RMy, then set MR1 bit A0 to 0 to enable the DLL.
7. Wait tMRD, then set MR1 bit A8 to 1 to start DLL Reset.
8. Wait tMRD, then set mode registers with appropriate values (an update of CL, CWL, and WR may be necessary. After tMOD is satisfied from any proceeding MRS command, a ZQCL command can also be issued during or after tDLLK.)
9. Wait for tMOD, then DRAM is ready for the next command. (Remember to wait tDLLK after DLL RESET before applying any command requiring a locked DLL.) In addition, wait for tZQoper in case a ZQCL command was issued.

DLL Switch Sequence from DLL Off to DLL On



NOTE 1 Starting in the idle state.
NOTE 2 Enter SR.
NOTE 3 Change frequency.
NOTE 4 Clock must be stable tCKSRX.
NOTE 5 Exit SR.
NOTE 6 Set DLL to on by setting MR1 ro A0 = 0.
NOTE 7 Update mode registers.
NOTE 8 Issue any valid command.

Input Clock Frequency Change

After the DDR4 SDRAM is initialized, the DDR4 SDRAM requires the clock to be stable during almost all states of normal operation. This means that after the clock frequency has been set and is to be in the stable state, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate only when in self refresh mode. Outside of self refresh mode, it is illegal to change the clock frequency.

After the DDR4 SDRAM has been successfully placed in self refresh mode and tCKSRE has been satisfied, the state of the clock becomes a "Don't Care." Following a "Don't Care," changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met as outlined in Self-Refresh Operation.

Because DDR4 DLL lock time ranges from 597nCK at 1333MT/s to 1024nCK at 3200MT/s, additional MRS commands may need to be issued for the new clock frequency. If DLL is enabled, tDLLK must be programmed according to the value defined in AC parameter tables, and the DLL must be RESET by an explicit MRS command (MR0[8]=1) when the input clock frequency is different before and after self refresh.

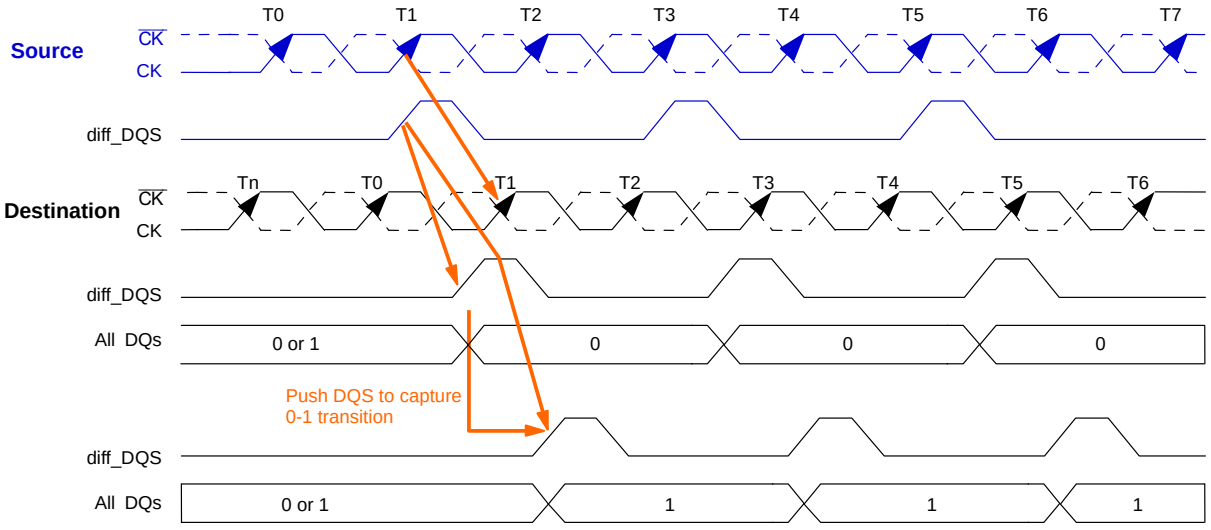
The DDR4 SDRAM input clock frequency can change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on mode to DLL_off mode transition sequence (see DLL On/Off Switching Procedure).

Write Leveling

For better signal integrity, the DDR4 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR4 SDRAM supports a write-leveling feature to allow the controller to compensate for skew. This feature may not be required under some system conditions, provided the host can maintain the tDQSS, tDSS, and tDSH specifications.

The memory controller can use the write leveling feature and feedback from the DDR4 SDRAM to adjust the DQS - $\overline{DQS}$ to CK - $\overline{CK}$ relationship. The memory controller involved in the leveling must have an adjustable delay setting on DQS - $\overline{DQS}$ to align the rising edge of DQS - $\overline{DQS}$ with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - $\overline{CK}$, sampled with the rising edge of DQS - $\overline{DQS}$, through the DQ bus. The controller repeatedly delays DQS - $\overline{DQS}$ until a transition from 0 to 1 is detected. The DQS - $\overline{DQS}$ delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - $\overline{DQS}$ signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the AC Timing Parameters section in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown below.

Write-Leveling Concept



DQS - $\overline{DQS}$ driven by the controller during leveling mode must be terminated by the DRAM based on the ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits carry the leveling feedback to the controller across the DRAM configurations x4, x8, and x16. On a x16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS)-to-clock relationship; the lower data bits would indicate the lower diff_DQS(diff_LDQS)-to-clock relationship.

The Figure below is another representative way to view the write leveling procedure. Although it shows the clock varying to a static strobe, this is for illustrative purpose only; the clock does not actually change phase, the strobe is what is actually varied. By issuing multiple WL bursts, the DQS strobe can be varied to capture when the clock edge arrives at the DRAM clock input buffer fairly accurately.

DRAM Setting for Write Leveling and DRAM Termination Function in that Mode

DRAM enters into write leveling mode if A7 in MR1 is HIGH, and after finishing leveling, DRAM exits write leveling mode if A7 in MR1 is LOW (see the MR leveling table below). Note that in write leveling mode, only DQS/$\overline{\text{DQS}}$ terminations are activated and deactivated via the ODT pin, unlike normal operation (see DRAM termination table below).

MR Settings for Leveling Procedures

Function	MR1	Enable	Disable
Write Leveling enable	A7	1	0
Qoff (Data output disable)	A12	0	1

DRAM Termination Function in Leveling Mode

ODT Pin at DRAM	DQS/$\overline{\text{DQS}}$ Termination	DQ Termination
RTT_NOM with ODT HIGH	On	Off
RTT_PARK with ODT LOW	On	Off

NOTE 1 In write-leveling mode with its output buffer disabled (MR1[bit7] = 1 with MR1[bit12] =1) all RTT_NOM and RTT_PARK settings are supported; in write-leveling mode with its output buffer enabled (MR1[bit7] = 1 with MR1[bit12] = 0) RTT_NOM and RTT_PARK settings are supported while RTT_WR i s not allowed.

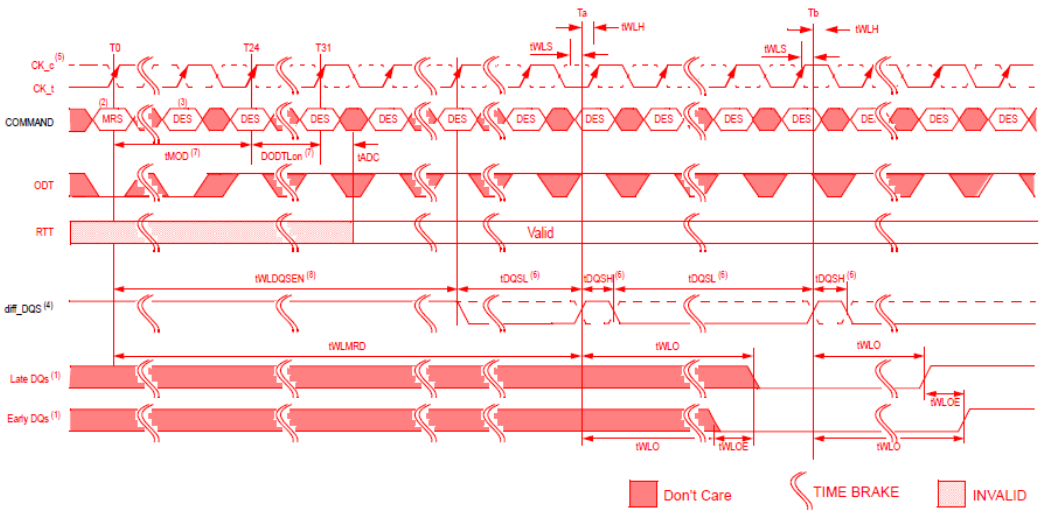
Procedure Description

The memory controller initiates the leveling mode of all DRAM by setting bit 7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only the DESELECT command is supported, as well as an MRS command to change the Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7] = 0) may also change MR1 bits of TBD. Because the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The controller may drive DQS LOW and $\overline{DQS}$ HIGH after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS, $\overline{DQS}$ edge which is used by the DRAM to sample CK - $\overline{CK}$ driven from the controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK - $\overline{CK}$ status with the rising edge of DQS - $\overline{DQS}$ and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS, $\overline{DQS}$) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS - $\overline{DQS}$ delay setting and launches the next DQS - $\overline{DQS}$ pulse after some time, which is controller dependent. After a 0-to-1 transition is detected, the controller locks the DQS - $\overline{DQS}$ delay setting, and write leveling is achieved for the device. The following figure shows the timing diagram and parameters for the overall write leveling procedure.

Write-Leveling Sequence



NOTE 1 DDR4 SDRAM drives leveling feedback on all DQs

NOTE 2 MRS : Load MR1 to enter write leveling mode

NOTE 3 DES : Deselect

NOTE 4 diff_DQS is the differential data strobe (DQS-$\overline{DQS}$). Timing reference points are the zero crossings. DQS is shown with solid line, $\overline{DQS}$ is shown with dotted line

NOTE 5 CK/$\overline{CK}$: CK is shown with solid dark line, where as $\overline{CK}$ is drawn with dotted line.

NOTE 6 DQS , $\overline{DQS}$ needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent

NOTE 7 tMOD(Min) = max(24nCK, 15ns), WL = 9 (CWL = 9, AL = 0, PL = 0), DODTLon = WL -2 = 7

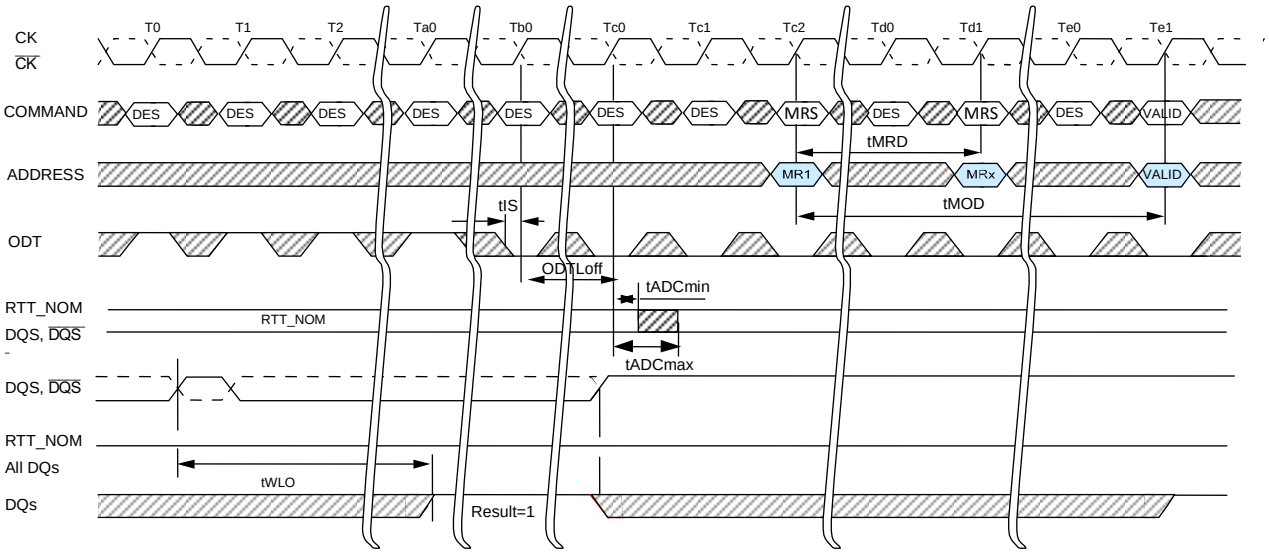
NOTE 8 tWLDQSEN must be satisfied following equation when using ODT. - tWLDQSEN > tMOD(Min) + ODTLon + tADC : at DLL = Enable - tWLDQSEN > tMOD(Min) + tAONAS : at DLL = Disable

Write-Leveling Mode Exit

Write leveling mode should be exited as follows:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note that from this point now on, DQ pins are in undefined driving mode and will remain undefined, until tMOD after the respective MR command (Te1).
2. Drive ODT pin LOW (tIS must be satisfied) and continue registering LOW (see Tb0).
3. After the RTT is switched off, disable write-leveling mode via the MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command can be registered. (MR commands can be issued after tMRD [Td1]).

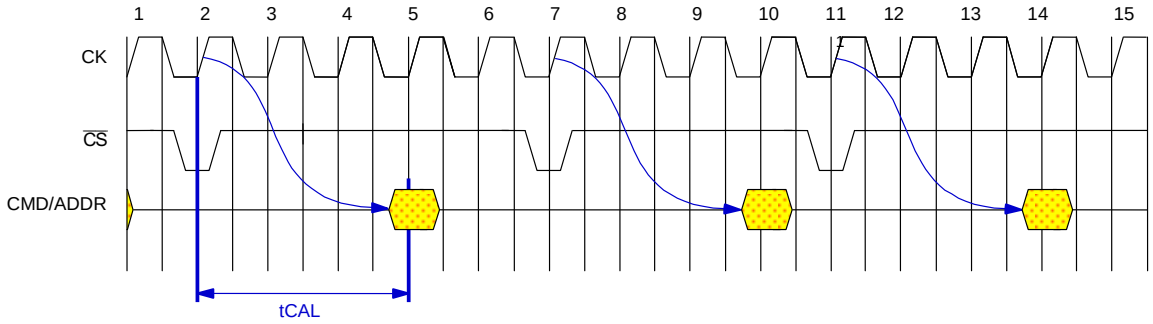
Write-Leveling Exit



$\overline{CS}$ to Command Address Latency (CAL)

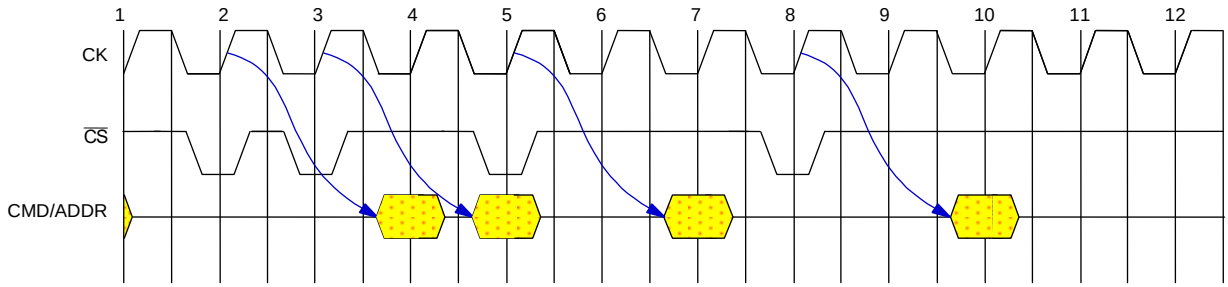
DDR4 supports the Command Address Latency (CAL) function as a power savings feature. This feature can be enabled or disabled via the MRS setting. CAL timing is defined as the delay in clock cycles (tCAL) between a $\overline{CS}$ registered LOW and its corresponding registered command and address. The value of CAL in clocks must be programmed into the mode register (see MR1 Register Definition table) and is based on the equation tCK(ns) / tCAL(ns), rounded up in clocks.

CAL Timing Definition



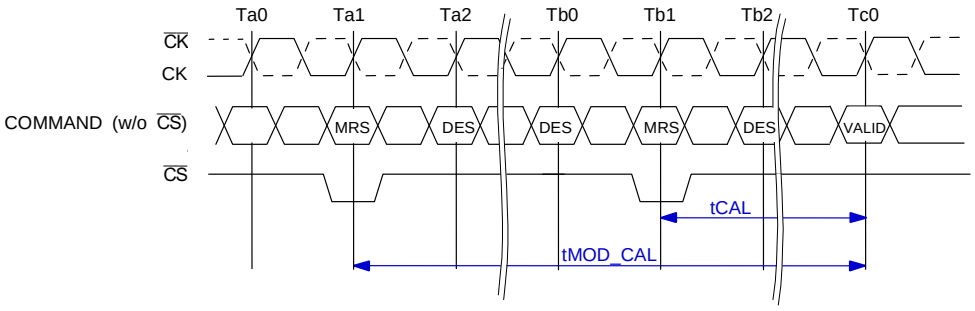
$\overline{CS}$ used to wake up the receivers. CAL gives the DRAM time to enable the command and address receivers before a command is issued. After the command and the address are latched, the receivers can be disabled if $\overline{CS}$ returns to HIGH. For consecutive commands, the DRAM will keep the command and address input receivers enabled for the duration of the command sequence.

CAL Timing Example (Consecutive $\overline{CS}$ = LOW)



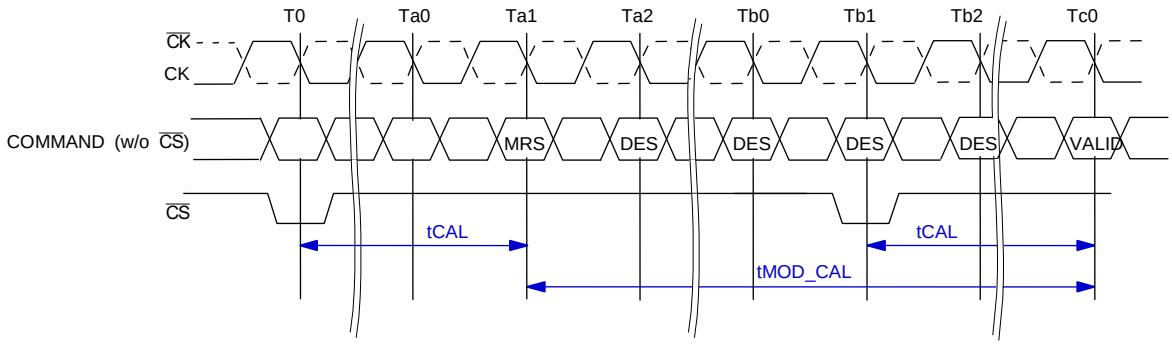
When the Command Address Latency mode, CAL, is enabled; additional time is required for the MRS command to complete. The earliest the next valid command can be issued is tMOD_CAL which should be equal to tMOD+tCAL. The two following figures are examples.

CAL Enable Timing - tMOD_CAL



NOTE 1 Command Address Latency mode is enabled at T1.

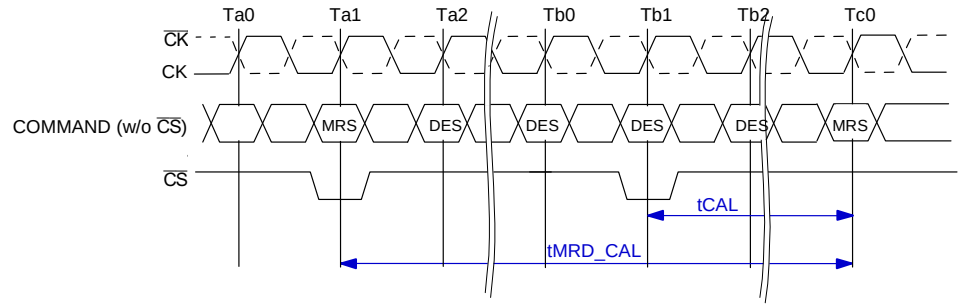
tMOD_CAL, MRS to Valid Command Timing with CAL Enabled



NOTE 1 MRS at Ta1 may or may not modify CAL, tMOD_CAL is computed based on new tCAL setting if modified.

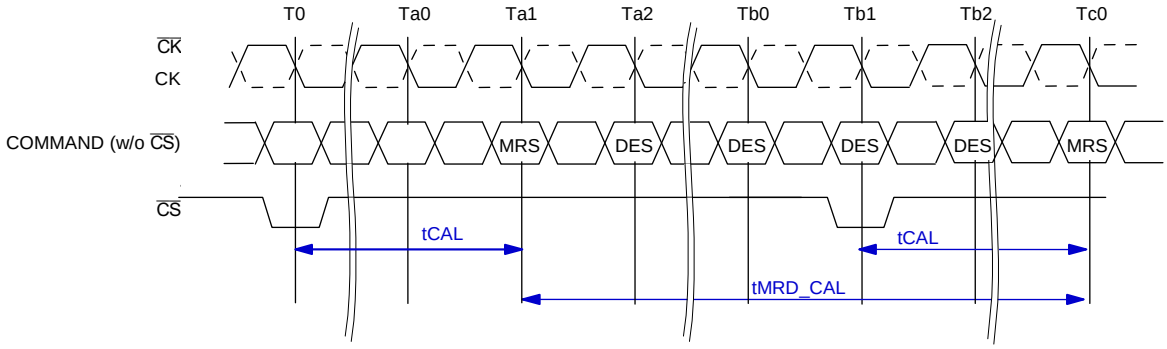
When the Command Address Latency mode is enabled or being enabled, the earliest the next MRS command can be issued is tMRD_CAL is equal to tMOD+tCAL. The two following figures are examples.

CAL Enabling MRS to Next MRS Command, tMRD_CAL



NOTE 1 Command Address Latency mode is enabled at T1.

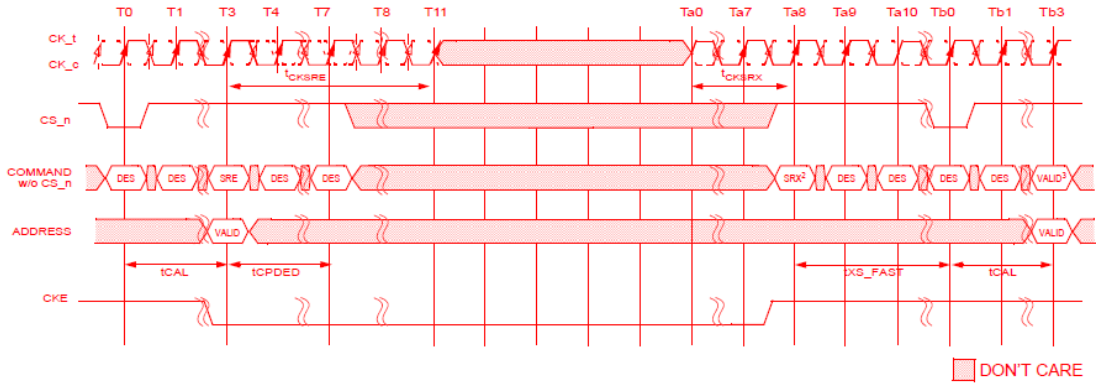
tMRD_CAL, Mode Register Cycle Time With CAL Enabled



NOTE 1 MRS at Ta1 may or may not modify CAL, tMRD_CAL is computed based on new tCAL setting if modified.

Command Address Latency Examples: Consecutive READ BL8 with two different CALs and 1tCK Preamble in Different Bank Group shown in figures below.

Self Refresh Entry, Exit Timing with CAL

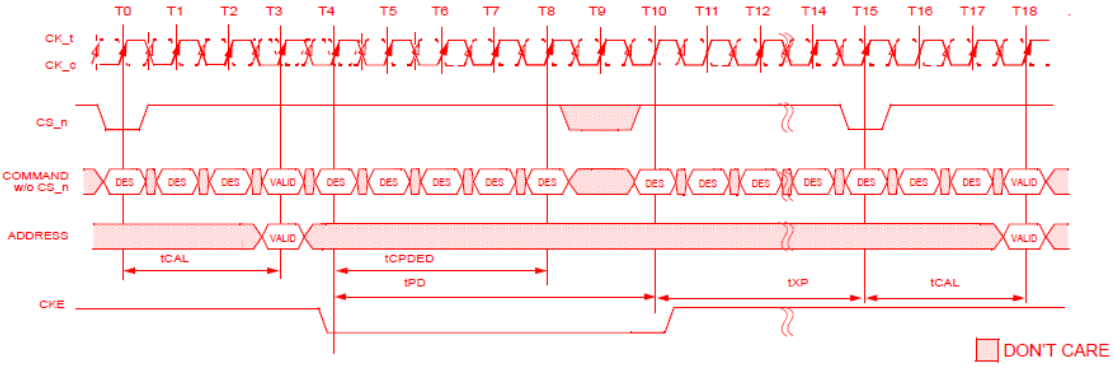


NOTE 1 tCAL = 3nCK, tCPDED = 4nCK, tCKSRE = 8nCK, tCKSRX = 8nCK, tXS_FAST = tRFC4(min) + 10ns

NOTE 2 $\overline{CS}$ = H, $\overline{ACT}$ = Don't Care, $\overline{RAS}$/A16 = Don't Care, $\overline{CAS}$/A15 = Don't Care, $\overline{WE}$/A14 = Don't Care

NOTE 3 Only MRS (limited to those described in the Self-Refresh Operation section). ZQCS or ZQCL command allowed.

Power Down Entry, Exit Timing with CAL



NOTE 1 tCAL = 3nCK, tCPDED = 4nCK, tPD = 6nCK, tXP = 5nCK

Low-Power Auto Self Refresh Mode (LPASR)

An auto self refresh mode is provided for application ease. Auto self refresh mode is enabled by setting MR2[6] = 1 and MR2[7] = 1. The device will manage self refresh entry over the supported temperature range of the DRAM. In this mode, the device will change its self refresh rate as the DRAM operating temperature changes, going lower at low temperatures and higher at high temperatures.

Manual Self Refresh Mode

If auto self refresh mode is not enabled, the low-power auto self refresh mode register must be manually programmed to one of the three self refresh operating modes. This mode provides the flexibility to select a fixed self refresh operating mode at the entry of the self refresh, according to the system memory temperature conditions. The user is responsible for maintaining the required memory temperature condition for the mode selected during the self refresh operation. The user may change the selected mode after exiting self refresh and before entering the next self refresh. If the temperature condition is exceeded for the mode selected, there is a risk to data retention resulting in loss of data.

Auto Self Refresh Mode

MR2 [7]	MR2 [6]	Low-Power Auto Self Refresh Mode	Self Refresh Operation
0	0	Normal[1]	Fixed normal self refresh rate maintains data retention at the normal operating temperature. User is required to ensure that 85°C DRAM $T_{CASEMAX}$ is not exceeded to avoid any risk of data loss.
0	1	Extended Temp[2]	Fixed high self refresh rate optimizes data retention to support the extended temperature range.
1	0	Reduced Temp[3]	Variable or fixed self refresh rate or any other DRAM power consumption reduction control for the reduced temperature range. User is required to ensure 45°C DRAM TCASEMAX is not exceeded to avoid any risk of data loss.
1	1	Auto Self Refresh	Auto self refresh mode enabled. Self refresh power consumption and data retention are optimized for any given operating temperature condition.

NOTE 1 The Normal range depends on product's grade.
- Commercial Grade = 0℃~85℃
- Industrial Grade (**-I**) = -40℃~85℃

NOTE 2 The Extended range depends on product's grade.
- Commercial Grade = 85℃~95℃
- Industrial Grade (**-I**) = 85℃~95℃

NOTE 3 The Reduced range depends on product's grade.
- Commercial Grade = 0℃~45℃
- Industrial Grade (**-I**) = -40℃~45℃

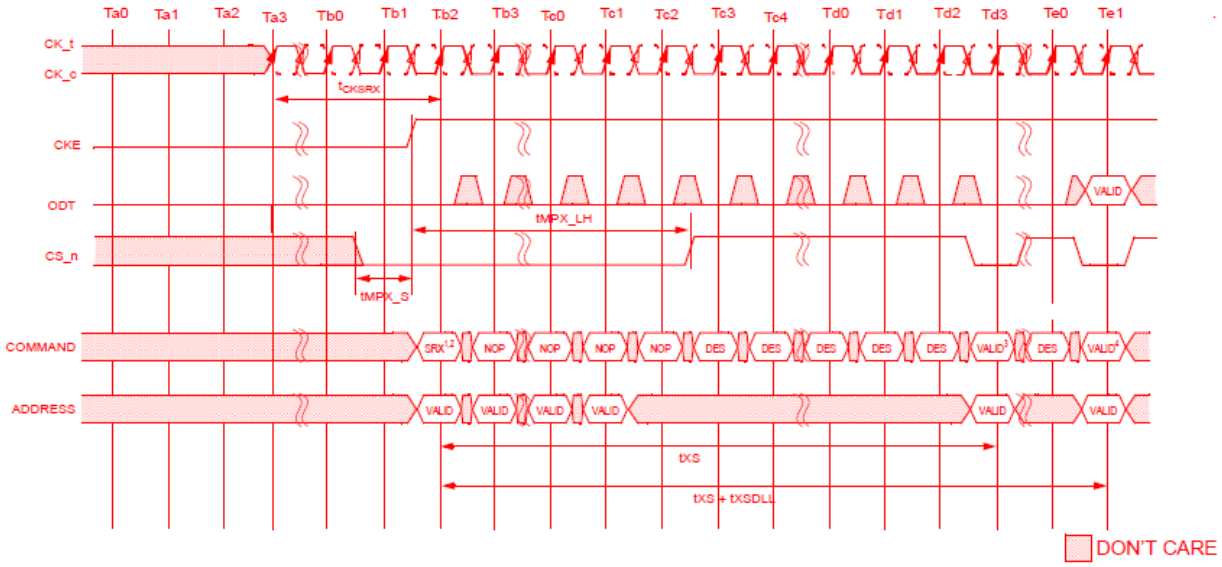
Self Refresh Exit with No Operation command

Self Refresh Exit with No Operation command (NOP) allows for a common command/address bus between active DRAM and DRAM in Max Power Saving Mode. Self Refresh Mode may exit with No Operation commands (NOP) provided:

(1) The DRAM entered Self Refresh Mode with CA Parity and CAL disabled.

(2) tMPX_S and tMPX_LH are satisfied.

(3) NOP commands are only issued during tMPX_LH window. No other command is allowed during tMPX_LH window after SRX command is issued.



NOTE 1 $\overline{CS}$ = L, $\overline{ACT}$ = H, $\overline{RAS}$/A16 = H, $\overline{CAS}$/A15 = H, $\overline{WE}$/A14 = H at Tb2 (No Operation command)

NOTE 2 SRX at Tb2 is only allowed when DRAM shared Command/Address bus is under exiting Max Power Saving Mode.

NOTE 3 Valid commands not requiring a locked DLL

NOTE 4 Valid commands requiring a locked DLL

NOTE 5 tXS_FAST and tXS_ABORT are not allowed this case.

NOTE 6 Duration of $\overline{CS}$ Low around CKE rising edge must satisfy tMPX_S and tMPX_LH as defined by Max Power Saving Mode AC parameters.

Multipurpose Register (MPR)

The multipurpose register (MPR) function, MPR Access Mode, is used to write/read specialized data to/from the DRAM. The MPR consists of four logical Pages, MPR Page 0 through MPR Page 3, with each Page having four 8-bit registers, MPR0 through MPR3.

MPR mode enable and Page selection is done with MRS commands. Data Bus Inversion (DBI) is not allowed during MPR Read operation. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register.

Once the MPR Access Mode is enabled (MR3[2] = 1), only the following commands are allowed: MRS, RD, RDA WR, WRA, DES, REF and Reset; RDA/WRA have the same functionality as RD/WR which means the auto precharge part of RDA/WRA is ignored. The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power Down mode and Self-Refresh command are not allowed during MPR enable Mode.

No other command can be issued within tRFC after a REF command has been issued; 1x Refresh {only} is to be used during MPR Access Mode. While in MPR Access Mode, MPR read or write sequences must be completed prior to a refresh command. The reset function is supported during MPR mode, which requires re-initialization of the DDR4 SDRAM.

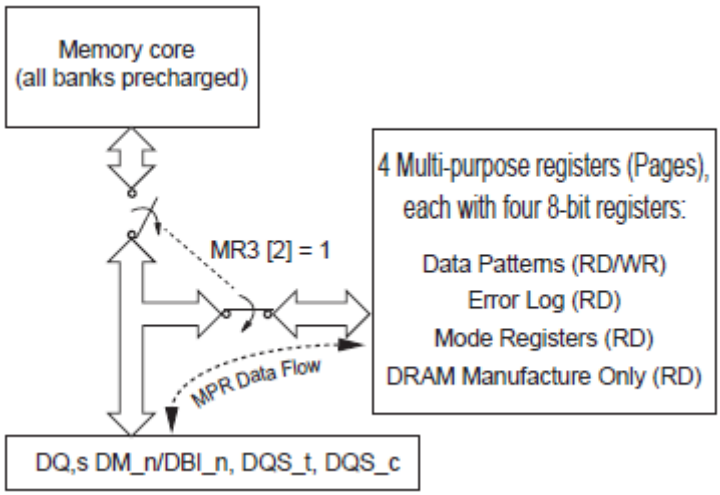
Allow	Not Allow
1. MPR Read with BL8 or BC4 (A[2:0] = 000 or 100) 2. MRS, RD, RDA WR, WRA, DESELECT, REFRESH and Reset	1. BL OTF 2. Data Bus Inversion (DBI) 3. Power Down mode and Self-Refresh

MPR pages

After power-up, the content of MPR page 0 has the default values, defined in the MPR Data Format table. MPR page 0 can be rewritten via an MPR WRITE command. The DRAM maintains the default values unless it is re-written by the DRAM controller. If DRAM's controller does overwrite the default values (Page 0 only), the device will maintain the new values unless re-initialized or power loss.

MPR	Page 0	Page 1	Page 2	Page 3
Definition	**WRITE** and **READ** system patterns used for data bus calibration	**Readout** of the error frame when the C/A parity is enabled	**Readout** of the contents of the MRn registers	RFU
Can be used for	• DRAM controller receiver training. • DRAM controller DQS to DQ phase training.	• Clock to address phase training. • RAS (reliability, accessibility and serviceability) Support: Logging of C/A parity and CRC error information	• Mode Register Confirmation.	N/A.
Readout format	serial, parallel, or staggered	serial	serial	serial

MPR Block Diagram



Bit Number of MPR Definition

128 bits	=	MPR Page	×	MPR Location	×	Address Bit
		MPRx (MR3[1:0])		MPRy (MPR BA[1:0])		MPR burst bit (BL8)

DRAM Address to MPR UI Translation

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DRAM Address - Ax	A7	A6	A5	A4	A3	A2	A1	A0
MPR UI - Uix	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

MPR necessary settings

MPR Read Format — MR3[12:11]

MR3		MPR Read Format
A12	A11	
0	0	Serial
0	1	Parallel
1	0	Staggered
1	1	RFU

MPR Operation — MR3[2]

MR3	MPR Operation
A2	
0	Normal Operation
1	Data flow from MPR

MPR Page Selection — MR3[1:0]

MR3		MPR Page Selection
A1	A0	
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

MPR Location — MPR BA[1:0]

MPR		MPR Location
BA1	BA0	
0	0	MPR0
0	1	MPR1
1	0	MPR2
1	1	MPR3

MPR Page and MPRx Definitions

MPR Page MR3[1:0]	Purpose	MPR Location BA[1:0]	MPR Bit Write Location [7:0]							
			7	6	5	4	3	2	1	0
			Read Burst Order (serial mode)							
			UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
00 Page 0	Training Patterns	**00** = MPR0	0	1	0	1	0	1	0	1
		01 = MPR1	0	0	1	1	0	0	1	1
		10 = MPR2	0	0	0	0	1	1	1	1
		11 = MPR3	0	0	0	0	0	0	0	0
01 Page 1	C/A Parity Error Log	**00** = MPR0	A7	A6	A5	A4	A3	A2	A1	A0
		01 = MPR1	$\overline{CAS}$/A15	$\overline{WE}$/A14	A13	A12	A11	A10	A9	A8
		10 = MPR2	PAR	$\overline{ACT}$	BG1	BG0	BA1	BA0	A17[2]	$\overline{RAS}$/A16
		11 = MPR3	CRC Error Status	CA Parity Error Status[1]	CA Parity Latency[4]			RFU	RFU	RFU
					MR5 [A2]	MR5 [A1]	MR5 [A0]			
10 Page 2	MRS Readout	**00** = MPR0	RFU	RFU	RFU	Temperature Sensor Status[5]		CRC Write Enable	R_{TT}_WR	
						Refer to next table		MR2	MR2	
								A12	A10	A9
		01 = MPR1	Vref DQ Tmg range	Vref DQ training Value						Geardown Enable
			MR6	MR6						MR3
			A6	A5	A4	A3	A2	A1	A0	A3
		10 = MPR2	CAS Latency				RFU	CAS Write Latency		
			MR0					MR2		
			A6	A5	A4	A2		A5	A4	A3
		11 = MPR3	R_{TT}_NOM			R_{TT}_PARK			Driver Impedance	
			MR1			MR5			MR1	
			A10	A9	A6	A8	A7	A6	A2	A1
11 Page 3	RFU	**00** = MPR0	Don't care							
		01 = MPR1	Don't care							
		10 = MPR2	Don't care							
		11 = MPR3	Don't care							

NOTE 1 MPR page 1 used for C/A parity error log readout is enabled by setting A[2] in MR3.

NOTE 2 For higher density of DRAM, where A[17] is not used, MPR page 1's MPR2[1] should be treated as don't care.

NOTE 3 If a device is used in monolithic application, where C[2:0] are not used, then MPR page 1's MPR3[2:0] should be treated as don't care.

NOTE 4 MPR page 1's MPR3 bit 0-2 (CA parity latency) reflects the latest programmed CA parity latency values.

NOTE 5 MPR page 2's Temperature Sensor Readout

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range	MR3[5]
0	0	Sub 1x refresh (>tREFI)	**MR3 bit A5=1 (Temperature sensor readout = Enabled)** DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A[4:3]). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits. **MR3 bit A5=0 (Temperature sensor readout = Disabled)** DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A[4:3])
0	1	1x refresh rate (= tREFI)	
1	0	2x refresh rate (1/2 x tREFI)	
1	1	RFU	

MPR Reads

The DRAM is required to drive associated strobes with the read data similar to normal operation (such as using MRS preamble settings). Timing in MPR Mode should follow below rules:

- Reads (back-to-back) from Page 0 may use tCCD_S timing between read commands.
- Reads (back-to-back) from Pages 1, 2, or 3 may not use tCCD_S timing between read commands; tCCD_L must be used for timing between read commands.

The following steps are required to use the MPR to read out the contents of a mode register (MPR Page x, MPRy).

1. The DLL must be locked if enabled.
2. Precharge all; wait until tRP is satisfied.
3. MRS command to MR3[2] = 1 (Enable MPR data flow), MR3[12:11] = MPR Read Format, and MR3[1:0] = MPR Page.
   a. MR3[12:11] MPR Read Format:
      00 = Serial read format
      01 = Parallel read format
      10 = staggered read format
      11 = RFU
   b. MR3[1:0] MPR Page:
      00 = MPR Page 0
      01 = MPR Page 1
      10 = MPR Page 2
      11 = MPR Page 3
4. tMRD and tMOD must be satisfied.
5. Redirect all subsequent READ commands to specific MPRx location.
6. Issue RD or RDA command:
   a. BA1 and BA0 indicate MPRx location:
      00 = MPR0
      01 = MPR1
      10 = MPR2
      11 = MPR3
   b. A12/BC = 0 or 1; BL8 or BC4 Fixed only, BC4 OTF not supported.
      If BL=8 and MR0 A[1:0] = 01, A12/BC must be set to 1 during MPR Read commands.
   c. A[2] = burst type dependant:
      BL8: A[2] = 0 with burst order fixed at 0, 1, 2, 3, 4, 5, 6, 7
      BL8: A[2] = 1 with burst order fixed at 4, 5, 6, 7, 0, 1, 2, 3
      BC4: A[2] = 0 with burst order fixed at 0, 1, 2, 3, T, T, T, T
      BC4: A[2] = 1 with burst order fixed at 4, 5, 6, 7, T, T, T, T
   d. A[1:0] = 00, data burst is fixed nibble start at 00.
   e. Remaining address inputs, including A10, and BG1 and BG0 are don't care.
7. After RL = AL + CL, DRAM bursts data from MPRx location; MPR readout format determined by MR3 [A12,11,1,0].
8. Steps 5 through 7 may be repeated to read additional MPRx locations.
9. After the last MPRx Read burst, tMPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR[3] = 0.
11. Once tMOD sequence is completed; the DRAM is ready for normal operation from the core such as ACT.

MPR Readout Serial Format

Serial format implies that the same pattern is returned on all DQ lanes.

MPR Readout Parallel Format

Parallel format implies that the MPR data is returned in the first data UI and then repeated in the remaining UIs of the burst as shown in the MPR Readout Parallel Format table. Data pattern location 0 is the only location used for the parallel format. RD/RDA from data pattern locations 1, 2, and 3 are not allowed with parallel data return mode.

Example: The pattern programmed in the data pattern location 0 is 0111 1111. The x4 configuration only outputs the first four bits (0111 in this example). For the x16 configuration, the same pattern is repeated on both the upper and lower bytes.

Serial

X4 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1

X8 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1

X16 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

Parallel

X4 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1

X8 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1

X16 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
DQ8	0	0	0	0	0	0	0	0
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

MPR Readout Staggered Format

Staggered format of data return is defined as the staggering of the MPR data across the lanes. In this mode, an RD/RDA command is issued to a specific data pattern location and then the data is returned on the DQ from each of the different data pattern locations.

For the x4 configuration, an RD/RDA to data pattern location 0 will result in data from location 0 being driven on DQ0, data from location 1 being driven on DQ1, data from location 2 being driven on DQ2, and so on. Similarly, an RD/RDA command to data pattern location 1 will result in data from location 1 being driven on DQ0, data from location 2 being driven on DQ1, data from location 3 being driven on DQ2, and so on. It is expected that the DRAM can respond to back to back RD/RDA commands to the MPR for all DDR4 frequencies so that a stream as follows can be created on the data bus with no bubbles or clocks between read data. In this case system memory controller issues a sequence of RD(MPR0), RD(MPR1), RD(MPR2), RD(MPR3), RD(MPR0), RD(MPR1), RD(MPR2), and RD(MPR3).

For the x8 configuration, the same pattern is repeated on the lower nibble as on the upper nibble. READs to other MPR data pattern locations follow the same format as the x4 case.

MPR Readout Staggered Format, x4

MPR0(BA[1:0]=''00')		MPR0(BA[1:0]=''01')		MPR0(BA[1:0]=''10')		MPR0(BA[1:0]=''11')	
Stagger	UI0-7	Stagger	UI0-7	Stagger	UI0-7	Stagger	UI0-7
DQ0	MPR0	DQ0	MPR1	DQ0	MPR2	DQ0	MPR3
DQ1	MPR1	DQ1	MPR2	DQ1	MPR3	DQ1	MPR0
DQ2	MPR2	DQ2	MPR3	DQ2	MPR0	DQ2	MPR1
DQ3	MPR3	DQ3	MPR0	DQ3	MPR1	DQ3	MPR2

MPR Readout Staggered Format, x4 – Consecutive READs

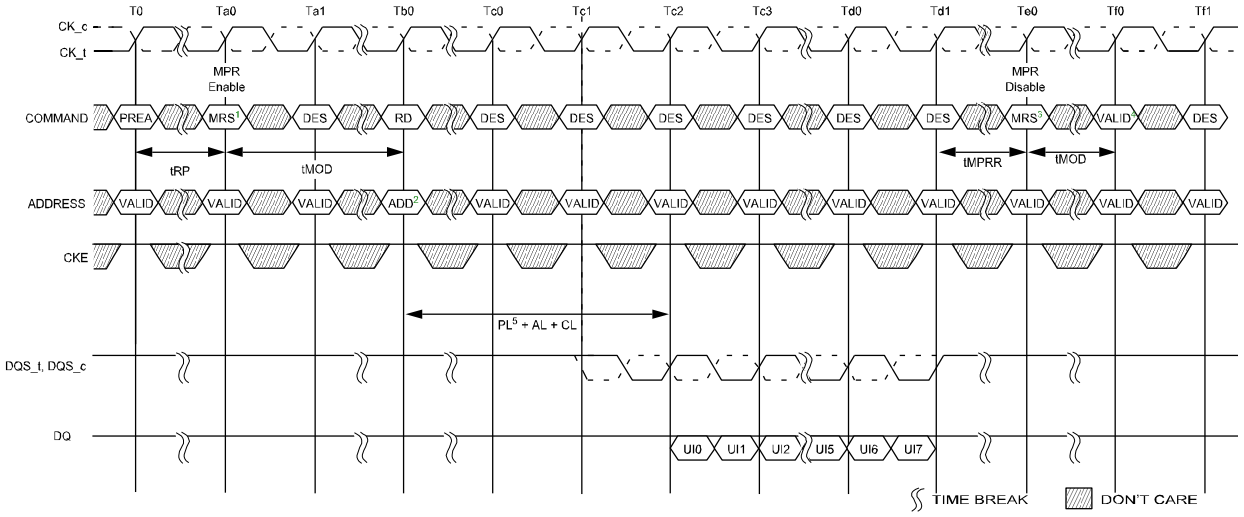
Stagger	UI0-7	UI 8-15	UI 16-23	UI 24-31	UI 32-39	UI 40-47	UI 48-55	UI 56-63
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

MPR Readout Staggered Format, x8 and x16

X8		X16			
Stagger	UI0-7	Stagger	UI0-7	Stagger	UI0-7
DQ0	MPR0	DQ0	MPR0	DQ8	MPR0
DQ1	MPR1	DQ1	MPR1	DQ9	MPR1
DQ2	MPR2	DQ2	MPR2	DQ10	MPR2
DQ3	MPR3	DQ3	MPR3	DQ11	MPR3
DQ4	MPR0	DQ4	MPR0	DQ12	MPR0
DQ5	MPR1	DQ5	MPR1	DQ13	MPR1
DQ6	MPR2	DQ6	MPR2	DQ14	MPR2
DQ7	MPR3	DQ7	MPR3	DQ15	MPR3

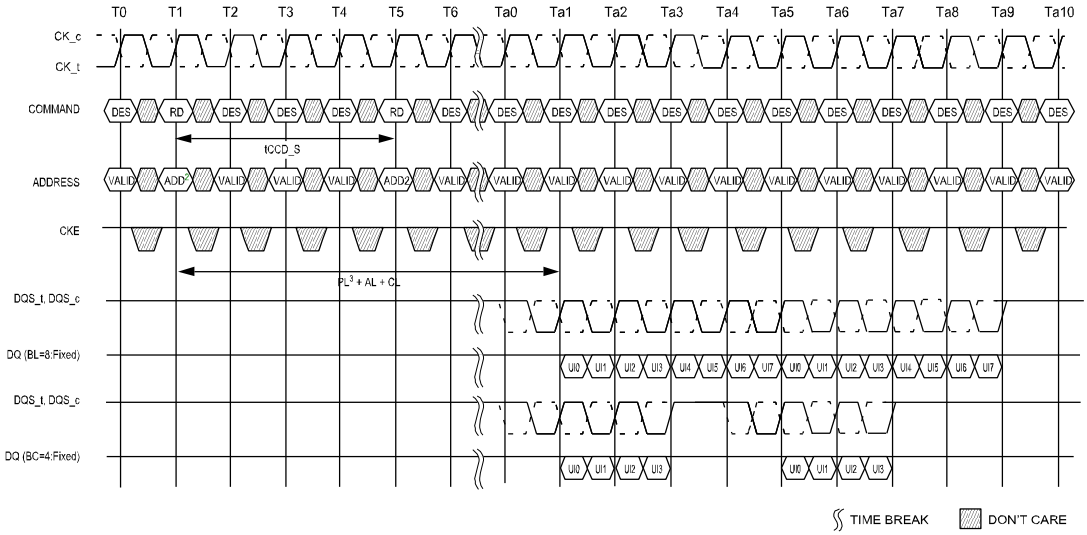
MPR Read Waveforms

MPR READ Timing



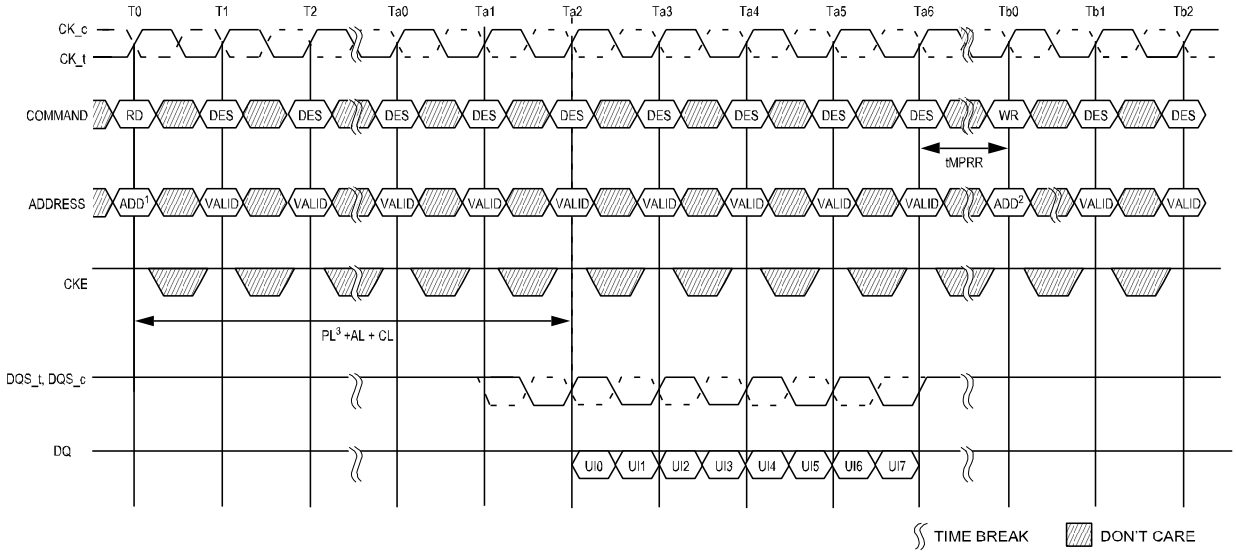
NOTE 1 Multipurpose registers Read/Write Enable (MR3 A2 = 1). Redirect all subsequent reads and writes to MPR locations.
NOTE 2 Address setting:
A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)
A[2]= 0b (For BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care" including BG1 and BG0.
A12 is don't care when MR0 A[1:0] = 00 or 10, and must be 1b when MR0 A[1:0] = 01
NOTE 3 Multipurpose registers Read/Write Disable (MR3 A2 = 0).
NOTE 4 Continue with regular DRAM command.
NOTE 5 Parity latency (PL) is added to data output delay when C/A parity latency mode is enabled. BL = 8, AL = 0, CL = 11, CAL = 3, Preamble = 1tCK.

MPR Back-to-Back READ Timing



NOTE 1 Multipurpose registers Read/Write Enable (MR3 A2 = 1). Redirect all subsequent reads and writes to MPR locations.
NOTE 2 Address setting:
A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
A[2] = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7; for BC = 4, burst order is fixed at 0, 1, 2, 3, T, T, T, T)
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care" including BG1 and BG0.
A12 is "Don't Care" when MR0 A[1:0] = 00 or 10, and must be 1b when MR0 A[1:0] = 01
NOTE 3 Parity latency (PL) is added to data output delay when C/A parity latency mode is enabled.

MPR READ-to-WRITE Timing



NOTE 1 Address setting:
A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
A[2]= 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care" including BG1 and BG0.
A12 is "Don't Care" when MR0 A[1:0] = 00, and must be 1b when MR0 A[1:0] = 01

NOTE 2 Address setting:
BA1 and BA0 indicate the MPR location
A [7:0] = data for MPR
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care"

NOTE 3 Parity latency (PL) is added to data output delay when C/A parity latency mode is enabled.

MPR Writes

MPR Access Mode allows 8-bit writes to the MPR location using the address bus A7:0.

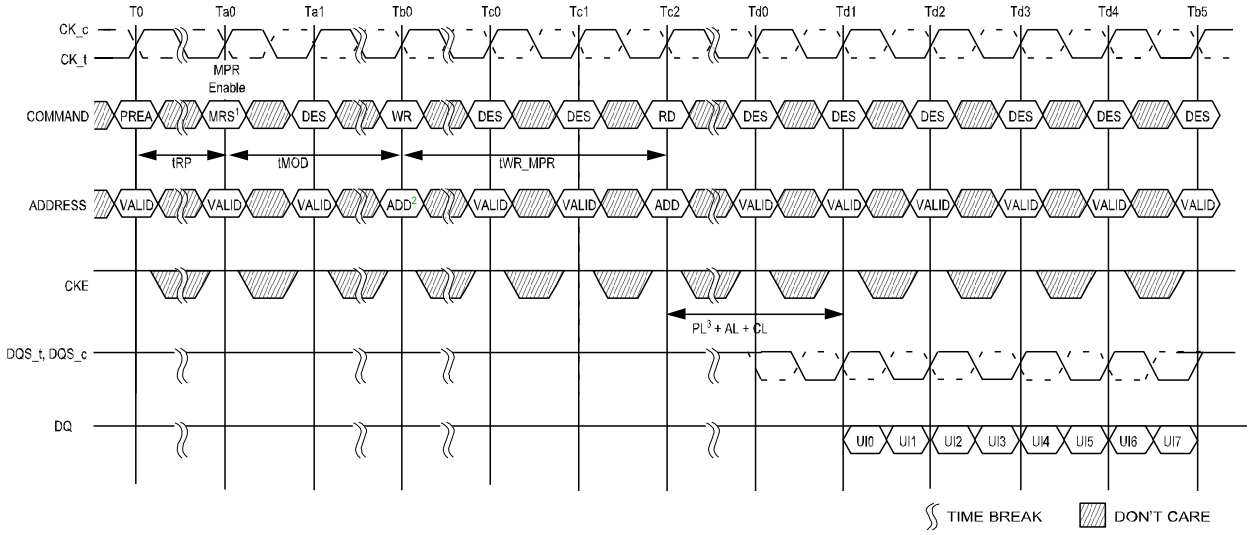
Data Bus Inversion (DBI) is not allowed during MPR Write operation. The DRAM will maintain the new written values unless re-initialized or power loss.

The following steps are required to use the MPR to write to mode register MPR Page 0, MPRy).

1. The DLL must be locked if enabled.
2. Precharge all; wait until tRP is satisfied.
3. MRS command to MR3[2] = 1 (Enable MPR data flow) and MR3[1:0] = 00 (MPR Page 0); 01, 10, 11 = Not allowed.
4. tMRD and tMOD must be satisfied.
5. Redirect all subsequent Write commands to specific MPRx location.
6. Issue WR or WRA command:
   a. BA1 and BA0 indicate MPRx location:
      00 = MPR0
      01 = MPR1
      10 = MPR2
      11 = MPR3
   b. A[7:0] = data for MPR Page 0, mapped A[7:0] to UI[0:7] .
   c. Remaining address inputs, including A10, BG0 and BG1 are don't care.
7. tWR_MPR must be satisfied to complete MPR Write.
8. Steps 5 through 7 may be repeated to write additional MPRx locations.
9. After the last MPRx Write, tMPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR[3] = 0.
11. Once tMOD sequence is completed; the DRAM is ready for normal operation from the core such as ACT.

MPR Write Waveforms

MPR WRITE and WRITE-to-READ Timing

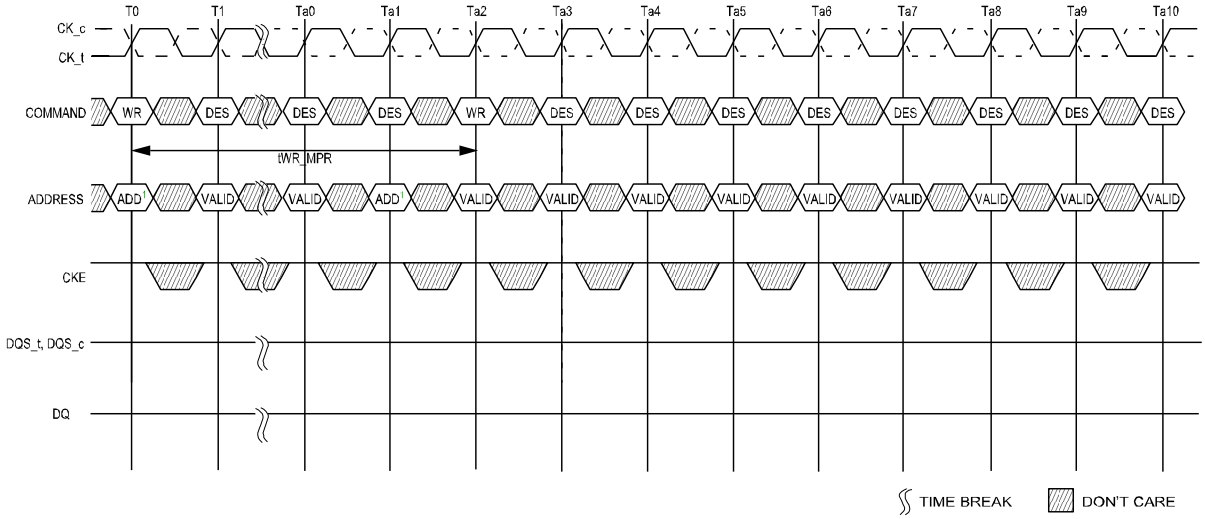


NOTE 1 Multipurpose registers Read/Write Enable (MR3 A2 = 1).

NOTE 2 Address setting:
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care"

NOTE 3 Parity latency (PL) is added to data output delay when C/A parity latency mode is enabled.

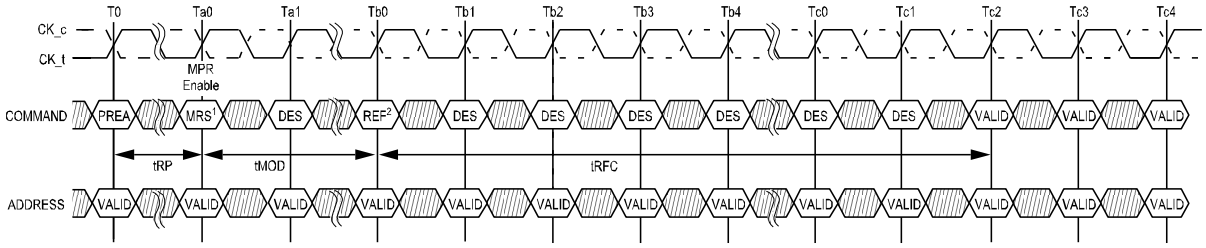
MPR Back-to-Back WRITE Timing



NOTE 1 Address setting:
BA1 and BA0 indicate the MPR location
A [7:0] = data for MPR
A10 and other address pins are "Don't Care"

MPR Refresh Waveforms

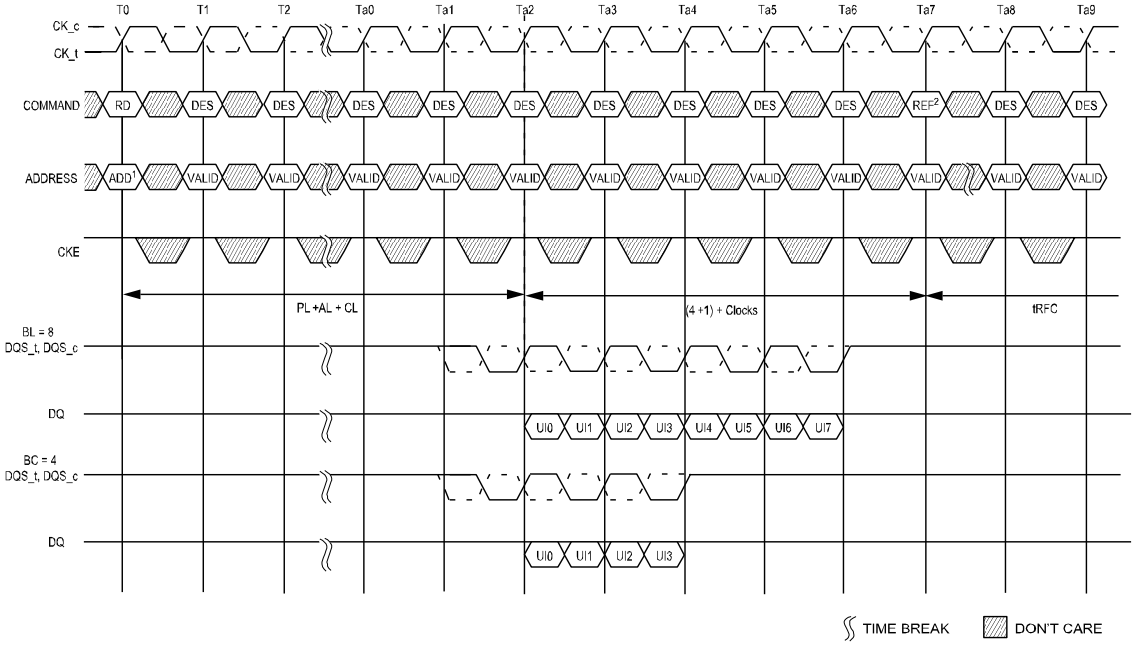
REFRESH Timing



NOTE 1 Multipurpose registers Read/Write Enable (MR3 A2 = 1). Redirect all subsequent read and writes to MPR locations.

NOTE 2 1x refresh is only allowed when MPR mode is enabled.

READ-to-REFRESH Timing



NOTE 1 Address setting:

A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)

A[2]= 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)

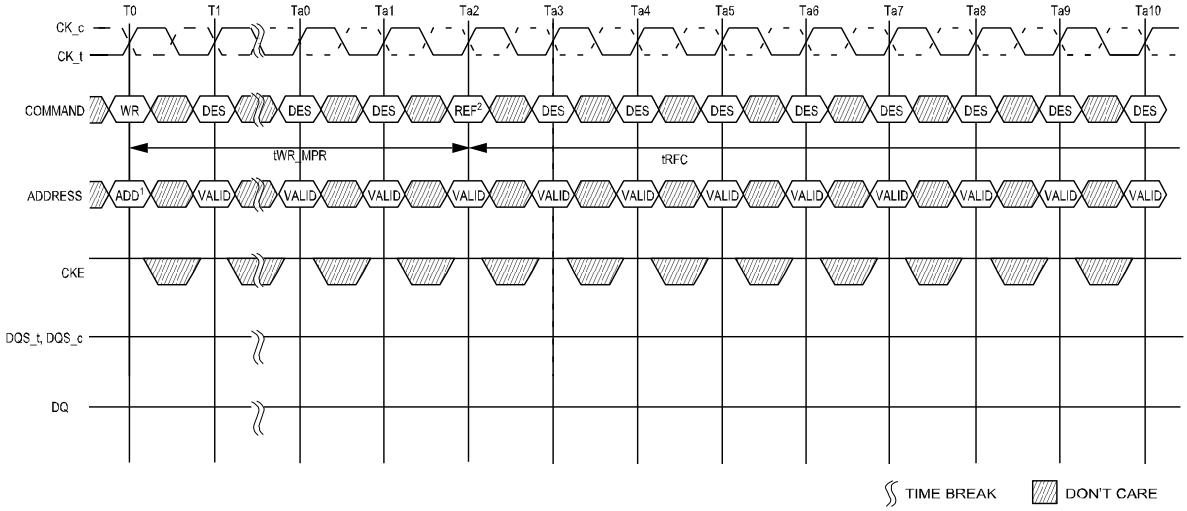
BA1 and BA0 indicate the MPR location

A10 and other address pins are "Don't Care" including BG1 and BG0.

A12 is "Don't Care" when MR0 A[1:0] = 00 or 10, and must be 1b when MR0 A[1:0] = 01

NOTE 2 1x refresh is only allowed when MPR mode is enabled.

WRITE-to-REFRESH Timing

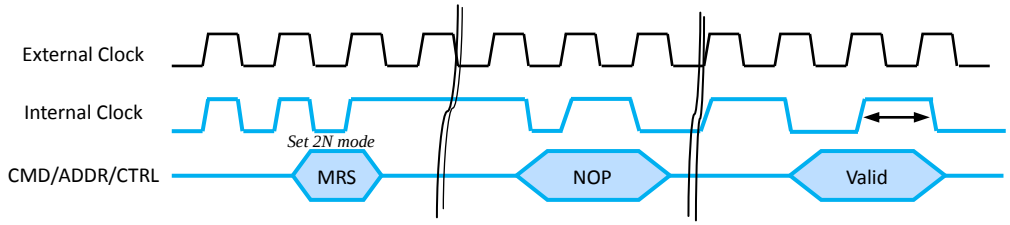


NOTE 1 Address setting: BA1 and BA0 indicate the MPR location A [7:0] = data for MPR A10 and other address pins are "Don't Care"

NOTE 2 1x refresh is only allowed when MPR mode is enabled.

Gear-down Mode

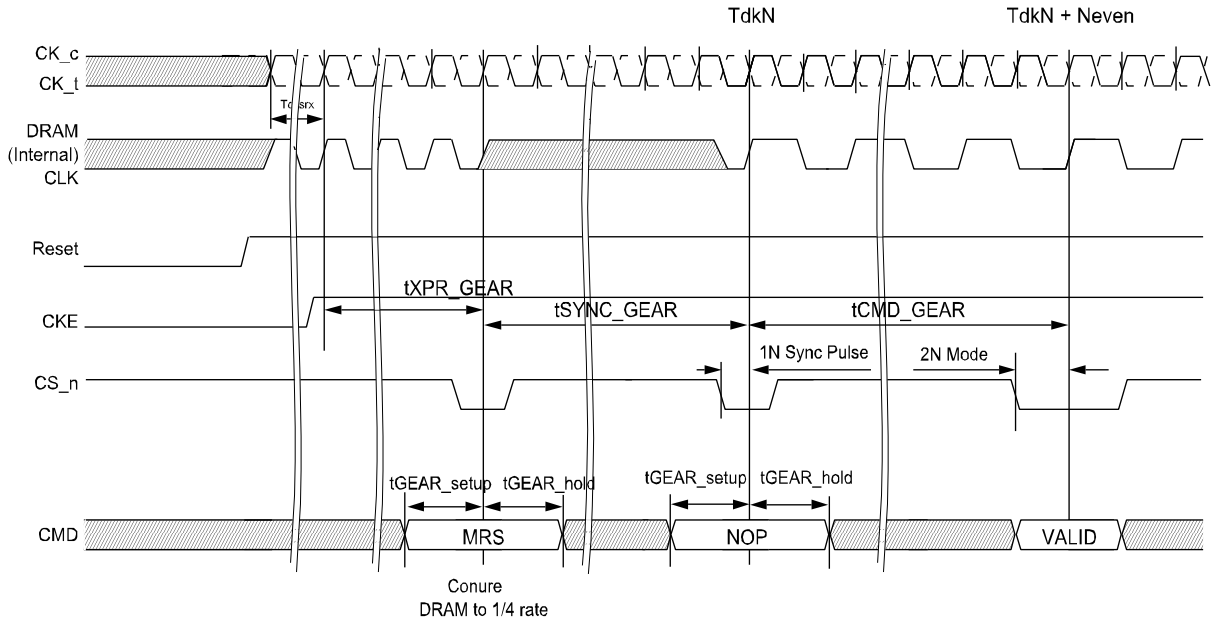
The DDR4 SDRAM defaults in 1/2 rate (1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines $\overline{CS}$, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode, no MRS command or sync pulse is required.



The general sequence for operation in 1/4 rate during initialization is as follows:

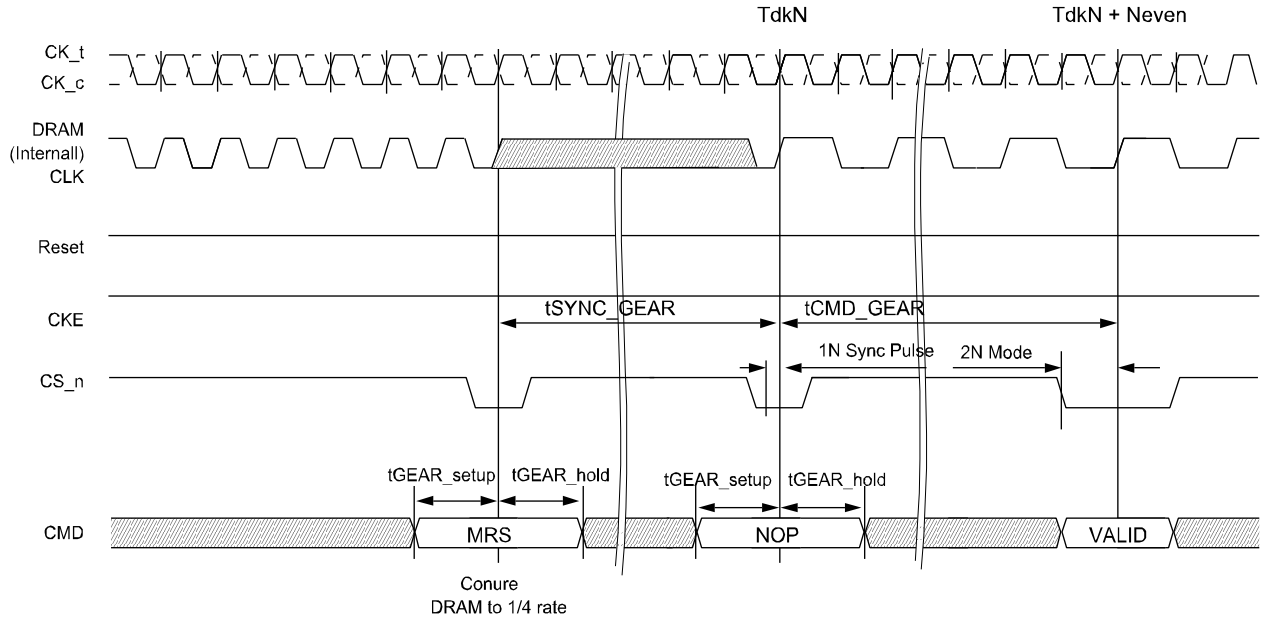
1. DDR4 SDRAM defaults to a 1/2 rate (1N mode) internal clock at power-up/reset.
2. Assertion of reset.
3. Assertion of CKE enables the rank.
4. CAL and CA parity mode must be disabled prior to Gear-down MRS command. They can be enabled again after tSYNC_GEAR and tCMD_GEAR periods are satisfied.
5. MRS is accessed with a low frequency NxtCK MRS Gear-down CMD. (NtCK static MRS command is qualified by 1N $\overline{CS}$.)
6. The memory controller shall send a 1N sync pulse with a low frequency N*tCK NOP CMD;. Clock tSYNC_GEAR is an even number of clocks; sync pulse on even edge from MRS CMD.
7. Normal operation in 2N mode starts tCMD_GEAR clocks later. When operating in 1/4 rate Gear-down Mode, the following MR settings apply:
   - CAS Latency (MR0 [6:4,2]): Even numbers
   - Write Recovery and Read to Precharge (MR0 [11:9]) : Even numbers
   - CAS Write Latency (MR2 A[5:3]) : Even numbers
   - $\overline{CS}$ to Command/Address Latency Mode (MR4 [8:6]) : Even numbers
   - CA Parity Latency Mode (MR5 [2:0]) : Even numbers
   - Additive Latency (MR1 [4:3]): CL–2

Gear down (2N) mode entry sequence during initialization



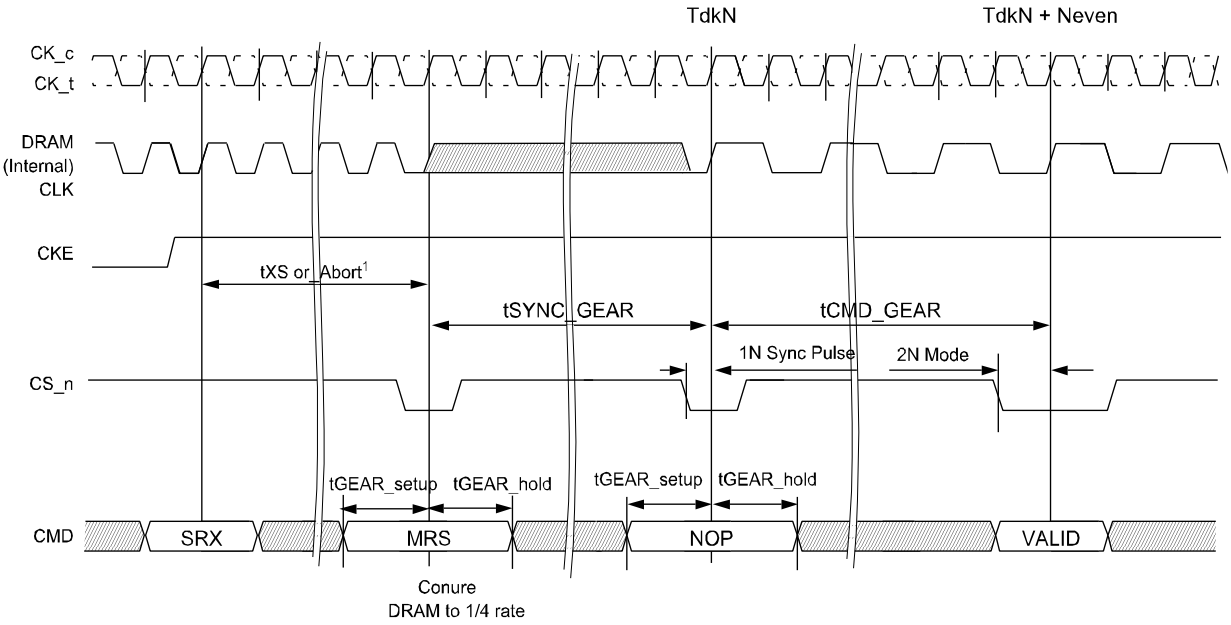
NOTE 1 The diagram below represents the operation of geardown(1/2 rate to 1/4 rate)mode during normal operation with CKE and Reset set high.

Clock Mode Change from 1/2 Rate to 1/4 Rate (Normal Operation)



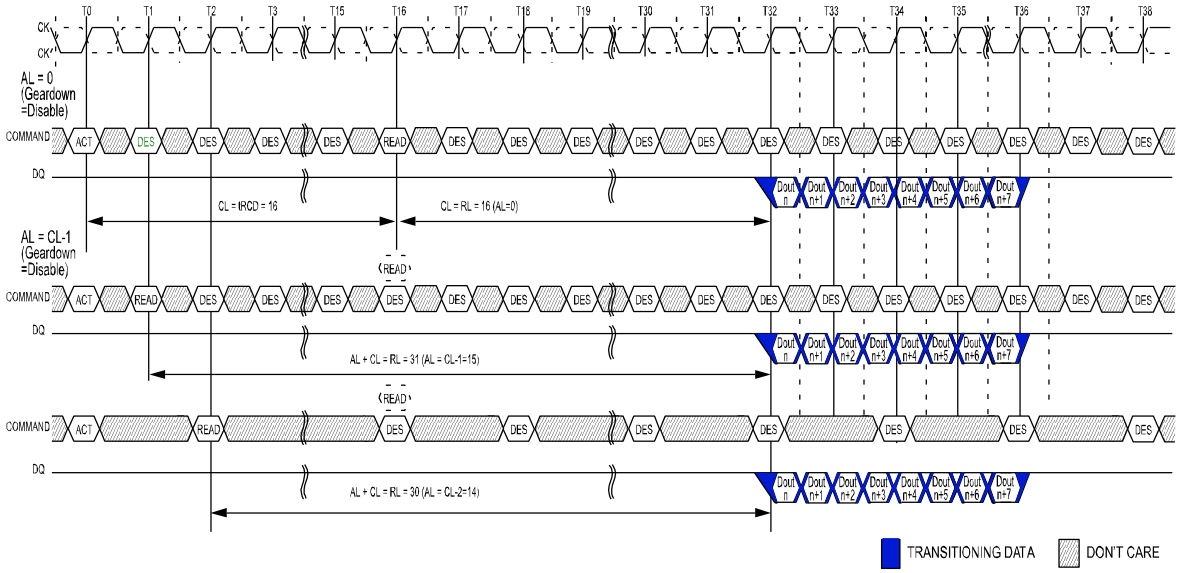
If the operation is in 1/2 rate (1N) mode before and after self refresh, no MRS command or sync pulse is required after self refresh exit. However, if the clock mode is set to 1/4 rate (2N) before and after self refresh mode, the DDR4 SDRAM requires an MRS command and sync pulse as shown in the figure below.

Clock Mode Change After Exiting Self Refresh



NOTE 1 CKE High Assert to Gear Down Enable Time (tXS, tXS_Abort) depend on MR setting. A correspondence of tXS/tXS_Abort and MR Setting is as follows. - MR4[A9] = 0 : tXS - MR4[A9] = 1 : tXS_Abort

Comparison Between Gear-down Disable and Gear-down Enable



NOTE 1 BL=8, tRCD=CL=16

NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

Maximum Power-Saving Mode (MPSM)

This mode provides the lowest power mode where data retention is not required. When DDR4 SDRAM is in the maximum power-saving mode, it does not maintain data retention or respond to any external command, except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of $\overline{\text{RESET}}$ signal LOW. This mode is more like a “hibernate mode” than a typical power savings mode. The intent is to be able to park the DRAM at very low powered state so the device can be switched to an active state via PDA mode.

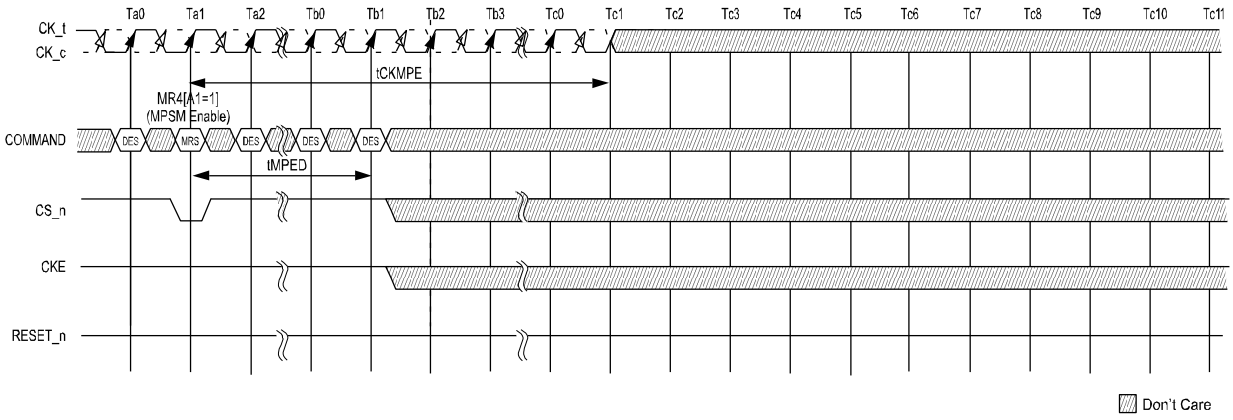
Maximum Power-Saving Mode Entry

Max power saving mode is entered through an MRS command. For devices with shared control/address signals, a single DRAM device can be entered into the max power saving mode using the per DRAM Addressability MRS command. Large $\overline{\text{CS}}$ hold time to CKE upon the mode exit could cause DRAM malfunction; thus, it is required CA parity, CAL and Gear-down modes are disabled prior to the max power saving mode entry MRS command.

The MRS command may use both address and DQ information as defined in Per DRAM Addressability section. After tMPED from the MRS mode entry command, the DRAM is not responsive to any input signals except CKE, $\overline{\text{CS}}$, and $\overline{\text{RESET}}$. All other inputs are disabled (external input signals may become hi-Z).

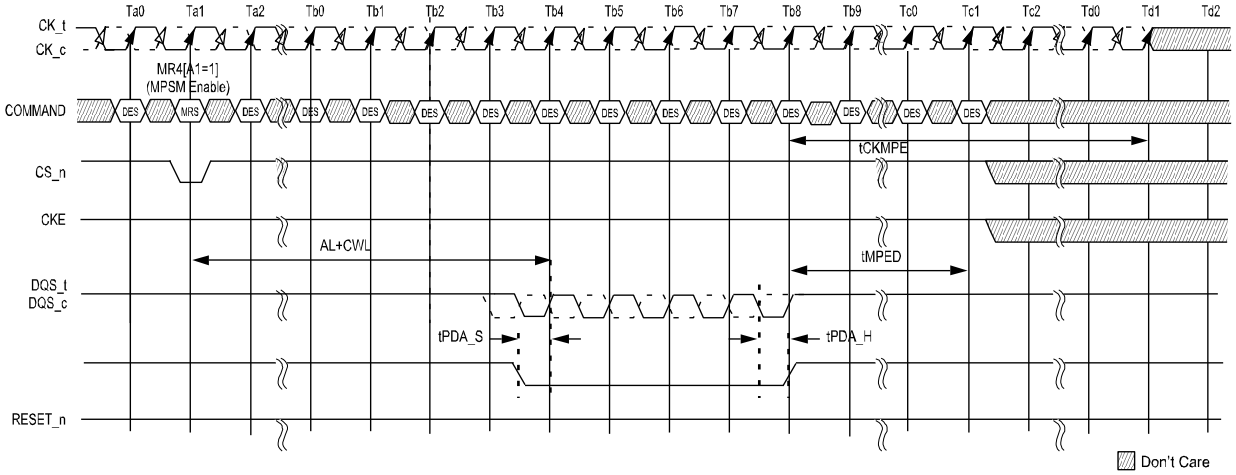
The system will provide a valid clock until tCKMPE expires at which time clock inputs (CK, $\overline{\text{CK}}$) should be disabled (external clock signals may become hi-Z).

Maximum Power Saving Mode Entry



Maximum Power-Saving Mode Entry in PDA

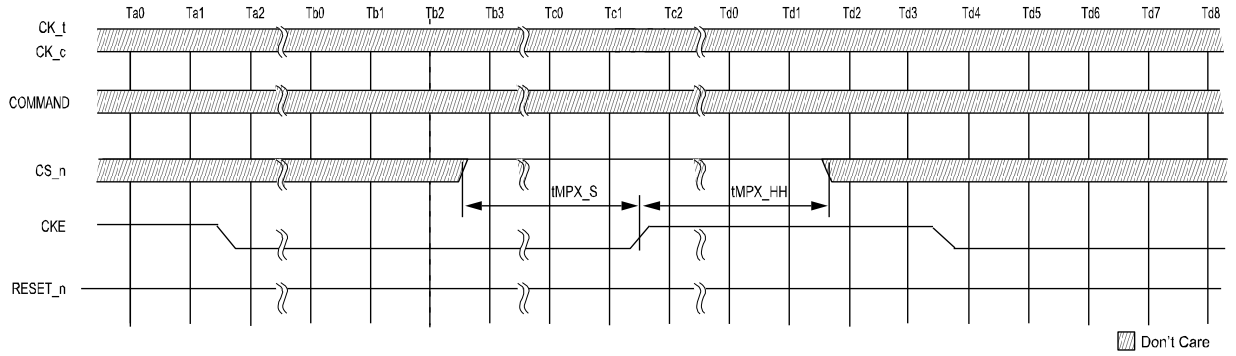
The sequence and timing required for the maximum power saving mode with the per DRAM addressability (PDA) enabled is illustrated in Figure below.



CKE Transition during Maximum Power-Saving Mode

The following figure shows how to maintain maximum power-saving mode even though the CKE input may toggle. To prevent the device from exiting the mode, $\overline{CS}$ should be HIGH at the CKE LOW-to-HIGH edge, with appropriate setup (tMPX_S) and hold (tMPX_H) timings.

CKE Transition Limitation to hold Maximum Power Saving Mode

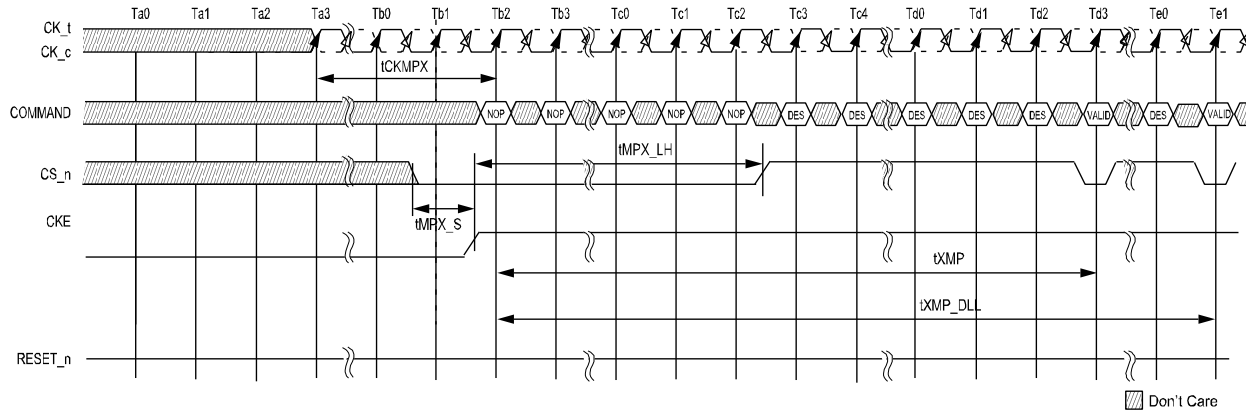


Maximum Power-Saving Mode Exit

To exit the maximum power-saving mode, $\overline{CS}$ should be LOW at the CKE LOW-to-HIGH transition, with appropriate setup (tMPX_S) and hold (tMPX_LH) timings as shown in the figure below. Because the clock receivers (CK, $\overline{CK}$) are disabled during this mode, $\overline{CS}$ = LOW is captured by the rising edge of the CKE signal. If the $\overline{CS}$ signal level is detected LOW, the DRAM clears the maximum power saving mode MRS bit and begins the exit procedure from this mode. The external clock must be restarted and stable by tCKMPX timing before the device can exit the maximum power saving mode.

During the exit time (tXMP) only NOP and DES commands are allowed, NOP during tMPX_LH, and DES the remainder of tXMP. Once tXMP expires, valid commands not requiring a locked DLL are allowed and after tXMP_DLL expires valid commands requiring a locked DLL are allowed.

Maximum Power-Saving Mode Exit



Command/Address Parity (CAP)

CAP's Pros and Cons

In favor of	In opposition
• Enhances the reliability of a system as it extends parity all the way to the DRAM	• The processing of the command at the DRAM is delayed by the time it takes the DRAM to calculate parity and release the command for execution (typically 4 to 6 clock cycles). Note this latency is applicable for all commands • Additional signals compared to DDR3

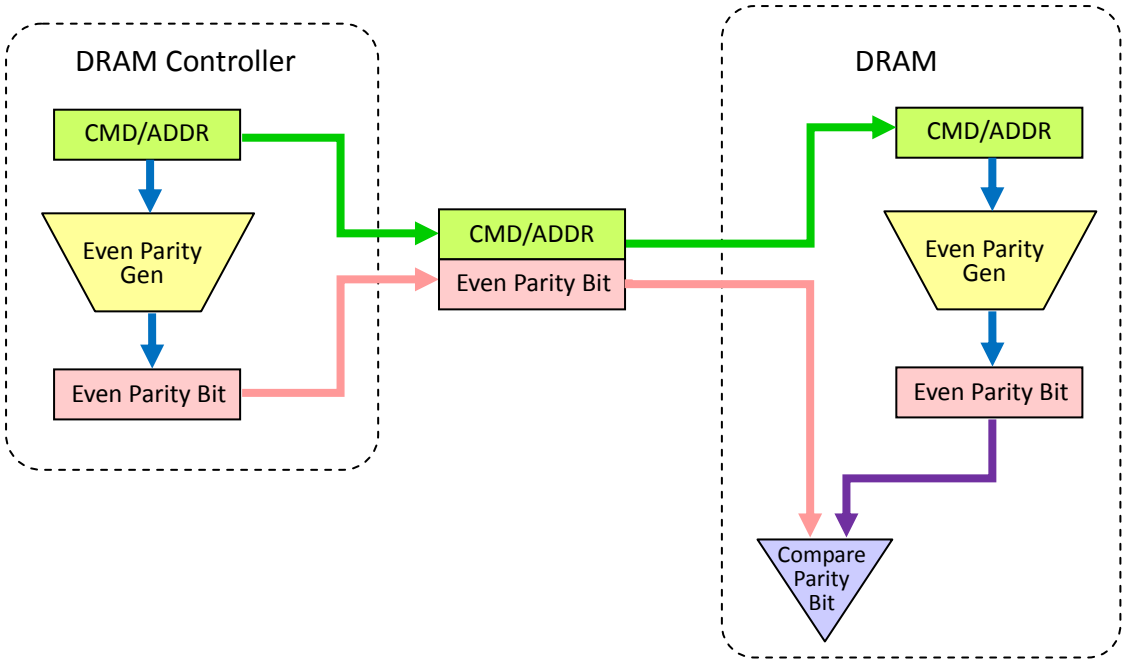
Command/address (CA) Parity takes the PAR input carrying the parity bit for the generated address and commands signals and matches it to the internally generated parity from the captured address and commands signals.

CA Parity is disabled or enabled via MRS command. If CA parity is enabled by programming a non-zero value to CA parity latency in the MR, then the DRAM will ensure that there is no parity error before executing commands. There is an additional delay required for executing the commands versus when parity is disabled and it is programmed in the MR when CA parity is enabled (Parity Latency) and is applied to all commands. When CA parity is enabled, only DESELECT are allowed between valid commands to prevent the device from malfunctioning. CA parity signal (PAR) will go active when the DRAM detects a CA Parity error.

CA Parity covers $\overline{ACT}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and the address bus, including bank address and bank group bits; the control signals CKE, ODT, and $\overline{CS}$ are not covered. For example, for a 4 Gig x4 monolithic device, parity is computed across BG[1:0], BA[1:0], A16/$\overline{RAS}$, A15/$\overline{CAS}$, A14/$\overline{WE}$, A[13:0], and $\overline{ACT}$. The DRAM treats any unused address pins internally as zeros; for example, if a common die has stacked pins but the device is used in a monolithic application, then the address pins used for stacking and not connected are treated internally as zeros.

The convention for parity is even parity; for example, valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words, the parity bit is chosen so that the total number of ones in the transmitted signal, including the parity bit, is even. Even parity is a special case of a cyclic redundancy check (CRC), where the 1-bit CRC is generated by the polynomial x+1.

Command/Address Parity Operation



If a DRAM device detects a CA Parity error in any command qualified by $\overline{CS}$, then it will perform the following steps:

1. Ignore the erroneous command. Commands in MAX NnCK window (tPAR_UNKNOWN) prior to the erroneous command are not guaranteed to be executed. When a READ command in this NnCK window is not executed, the device does not activate DQS outputs.
2. Log the error by storing the erroneous command and address bits in the MPR error log.
3. Set the parity error status bit in the mode register to one. The Parity Error Status bit must be set before the $\overline{ALERT}$ signal is released by the DRAM (i.e. tPAR_ALERT_ON + tPAR_ALERT_PW(min)).
4. Assert the $\overline{ALERT}$ signal to the host ($\overline{ALERT}$ is active LOW) within tPAR_ALERT_ON time.
5. Wait for all in-progress commands to complete. These commands were received tPAR_UNKOWN before the erroneous command.
6. Wait for tRAS_min before closing all the open pages. The DRAM is not executing any commands during the window defined by (tPAR_ALERT_ON +tPAR_ALERT_PW).
7. After tPAR_ALERT_PW_min has been satisfied, the device may de-assert $\overline{ALERT}$.

After the DRAM has returned to a known pre-charged state it may de-assert $\overline{ALERT}$.

8. When the device is returned to a known pre-charged state, $\overline{ALERT}$ is allowed to be de-asserted.
9. After (tPAR_ALERT_PW_max) the DRAM is ready to accept commands for normal operation. Parity latency will be in effect; however, parity checking will not resume until the memory controller has cleared the parity error status bit by writing a zero. The DRAM will execute any erroneous commands until the bit is cleared; unless Persistent mode is enabled.

- The DRAM should have only DESELECT commands issued around $\overline{ALERT}$ going high such that at least 3 clocks prior and 1 clock plus 3ns after the release of $\overline{ALERT}$.

- It is possible that the device might have ignored a REFRESH command during tPAR_ALERT_PW or the REFRESH command is the first erroneous frame so it is recommended that extra REFRESH cycles be issued, as needed.
- The parity error status bit may be read anytime after tPAR_ALERT_ON +tPAR_ALERT_PW to determine which DRAM had the error. The device maintains the error log for the first erroneous command until the parity error status bit is reset to a zero or a second CA Parity occurs prior to resetting.

The mode register for the CA parity error is defined as follows: CA parity latency bits are write only, the parity error status bit is read/write, and error logs are read-only bits. The DRAM controller can only program the Parity Error Status bit to zero. If the DRAM controller illegally attempts to write a one to the Parity Error Status bit, the DRAM can not be certain that parity will be checked; the DRAM may opt to block the DRAM controller from writing a one to the Parity Error Status bit.

DDR4 SDRAM supports Persistent Parity Error Mode. This mode is enabled by setting MR5[9] = 1; and when enabled, CA Parity resumes checking after the $\overline{\text{ALERT}}$ is de-asserted, even if Parity Error Status bit remains a one. If multiple errors occur before the Error Status bit is cleared the Error log in MPR Page 1 should be treated as 'Don't Care'. In Persistent Parity Error Mode the $\overline{\text{ALERT}}$ pulse will be asserted and de-asserted by the DRAM as defined with the min. and max. value tPAR_ALERT_PW. The DRAM controller must issue DESELECT commands once it detects the $\overline{\text{ALERT}}$ signal, this response time is defined as tPAR_ALERT_RSP.The following figures capture the flow of events on the C/A bus and the $\overline{\text{ALERT}}$ signal.

Mode Register Setting for C/A Parity

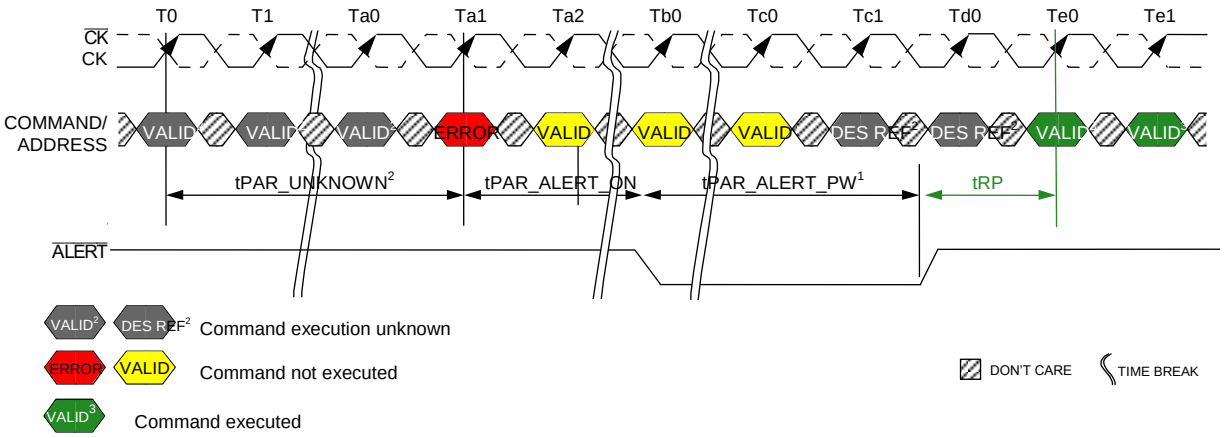
C/A Parity Latency MR5[2:0][1]	Speed bins	C/A Parity Error Status MR5[4]	Parity Persistent Mode MR5 [9]	Errant C/A Frame
000= Disabled	NA	0=clear	0 = Disabled	$\overline{ACT}$, PAR, BG1, BG0, BA0, BA1, A16/$\overline{RAS}$, A15/$\overline{CAS}$, A14/$\overline{WE}$, A[17,13:0]
001= 4 Clocks	2133			
010= 5 Clocks	2400	1=Error	1 = Enabled	
011= 6 Clocks	RFU			
100= 8 Clocks	RFU			

NOTE 1 Parity latency is applied to all commands.

NOTE 2 Parity latency can be changed only from a CA parity disabled state; for example, a direct change from PL = 3 to PL = 4 is not allowed. The correct sequence is PL = 3 to disabled to PL = 4.

NOTE 3 Parity Latency is applied to write and read latency. Write Latency = AL+CWL+PL. Read Latency = AL+CL+PL.

Command/Address Parity During Normal Operation

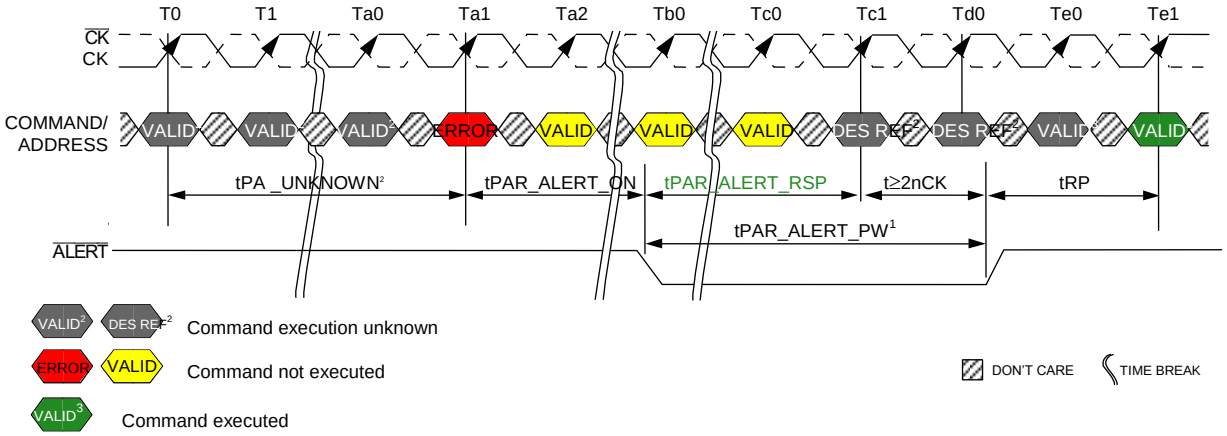


NOTE 1 DRAM is emptying queues. Precharge all and parity checking off until Parity Error Status bit cleared.

NOTE 2 Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 3 Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Parity checking off until Parity Error Status bit cleared.

Persistent CA Parity Error Checking Operation

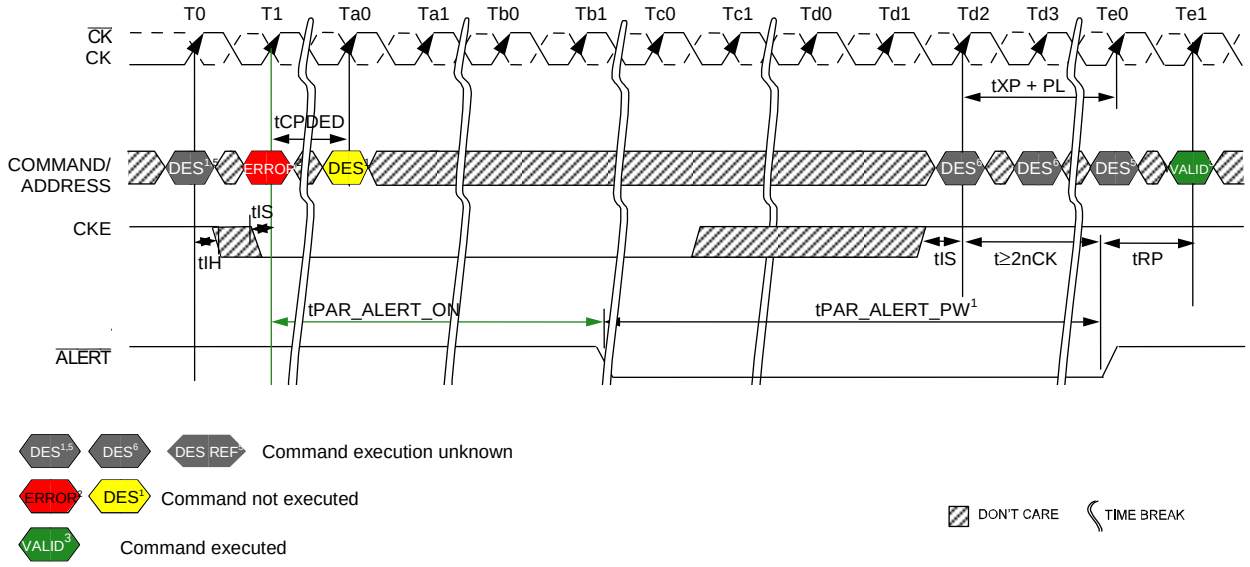


NOTE 1 DRAM is emptying queues. Precharge all and parity check re-enable finished by tPAR_ALERT_PW.

NOTE 2 Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 3 Normal operation with parity latency and parity checking (CA Parity Persistent Error Mode enabled).

CA Parity Error Checking - SRE Attempt



NOTE 1 Deselect command only allowed.

NOTE 2 Self Refresh command error. DRAM masks the intended SRE command and enters Precharge Power Down.

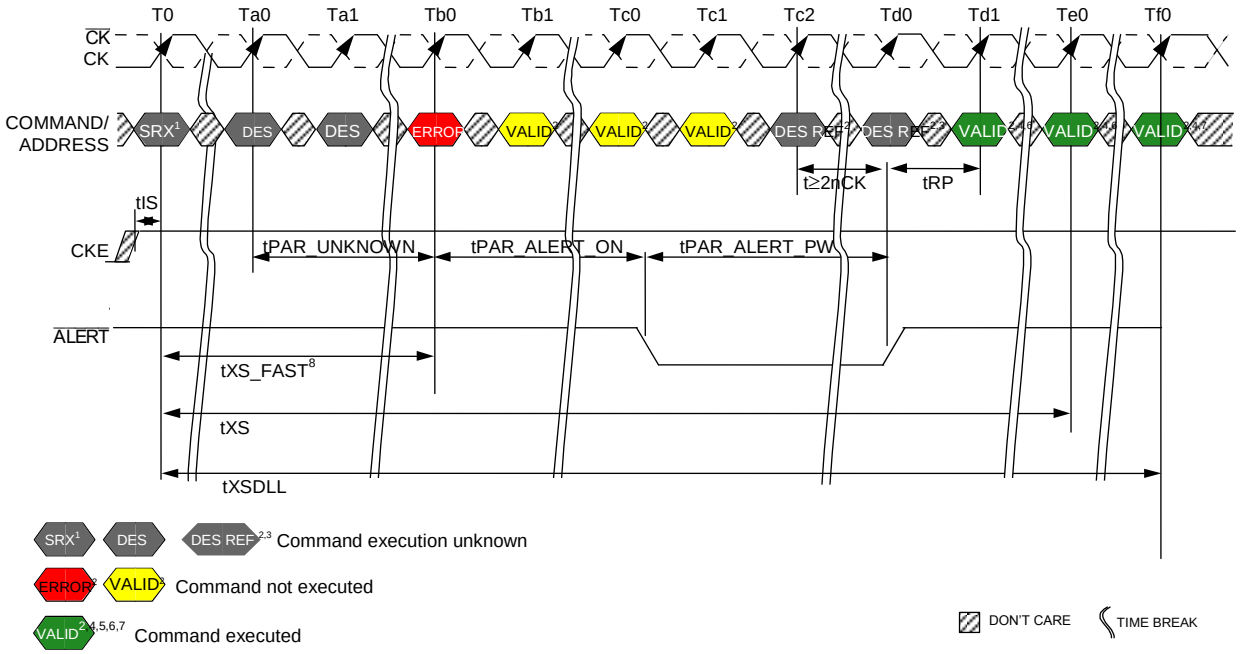
NOTE 3 Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Parity checking is off until Parity Error Status bit cleared.

NOTE 4 Controller cannot disable clock until it has been able to have detected a possible C/A Parity error.

NOTE 5 Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 6 Deselect command only allowed; CKE may go high prior to Tc2 as long as DES commands are issued.

CA Parity Error Checking - SRX Attempt



NOTE 1 Self Refresh Abort = Disable: MR4 [9] = 0.

NOTE 2 Input commands are bounded by tXSDLL, tXS, tXS_ABORT and tXS_FAST timing.

NOTE 3 Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 4 Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Parity checking off until Parity Error Status bit cleared.

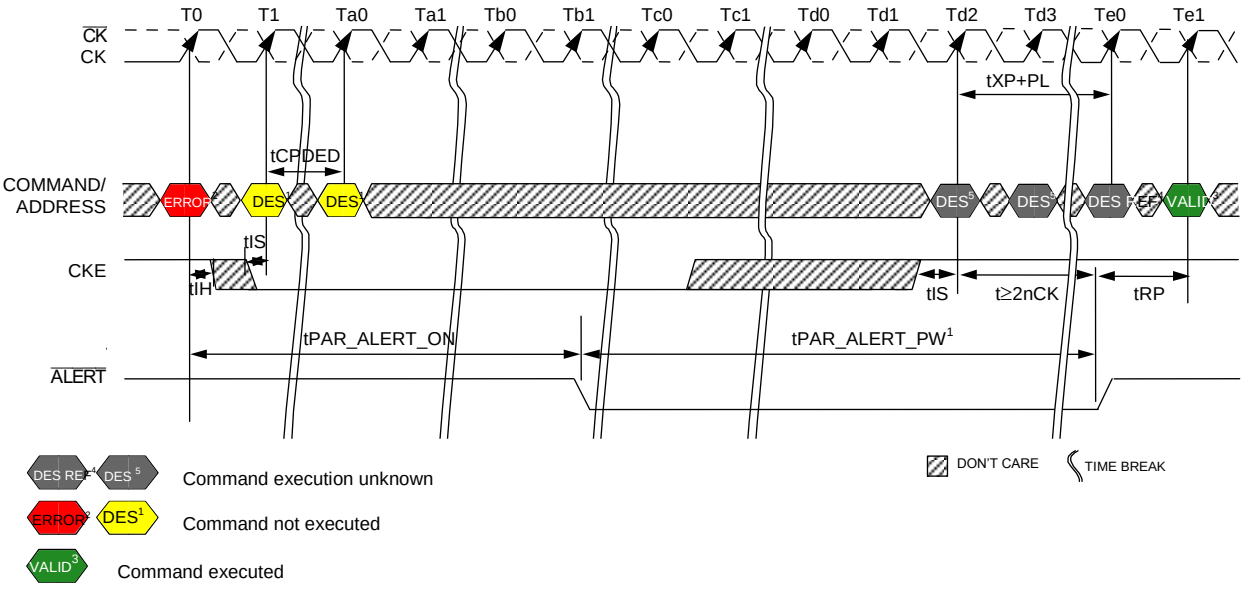
NOTE 5 Only MRS (limited to those described in the Self-Refresh Operation section), ZQCS, or ZQCL command allowed

NOTE 6 Valid commands not requiring a locked DLL.

NOTE 7 Valid commands requiring a locked DLL.

NOTE 8 This figure shows the case from which the error occurred after tXS_FAST. An error may also occur after tXS_ABORT and tXS.

CA Parity Error Checking - PDE/PDX



NOTE 1 Deselect command only allowed.

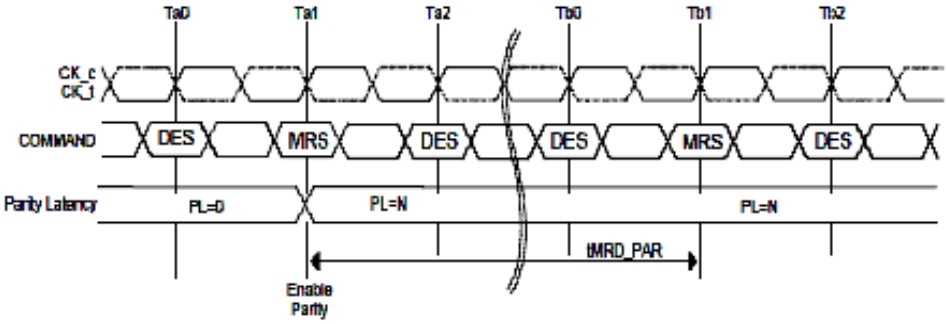
NOTE 2 Error could be Precharge or Activate.

NOTE 3 Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Parity checking is off until Parity Error Status bit cleared.

NOTE 4 Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.

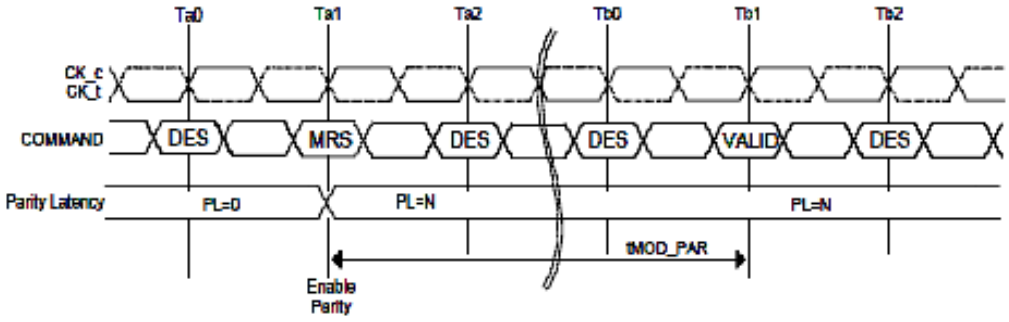
NOTE 5 Deselect command only allowed; CKE may go high prior to Td2 as long as DES commands are issued.

Parity Entry Timing Example - tMRD_PAR



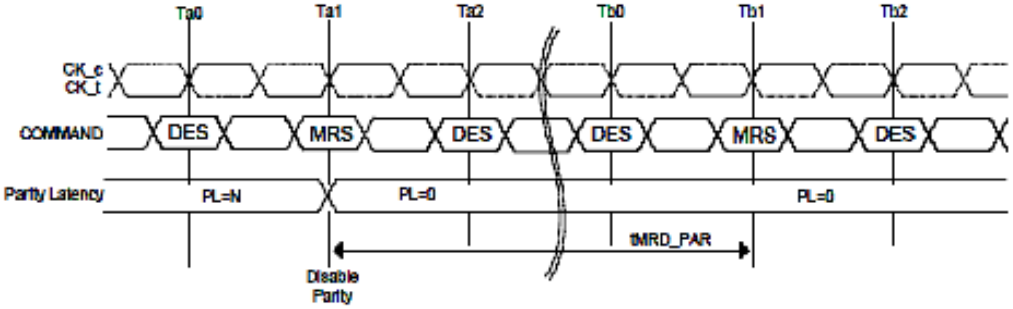
NOTE 1 tMRD_PAR = tMOD + N; where N is the programmed parity latency.

Parity Entry Timing Example - tMOD_PAR



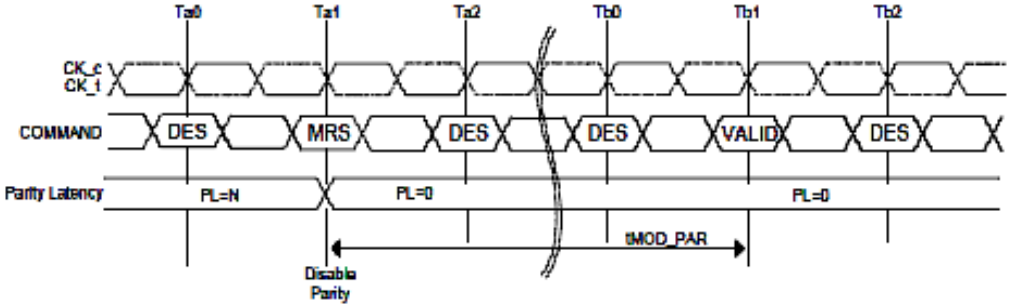
NOTE 1 tMOD_PAR = tMOD + N; where N is the programmed parity latency.

Parity Exit Timing Example - tMRD_PAR



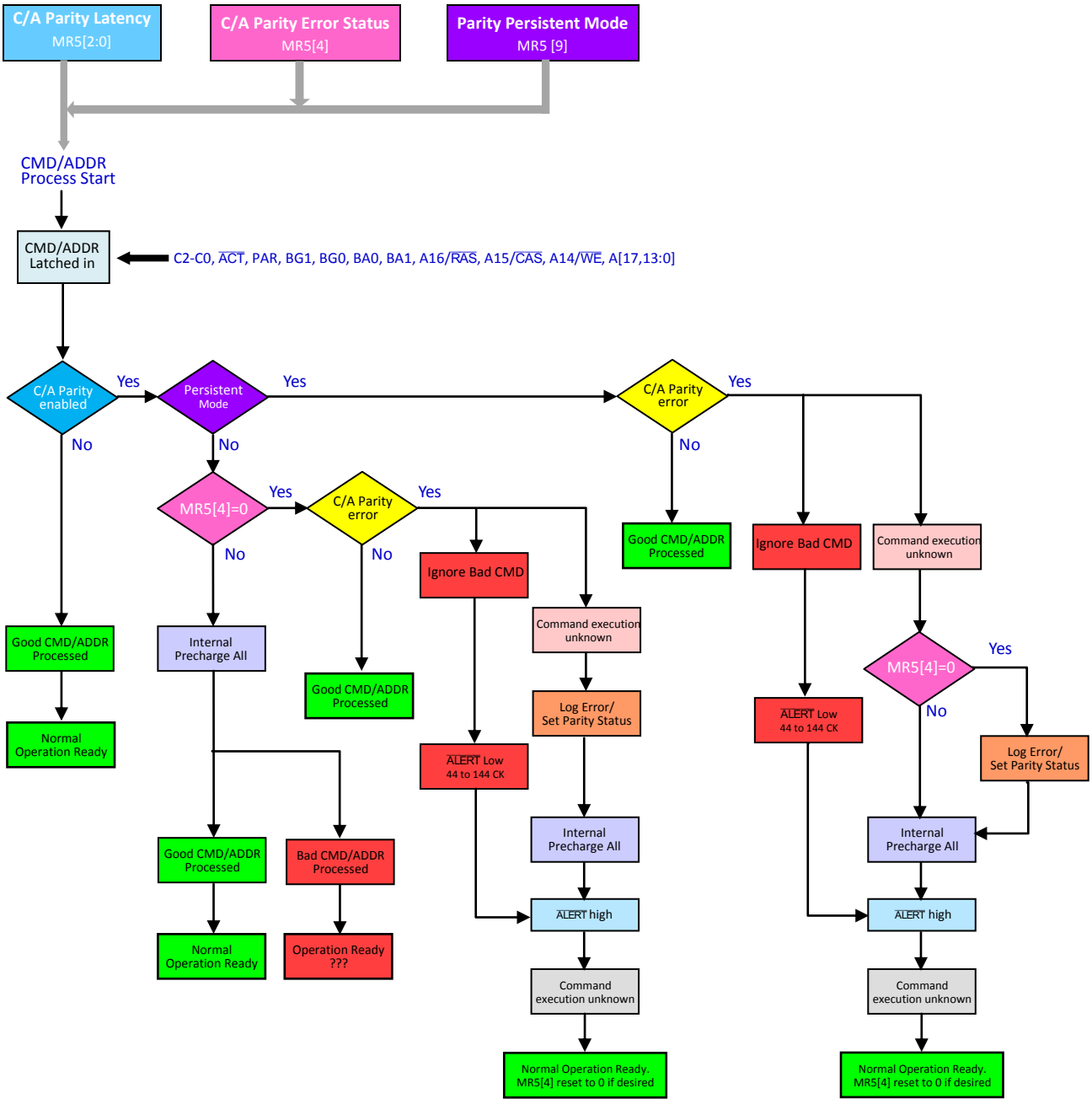
NOTE 1 tMRD_PAR = tMOD + N; where N is the programmed parity latency.

Parity Exit Timing Example - tMOD_PAR



NOTE 1 tMOD_PAR = tMOD + N; where N is the programmed parity latency.

CA Parity Flow



Per-DRAM Addressability (PDA Mode)

DDR4 allows programmability of a single, specific DRAM on a rank. As an example, this feature can be used to program different ODT or VREF values on each DRAM on a given rank. Since PDA mode may be used to program optimal Vref for the DRAM, the data set up for first DQ0 transfer or the hold time for the last DQ0 transfer cannot be guaranteed.

The DRAM may sample DQ0 on either the first falling or second rising DQS transfer edge. This supports a common implementation between BC4 and BL8 modes on the DRAM. The DRAM controller is required to drive DQ0 to a 'Stable Low or High' during the length of the data transfer for BC4 and BL8 cases.

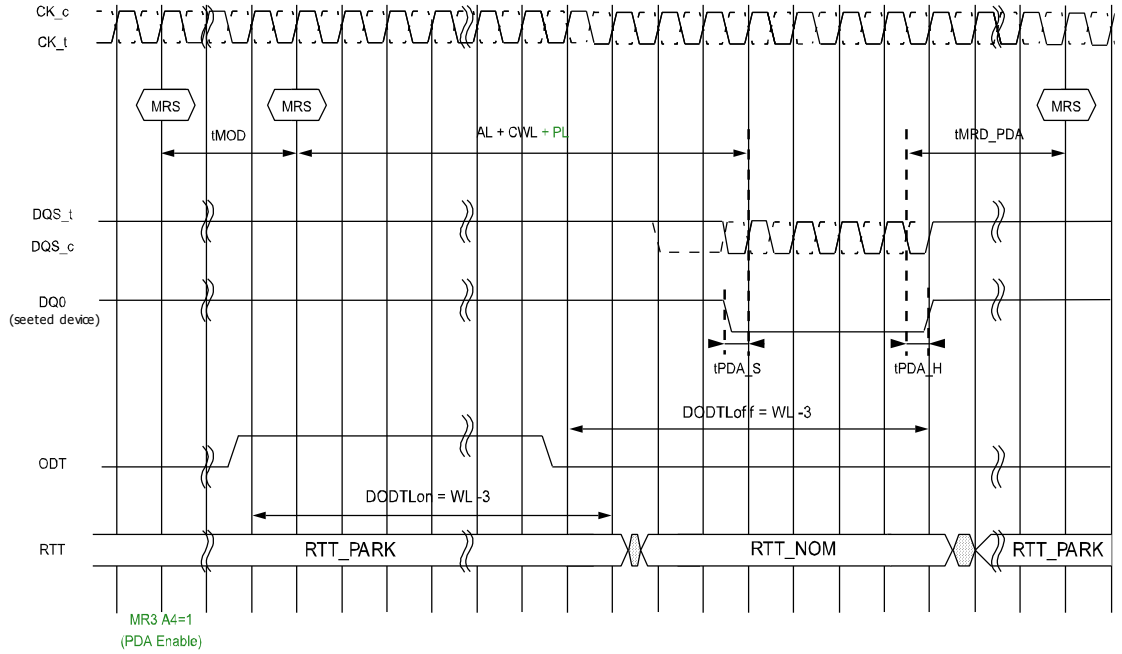
1. Before entering Per-DRAM addressability mode, write leveling is required.
   - BL8 or BC4 may be used.
2. Before entering per-DRAM addressability mode, the following MR settings are possible:
   - RTT_PARK MR5 A[8:6] = Enabled
   - RTT_NOM MR1 A[9, 6, 2] = Enabled
3. Enable per-DRAM addressability mode using MR3 [4] = 1. (The default programmed value of MR3[4] = 0 .)
4. In the per-DRAM addressability mode, all MRS commands are qualified with DQ0. The device captures DQ0 by using DQS and $\overline{DQS}$ signals. If the value on DQ0 is low, the DRAM executes the MRS command. If the value on DQ0 is high, the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits.
5. Program the desired DRAM and mode registers using the MRS command and DQ0.
6. In per-DRAM addressability mode, only MRS commands are allowed.
7. The MODE REGISTER SET command cycle time in per-DRAM addressability mode, AL + CWL + 3.5nCK + tMRD_PDA is required to complete the WRITE operation to the mode register and is the minimum time required between two MRS commands.
8. Remove the device from per-DRAM addressability mode by setting MR3[4] = 0. (This command requires DQ0 = 0.)

NOTE: Removing the device from per-DRAM addressability mode will require programming the entire MR3 when the MRS command is issued. This may impact some per-DRAM addressability values programmed within a rank as the EXIT command is sent to the rank. In order to avoid such a case, the PDA Enable/Disable Control bit is located in a mode register that does not have any Per-DRAM addressability mode controls.

In per-DRAM addressability mode, the device captures DQ0 using DQS and $\overline{DQS}$ like normal WRITE operation; however, dynamic ODT is not supported. Extra care is required for the ODT setting. If RTT_NOM MR1 [10:8] = Enable, DDR4 SDRAM data termination needs to be controlled by the ODT pin and applies the same timing parameters as defined in direct ODT function that is shown below.

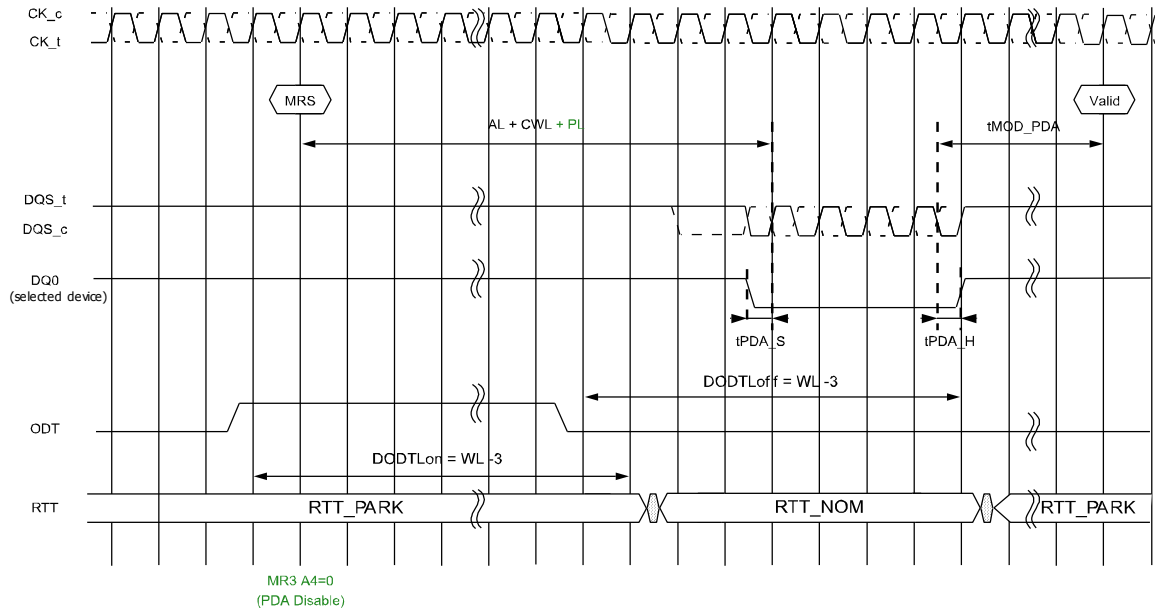
Symbol	Parameter
DODTLon	Direct ODT turn on latency
DODTLoff	Direct ODT turn off latency
tADC	RTT change timing skew
tAONAS	Asynchronous RTT_NOM turn-on delay
tAOFAS	Asynchronous RTT_NOM turn-off delay

PDA Operation Enabled, BL8



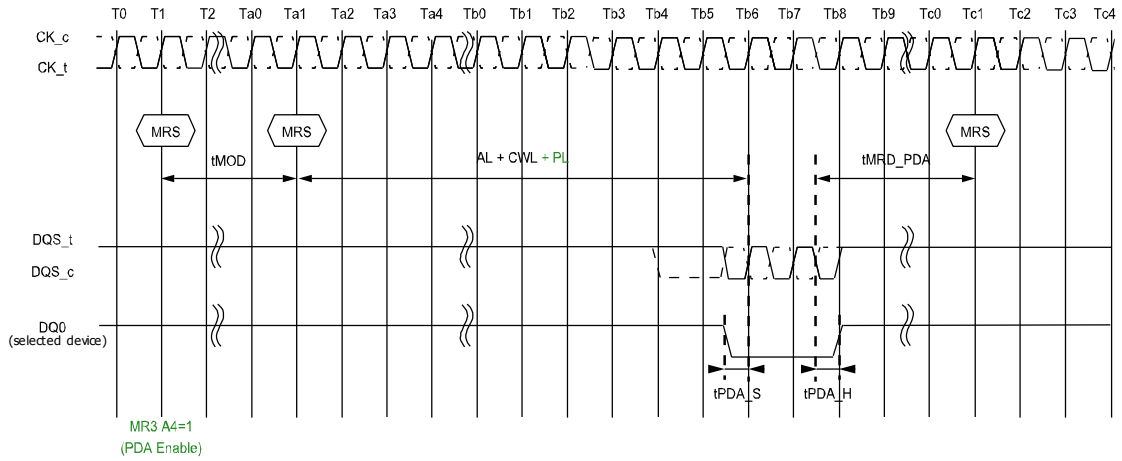
NOTE 1 RTT_PARK = Enable, RTT_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON, CA parity is used

MRS w/ per DRAM addressability (PDA) Exit



NOTE 1 RTT_PARK = Enable; RTT_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON.

PDA using Burst Chop 4

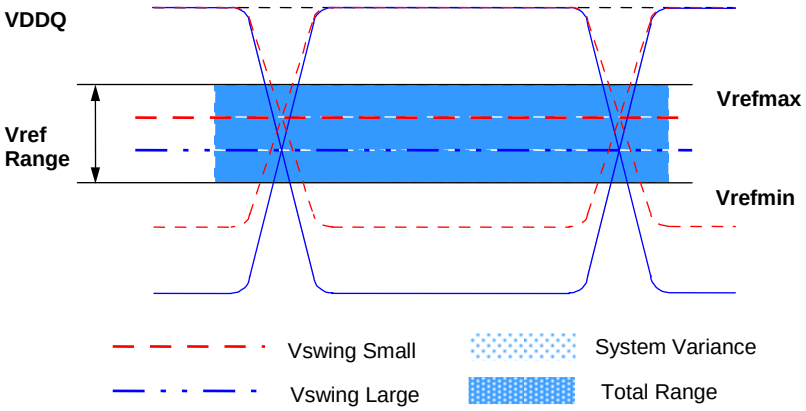


VREFDQ Training

The data bus is terminated to VDDQ so that the Vref level will change based on drive strength and loading. Therefore VrefDQ is not any more supplied externally, but VrefDQ is generated internally in the DRAM. The DRAM VREFDQ does not have a default value upon power-up and must be set to the desired value, usually via VREFDQ training. The DDR4 DRAM memory controller is responsible for VREFDQ calibration to determine the best internal VREFDQ level. The VREFDQ calibration is enabled/disabled via MR6 [7], MR6 [6] selects Range 1 (60% to 92.5% of VDDQ) or Range 2 (45% to 77.5% of VDDQ), and an MRS protocol using MR6 [5:0] to adjust up and adjust down the VREFDQ level. MR6 [6:0] bits can be altered via MR command set if MR6 [7] is disabled. The DRAM controller will likely use a series of Writes and Reads in conduction with VREFDQ adjustments to obtain the best VREFDQ which in turn optimizes the data eye.

DDR4 SDRAM internal VREFDQ specification parameters: voltage range, step-size, VREF step time, VREF full step time, and VREF valid level. The voltage operating range specifies the minimum required VREF setting range for DDR4 DRAM devices. The minimum range is defined by VREFDQ,min and VREFDQ,max. As noted, a calibration sequence, determined by the DRAM controller, should be performed to adjust VREFDQ and optimize the timing and voltage margin of the DRAM data input receivers.

VREFDQ Voltage Range



VREFDQ Range and Levels

A[5:0]	Range 1 (A6=0)	Range 2 (A6=1)	A[5:0]	Range 1 (A6=0)	Range 2 (A6=1)	A[5:0]	Range 1 (A6=0)	Range 2 (A6=1)	A[5:0]	Range 1 (A6=0)	Range 2 (A6=1)
00 0000	60.00%	45.00%	00 1101	68.45%	53.45%	01 1010	76.90%	61.90%	10 0111	85.35%	70.35%
00 0001	60.65%	45.65%	00 1110	69.10%	54.10%	01 1011	77.55%	62.55%	10 1000	86.00%	71.00%
00 0010	61.30%	46.30%	00 1111	69.75%	54.75%	01 1100	78.20%	63.20%	10 1001	86.65%	71.65%
00 0011	61.95%	46.95%	01 0000	70.40%	55.40%	01 1101	78.85%	63.85%	10 1010	87.30%	72.30%
00 0100	62.60%	47.60%	01 0001	71.05%	56.05%	01 1110	79.50%	64.50%	10 1011	87.95%	72.95%
00 0101	63.25%	48.25%	01 0010	71.70%	56.70%	01 1111	80.15%	65.15%	10 1100	88.60%	73.60%
00 0110	63.90%	48.90%	01 0011	72.35%	57.35%	10 0000	80.80%	65.80%	10 1101	89.25%	74.25%
00 0111	64.55%	49.55%	01 0100	73.00%	58.00%	10 0001	81.45%	66.45%	10 1110	89.90%	74.90%
00 1000	65.20%	50.20%	01 0101	73.65%	58.65%	10 0010	82.10%	67.10%	10 1111	90.55%	75.55%
00 1001	65.85%	50.85%	01 0110	74.30%	59.30%	10 0011	82.75%	67.75%	11 0000	91.20%	76.20%
00 1010	66.50%	51.50%	01 0111	74.95%	59.95%	10 0100	83.40%	68.40%	11 0001	91.85%	76.85%
00 1011	67.15%	52.15%	01 1000	75.60%	60.60%	10 0101	84.05%	69.05%	11 0010	92.50%	77.50%
00 1100	67.80%	52.80%	01 1001	76.25%	61.25%	10 0110	84.70%	69.70%	11 0011 to 111111	Reserved	Reserved

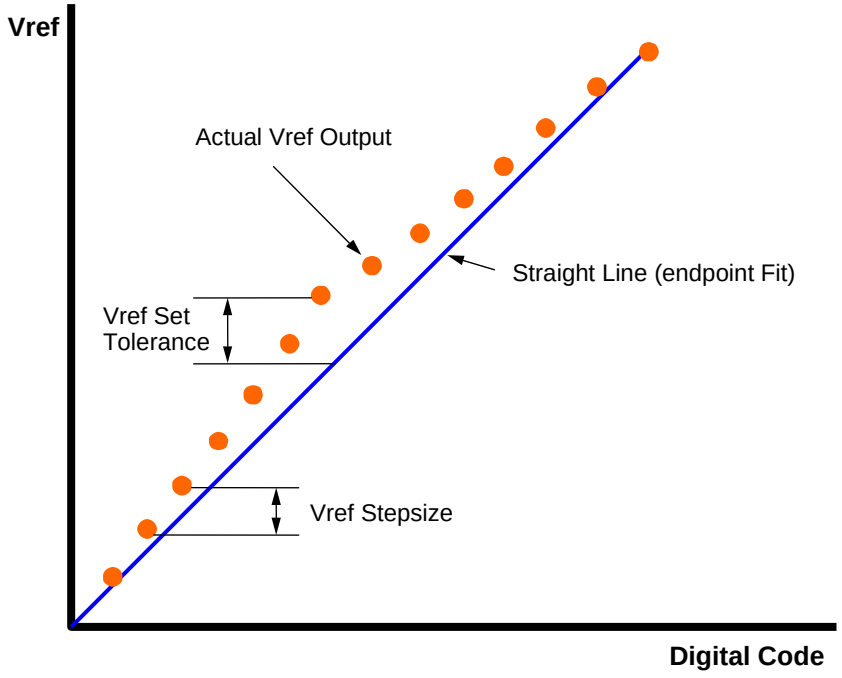
VREFDQ Step Size

The VREF step size is defined as the step size between adjacent steps. VREF step size ranges from 0.5% VDDQ to 0.8% VDDQ. However, for a given design, DRAM has one value for VREF step size that falls within the range.

The VREF set tolerance is the variation in the VREF voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for VREF set tolerance uncertainty. The range of VREF set tolerance uncertainty is a function of number of steps *n*.

The VREF set tolerance is measured with respect to the ideal line which is based on the two endpoints where the endpoints are at the MIN and MAX VREF values for a specified range.

Example of VREF Set Tolerance and Step Size



VREFDQ Increment and Decrement Timing

The V_{REF} increment/decrement step times are define by $V_{REF\_time\text{-}short}$ and $V_{REF\_time\text{-}long}$. $V_{REF\_time\text{-}short}$ and $V_{REF\_time\text{-}long}$ are defined from t0 to t1, where t1 is referenced to the V_{REF} voltage at the final DC level within the V_{REF} valid tolerance ($V_{REF\_val\_tol}$). The V_{REF} valid level is defined by V_{REF_val} tolerance to qualify the step time t1. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment. $V_{REF\_time\text{-}short}$ is for a single stepsize increment/decrement change in V_{REF} voltage. $V_{REF\_time\text{-}long}$ is the time including up to $V_{REF,min}$ to $V_{REF,max}$ or $V_{REF,max}$ to $V_{REF,min}$ change in V_{REF} voltage.

Note:

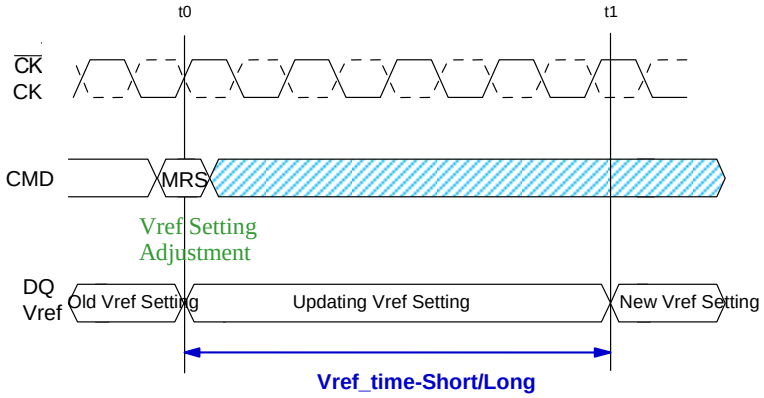
t0 - is referenced to the MRS command clock

t1 - is referenced to V_{REF_tol}

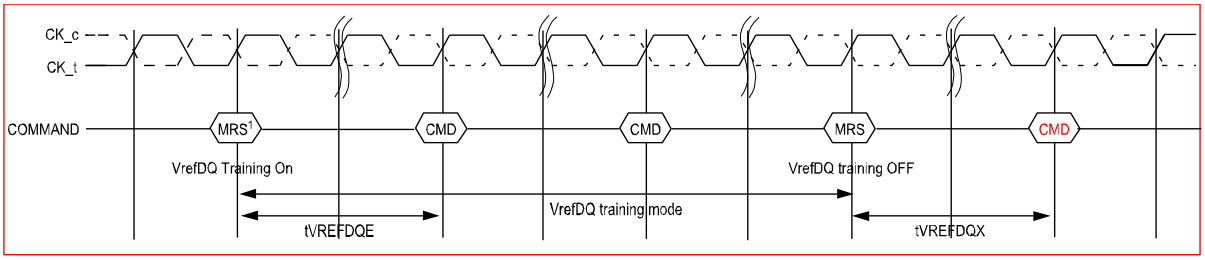
VREFDQ Short and Long Timing Diagram for VREF_time Parameter

An MRS command to the mode register MR6[5:0] is used to program the VREF value. The minimum time required between two VREF MRS commands is VREF_time-short for single step and VREF_time-long for a full voltage range step. VREFDQ training mode is enabled or disabled by MR6[7] and training range is selected by MR6[6]. When VREFDQ training mode is entered or exited, the parameters tVREFDQE and tVREFDQX need to be satisfied inorder to prevent excessive current consumption as well as provide stable operation.

Vref_time for short and long timing diagram



VREFDQ Training Mode Entry and Exit Timing Diagram

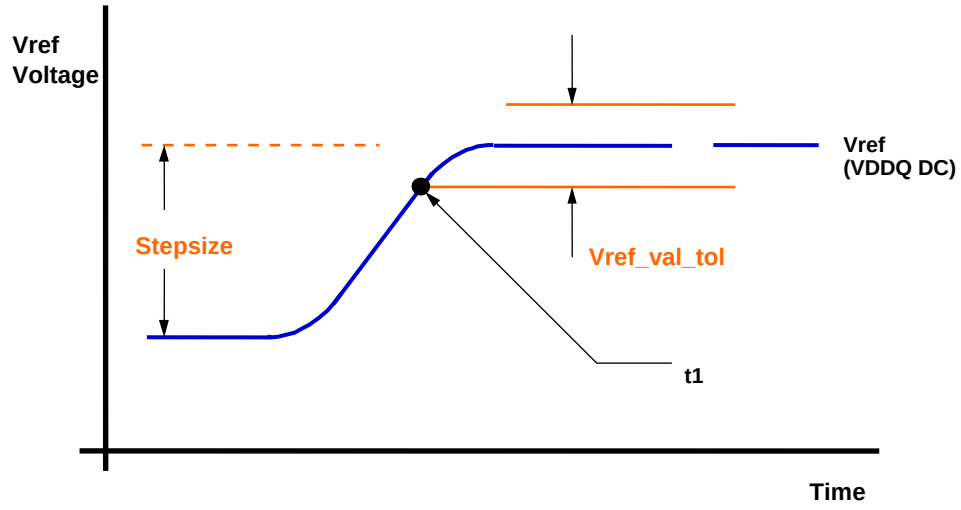


NOTE 1 New VREFDQ value is not allowed with MRS command during training mode exit.

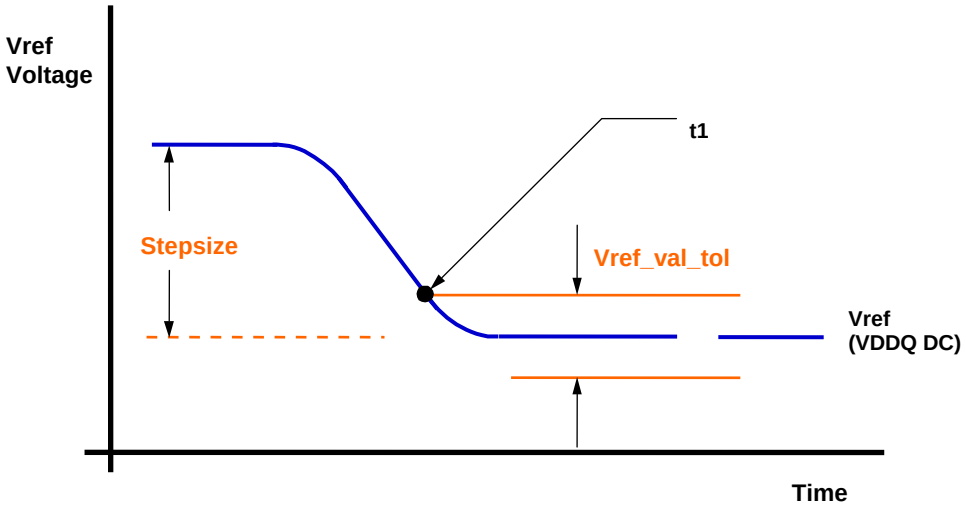
NOTE 2 Depending on the step size of the latest programmed VREF value, Vref_time_short or Vref_time_long must be satisfied before disabling VrefDQ training mode.

Speed		DDR4-2133,2400,2666,3200		Units	NOTE
Parameter	Symbol	Min	Max		
VrefDQ training					
Enter VrefDQ training mode to the first valid command delay	**tVREFDQE**	150	–	ns	
Exit VrefDQ training mode to the first valid command delay	**tVREFDQX**	150	–	ns	

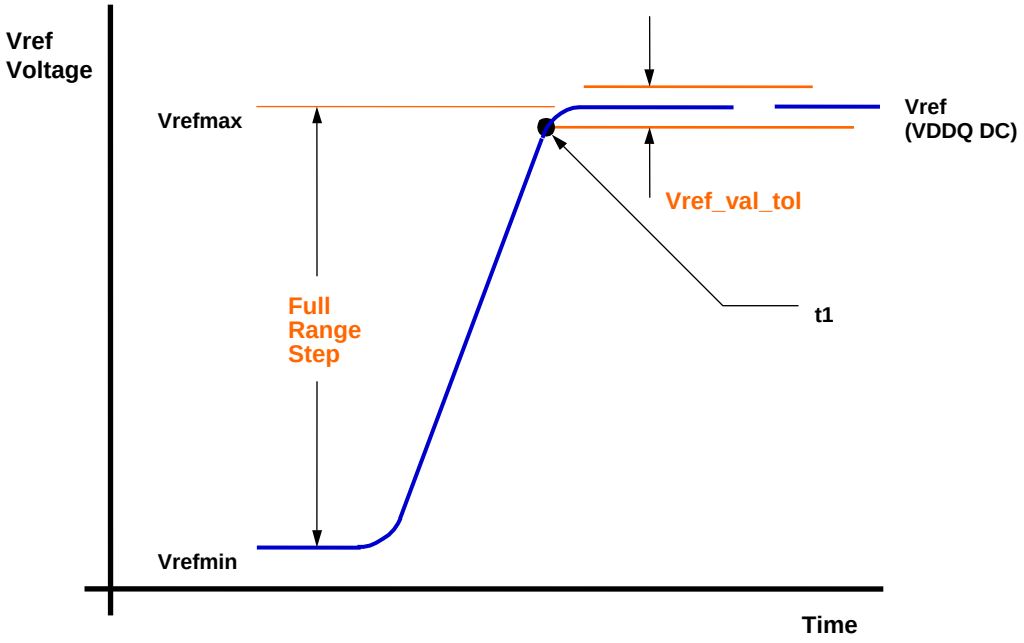
VREF Step Single Step Size Increment Case



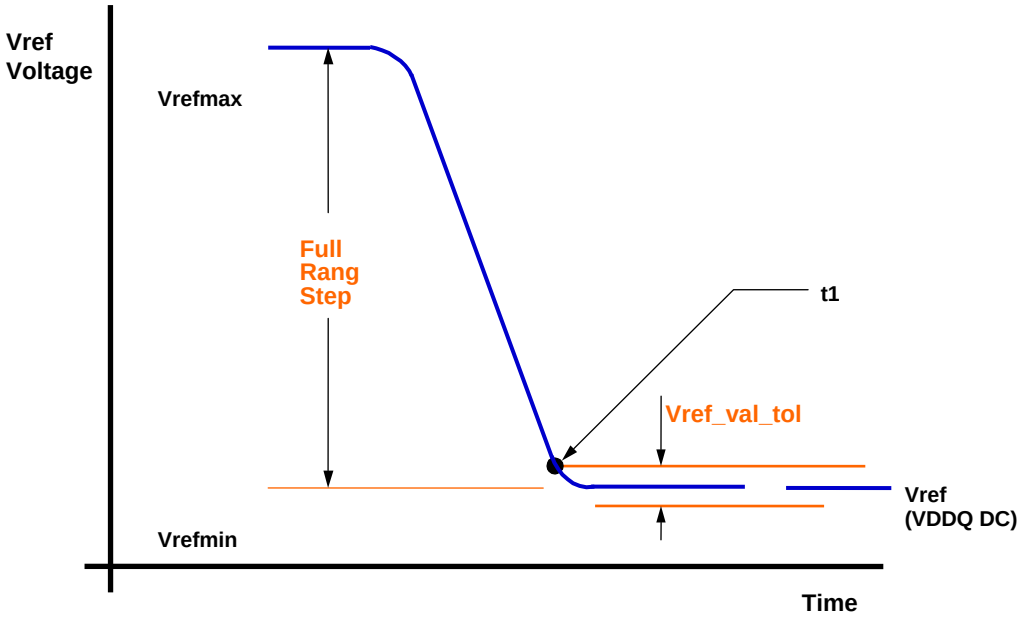
VREF Step Single Step Size Decrement Case



VREF Full Step From VREF,min to VREF,maxCase



VREF Full Step From VREF,max to VREF,minCase



VREFDQ Supply and Calibration Ranges

The DDR4 SDRAM internally generates its own V_{REFDQ}. DRAM internal V_{REFDQ} specification parameters: voltage range, step-size, V_{REF} step time, V_{REF} full step time, and V_{REF} valid level. The voltage operating range specifies the minimum required V_{REF} setting range for DDR4 DRAM devices. The minimum range is defined by $V_{REFDQ,min}$ and $V_{REFDQ,max}$. A calibration sequence should be performed by the DRAM controller to adjust V_{REFDQ} and optimize the timing and voltage margin of the DRAM data input receivers.

VREFDQ Specification

Symbol	Prarmeter	Min	Typ	Max	Unit	NOTE
VrefDQ R1	Range 1 VrefDQ operating points	60%	–	92%	VDDQ	1, 11
VrefDQ R2	Range 2 VrefDQ operating points	45%	–	77%	VDDQ	1, 11
Vref step	Vref Stepsize	0.50%	0.65%	0.80%	VDDQ	2
Vref_set_tol	Vref Set Tolerance	-1.625%	0.00%	1.625%	VDDQ	3, 4, 6
		-0.15%	0.00%	0.15%	VDDQ	3, 5, 7
Vref_time-Short	Vref Step Time	–	–	60	ns	8, 12
Vref_time-Long		–	–	150	ns	9,12
Vref_val_tol	Vref Valid tolerance	-0.15%	0.00%	0.15%	VDDQ	10

NOTE 1 VREF(DC) voltage is referenced to VDDQ(DC). VDDQ(DC) is 1.2V.

NOTE 2 VREF step size increment/decrement range. VREF at DC level.

NOTE 3 VREF_new = VREF_old ± n × VREF_step; n = number of steps. If increment, use “+;” if decrement,use “-.”

NOTE 4 For n >4, the minimum value of VREF setting tolerance = VREF_new - 1.625% × VDDQ. The maximum value of VREF setting tolerance = VREF_new + 1.625% × VDDQ.

NOTE 5 For n ≤4, the minimum value of VREF setting tolerance = VREF_new - 0.15% × VDDQ. The maximum value of VREF setting tolerance = VREF_new + 0.15% × VDDQ.

NOTE 6 Measured by recording the MIN and MAX values of the VREF output over the range,drawing a straight line between those points, and comparing all other VREF output settings to that line.

NOTE 7 Measured by recording the MIN and MAX values of the VREF output across four consecutive steps (n = 4), drawing a straight line between those points, and comparing al VREF output settings to that line.

NOTE 8 Time from MRS command to increment or decrement one step size for VREF.

NOTE 9 Time from MRS command to increment or decrement more than one step size up to the full range of VREF.

NOTE 10 Only applicable for DRAM component-level test/characterization purposes. Not applicable for normal mode of operation. VREF valid qualifies the step times, which will be characterized at the component level.

NOTE 11 DRAM range 1 or range 2 is set by the MRS6[6]6.

NOTE 12 If the Vref monitor is enabled, Vref_time-long and Vref_time-short must be derated by: +10ns if DQ bus load is 0pF and an additional +15ns/pF of DQ bus loading.

VREFDQ Ranges

MR6 [6] selects Range 1 (60% to 92.5% of V_{DDQ}) or Range 2 (45% to 77.5% of V_{DDQ}), and MR6 [5:0] sets the V_{REFDQ} level, as listed in the table below. The values in MR6 [6:0] will update the V_{DDQ} Range and level independent of MR6 [7] setting. It is recommended MR6 [7] be enabled when changing the settings in MR6 [6:0] and it is highly recommended MR6 [7] be enabled when changing the settings in MR6 [6:0] multiple times during a calibration routine.

VREFDQ Range and Levels

MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)	MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)	MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)	MR6 [5:0]	Range 1 (MR6[6]=0)	Range 2 (MR6[6]=1)
00 0000	60.00%	45.00%	00 1101	68.45%	53.45%	01 1010	76.90%	61.90%	10 0111	85.35%	70.35%
00 0001	60.65%	45.65%	00 1110	69.10%	54.10%	01 1011	77.55%	62.55%	10 1000	86.00%	71.00%
00 0010	61.30%	46.30%	00 1111	69.75%	54.75%	01 1100	78.20%	63.20%	10 1001	86.65%	71.65%
00 0011	61.95%	46.95%	01 0000	70.40%	55.40%	01 1101	78.85%	63.85%	10 1010	87.30%	72.30%
00 0100	62.60%	47.60%	01 0001	71.05%	56.05%	01 1110	79.50%	64.50%	10 1011	87.95%	72.95%
00 0101	63.25%	48.25%	01 0010	71.70%	56.70%	01 1111	80.15%	65.15%	10 1100	88.60%	73.60%
00 0110	63.90%	48.90%	01 0011	72.35%	57.35%	10 0000	80.80%	65.80%	10 1101	89.25%	74.25%
00 0111	64.55%	49.55%	01 0100	73.00%	58.00%	10 0001	81.45%	66.45%	10 1110	89.90%	74.90%
00 1000	65.20%	50.20%	01 0101	73.65%	58.65%	10 0010	82.10%	67.10%	10 1111	90.55%	75.55%
00 1001	65.85%	50.85%	01 0110	74.30%	59.30%	10 0011	82.75%	67.75%	11 0000	91.20%	76.20%
00 1010	66.50%	51.50%	01 0111	74.95%	59.95%	10 0100	83.40%	68.40%	11 0001	91.85%	76.85%
00 1011	67.15%	52.15%	01 1000	75.60%	60.60%	10 0101	84.05%	69.05%	11 0010	92.50%	77.50%
00 1100	67.80%	52.80%	01 1001	76.25%	61.25%	10 0110	84.70%	69.70%	11 0011 to 111111	Reserved	Reserved

Connectivity Test Mode (CT)

Connectivity Test (CT) mode is similar to boundary scan testing but is designed to significantly speed up testing of electrical continuity of pin interconnections on the PC boards between the DDR4 and the memory controller. Designed to work seamlessly with any boundary scan device, CT mode is supported in x16 DDR4 SDRAMs.

When TEN pin asserted HIGH, this causes the device to enter the CT mode. In CT mode, the normal memory function inside the device is bypassed and the I/O pins appear as a set of test input and output pins to the external controlling agent. The TEN pin is dedicated to the connectivity check function and will not be used during normal device operation.

Contrary to other conventional shift register-based test modes, where test patterns are shifted in and out of the memory devices serially during each clock, the DDR4 CT mode allows test patterns to be entered on the test input pins in parallel and the test results to be extracted from the test output pins of the device in parallel at the same time, significantly increasing the speed of the connectivity check. When placed in CT mode, the device appears as an asynchronous device to the external controlling agent. After the input test pattern is applied, the connectivity test results are available for extraction in parallel at the test output pins after a fixed propagation delay time.

Note: A reset of the device is required after exiting CT mode (see RESET and Initialization Procedure).

Boundary Scan Mode Pin Map and Switching Levels

Only digital pins can be tested via the CT mode. For the purposes of a connectivity check, all the pins used for digital logic in the DDR4 memory device are classified as one of the following 5 types:

Types	CT Mode Pins		Pin Names during Normal Memory Operation	Switching Level
1	Test Enable		TEN [1,5]	CMOS (20% / 80% VDD)
2	Chip Select		$\overline{CS}$ [7]	VREFCA ± 200mV
3	Test Input[8]	A	BA[1:0], BG[1:0], A[9:0], A10/AP, A11, A12/$\overline{BC}$, A13, $\overline{WE}$/A14, $\overline{CAS}$/A15, $\overline{RAS}$/A16, CKE, $\overline{ACT}$, ODT, CK, $\overline{CK}$, PAR	VREFCA ± 200mV
		B	$\overline{LDM}$/$\overline{LDBI}$, $\overline{UDM}$/$\overline{UDBI}$, $\overline{DM}$/$\overline{DBI}$	VREFDQ ± 200mV
		C	$\overline{ALERT}$ [1,6]	CMOS (20% / 80% VDD)
4		D	$\overline{RESET}$ [1,10]	CMOS (20% / 80% VDD)
5	Test Output[9]		DQ[15:0], DQSU, $\overline{DQSU}$, DQSL, $\overline{DQSL}$, DQS, $\overline{DQS}$	VTT ± 100mV

NOTE 1 CMOS is rail-to-rail signal with DC high at 80% and DC low at 20% of VDD, i.e, 960mV for DC high and 240mV for DC low.

NOTE 2 VREFCA should be at VDD/2.

NOTE 3 VREFDQ should be at VDDQ/2.

NOTE 4 VTT should be set to VDD/2.

NOTE 5 Connectivity Test Mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation.

NOTE 6 $\overline{ALERT}$ switching level is not a final setting.

NOTE 7 When asserted LOW, this pin enables the test output pins in the DDR4 memory device. When de-asserted, the output pins in the DDR4 memory device will be High-Z. The $\overline{CS}$ pin in the device serves as the $\overline{CS}$ pin in CT mode.

NOTE 8 A group of pins used during normal DDR4 DRAM operation designated as test input pins. These pins are used to enter the test pattern in CT mode.

NOTE 9 A group of pins used during normal DDR4 DRAM operation designated as test output pins. These pins are used for extraction of the connectivity test results in CT mode.

NOTE 10 Fixed high level is required during CT mode, same as normal function.

Min Terms Definition for Logic Equations

Min Term Equations

MTx is an inernal signal to be used to generate the signal to drive the output signals..

MT0 = XOR (A1, A6, PAR)

MT1 = XOR (A8, $\overline{\text{ALERT}}$, A9)

MT2 = XOR (A2, A5, A13)

MT3 = XOR (A0 A7, A11)

MT4 = XOR ($\overline{\text{CK}}$, ODT, $\overline{\text{CAS}}$/A15)

MT5 = XOR (CKE, $\overline{\text{RAS}}$/A16, A10/AP)

MT6 = XOR ($\overline{\text{ACT}}$, A4, BA1)

MT7 = XOR (($\overline{\text{UDM}}$ / $\overline{\text{UDBI}}$), ($\overline{\text{LDM}}$ / $\overline{\text{LDBI}}$), CK)

MT8 = XOR ($\overline{\text{WE}}$ / A14, A12 / BC, BA0)

MT9 = XOR (BG0, A3, ($\overline{\text{RESET}}$ and TEN))

Output equations for x16 devices

DQ0 = MT0

DQ1 = !DQ0

DQ2 = MT1

DQ3 = !DQ2

DQ4 = MT2

DQ5 = !DQ4

DQ6 = MT3

DQ7 = !DQ6

DQ8 = MT4

DQ9 = !DQ8

DQ10 = MT5

DQ11 = !DQ10

DQ12 = MT6

DQ13 = MT7

DQ14 = MT8

DQ15 = !DQ14

DQSL = MT9

$\overline{\text{DQSL}}$ = !DQ12

DQSU = !DQSL

$\overline{\text{DQSU}}$ = !DQ13

CT Input Timing Requirements

During CT Mode, input levels are defined below.

1. TEN pin : CMOS rail-to-rail with DC high and low at 80% and 20% of VDD.
2. $\overline{CS}$: Pseudo differential signal referring to VrefCA
3. Test Input pin A : Pseudo differential signal referring to VrefCA
4. Test Input pin B : Pseudo differential signal referring to internal Vref 0.5*VDD
5. $\overline{RESET}$: CMOS DC high above 70 % VDD
6. $\overline{ALERT}$: Terminated to VDD. Swing level is TBD.

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

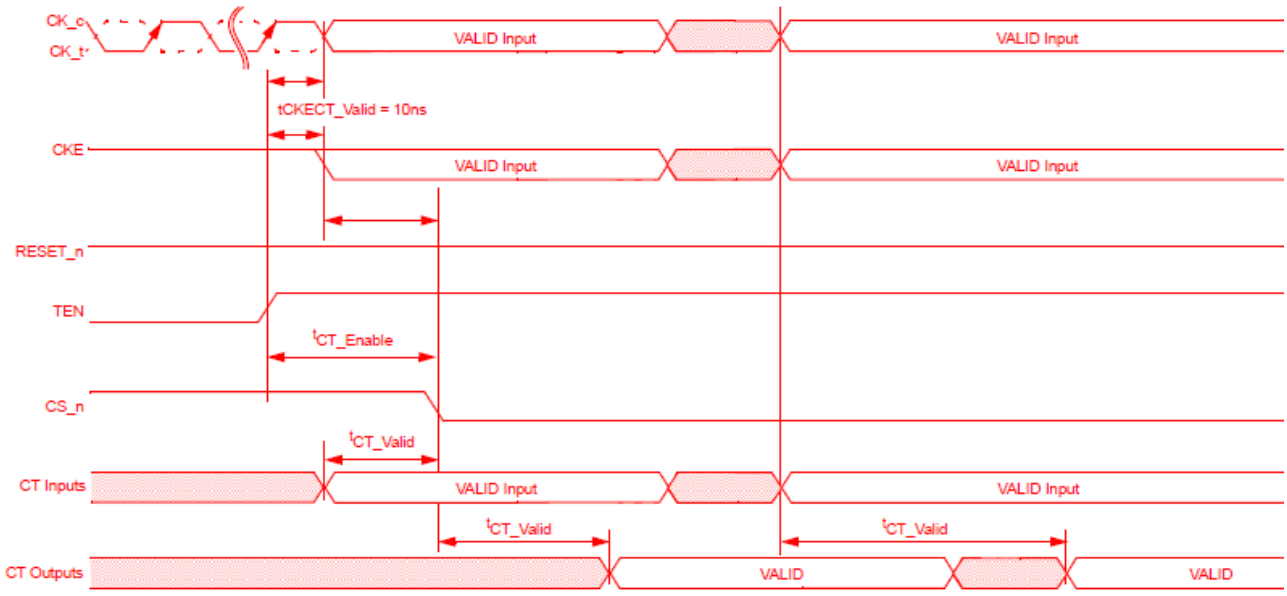
Upon the assertion of the TEN pin, the CK and $\overline{CK}$ signals will be ignored and the DDR4 memory device enter into the CT mode after tCT_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted after the DRAM has completed power-on; once the DRAM is initialized and VREFdq is calibrated, CT Mode may no longer be used.

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR4 memory device are unknown and the integrity of the original content of the memory array is not guaranteed and therefore the reset initialization sequence is required.

All output signals at the test output pins will be stable within tCT_valid after the test inputs have been applied to the test input pins with TEN input and $\overline{CS}$ input maintained High and Low respectively.

Connectivity Test Mode Entry

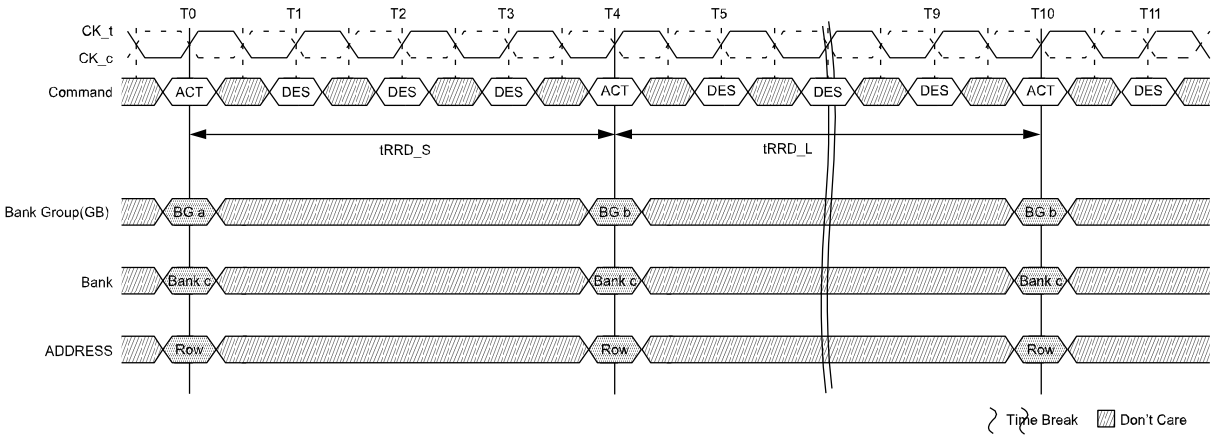


Symbol	Min	Max	Unit
tCT_Enable	200	—	ns
tCT_Valid	—	200	ns

ACTIVATE Command

The ACTIVATE command is used to open (activate) a row in a particular bank for subsequent access. The values on the BG[1:0] inputs select the bank group; the BA[1:0] inputs select the bank within the bank group; and the address provided on inputs A[17:0] selects the row within the bank. This row remains active (open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank. Bank-to-bank command timing for ACTIVATE commands uses two different timing parameters, depending on whether the banks are in the same or different bank group. tRRD_S (short) is used for timing between banks located in different bank groups. tRRD_L (long) is used for timing between banks located in the same bank group. Another timing restriction for consecutive ACTIVATE commands (issued at tRRD (MIN) is tFAW (fifth activate window). Since there is a maximum of four banks in a bank group, the tFAW parameter applies across different bank groups because five activate commands issued at tRRD_L (MIN) to the same bank group would be limited by tRC.

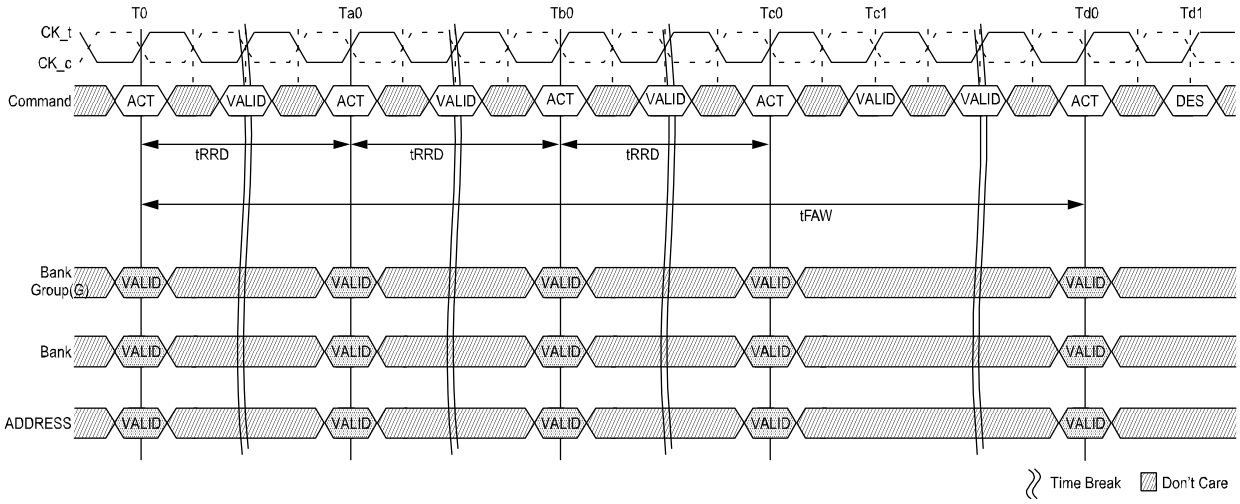
tRRD Timing



NOTE 1 tRRD_S; ACTIVATE-to-ACTIVATE command period (short); applies to consecutive ACTIVATE commands to different bank groups (i.e., T0 and T4) .

NOTE 2 tRRD_L; ACTIVATE-to-ACTIVATE command period (long); applies to consecutive ACTIVATE commands to the different banks in the same bank group (i.e., T4 and T10).

tFAW Timing



NOTE 1 tFAW; four activate window.

PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation for a specified time (tRP) after the PRECHARGE command is issued. An exception to this is the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

The auto-precharge function is engaged when a Read or Write command is issued with A10 High. The auto-precharge function utilizes the RAS lockout circuit to internally delay the precharge operation until the array restore operation has completed. The RAS lockout circuit feature allows the precharge operation to be partially or completely hidden during burst read cycles when the auto-precharge function is engaged. The precharge operation will not begin until after the last data of the burst write sequence is properly stored in the memory array.

REFRESH Command

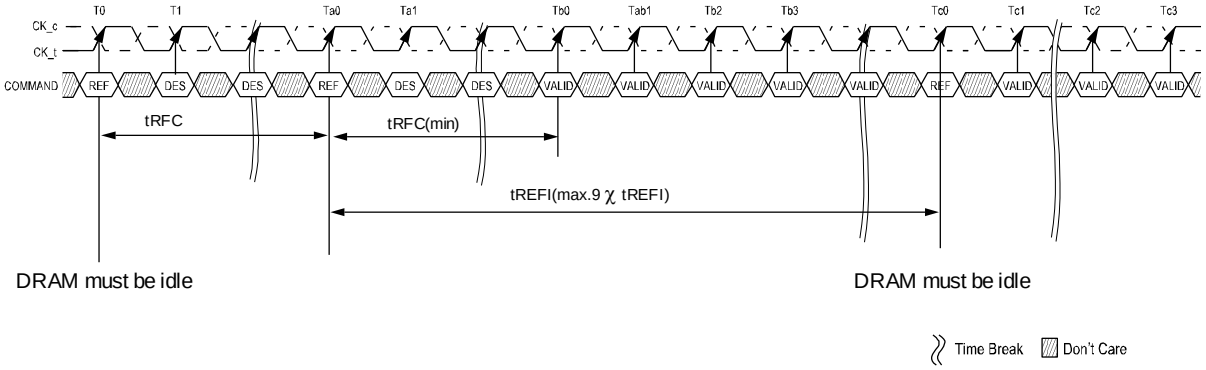
The REFRESH command (REF) is used during normal operation of the device. This command is nonpersistent, so it must be issued each time a refresh is required. The device requires REFRESH cycles at an average periodic interval of tREFI. When $\overline{CS}$, $\overline{RAS}$/A16 and $\overline{CAS}$/A15 are held LOW and $\overline{WE}$/A14 HIGH at the rising edge of the clock, the chip enters a REFRESH cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP (MIN) before the REFRESH command can be applied. The refresh addressing is generated by the internal DRAM refresh controller. This makes the address bits “Don’t Care” during a REFRESH command. An internal address counter supplies the addresses during the REFRESH cycle. No control of the external address bus is required once this cycle has started. When the REFRESH cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the REFRESH command and the next valid command, except DES, must be greater than or equal to the minimum REFRESH cycle time tRFC (MIN). The tRFC timing parameter depends on memory density.

In general, a REFRESH command needs to be issued to the device regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pullingin the refresh command. A limited number Refresh commands can be postponed depending on Refresh mode: maximum of 8 Refresh commands can be postponed when the device is in 1X refresh mode; a maximum of 16 Refresh commands can be postponed when the device is in 2X refresh mode, and a maximum of 32 Refresh commands can be postponed when the device is in 4X refresh mode.

At any point in time no more than a total of 8, 16, 32 Refresh commands are allowed to be postponed. When 8 consecutive Refresh commands are postponed, the resulting maximum interval between the surrounding Refresh commands is limited to 9 x tREFI (). For both the 2X and 4X Refresh modes, the maximum consecutive Refresh commands allowed is limited to 17 x tREFI2 and 36 xtREFI4, respectively.

A limited number Refresh commands can be pulled-in as well. A maximum of 8 additional Refresh commands can be issued in advance or “pulled-in” in 1X refresh mode; a maximum of 16 additional Refresh commands can be issued when in advance in 2X refresh mode; and a maximum of 32 additional Refresh commands can be issued in advance when in 4X refresh mode; with each Refresh command reducing the number of regular Refresh commands required later by one. Note that pulling in more than the maximum allowed Refresh command, Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 x tREFI, 18 x tRFEI2 and 36 x tREFI4 respectively. At any given time, a maximum of 16 REF commands can be issued within 2 x tREF; 32 REF2 commands can be issued within 4 x tREF; and 64 REF4 commands can be issued within 8 x tREFI4.

REFRESH Command Timing

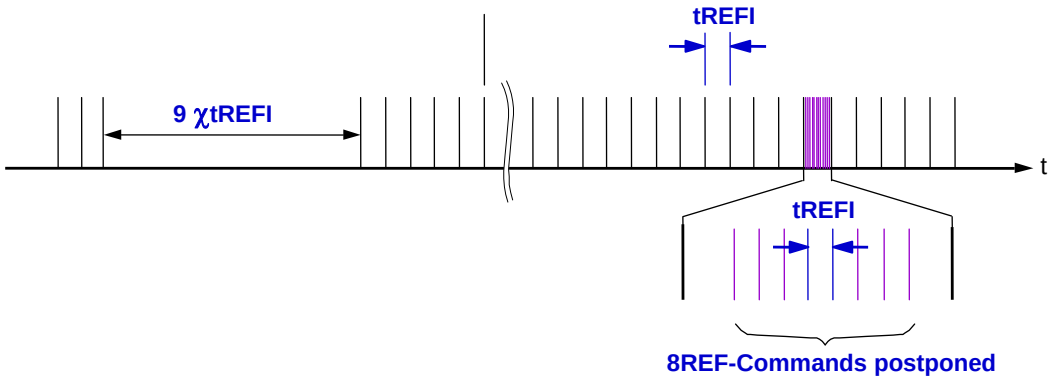


NOTE : 1. Only DES commands allowed after Refresh commandregistered untill tRFC(min) expires.
2. Time interval between two Refresh commands may be extended to a maximum of 9 X tREFI.

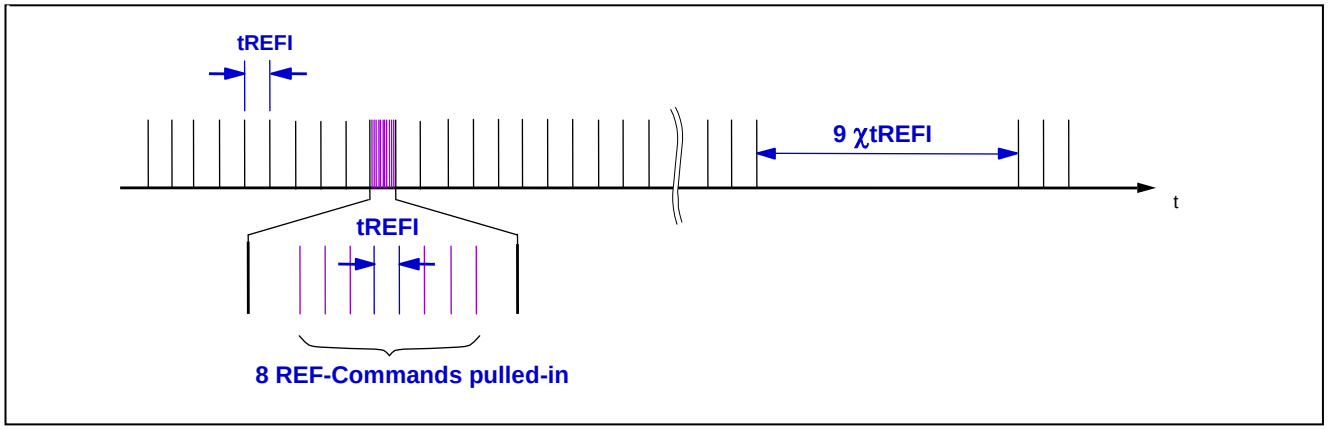
NOTE 1 Only DES commands allowed after REFRESH command registered until tRFC (MIN) expires.

NOTE 2 Time interval between two REFRESH commands may be extended to a maximum of 9 x tREFI.

Postponing REFRESH Commands (Example of 1X Refresh mode)



Pulling In REFRESH Commands (Example of 1X Refresh mode)



Temperature-Controlled Refresh Mode (TCR)

During normal operation, TCR mode disabled, the DRAM must have a Refresh command issued once every tREFI, except for what is allowed by posting (see Refresh Command section). This means a refresh command must be issued once every 3.9µs if TC greater than or equal to 85 °C and once every 7.8µs if TC less than 85 °C, as shown in table below.

Normal tREFI Refresh (TCR Disabled)

Temperature	Normal Temperature		Extended Temperature	
	External Refresh Period	Internal Refresh Period	External Refresh Period	Internal Refresh Period
Tc < +45℃	7.8µs	7.8µs	3.9µs	3.9µs
+45℃ ≦ Tc < +85℃				
+85℃ ≦ Tc < +95℃	(Not Applicable)			

NOTE 1 If TC is less than +85°C then the external refresh period can be 7.8µs if the DRAM can arbitrate between the temperature switching at the 85°C point.

TCR Mode

When TCR mode is enabled, the DRAM will register the externally supplied Refresh Command and adjust the internal refresh period to be longer than tREFI of the normal temperature range, when allowed, by skipping REFRESH commands with the proper gear ratio. TCR Mode has two ranges to select between - Normal Temperature Range and Extended Temperature Range; the correct range must be selected so the internal control operates correctly The DRAM is to have the correct REFRESH rate applied externally; the internal refresh rate is determined by the DRAM based upon the temperature.

TCR Mode - Normal Temperature Range

REFRESH commands are to be issued to DRAM with the refresh period equal to or shorter than tREFI of normal temperature range (0°C to +85°C). In this mode, the system guarantees that the DRAM temperature does not exceed 85°C. The DRAM may adjust the internal refresh period to be longer than tREFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio when Tc is below 45°C. The internal refresh period is automatically adjusted inside the DRAM and the DRAM controller does not need to provide any additional control.

TCR Mode - Extended Temperature Range

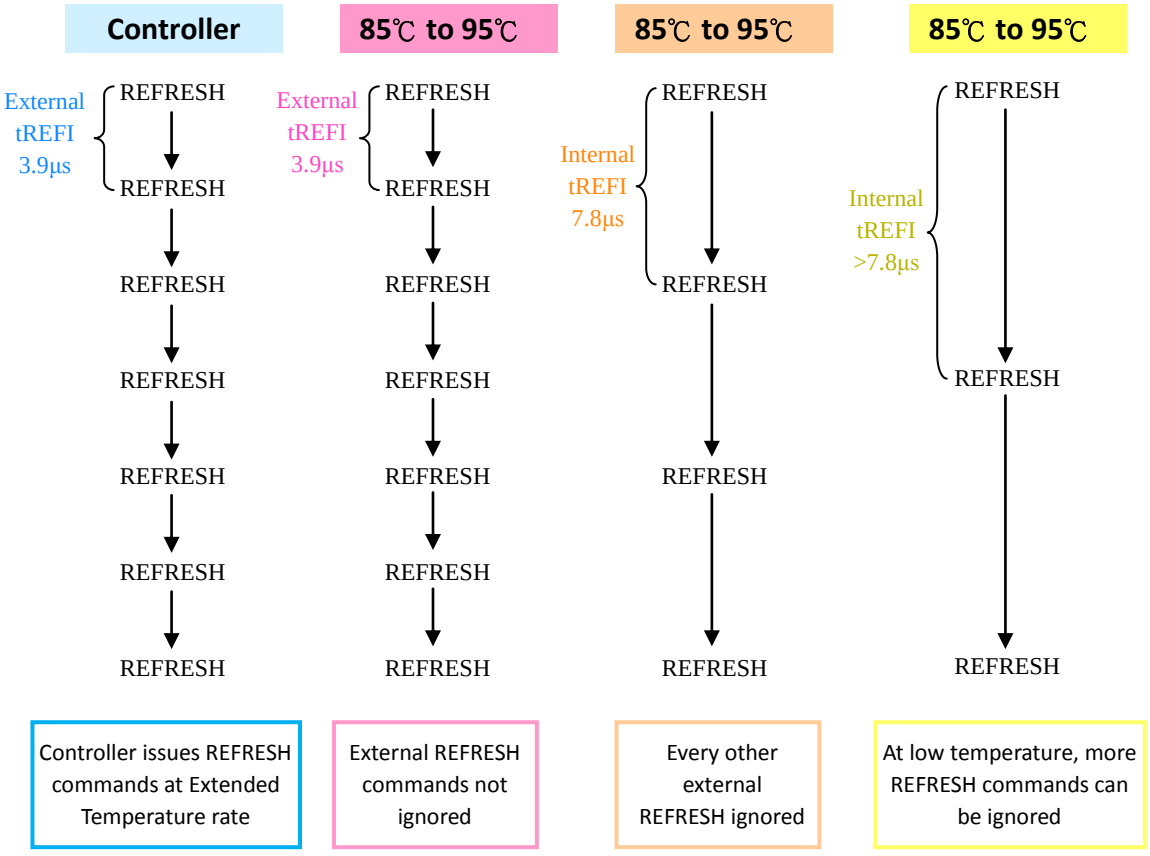
REFRESH commands should be issued to DRAM with the refresh period equal to or shorter than tREFI of extended temperature range (+85°C to +95°C). Even though the external Refresh supports the extended temperature range, the DRAM will adjust its internal refresh period to tREFI of the normal temperature range by skipping external REFRESH commands with proper gear ratio when operating in the normal temperature range (0°C to +85°C). The DRAM may adjust the internal refresh period to be longer than tREFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio when Tc is below 45°C. The internal refresh period is automatically adjusted inside the DRAM and the DRAM controller does not need to provide any additional control.

Normal tREFI Refresh (Temperature-Controlled Refresh Enabled)

Temperature	Normal Temperature		Extended Temperature	
	External Refresh Period	Internal Refresh Period	External Refresh Period	Internal Refresh Period
Tc < +45℃	7.8µs	>> 7.8µs	3.9µs	>> 7.8µs
+45℃ ≦ Tc < +85℃	7.8µs	7.8µs		7.8µs
+85℃ ≦ Tc < +95℃	(Not Applicable)			3.9µs

NOTE 1 If the external refresh period is 7.8µs then DRAM will refresh internally at half the listed refresh rate and will violate refresh specifications.

TCR Mode Example



Fine Granularity Refresh Mode (FGRM)

Mode Register and Command Truth Table

The REFRESH cycle time (tRFC) and the average refresh interval (tREFI) of DDR4 SDRAM can be programmed by the MRS command. The appropriate setting in the mode register will set a single set of REFRESH cycle time and average refresh interval for the DDR4 SDRAM device (fixed mode), or allow the dynamic selection of one of two sets of REFRESH cycle time and average refresh interval for the DDR4 SDRAM device (on-the-fly mode [OTF]). OTF mode must be enabled by MRS before any OTF REFRESH command can be issued.

MRS Definition

MR3[8]	MR3[7]	MR3[6]	Fine Granularity Refresh
0	0	0	Normal mode (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 1x/2x
1	1	0	Enable on the fly 1x/4x
1	1	1	Reserved

There are two types of OTF modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register. When either of the two OTF modes is selected, DDR4 SDRAM evaluates the BG0 bit when a REFRESH command is issued, and, depending on the status of BG0, it dynamically switches its internal refresh configuration between 1x and 2x (or 1x and 4x) modes, then executes the corresponding REFRESH operation.

REFRESH Command Truth Table

REFRESH	CS	$\overline{ACT}$	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG1	BG0	BA0-1	A10/ AP	A[9:0], A[12:11], A17	MR3[8:6]
Fixed rate	L	H	L	L	H	V	**V**	V	V	V	**0vv**
OTF – 1x	L	H	L	L	H	V	**L**	V	V	V	**1vv**
OTF – 2x	L	H	L	L	H	V	**H**	V	V	V	**101**
OTF – 4x											**110**

tREFI and tRFC Parameters

The default refresh rate mode is fixed 1x mode where REFRESH commands should be issued with the normal rate, i.e. tREFI1 = tREFI(base) (for TCASE ≤ 85°C), and the duration of each REFRESH command is the normal refresh cycle time (tRFC1). In 2x mode (either fixed 2x or OTF 2x mode), REFRESH commands should be issued to the DRAM at the double frequency (tREFI2 = tREFI(base)/2) of the normal refresh rate. In 4x mode, REFRESH command rate should be quadrupled (tREFI4 = tREFI(base)/4). Per each mode and command type, tRFC parameter has different values as defined in the following table.

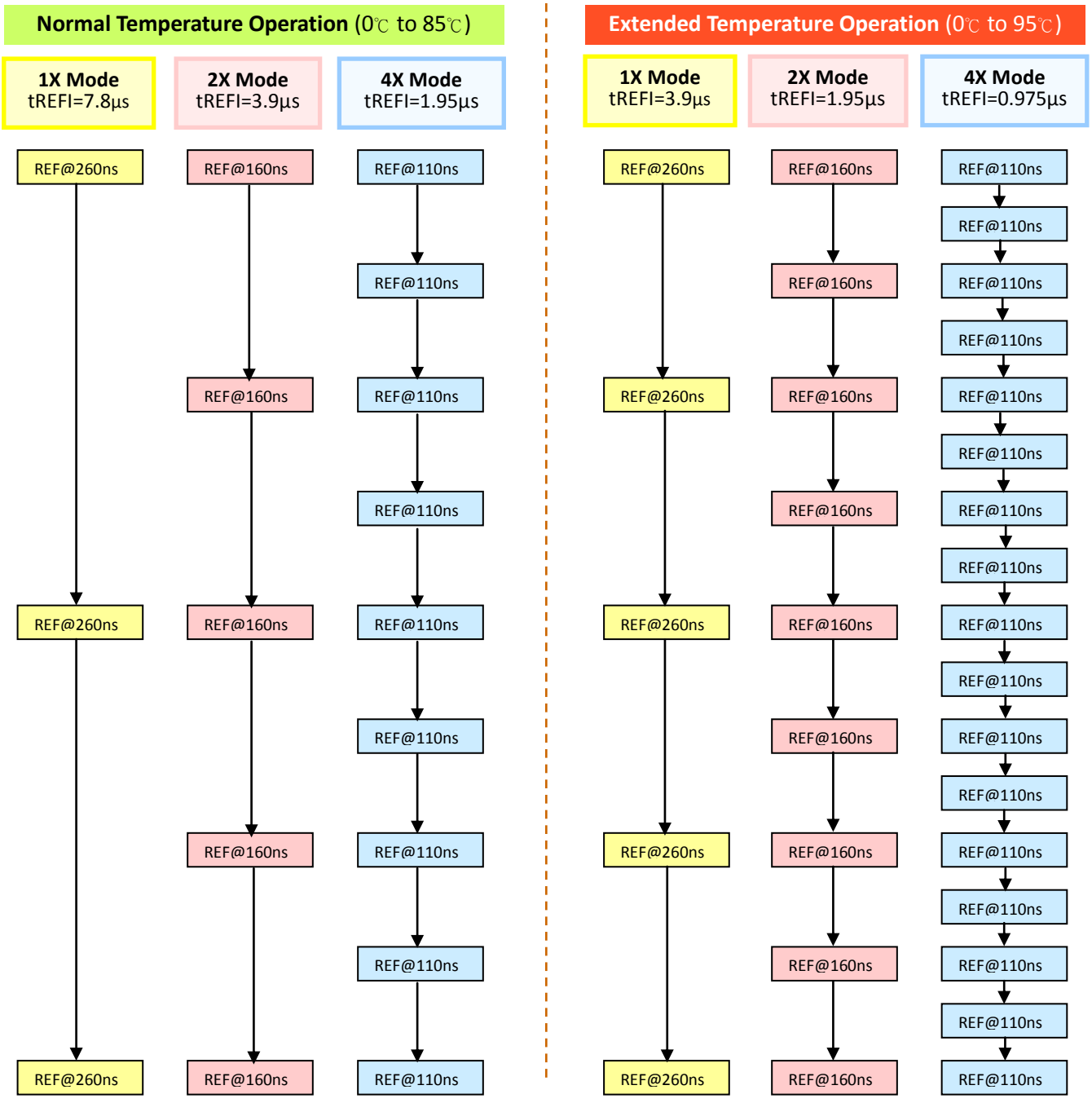
For discussion purposes, the REFRESH command that should be issued at the normal refresh rate and has the normal refresh cycle duration may be referred to as a REF1x command. The refresh command that should be issued at the double frequency (tREFI2 = tREFI(base)/2) may be referred to as a REF2x command. Finally, the REFRESH command that should be issued at the quadruple rate (tREFI4 = tREFI(base)/4) may be referred to as a REF4x command.

In the fixed 1x refresh rate mode, only REF1x commands are permitted. In the fixed 2x refresh rate mode, only REF2x commands are permitted. In the fixed 4x refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the OTF 1x/4x refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

tREFI and tRFC Parameters

Refresh Mode	Parameter		4Gb	Unit
	tREFI (base)		**7.8**	µs
1X mode	**tREFI1**	0°C ≤ TCASE ≤ 85°C	**tREFI(base)**	µs
		85°C < TCASE ≤ 95°C	**tREFI(base)/2**	µs
	tRFC1 (min)		**260**	ns
2X mode	**tREFI2**	0°C <= TCASE ≤ 85°C	**tREFI(base)/2**	µs
		85°C < TCASE ≤ 95°C	**tREFI(base)/4**	µs
	tRFC2 (min)		**160**	ns
4X mode	**tREFI4**	0°C <= TCASE ≤ 85°C	**tREFI(base)/4**	µs
		85°C < TCASE ≤ 95°C	**tREFI(base)/8**	µs
	tRFC4 (min)		**110**	ns

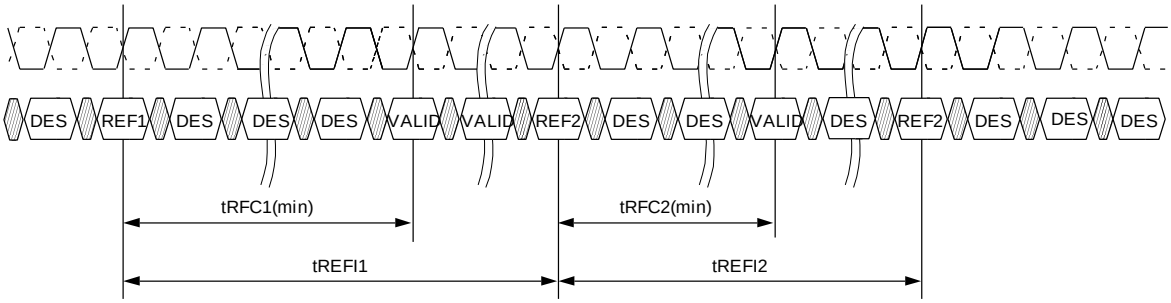
4Gb with Fine Granularity Refresh Mode Example



Changing Refresh Rate

If the refresh rate is changed by either MRS or OTF, new tREFI and tRFC parameters would be applied from the moment of the rate change. When the REF1x command is issued to the DRAM, then tREF1 and tRFC1 are applied from the time that the command was issued. And then, when REF2x command is issued, then tREF2 and tRFC2 should be satisfied.

On-the-fly REFRESH Command Timing



The following conditions must be satisfied before the refresh rate can be changed. Otherwise, data retention of DDR4 SDRAM cannot be guaranteed.

- In the fixed 2x refresh rate mode or the OTF 1x/2x refresh mode, an even number of REF2x commands must be issued to the DDR4 SDRAM since the last change of the refresh rate mode with an MRS command before the refresh rate can be changed by another MRS command.
- In the OTF1x/2x refresh rate mode, an even number of REF2x commands must be issued between any two REF1x commands.
- In the fixed 4x refresh rate mode or the OTF 1x/4x refresh mode, a multiple-of-four number of REF4x commands must be issued to the DDR4 SDRAM since the last change of the refresh rate with an MRS command before the refresh rate can be changed by another MRS command.
- In the OTF1x/4x refresh rate mode, a multiple-of-four number of REF4x commands must be issued between any two REF1x commands. There are no special restrictions for the fixed 1x refresh rate mode. Switching between fixed and OTF modes keeping the same rate is not regarded as a refresh rate change.

Usage with Temperature Controlled Refresh Mode

If the temperature controlled refresh mode is enabled, then only the normal mode (fixed 1x mode, MR3[8:6] = 000) is allowed. If any other refresh mode than the normal mode is selected, then the temperature controlled refresh mode must be disabled.

Self Refresh Entry and Exit

DDR4 SDRAM can enter self refresh mode anytime in 1x, 2x, and 4x mode without any restriction on the number of REFRESH commands that have been issued during the mode before the self refresh entry. However, upon self refresh exit, extra REFRESH command(s) may be required, depending on the condition of the self refresh entry.

The conditions and requirements for the extra REFRESH command(s) are defined as follows:

- There are no special restrictions on the fixed 1x refresh rate mode.
- In the fixed 2x refresh rate mode or the enable-OTF 1x/2x refresh rate mode, it is recommended that there should be an even number of REF2x commands before entry into self refresh because the last SELF REFRESH EXIT or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon self refresh exit. In the case that this condition is not met, either one extra REF1x command or two extra REF2x commands are required to be issued to the DDR4 SDRAM upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval (t_{REFI}).
- In the fixed 4x refresh rate mode or the enable-OTF 1x/4x refresh rate mode, it is recommended that there should be a multiple-of-four number of REF4x commands before entry into self refresh since the last self refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon self refresh exit. In the case that this condition is not met, either one extra REF1x command or four extra REF4x commands are required to be issued to the DDR4 SDRAM upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval (t_{REFI}).

This section does not change the requirement regarding postponed REFRESH commands. The requirement for the additional REFRESH command(s) described above is independent of the requirement for the postponed refresh commands.

Self Refresh Operation

The SELF REFRESH command can be used to retain data in the DDR4 SDRAM, even if the rest of the system is powered down. When in self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate SELF REFRESH operation. The SELF REFRESH command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and CKE held LOW with $\overline{WE}$ and $\overline{ACT}$ HIGH at the rising edge of the clock.

Before issuing the SELF REFRESH ENTRY command, the device must be idle with all banks in the precharge state and tRP satisfied. Idle state is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.). After the SELF REFRESH ENTRY command is registered, CKE must be held LOW to keep the device in self refresh mode. DRAM automatically disables ODT termination, regardless of the ODT pin, when it enters self refresh mode and automatically enables ODT upon exiting self refresh. During normal operation (DLL on), the DLL is automatically disabled upon entering self refresh and is automatically enabled (including a DLL reset) upon exiting self refresh.

When the device has entered self refresh mode, all of the external control signals, except CKE and $\overline{RESET}$, are “Don’t Care.” For proper SELF REFRESH operation, all power supply and reference pins (V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}, V_{PP}, and V_{REFCA}) must be at valid levels.

The DRAM internal VREFDQ generator circuitry may remain ON or turned OFF depending on the MRx bit y setting. If the DRAM internal VREFDQ circuit is ON in self refresh, first WRITE operation or first write-leveling activity may occur after tXS time after self refresh exit. If the DRAM internal VREFDQ circuitry is turned OFF in self refresh, when the DRAM exits the self refresh state, it ensures that the VREFDQ generator circuitry is powered up and stable within the tXSDLL period. First WRITE operation or first writeleveling activity may not occur earlier than tXSDLL after exiting self refresh. The DRAM initiates a minimum of one REFRESH command internally within the tCKE period once it enters self refresh mode.

The clock is internally disabled during a SELF REFRESH operation to save power. The minimum time that the device must remain in self refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE after self refresh entry is registered; however, the clock must be restarted and tCKSRX must be stable before the device can exit SELF REFRESH operation.

The procedure for exiting self refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a SELF REFRESH EXIT command (SRX, combination of CKE going HIGH and DESELECT on the command bus) is registered, the following timing delay must be satisfied:

Commands that do not require locked DLL:

• tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8.

• tXSFast - ZQCL, ZQCS, MRS commands. For an MRS command, only DRAM CL and the WR/RTP register in MR0, the CWL register in MR2, and geardown mode in MR3 are allowed to be accessed, provided DRAM is not in per DRAM addressability mode.

Access to other DRAM mode registers must satisfy tXS timing.

Commands that require locked DLL:

• tXSDLL - RD, RDS4, RDS8, RDA, RDAS4, RDAS8.

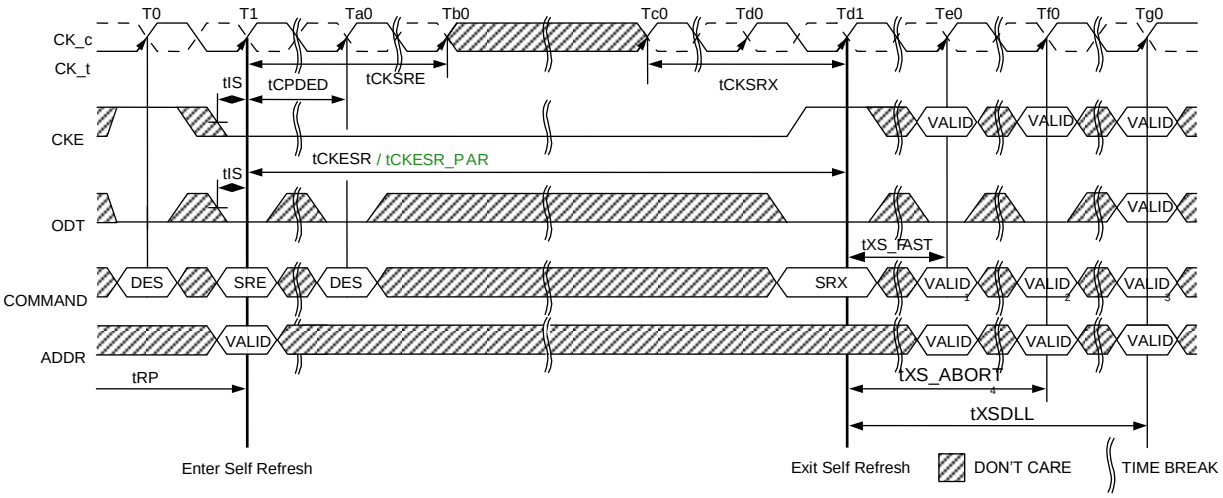
Depending on the system environment and the amount of time spent in self refresh, ZQ CALIBRATION commands may be required to compensate for the voltage and temperature drift described in the ZQ Calibration Commands section. To issue ZQ CALIBRATION commands, applicable timing requirements must be satisfied.

CKE must remain HIGH for the entire self refresh exit period tXSDLL for proper operation except for self refresh re-entry. Upon exit from self refresh, the device can be put back into self refresh mode or power-down mode after waiting at least tXS period and issuing one REFRESH command (refresh period of tRFC). The DESELECT command must be registered on each positive clock edge during the self refresh exit interval tXS.

ODT must be turned off during tXSDLL.

The use of self refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self refresh mode. Upon exit from self refresh, the device requires a minimum of one extra REFRESH command before it is put back into self refresh mode.

Self Refresh Entry/Exit Timing



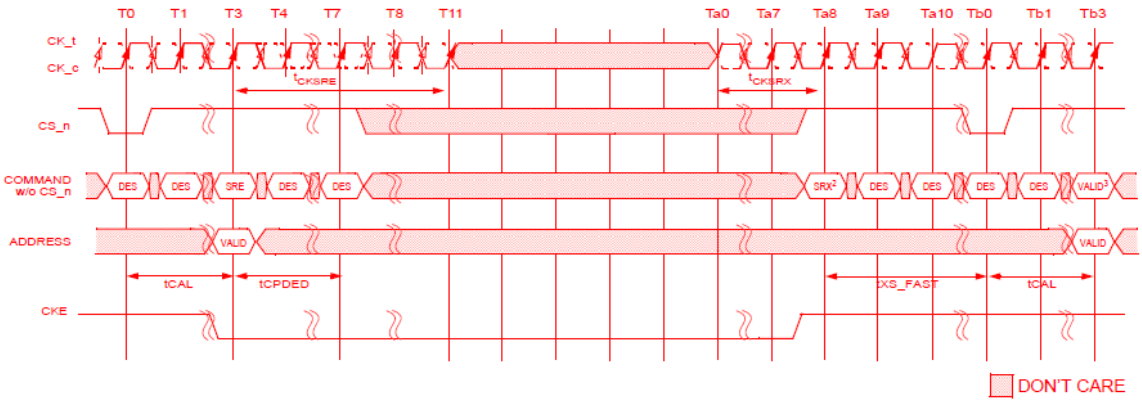
NOTE 1 Only MRS (limited to those described in the Self-Refresh Operation section). ZQCS or ZQCL command allowed.

NOTE 2 Valid commands not requiring a locked DLL

NOTE 3 Valid commands requiring a locked DLL

NOTE 4 Only DES is allowed during tXS_ABORT

Self Refresh Entry/Exit Timing with CAL



NOTE 1 tCAL = 3nCK, tCPDED = 4nCK, tCKSRE= 8nCK, tCKSRX= 8nCK, tXS_FAST = tREFC4(min)+10ns

NOTE 2 $\overline{CS}$ = high, $\overline{ACT}$= Don't Care, $\overline{RAS}$/A16 = Don't Care, $\overline{CAS}$/A15 = Don't Care, $\overline{WE}$/A14 = Don't Care,

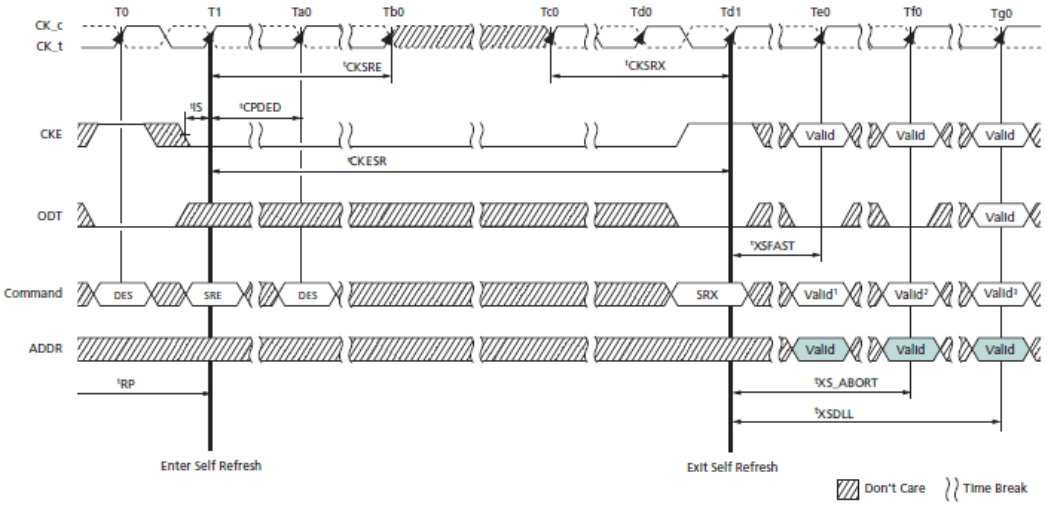
NOTE 3 Only MRS(limited to thise described in the Self-Refresh Operation section), ZQCS, or ZQCL commands are allowed.

Self Refresh Abort

The exit timing from self refresh exit to the first valid command not requiring a locked DLL is tXS. The value of tXS is (tRFC+10ns). This delay is to allow any refreshes started by the DRAM time to complete. tRFC continues to grow with higher density devices so tXS will grow as well. An MRS bit enables the self refresh abort mode. If the bit is disabled then the controller uses tXS timings (location MR4, bit 9). If the bit is enabled, then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command not requiring a locked DLL after a delay of tXS_abort.

Upon exit from self refresh, the device requires a minimum of one extra REFRESH command before it is put back into self refresh mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.

Self Refresh Abort



NOTE 1 Only MRS limited to those described in the Self Refresh Operation section), ZQCS, or ZQCL command allowed.

NOTE 2 Valid commands not requiring a locked DLL with self refresh abort mode enabled in the mode register.

NOTE 3 Valid commands requiring a locked DLL.

Self Refresh Exit with NOP Command

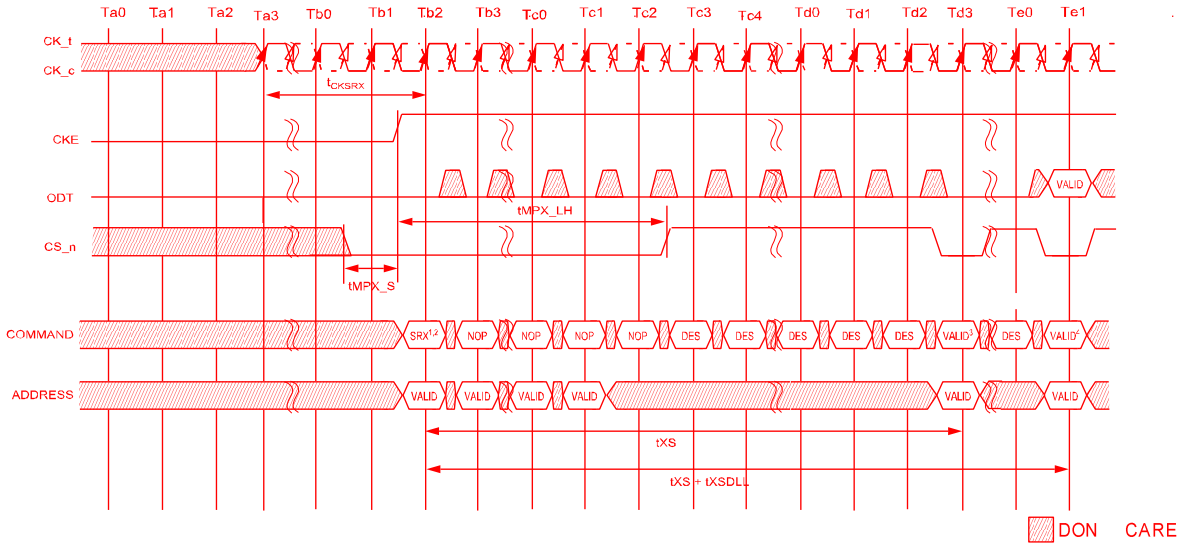
Exiting Self-Refresh Mode using the No Operation command (NOP) is allowed under a specific system application. This special use of NOP allows for a common command/address bus between active DRAMs and DRAM(s) in Max Power Saving Mode. Self Refresh Mode may exit with No Operation commands (NOP) provided:

• The DRAM entered Self Refresh Mode with CA Parity and CAL disabled.

• tMPX_S and tMPX_LH are satisfied.

• NOP commands are only issued during tMPX_LH window.

No other command is allowed during tMPX_LH window after SRX command is issued.



NOTE 1 $\overline{CS}$ = L, $\overline{ACT}$ = H, $\overline{RAS}$/A16 = H, $\overline{CAS}$/A15 = H, $\overline{WE}$/A14 = H at Tb2 (No Operation command)

NOTE 2 SRX at Tb2 is only allowed when DRAM shared Command/Address bus is under exiting Max Power Saving Mode.

NOTE 3 Valid commands not requiring a locked DLL

NOTE 4 Valid commands requiring a locked DLL

NOTE 5 tXS_FAST and tXS_ABORT are not allowed this case.

NOTE 6 Duration of $\overline{CS}$ Low around CKE rising edge must satisfy tMPX_S and tMPX_LH as defined by Max Power Saving Mode AC parameters.

Power-Down Mode

Power-down is synchronously entered when CKE is registered LOW (along with a DESELECT command). CKE is not allowed to go LOW when the following operations are in progress: MODE REGISTER SET command, MPR operations, ZQCAL operations, DLL locking, or READ/WRITE operations. CKE is allowed to go LOW while any other operations, such as ROW ACTIVATION, PRECHARGE or auto precharge, or REFRESH, are in progress, but the power-down IDD spec will not be applied until those operations are complete. Timing diagrams below illustrate entry and exit of power-down. The DLL should be in a locked state when power-down is entered for fastest powerdown exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as the DRAM controller complies with DRAM specifications. During power-down, if all banks are closed after any in-progress commands are completed, the device will be in precharge power-down mode; if any bank is open after inprogress commands are completed, the device will be in active power-down mode. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, CKE and $\overline{RESET}$. In power-down mode, DRAM ODT input buffer deactivation is based on MRx bit Y. If it is configured to 0b, the ODT input buffer remains on and ODT input signal must be at valid logic level. If it is configured to 1b, ODT input buffer is deactivated and DRAM ODT input signal may be floating and DRAM does not provide RTT_NOM termination. Note that the device continues to provide RTT_PARK termination if it is enabled in the mode register MRa bit B.To protect internal delay on the CKE line to block the input signals, multiple DES commands are needed during the CKE switch off and on cycle(s); this timing period is defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

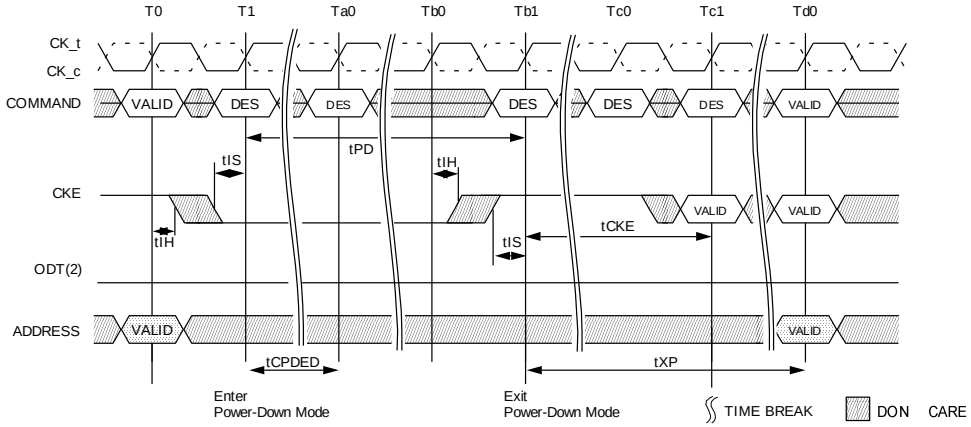
Power-Down Entry Definitions

Status of DRAM	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	On	Fast	tXP to any valid command
Precharged (All banks Precharged)	On	Fast	tXP to any valid command.

The DLL is kept enabled during precharge power-down or active power-down. In power-down mode, CKE is LOW, $\overline{RESET}$ is HIGH, and a stable clock signal must be maintained at the inputs of the device. ODT should be in a valid state, but all other input signals are "Don't Care." (If $\overline{RESET}$ goes LOW during power-down, the device will be out of power-down mode and in the reset state.) CKE LOW must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 x tREFI.

The power-down state is synchronously exited when CKE is registered HIGH (along with DES command). CKE HIGH must be maintained until tCKE has been satisfied. The ODT input signal must be at a valid level when the device exits from power-down mode, independent of MRx bit Y if RTT_NOM is enabled in the mode register. If RTT_NOM is disabled, then the ODT input signal may remain floating. A valid, executable command can be applied with power-down exit latency, tXP and/or tXPDLL after CKE goes HIGH. Power-down exit latency is defined in the AC Specifications table.

Active Power-Down Entry and Exit (MR5 bit A5 =0)



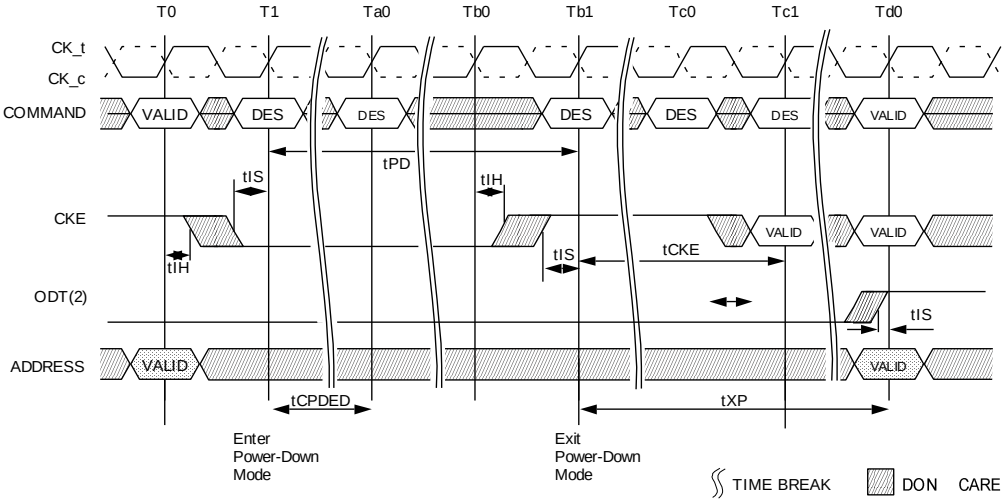
NOTE : 1. VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.
2. ODT pin driven to a valid state. MR5 bit A5=0 (default setting) is shown.

NOTE 1 Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.

NOTE 2 ODT pin driven to a valid state; MR5 [5] = 0 (normal setting).

NOTE 3 ODT pin driven to a valid state; MR5 [5] = 1.

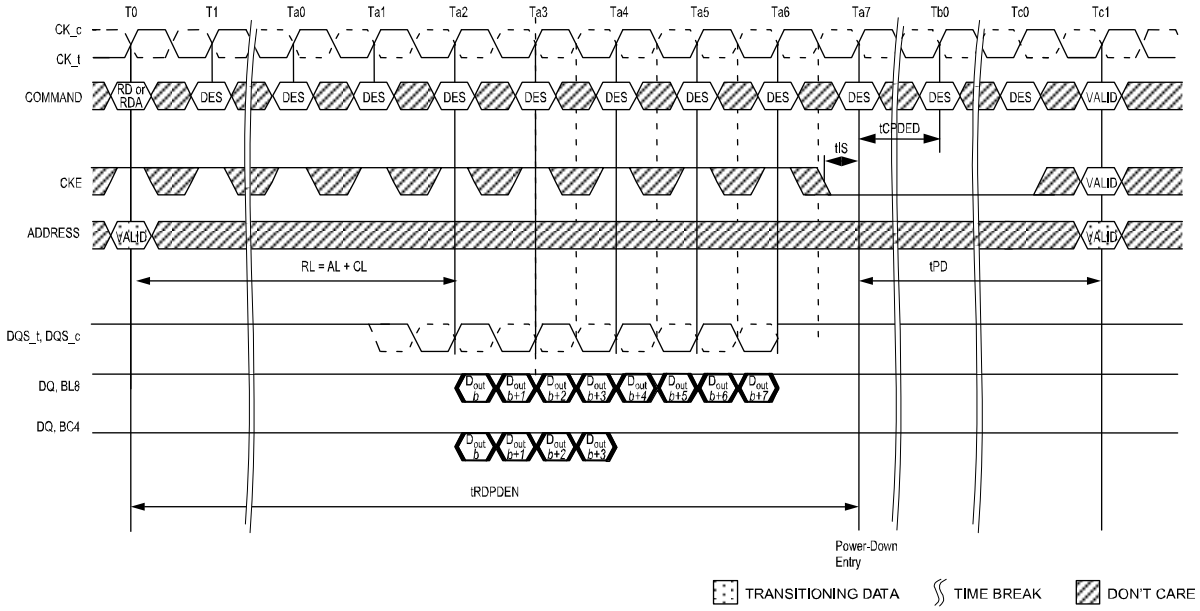
Active Power-Down Entry and Exit (MR5 bit A5 =1)



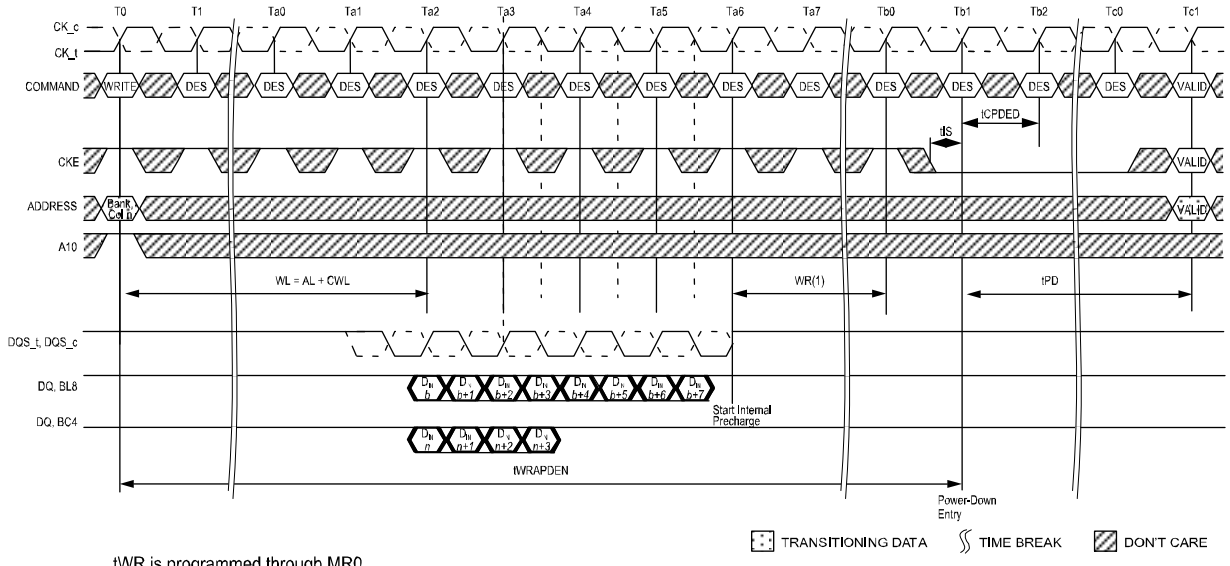
NOTE : 1. VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.
2. ODT pin driven to a valid state. MR5 bit A5=1 is shown.

NOTE 1 Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command. ODT pin driven to a valid state; MR5 [5] = 1.

Power-Down Entry After Read and Read with Auto Precharge



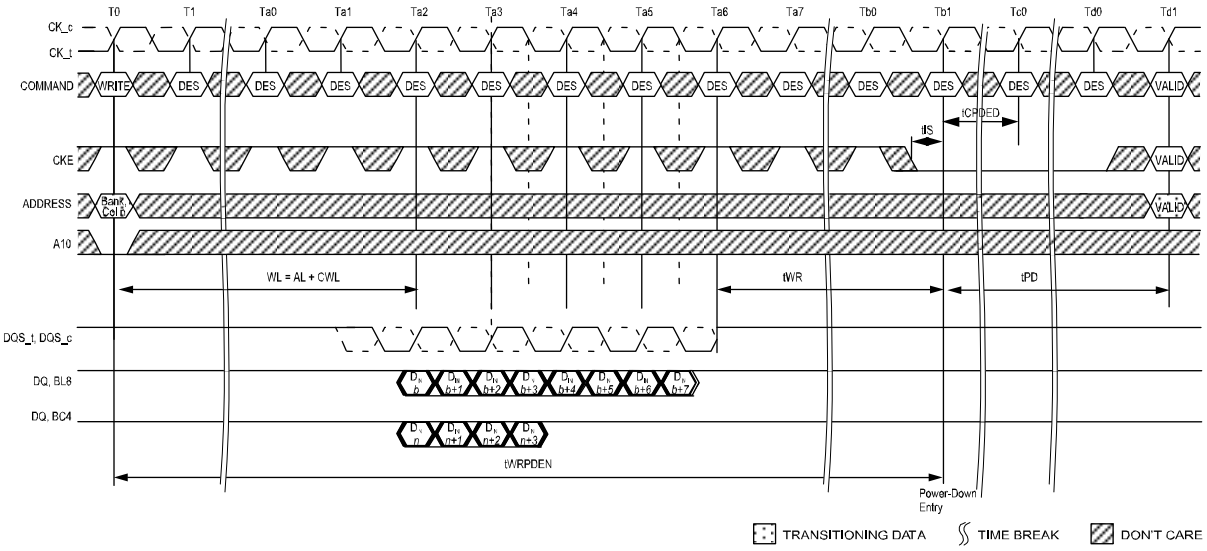
Power-Down Entry After Write and Write with Auto Precharge



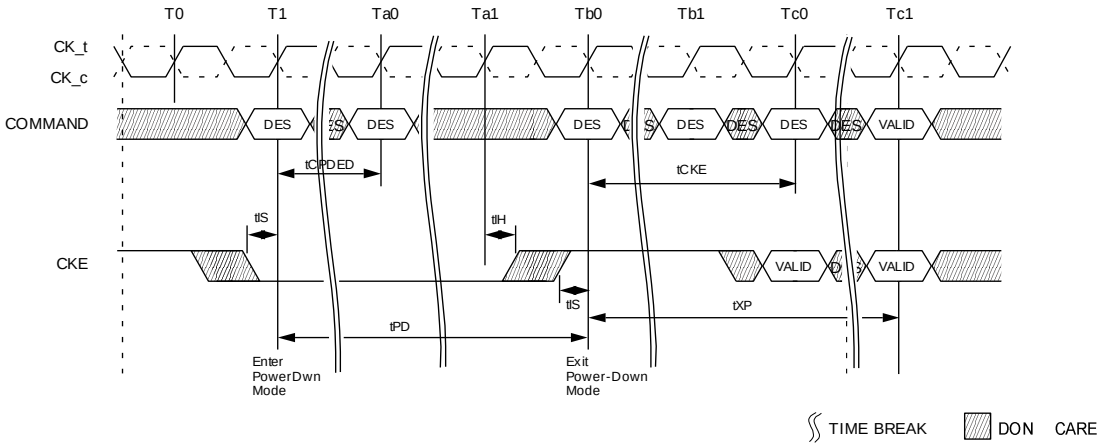
NOTE 1. tWR is programmed through MR0.

NOTE 1 Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.

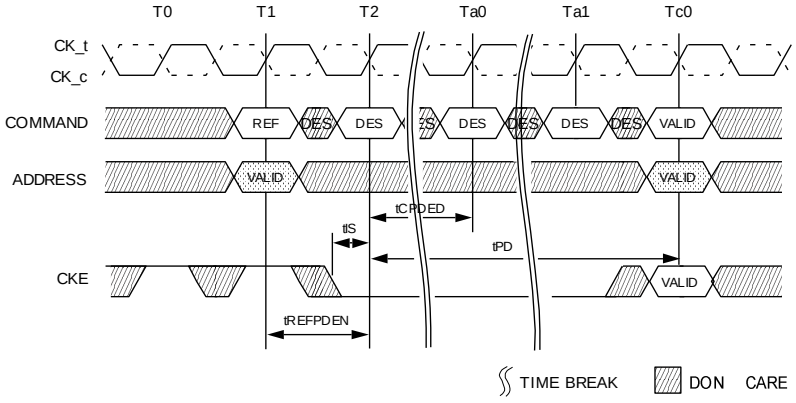
Power-Down Entry After Write



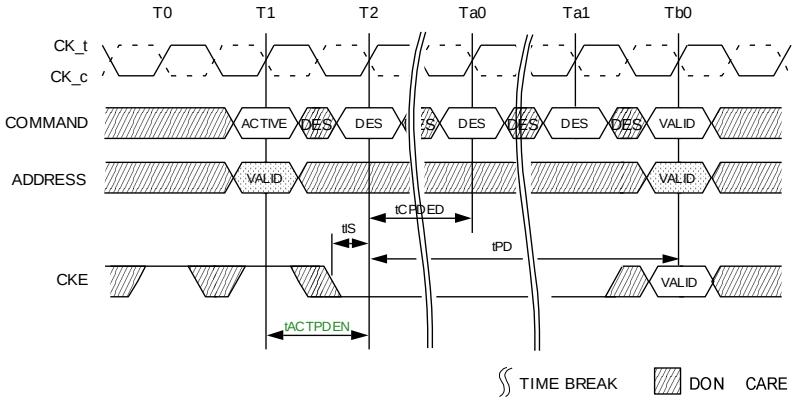
Precharge Power-Down Entry and Exit



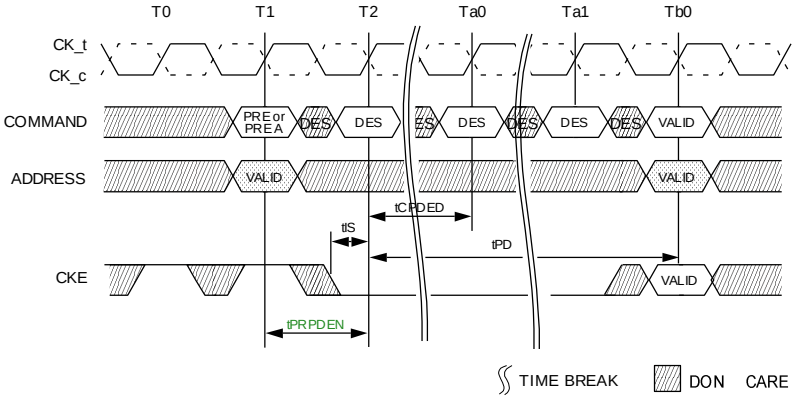
Refresh Command to Power-Down Entry



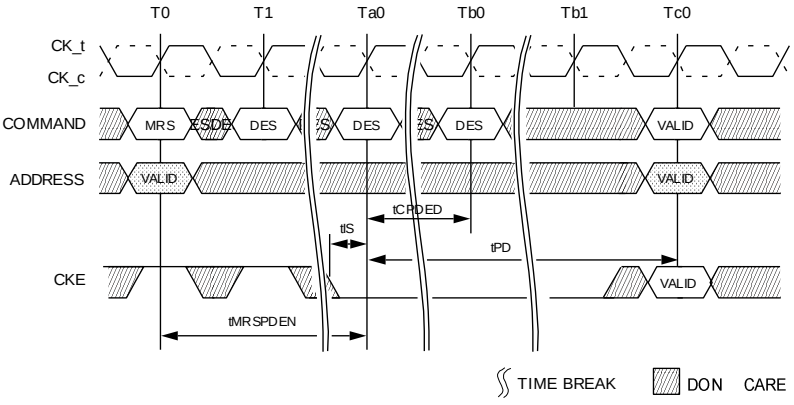
Active Command to Power-Down Entry



Precharge/Precharge All Command to Power-Down Entry

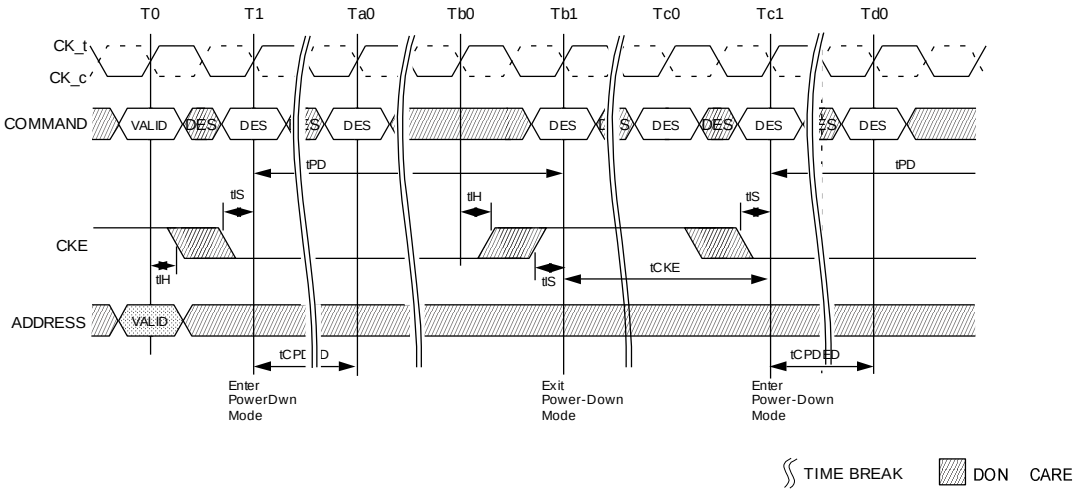


MRS Command to Power-Down Entry



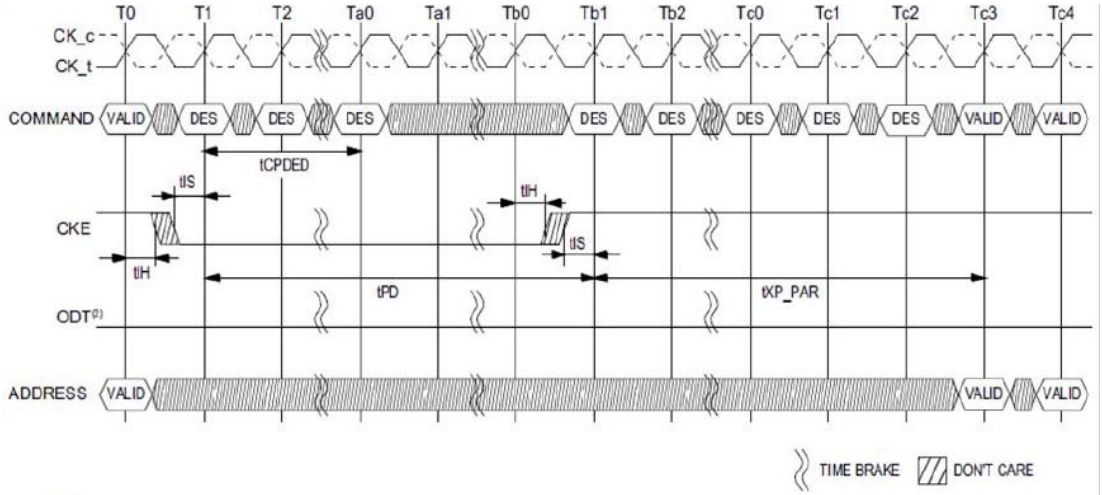
Power-Down Clarifications – Case 1

When CKE is registered LOW for power-down entry, tPD (MIN) must be satisfied before CKE can be registered HIGH for power-down exit. The minimum value of parameter tPD (MIN) is equal to the minimum value of parameter tCKE (MIN) as shown in the Timing Parameters by Speed Bin table. A detailed example of Case 1 is shown below.



Power Down Entry, Exit Timing with CAL

Command Address Lantency is used, additional timing restrictions are required when entering Power Down; as noted in figures below.



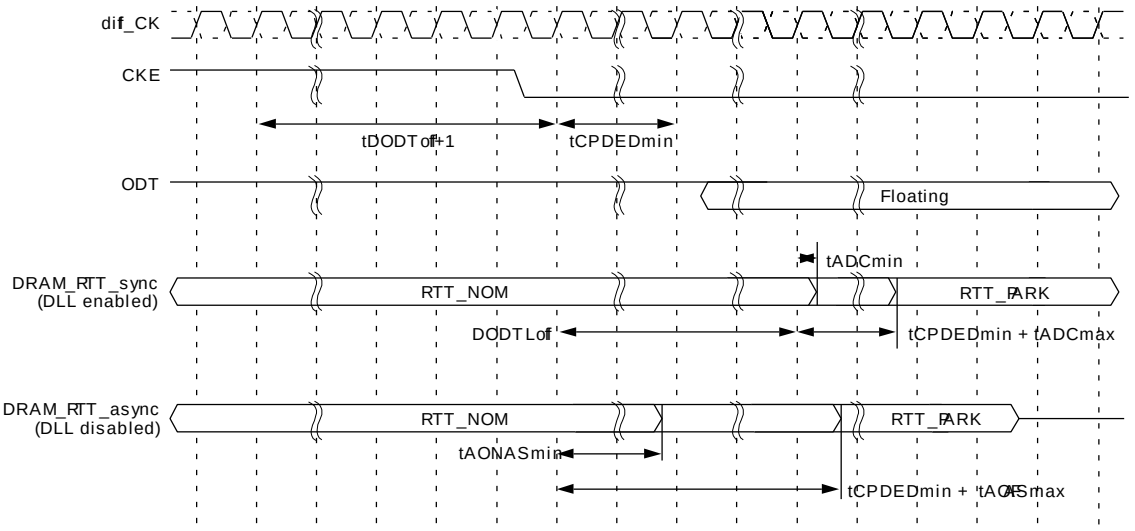
NOTE
1. VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.
2. ODT pin driven to a valid state. MR5[A5 = 0] (default setting) is shown.
3. CA Parity = Enable

ODT Input Buffer Disable Mode for Power down

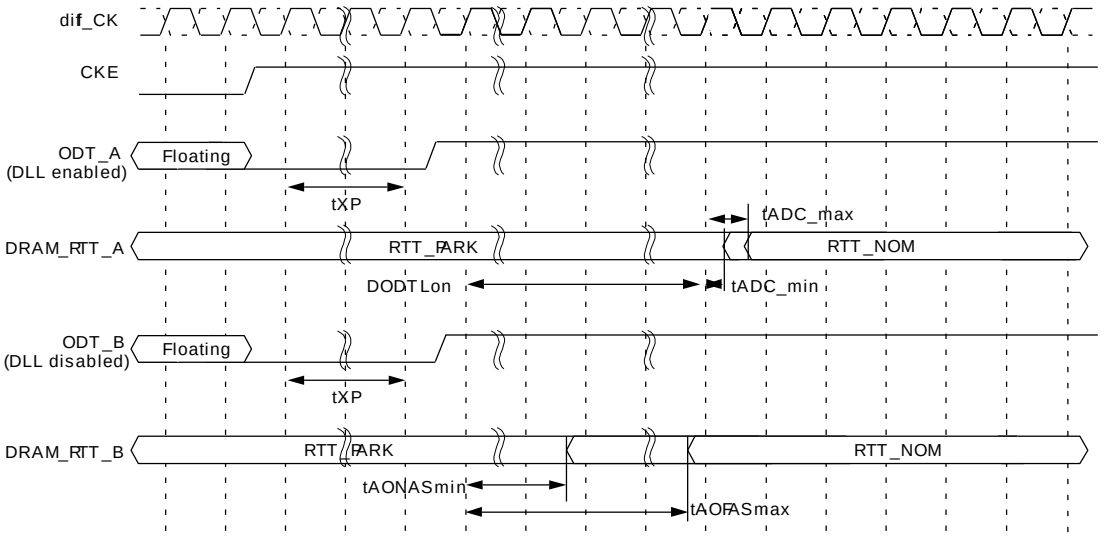
ODT Input Buffer Disable Mode, when enabled via MR5[5], will prevent the DRAM from providing Rtt_NOM termination during power down for additional power savings. The DRAM internal delay on CKE path to disable the ODT buffer and block the sampled output must be accounted for; thereby ODT must be continuously driven to a valid level, either low or high, when entering power down. However, once tCPDEDmin has been satisfied, ODT signal may then float.

When ODT Input Buffer Disable Mode is enabled, RTT_NOM termination corresponding to sampled ODT after CKE is first registered low (and tANPD before that) may not be provided. tANPD is equal to (WL-1) and is counted backwards from PDE, CKE registered low .

ODT Power-Down Entry with ODT Buffer Disable Mode



ODT Power-Down Exit with ODT Buffer Disable Mode

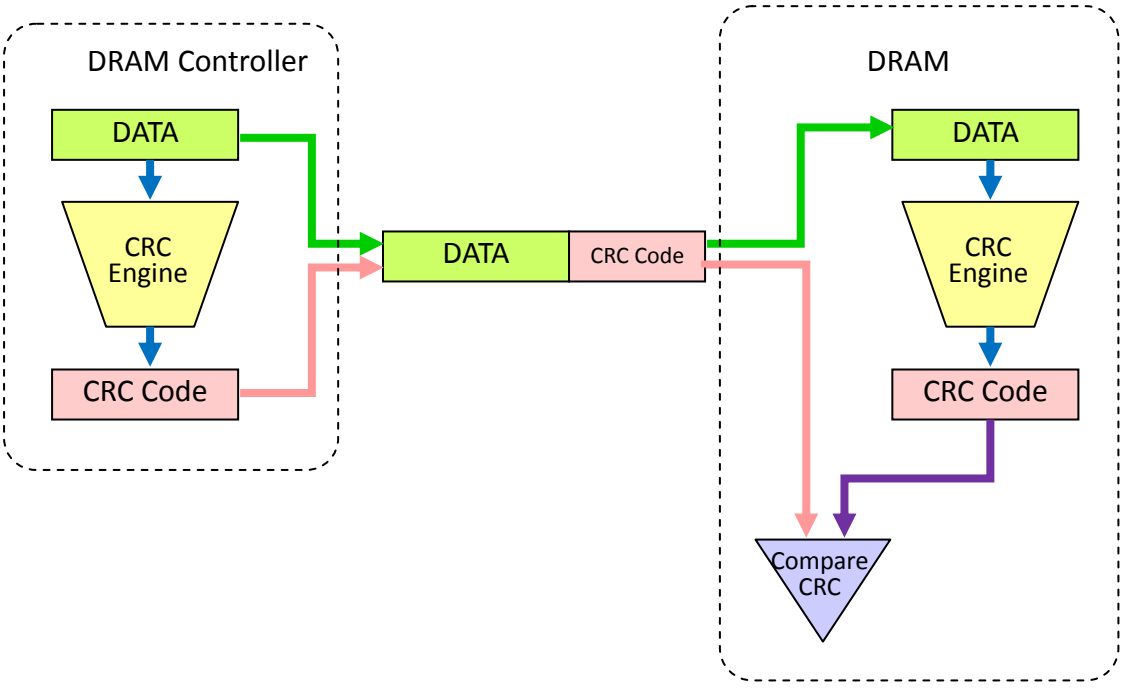


CRC Write Data Feature

CRC Write Data

The CRC Write Data feature takes the CRC generated data from the DRAM controller and compares it to the internally CRC generated data and determines if the two match (no CRC error) or if the two do not match (CRC error).

CRC Write Data Operation



Write CRC Data Operation

A DRAM controller generates a CRC checksum using a 72-bit CRC tree and forms the write data frames as shown in the CRC data mapping tables for the x4, x8, and x16 configurations below. A x4 device has a CRC tree with 32 input data bits, with the remaining upper 40 bits D[71:32] are 1s. A x8 device has a CRC tree with 64 input data bits, with the remaining upper 8 bits dependant upon if $\overline{DM}/\overline{DBI}$ is used (1s are sent when not used). A x16 device has two identical CRC trees each, one for lower byte an done for upper byte, with 64 input data bits, with the remaining upper 8 bits dependant upon if $\overline{DM}/\overline{DBI}$ is used (1s are sent when not used). For a x8 and x16 DRAMs, the DRAM memory controller must send 1s in transfer 9 location.

The DRAM checks for an error in a received code word D[71:0] by comparing the received checksum against the computed checksum and reports errors using the $\overline{ALERT}$ signal if there is a mismatch. The DRAM can write data to the DRAM core without waiting for the CRC check for full writes when DM is disabled. If bad data is written to the DRAM core, then the DRAM memory controller should try to overwrite the bad data with good data; this means the DRAM controller is responsible for data coherency when DM is disabled. However, in the case where both CRC and DM are enabled via MRS (i.e. persistant mode), the DRAM will not write bad data to the core when a CRC error is detected.

$\overline{DBI}$ and CRC Both Enabled

The DRAM computes the CRC for received written data d[71:0]. Data is not inverted back based on DBI before it is used for computing CRC. The data is inverted back based on DBI before it is written to the DRAM core.

$\overline{DM}$ and CRC Both Enabled

When both DM and Write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array. If there is a CRC error, the DRAM blocks the write operation and discards the data.

CRC Simultaneous Operation Restrictions

When Write CRC is enabled MPR Writes or Per DRAM operation is not allowed.

CRC Polynomial

The CRC polynomial used by DDR4 is the ATM-8 HEC, X^8+X^2+X^1+1

A combinatorial logic block implementation of this 8-bit CRC for 72 bits of data includes 272 two-input XOR gates contained in eight 6-XOR-gate-deep trees.

The CRC polynomial and combinatorial logic used by DDR4 is the same as used on GDDR5.

The error coverage from the DDR4 polynomial used is shown in the following table.

CRC Error Detection Coverage

Error Type	Detection Capability
Random Single Bit Error	100%
Random Double Bit Error	100%
Random Odd Count Error	100%
Random one Multi-bit UI vertical column error detection excluding DBI bits	100%

CRC Combinatorial Logic Equations

```
module CRC8_D72;

// polynomial: (0 1 2 8)

// data width: 72

// convention: the first serial data bit is D[71]

// initial condition all 0 implied

function [7:0]

nextCRC8_D72;

input [71:0] Data;

reg [71:0] D;

reg [7:0] NewCRC;

begin D = Data;

NewCRC[0] = D[69] ^ D[68] ^ D[67] ^ D[66] ^ D[64] ^ D[63] ^ D[60] ^ D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^
D[48] ^ D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^ D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0] ;

NewCRC[1] = D[70] ^ D[66] ^ D[65] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^ D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^
D[45] ^ D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^ D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^ D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];

NewCRC[2] = D[71] ^ D[69] ^ D[68] ^ D[63] ^ D[62] ^ D[61] ^ D[60] ^ D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^
D[46] ^ D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^ D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];

NewCRC[3] = D[70] ^ D[69] ^ D[64] ^ D[63] ^ D[62] ^ D[61] ^ D[59] ^ D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
D[45] ^ D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^ D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1]; NewCRC[4] = D[71] ^ D[70] ^ D[65] ^ D[64] ^ D[63] ^ D[62] ^ D[60] ^
D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^ D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^ D[30] ^
D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^ D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];

NewCRC[5] = D[71] ^ D[66] ^ D[65] ^ D[64] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^
D[46] ^ D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^ D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];

NewCRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62] ^ D[61] ^ D[58] ^ D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^
D[46] ^ D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^ D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];

NewCRC[7] = D[68] ^ D[67] ^ D[66] ^ D[65] ^ D[63] ^ D[62] ^ D[59] ^ D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^
D[47] ^ D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^ D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];

nextCRC8_D72 = NewCRC;
```

Burst Ordering for BL8

DDR4 supports fixed write burst ordering [A2:A1:A0 = 0:0:0] when write CRC is enabled in BL8 (fixed).

CRC Data Bit Mapping

CRC Data Mapping (X4 Configuration, BL8)

X4	Transfer Burst Bit (BL8)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	CRC4
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	CRC5
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	CRC6
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	CRC7

CRC Data Mapping (X8 Configuration, BL8)

X8	Transfer Burst Bit (BL8)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
$\overline{DM}$ / $\overline{DBI}$	D64	D65	D66	D67	D68	D69	D70	D71	1	1

CRC Data Mapping (X16 Configuration, BL8)

X16	Transfer Burst Bit (BL8)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
$\overline{LDM}$ / $\overline{LDBI}$	D64	D65	D66	D67	D68	D69	D70	D71	1	1
DQ8	D72	D73	D74	D75	D76	D77	D78	D79	CRC8	1
DQ9	D80	D81	D82	D83	D84	D85	D86	D87	CRC9	1
DQ10	D88	D89	D90	D91	D92	D93	D94	D95	CRC10	1
DQ11	D96	D97	D98	D99	D100	D101	D102	D103	CRC11	1
DQ12	D104	D105	D106	D107	D108	D109	D110	D111	CRC12	1
DQ13	D112	D113	D114	D115	D116	D117	D118	D119	CRC13	1
DQ14	D120	D121	D122	D123	D124	D125	D126	D127	CRC14	1
DQ15	D128	D129	D130	D131	D132	D133	D134	D135	CRC15	1
$\overline{UDM}$ / $\overline{UDBI}$	D136	D137	D138	D139	D140	D141	D142	D143	1	1

A x16 device is treated as two x8 devices; a x16 device will have two identical CRC trees implemented. CRC[7:0] covers data bits d[71:0]. CRC[15:8] covers data bits d[143:72].

CRC Enabled With BC4

If CRC and BC4 (fixed, OTF not allowed) are both enabled, then address bit A2 is used to transfer critical data first for BC4 writes.

CRC with BC4 Data Bit Mapping for x4 Devices

For a x4 device, the CRC tree inputs are 16 data bits; and the inputs for the remaining bits are 1.

CRC Data Mapping (x4 Configuration, BC4, A2 = 0)

X4	Transfer Burst Bit (BC4, A2=0)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	CRC4
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	CRC5
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	CRC6
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	CRC7

CRC Data Mapping (x4 Configuration, BC4, A2 = 1)

X4	Transfer Burst Bit (BC4, A2=1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	CRC4
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	CRC5
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	CRC6
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	CRC7

When A2 = 1, data bits d[7:4] are used as inputs for d[3:0], d[15:12] are used as inputs to d[11:8] and so forth for the CRC tree.

CRC With BC4 Data Bit Mapping for x8 Devices

For a x8 device, the CRC tree inputs are 36 data bits.

CRC Data Mapping (x8 Configuration, BC4, A2 = 0)

X8	Transfer Burst Bit (BC4, A2=0)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1
$\overline{DM}$ / $\overline{DBI}$	D64	D65	D66	D67	1	1	1	1	1	1

When A2 = 0, the input bits d[67:64]) are used if $\overline{DM}$ or $\overline{DBI}$ functions are enabled. If $\overline{DM}$ and $\overline{DBI}$ are disabled then d[67:64]) are 1s.

CRC Data Mapping (x8 Configuration, BC4, A2 = 1)

X8	Transfer Burst Bit (BC4, A2=1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	1
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1
$\overline{DM}$ / $\overline{DBI}$	D68	D69	D70	D71	1	1	1	1	1	1

CRC Data Mapping (x8 Configuration, BC4, A2 = 1)

When A2 = 1, data bits d[7:4] are used as inputs for d[3:0], d[15:12] are used as inputs to d[11:8] and so forth for the CRC tree. The input bits d[71:68]) are used if $\overline{DM}$ or $\overline{DBI}$ functions are enabled; if $\overline{DM}$ and $\overline{DBI}$ are disabled then d[71:68]) are 1's.

CRC With BC4 Data Bit Mapping for x16 Devices

There are two identical CRC trees for x16 devices, each have CRC tree inputs of 36 bits.

CRC Data Mapping (x16 Configuration, BC4, A2 = 0)

X16	Transfer Burst Bit (BC4, A2=0)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1
$\overline{LDM}$ / $\overline{LDBI}$	D64	D65	D66	D67	1	1	1	1	1	1
DQ8	D72	D73	D74	D75	1	1	1	1	CRC8	1
DQ9	D80	D81	D82	D83	1	1	1	1	CRC9	1
DQ10	D88	D89	D90	D91	1	1	1	1	CRC10	1
DQ11	D96	D97	D98	D99	1	1	1	1	CRC11	1
DQ12	D104	D105	D106	D107	1	1	1	1	CRC12	1
DQ13	D112	D113	D114	D115	1	1	1	1	CRC13	1
DQ14	D120	D121	D122	D123	1	1	1	1	CRC14	1
DQ15	D128	D129	D130	D131	1	1	1	1	CRC15	1
$\overline{UDM}$ / $\overline{UDBI}$	D136	D137	D138	D139	1	1	1	1	1	1

When A2 = 0, input bits d[67:64] are used if $\overline{DM}$ or $\overline{DBI}$ functions are enabled and if $\overline{DM}$ and $\overline{DBI}$ are disabled then d[67:64] are 1; input bits d[139:136] are used if $\overline{DM}$ or $\overline{DBI}$ functions are enabled and if $\overline{DM}$ and $\overline{DBI}$ are disabled, then d[139:136] are 1's.

CRC Data Mapping (x16 Configuration, BC4, A2 = 1)

X16	Transfer Burst Bit (BC4, A2=1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	1
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1
$\overline{\text{LDM}}$ / $\overline{\text{LDBI}}$	D68	D69	D70	D71	1	1	1	1	1	1
DQ8	D76	D77	D78	D79	1	1	1	1	CRC8	1
DQ9	D84	D85	D86	D87	1	1	1	1	CRC9	1
DQ10	D92	D93	D94	D95	1	1	1	1	CRC10	1
DQ11	D100	D101	D102	D103	1	1	1	1	CRC11	1
DQ12	D108	D109	D110	D111	1	1	1	1	CRC12	1
DQ13	D116	D117	D118	D119	1	1	1	1	CRC13	1
DQ14	D124	D125	D126	D127	1	1	1	1	CRC14	1
DQ15	D132	D133	D134	D135	1	1	1	1	CRC15	1
$\overline{\text{UDM}}$ / $\overline{\text{UDBI}}$	D140	D141	D142	D143	1	1	1	1	1	1

When A2 = 1, data bits d[7:4] are used as inputs for d[3:0], d[15:12] are used as inputs to d[11:8] and so forth for the CRC tree. Input bits d[71:68] are used if $\overline{\text{DM}}$ or $\overline{\text{DBI}}$ functions are enabled and if $\overline{\text{DM}}$ and $\overline{\text{DBI}}$ are disabled then d[71:68] are 1; input bits d[143:140] are used if $\overline{\text{DM}}$ or $\overline{\text{DBI}}$ functions are enabled and if $\overline{\text{DM}}$ and $\overline{\text{DBI}}$ are disabled, then d[143:140] are 1's.

Example shown below of CRC tree when X8 is used in BC4 mode, x4 and x16 have similar differences.

CRC equations for x8 device in BC4 mode with A2=0 are as follows:

CRC[0] = D[69]=1 ^ D[68]=1 ^ D[67] ^ D[66] ^ D[64] ^ D[63]=1 ^ D[60]=1 ^ D[56] ^ D[54]=1 ^ D[53]=1 ^ D[52]=1 ^ D[50] ^ D[49] ^ D[48] ^ D[45]=1 ^ D[43] ^ D[40] ^ D[39]=1 ^ D[35] ^ D[34] ^ D[31]=1^ D[30]=1 ^ D[28]=1 ^ D[23]=1 ^ D[21]=1 ^ D[19] ^ D[18] ^ D[16] ^ D[14]=1 ^ D[12]=1 ^ D[8] ^ D[7]=1 ^ D[6] =1 ^ D[0] ;

CRC[1] = D[70]=1 ^ D[66] ^ D[65] ^ D[63]=1 ^ D[61]=1 ^ D[60]=1 ^ D[57] ^D[56] ^ D[55]=1 ^ D[52]=1 ^ D[51] ^ D[48] ^ D[46]=1 ^ D[45]=1 ^ D[44]=1 ^ D[43] ^ D[41] ^ D[39]=1 ^ D[36]=1 ^ D[34] ^ D[32] ^ D[30]=1 ^ D[29]=1 ^ D[28]=1 ^ D[24] ^ D[23]=1 ^ D[22]=1 ^ D[21]=1 ^ D[20]=1 ^ D[18] ^ D[17] ^ D[16] ^ D[15]=1 ^ D[14]=1 ^ D[13]=1 ^ D[12]=1 ^ D[9] ^ D[6]=1 ^ D[1] ^ D[0];

CRC[2] = D[71]=1 ^ D[69]=1 ^ D[68]=1 ^ D[63]=1 ^ D[62]=1 ^ D[61]=1 ^ D[60]=1 ^ D[58] ^ D[57] ^ D[54]=1 ^ D[50] ^ D[48] ^ D[47]=1 ^ D[46]=1 ^ D[44]=1 ^ D[43] ^ D[42] ^ D[39]=1 ^ D[37]=1 ^ D[34] ^ D[33] ^ D[29]=1 ^ D[28]=1 ^ D[25] ^ D[24] ^ D[22]=1 ^ D[17] ^ D[15]=1 ^ D[13]=1 ^ D[12]=1 ^ D[10] ^ D[8] ^ D[6]=1 ^ D[2] ^ D[1] ^ D[0];

CRC[3] = D[70]=1 ^ D[69]=1 ^ D[64] ^ D[63]=1 ^ D[62]=1 ^ D[61]=1 ^ D[59] ^ D[58] ^ D[55]=1 ^ D[51] ^ D[49] ^ D[48] ^ D[47]=1 ^ D[45]=1 ^ D[44]=1 ^ D[43] ^ D[40] ^ D[38]=1 ^ D[35] ^ D[34] ^ D[30]=1 ^ D[29]=1 ^ D[26] ^ D[25] ^ D[23]=1 ^ D[18] ^ D[16] ^ D[14]=1 ^ D[13]=1 ^ D[11] ^ D[9] ^ D[7]=1 ^ D[3] ^ D[2] ^ D[1];

CRC[4] = D[71]=1 ^ D[70]=1 ^ D[65] ^ D[64] ^ D[63]=1 ^ D[62]=1 ^ D[60]=1 ^ D[59] ^ D[56] ^ D[52]=1 ^ D[50] ^ D[49] ^ D[48] ^ D[46]=1 ^ D[45]=1 ^ D[44]=1 ^ D[41] ^ D[39]=1 ^ D[36]=1 ^ D[35] ^ D[31]=1 ^ D[30]=1 ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15]=1 ^ D[14]=1 ^ D[12]=1 ^ D[10] ^ D[8] ^ D[4]=1 ^ D[3] ^ D[2];

CRC[5] = D[71]=1 ^ D[66] ^ D[65] ^ D[64] ^ D[63]=1 ^ D[61]=1 ^ D[60]=1 ^ D[57] ^ D[53]=1 ^ D[51] ^ D[50] ^ D[49] ^ D[47]=1 ^ D[46]=1 ^ D[45]=1 ^ D[42] ^ D[40] ^ D[37]=1 ^ D[36]=1 ^ D[32] ^ D[31]=1 ^ D[28]=1 ^ D[27] ^ D[25] ^ D[20]=1 ^ D[18] ^ D[16] ^ D[15]=1 ^ D[13]=1 ^ D[11] ^ D[9] ^ D[5]=1 ^ D[4]=1 ^ D[3];

CRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62]=1 ^ D[61]=1 ^ D[58] ^ D[54]=1 ^ D[52]=1 ^ D[51] ^ D[50] ^ D[48] ^ D[47]=1 ^ D[46]=1 ^ D[43] ^ D[41] ^ D[38]=1 ^ D[37]=1 ^ D[33] ^ D[32] ^ D[29]=1 ^ D[28]=1 ^ D[26] ^ D[21]=1 ^ D[19] ^ D[17] ^ D[16] ^ D[14]=1 ^ D[12]=1 ^ D[10] ^ D[6]=1 ^ D[5]=1 ^ D[4]=1;

CRC[7] = D[68]=1 ^ D[67] ^ D[66] ^ D[65] ^ D[63]=1 ^ D[62]=1 ^ D[59] ^ D[55]=1 ^ D[53]=1 ^ D[52]=1 ^ D[51] ^ D[49] ^ D[48] ^ D[47]=1 ^ D[44]=1 ^ D[42] ^ D[39]=1 ^ D[38]=1 ^ D[34] ^ D[33] ^ D[30]=1 ^ D[29]=1 ^ D[27] ^ D[22]=1 ^ D[20]=1 ^ D[18] ^ D[17] ^ D[15] =1^ D[13]=1 ^ D[11] ^ D[7]=1 ^ D[6]=1 ^ D[5]=1;

CRC equations for x8 device in BC4 mode with A2=1 are as follows:

CRC[0] = 1 ^ 1 ^ D[71] ^ D[70] ^ D[68] ^ 1 ^ 1 ^ D[60] ^ 1 ^ 1 ^ 1 ^ D[54] ^ D[53] ^ D[52] ^ 1 ^ D[47] ^ D[44] ^ 1 ^ D[39] ^ D[38] ^ 1^ 1 ^ 1 ^ 1 ^ 1 ^ D[23] ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[12] ^ 1 ^ 1 ^ D[4] ;

CRC[1] = 1 ^ D[70] ^ D[69] ^ 1 ^ 1 ^ 1 ^ D[61] ^ D[60] ^ 1 ^ 1 ^ D[55] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[45] ^ 1 ^ 1 ^ D[38] ^ D[36] ^ 1 ^ 1 ^ 1 ^ D[28] ^ 1 ^ 1 ^ 1 ^ 1 ^ D[22] ^ D[21] ^ D[20] ^1 ^ 1 ^1 ^ 1 ^ D[13] ^ 1 ^ D[5] ^ D[4];

CRC[2] = 1 ^ 1 ^ 1 ^1 ^1 ^ 1 ^ 1 ^ D[62] ^ D[61] ^ 1 ^ D[54] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[46] ^ 1 ^ 1 ^ D[38] ^ D[37] ^ 1 ^ 1 ^ D[29] ^ D[28] ^ 1 ^ D[21] ^ 1 ^ 1 ^ 1 ^ D[14] ^ D12] ^1 ^ D[6] ^ D[5] ^ D[4];

CRC[3] = 1 ^ 1 ^ D[68] ^ 1 ^ 1 ^ 1 ^ 1 ^ D[63] ^ D[62] ^ 1 ^ D[55] ^ D[53] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[44] ^ 1 ^ D[39] ^ D[38] ^ 1 ^ 1 ^ D[30] ^ D[29] ^ 1 ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[15] ^ D[13] ^ 1 ^ D[7] ^ D[6] ^ D[5];

CRC[4] = 1 ^1 ^ D[69] ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[63] ^ D[60] ^ 1 ^ D[54] ^ D[53] ^ D[52] ^ 1 ^1 ^ 1 ^ D[45] ^ 1 ^ 1 ^ D[39] ^1 ^ 1 ^ D[31] ^ D[30] ^ D[28] ^ D[23] ^ D[21] ^ 1 ^ 1 ^ 1 ^ D[14] ^ D[12] ^ 1 ^ D[7] ^ D[6];

CRC[5] = 1 ^ D[70] ^ D[69] ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[61] ^ 1 ^ D[55] ^ D[54] ^ D[53] ^ 1 ^ 1 ^ 1 ^ D[46] ^ D[44] ^ 1 ^ 1 ^ D[36] ^ 1 ^ 1 ^ D[31] ^ D[29] ^ 1 ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[15] ^ D[13] ^ 1 ^ 1 ^ D[7];

CRC[6] = D[71] ^ D[70] ^ D[69] ^ D[68] ^ 1 ^ 1 ^ D[62] ^ 1 ^ 1 ^ D[55] ^ D[54] ^ D[52] ^ 1 ^1 ^ D[47] ^ D[45] ^ 1 ^ 1 ^ D[37] ^ D[36] ^1 ^ 1 ^ D[30] ^ 1 ^ D[23] ^ D[21] ^ D[20] ^ 1 ^ 1 ^ D[14] ^ 1 ^ 1 ^ 1;

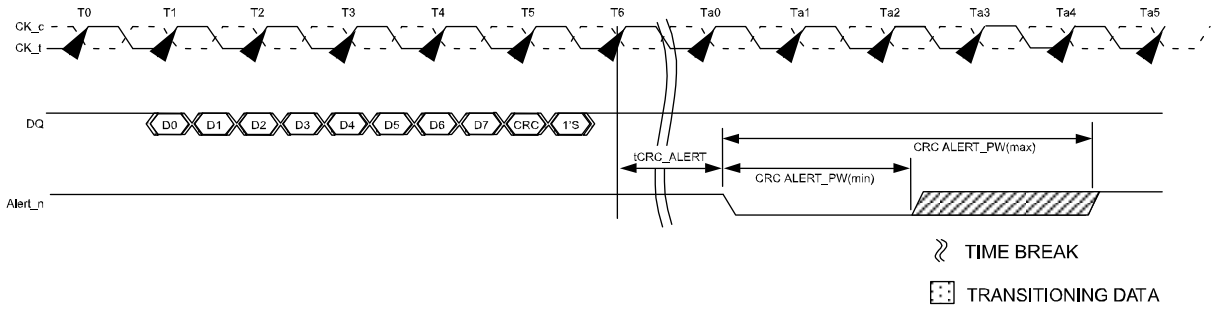
CRC[7] = 1 ^ D[71] ^ D[70] ^ D[69] ^ 1 ^ 1 ^ D[63] ^ 1 ^ 1 ^ 1 ^ D[55] ^ D[53] ^ D[52] ^ 1 ^ 1 ^ D[46] ^ 1 ^ 1 ^ D[38] ^ D[37] ^ 1 ^ 1 ^ D[31] ^ 1 ^ 1 ^ D[22] ^ D[21] ^ 1^ 1 ^ D[15] ^ 1 ^ 1 ^ 1;

CRC Error Handling

The CRC error mechanism shares the same $\overline{\text{ALERT}}$ signal as CA Parity for reporting write errors to the DRAM. The controller has two way to distinguish between CRC errors and CA Parity errors: (1) Read DRAM mode/MPR registers and (2) Measure time $\overline{\text{ALERT}}$ is low. To speed up recovery for CRC errors, CRC errors are only sent back as a "short" pulse; the maximum pulse width is in the neighborhood of ten clocks (unlike CA Parity where $\overline{\text{ALERT}}$ is low longer than 45 clocks). The $\overline{\text{ALERT}}$ low pulse could be longer than the maximum limit at the controller if there are multiple CRC errors as the $\overline{\text{ALERT}}$ is a daisy chain bus. The latency to $\overline{\text{ALERT}}$ signal is defined as tCRC_ALERT in the figure below.

The DRAM will set the Error Status bit located at MR5 [3] to a 1 upon detecting a CRC error; which will subsequently set the CRC Error Status flag in the MPR Error Log high (MPR Page1, MPR3[7]). The CRC Error Status bit [and CRC Error Status flag] remains set at 1 until the DRAM controller clears the CRC Error Status bit using an MRS command to set MR5 [3] to a 0. The DRAM controller, upon seeing an error as a pulse width, should retry the write transactions. The controller should consider the worst-case delay for $\overline{\text{ALERT}}$ (during initialization) and backup the transactions accordingly. The DRAM controller may also be made more intelligent and correlate the write CRC error to a specific rank or a transaction.

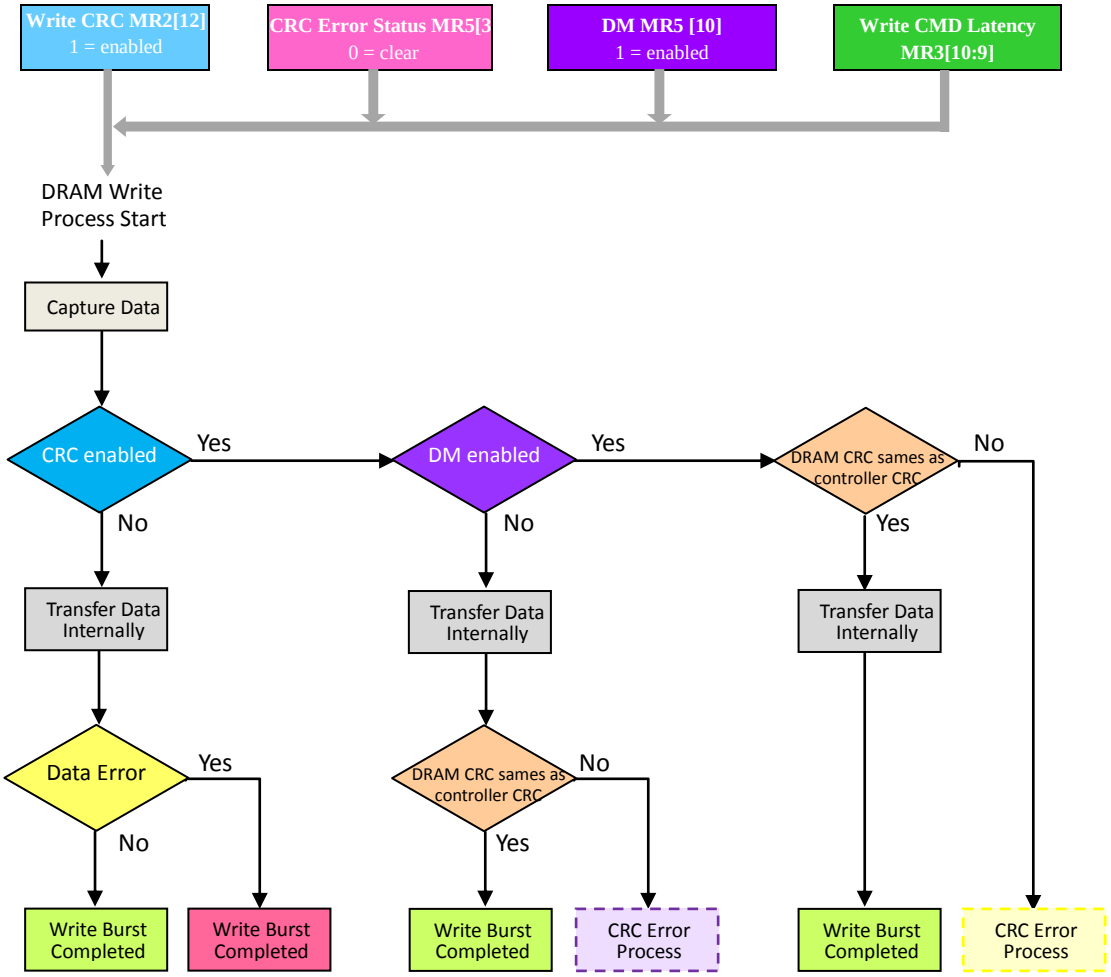
CRC Error Reporting



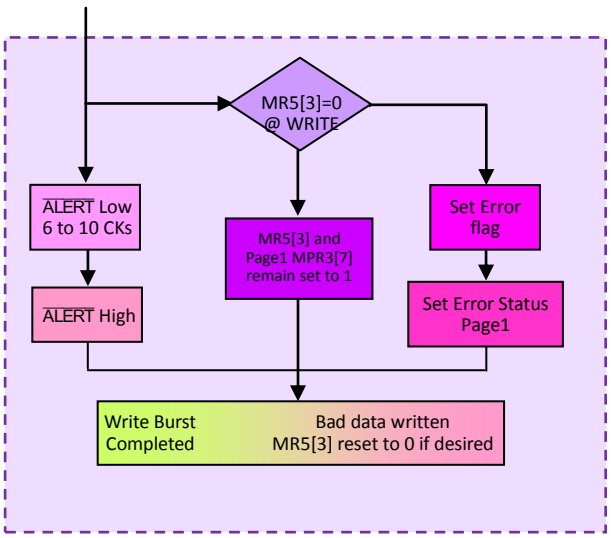
NOTE 1 D0 - D71 CRC computed by DRAM did not match CRC0-7 at T5 and started error generating process at T6.

NOTE 2 CRC ALERT_PW is specified from the point where the DRAM starts to drive the signal low to the point where the DRAM driver releases and the controller starts to pull the signal up. Timing diagram applies to x4, x8, and x16 devices.

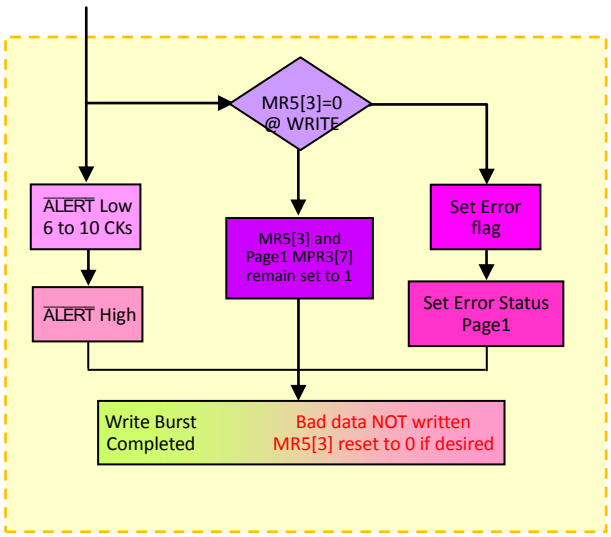
CRC Write Data Flow Diagram



CRC Error Process without DM



CRC Error Process with DM



Data Bus Inversion

Data Bus Inversion

The DATA BUS INVERSION (DBI) function is supported only for x8 and x16 configurations (not supported on x4). DBI opportunistically inverts data bits; in conjunction with the $\overline{DBI}$ I/O, less than half of the DQs will switch low for a given DQS strobe edge. The DBI function shares a common pin with the DATA MASK (DM) and TDQS functions.

The DBI function applies to both READ and WRITE operations; DBI cannot be enabled at the same time the DM function is enabled or DBI is not allowed during MPR Read operation. Valid configurations for TDQS, DM, and DBI functions are shown below.

DBI vs. DM vs. TDQS Function Matrix

Read DBI MR5[12]	Write DBI MR5[11]	Data Mask MR5[10]	TDQS (x8 only) MR1[11]
Enabled or Disabled	Disabled	Enabled	Disabled
Enabled or Disabled	Enabled	Disabled	Disabled
Enabled or Disabled	Disabled	Disabled	Disabled
Disabled	Disabled	Disabled	Enabled

DBI During a WRITE Operation

If $\overline{DBI}$ is sampled LOW on a given byte lane during a WRITE operation, the DRAM inverts write data received on the DQ inputs prior to writing the internal memory array. If $\overline{DBI}$ is sampled HIGH on a given byte lane, the DRAM leaves the data received on the DQ inputs noninverted. The write DQ frame format is shown below for x8 and x16 configurations (The x4 configuration does not support the DBI function.)

DBI Write, DQ Frame Format (x8)

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
$\overline{DM}$ or $\overline{DBI}$	DM0 or DBI0	DM1 or DBI1	DM2 or DBI2	DM3 or DBI3	DM4 or DBI4	DM5 or DBI5	DM6 or DBI6	DM7 or DBI7

DBI Write, DQ Frame Format (x16)

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
$\overline{LDM}$ or $\overline{LDBI}$	$\overline{LDM0}$ or $\overline{LDBI0}$	$\overline{LDM1}$ or $\overline{LDBI1}$	$\overline{LDM2}$ or $\overline{LDBI2}$	$\overline{LDM3}$ or $\overline{LDBI3}$	$\overline{LDM4}$ or $\overline{LDBI4}$	$\overline{LDM5}$ or $\overline{LDBI5}$	$\overline{LDM6}$ or $\overline{LDBI6}$	$\overline{LDM7}$ or $\overline{LDBI7}$
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
$\overline{UDM}$ or $\overline{UDBI}$	$\overline{UDM0}$ or $\overline{UDBI0}$	$\overline{UDM1}$ or $\overline{UDBI1}$	$\overline{UDM2}$ or $\overline{UDBI2}$	$\overline{UDM3}$ or $\overline{UDBI3}$	$\overline{UDM4}$ or $\overline{UDBI4}$	$\overline{UDM5}$ or $\overline{UDBI5}$	$\overline{UDM6}$ or $\overline{UDBI6}$	$\overline{UDM7}$ or $\overline{UDBI7}$

DBI During a READ Operation

If the number of 0 data bits within a given byte lane is greater than four during a READ operation, the DRAM inverts read data on its DQ outputs and drives the $\overline{DBI}$ pin LOW. Otherwise the DRAM does not invert the read data and drives the $\overline{DBI}$ pin HIGH. The read DQ frame format is shown below for x8 and x16 configurations (The x4 configuration does not support the DBI function.)

DBI Read, DQ Frame Format (x8)

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
$\overline{DBI}$	$\overline{DBI}$0	$\overline{DBI}$1	$\overline{DBI}$2	$\overline{DBI}$3	$\overline{DBI}$4	$\overline{DBI}$5	$\overline{DBI}$6	$\overline{DBI}$7

DBI Read, DQ Frame Format (x16)

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
$\overline{LDBI}$	$\overline{LDBI}$0	$\overline{LDBI}$1	$\overline{LDBI}$2	$\overline{LDBI}$3	$\overline{LDBI}$4	$\overline{LDBI}$5	$\overline{LDBI}$6	$\overline{LDBI}$7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
$\overline{UDBI}$	$\overline{UDBI}$0	$\overline{UDBI}$1	$\overline{UDBI}$2	$\overline{UDBI}$3	$\overline{UDBI}$4	$\overline{UDBI}$5	$\overline{UDBI}$6	$\overline{UDBI}$7

Data Mask

Data Mask

The DATA MASK (DM) function, also described as PARTIAL WRITE, is supported only for x8 and x16 configurations (not supported on x4). The DM function shares a common pin with the $\overline{DBI}$ and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the DBI function is enabled. The valid configurations for the TDQS, DM, and DBI functions are shown here.

DM vs. TDQS vs. DBI Function Matrix

Data Mask MR5[10]	TDQS (x8 only) MR1[11]	Write DBI MR5[11]	Read DBI MR5[12]
Enabled	Disabled	Disabled	Enabled or Disabled
Disabled	Enabled	Disabled	Disabled
	Disabled	Enabled	Enabled or Disabled
	Disabled	Disabled	Enabled or Disabled

When enabled, the DM function applies during a WRITE operation. If $\overline{DM}$ is sampled LOW on a given byte lane, the DRAM masks the write data received on the DQ inputs. If $\overline{DM}$ is sampled HIGH on a given byte lane, the DRAM does not mask the data and writes this data into the DRAM core. The DQ frame format for x8 and x16 configurations is shown here. If both CRC Write and DM are enabled (via MRS), the CRC will be checked and valid prior to the DRAM writing data into the DRAM core. If a CRC error occurs while the DM feature is enabled, CRC Write Persistent Mode will be enabled and data will not be written into the DRAM core. In the case of CRC Write enabled and DM disabled (via MRS), ie. CRC Write non-Persistent Mode, data is written to the DRAM core even if a CRC error occurs.

Data Mask, DQ Frame Format (x8)

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
$\overline{DM}$ or $\overline{DBI}$	DM0 or DBI0	DM1 or DBI1	DM2 or DBI2	DM3 or DBI3	DM4 or DBI4	DM5 or DBI5	DM6 or DBI6	DM7 or DBI7

Data Mask, DQ Frame Format (x16)

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
$\overline{LDM}$ or $\overline{LDBI}$	$\overline{LDM0}$ or $\overline{LDBI0}$	$\overline{LDM1}$ or $\overline{LDBI1}$	$\overline{LDM2}$ or $\overline{LDBI2}$	$\overline{LDM3}$ or $\overline{LDBI3}$	$\overline{LDM4}$ or $\overline{LDBI4}$	$\overline{LDM5}$ or $\overline{LDBI5}$	$\overline{LDM6}$ or $\overline{LDBI6}$	$\overline{LDM7}$ or $\overline{LDBI7}$
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
$\overline{UDM}$ or $\overline{UDBI}$	$\overline{UDM0}$ or $\overline{UDBI0}$	$\overline{UDM1}$ or $\overline{UDBI1}$	$\overline{UDM2}$ or $\overline{UDBI2}$	$\overline{UDM3}$ or $\overline{UDBI3}$	$\overline{UDM4}$ or $\overline{UDBI4}$	$\overline{UDM5}$ or $\overline{UDBI5}$	$\overline{UDM6}$ or $\overline{UDBI6}$	$\overline{UDM7}$ or $\overline{UDBI7}$

Programmable Preamble Modes and DQS Postambles

Programable Preamble Modes and DQS Postambles

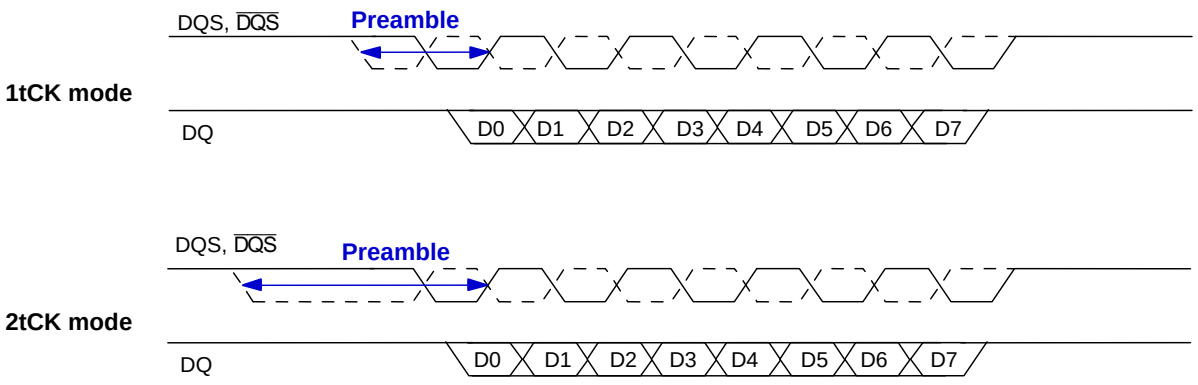
DDR4 supports programmable Write and Read Preamble Modes; either the normal 1 tCK Preamble Mode or special 2 tCK Preamble Mode. The 2 tCK Preamble Mode places special timing constraints on many operational features as well as the 2 tCK Preamble Mode is supported for data rates of DDR4-2666 and faster. The Write Preamble 1 tCK or 2 tCK Mode can be selected independently from Read Preamble 1 tCK or 2 tCK Mode.

Read Preamble Training is also supported; this mode can be used by the DRAM controller to train or "read level" the DQS receivers.

Write Preamble Mode

MR4 [12] = 0 selects 1 tCK Write Preamble Mode while MR4 [12] = 1 selects 2 tCK Write Preamble Mode, examples in the figures below.

1tCK vs 2tCK Write Preamble Mode



CWL has special considerations when in the 2 tCK Write Preamble Mode. The CWL value selected in MR2[5:3], as seen in table below, requires an additional clock(s) when the primary CWL value and 2 tCK Write Preamble mode are used while additional clock(s) are not required when the alternate CWL value and 2 tCK Write Preamble mode are used.

CWL Selection

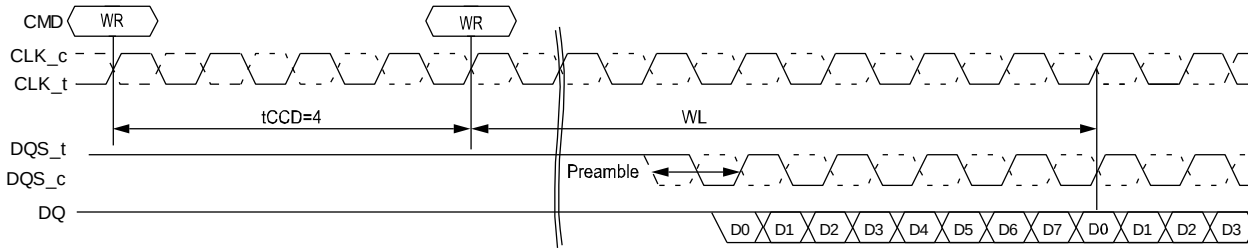
	CWL - Primary Choice		CWL - Alternate Choice	
Speed Bin	1 tCK Preamble	2 tCK Preamble	1 tCK Preamble	2 tCK Preamble
DDR4-2133	11	na	14	na
DDR4-2400	12	na	16	na
DDR4-2666	14	16	18	18
DDR4-3200	16	18	na	na

NOTE 1 CWL programmable requirement for MR2[5:3]

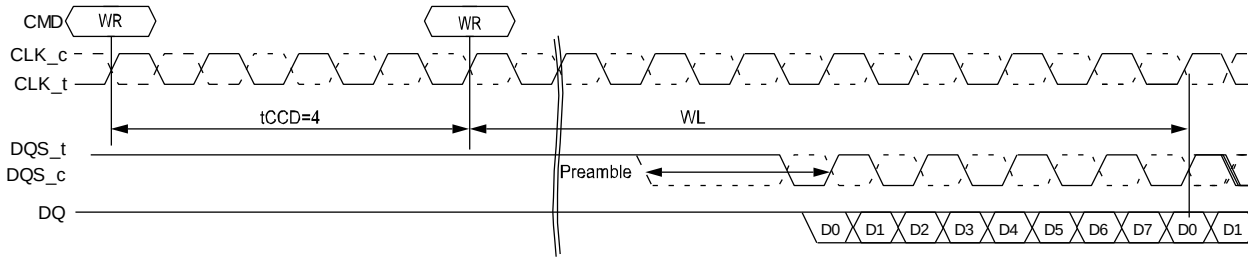
When operating in 2tCK Write Preamble Mode, tWTR (command based) and tWR (MR0[11:9]) must be programmed to a value 1 clock greater than the tWTR and tWR setting normally required for the applicable speed bin. The $\overline{CAS}$ to $\overline{CAS}$ command delay to either different bank group (tCCD_S) or same bank group (tCCD_L) have minimum timing requirements that must be satisfied between Write commands and are stated in the Timing Parameters by Speed Bin tables. When operating in 2tCK Write Preamble Mode, tCCD_S and tCCD_L must also be even number of clocks; if the minimum timing specification requires only 5tCKs, the 5tCKs has to be rounded up to 6tCKs when operating in 2tCK Write Preamble Mode while 5tCKs would be acceptable if operating in 1tCK Write Preamble Mode

1tCK vs 2tCK Write Preamble Mode, tCCD=4 (AL=PL=0)

1tCK mode

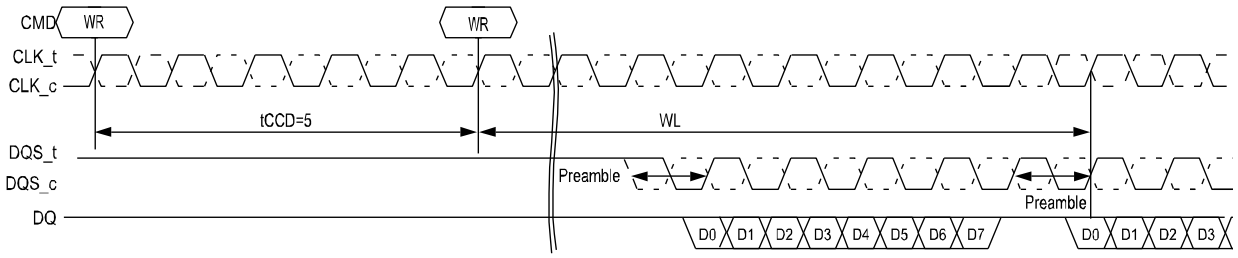


2tCK mode



1tCK vs 2tCK Write Preamble Mode, tCCD=5 (AL=PL=0)

1tCK mode

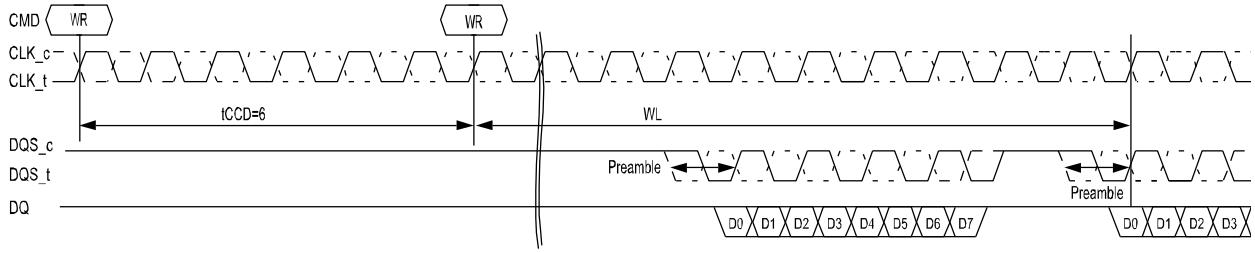


2tCK mode: tCCD=5 is not allowed in 2tCK mode

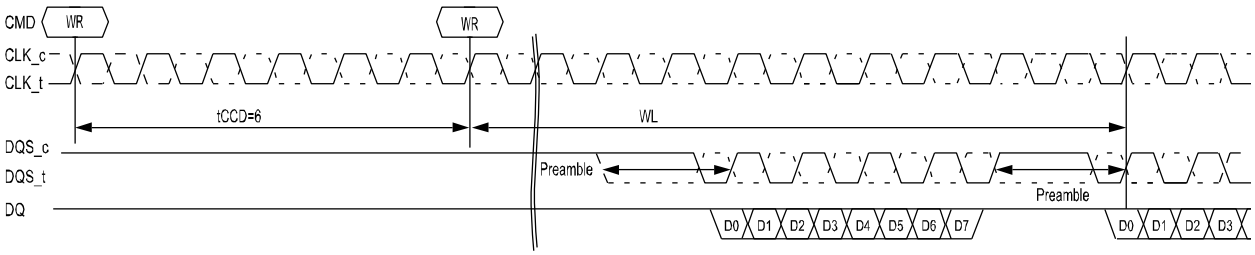
NOTE 1 tCCD__S and tCCD_L = 5 tCKs not allowed when in 2tCK Write Preamble Mode.

1tCK vs 2tCK Write Preamble Mode, tCCD=6 (AL=PL=0)

1tCK mode



2tCK mode



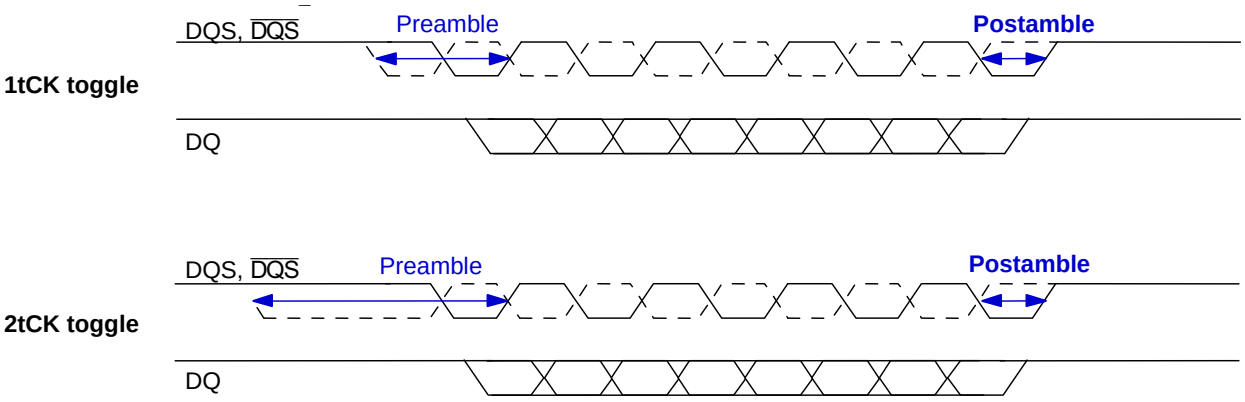
Write Postamble

Whether the 1 tCK or 2 tCK Write Preamble Mode is selected, the Write Postamble remains the same at 1/2 tCK.

DDR4 will support a fixed Write postamble.

Write postamble nominal is 0.5tck for preamble modes 1,2 Tck are shown below:

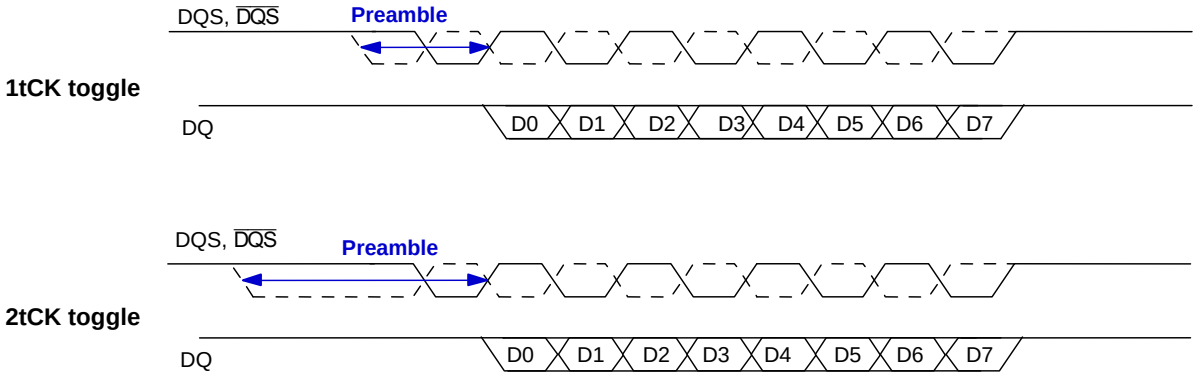
Write Postamble



Read Preamble Mode

MR4 [11] = 0 selects 1 tCK Read Preamble Mode while MR4 [12] = 1 selects 2 tCK Read Preamble Mode, example in the figures below.

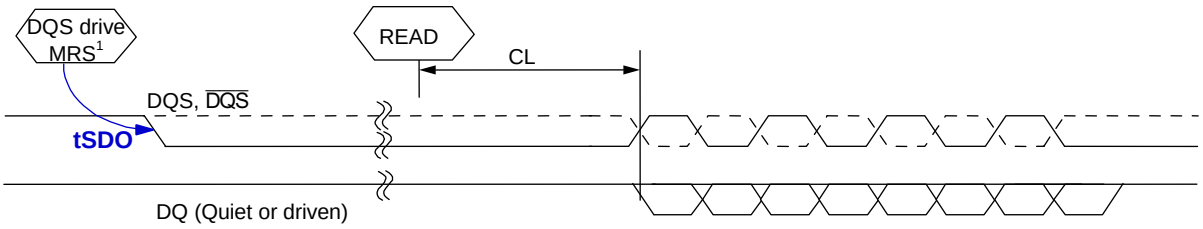
1tCK vs 2tCK Read Preamble Mode



Read Preamble Training

DDR4 supports Read Preamble Training via MPR Reads; that is Read Preamble Training is allowed only when the DRAM is in the MPR access mode. The Read Preamble Training Mode can be used by the DRAM controller to train or "read level" its DQS receivers. Read Preamble Training is entered via an MRS command; MR4[10] = 1 enabled while MR4[10] = 0 is disabled. Once the MRS command is issued to enable Read Preamble Training, the DRAM DQS and $\overline{DQS}$ signals are driven to a valid level by time tSDO is satisfied. During this time, the data bus DQ signals are held quiet, ie. driven HIGH. The DQS signal remain driven LOW and the $\overline{DQS}$ signal remain driven HIGH until an MPR Page1 READ (Page 0 through Page 3 determine which pattern is used) command is issued; and once CAS latency (CL) has expired, the DQS signals will toggle normally depending on the burst length setting. To exit Read Preamble Training Mode, an MRS command must be issued, MR4[10] = 0.

Read Preamble Training



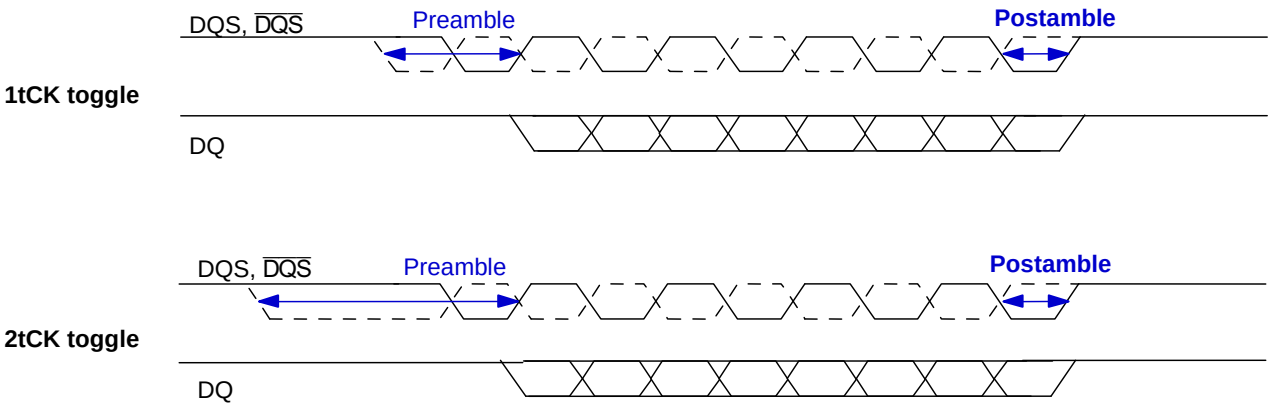
Read Postamble

Whether the 1 tCK or 2 tCK Read Preamble Mode is selected, the Read Postamble remains the same at 1/2 tCK.

DDR4 will support a fixed read postamble.

Read postamble of nominal 0.5tck for preamble modes 1,2 Tck are shown below:

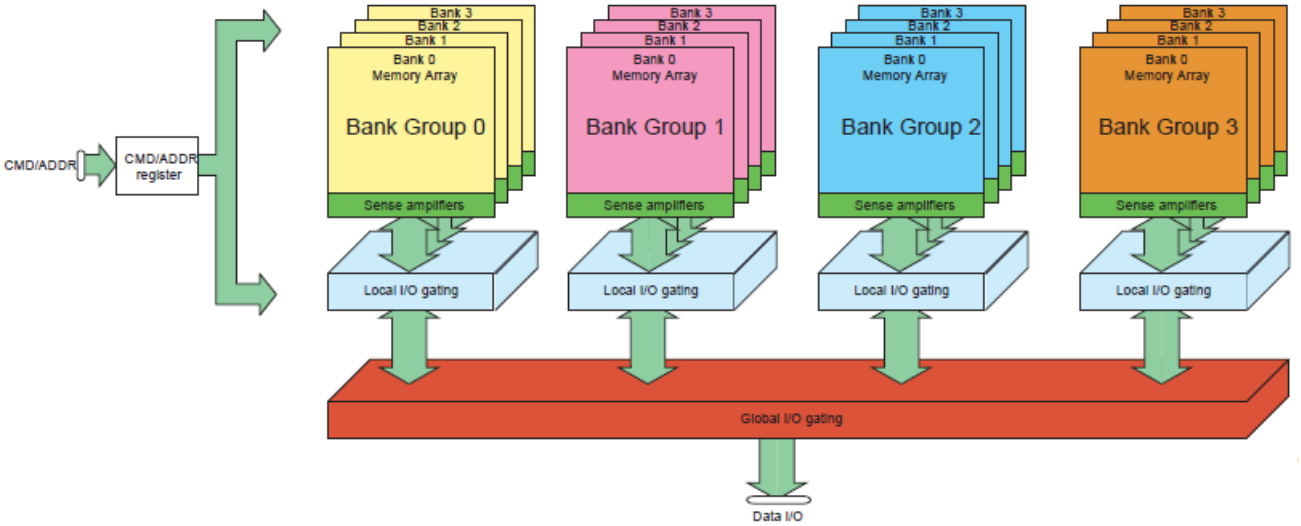
Read Postamble



Bank Access Operation

DDR4 supports bank grouping: x4/x8 DRAMs have four Bank Groups (BG[1:0]) and each bank group is comprised of four sub-banks (BA[1:0]); x16 DRAMs have two Bank Groups (BG[0]) and each bank group is comprised of made up of four sub-banks. Bank accesses to different banks groups require less time delay between accesses than Bank accesses to within the same banks group. Bank accesses to different bank groups requiretCCD_S (or short) delay between commands while Bank accesses within the same bank group requiretCCD_L (or long) delay between commands.

Bank Group x4/x8 Block Diagram



NOTE 1 Bank accesses to different bank groups require tCCD_S
NOTE 2 Bank accesses within the same bank group require tCCD_L

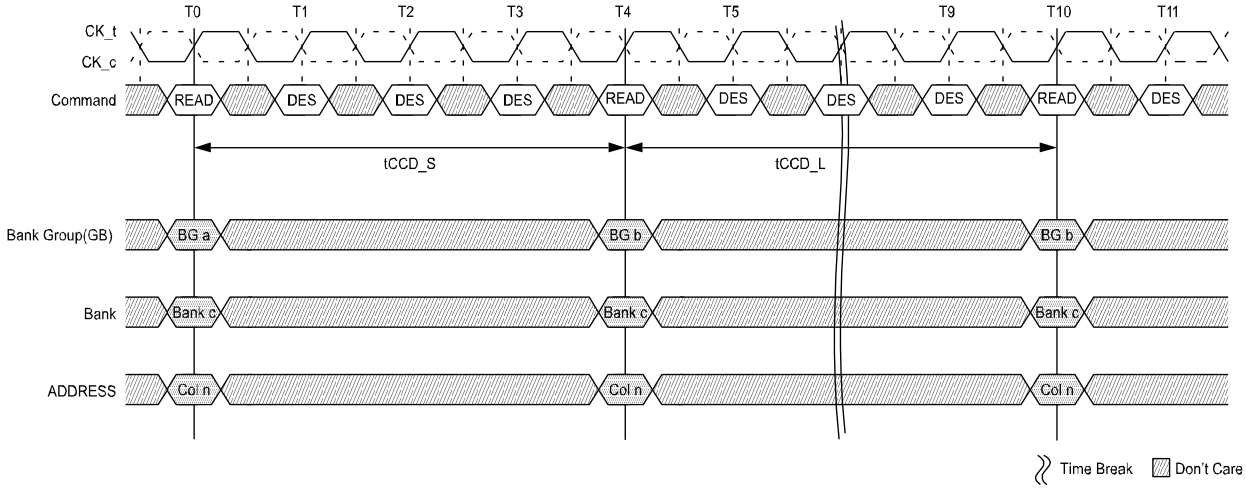
Splitting the Banks in to Bank Groups with sub-banks improved some bank access timings and increased others. However, considering DDR4 did not increase the prefetch from 8n to 16n, the penalty for staying 8n prefetch was significantly mitigated by using Bank Groups. The table below summaries the timings affected.

DDR4 Bank Group Timings

Parameter	DDR4-2133	DDR4-2400
tCCD_S	4 nCK	4 nCK
tCCD_L	6 nCK	6 nCK
tRRD_S(1/2K)	4 nCK or 3.7ns	4 nCK or 3.3ns
tRRD_L(1/2K)	4 nCK or 5.3ns	4 nCK or 4.9ns
tRRD_S(1K)	4 nCK or 3.7ns	4 nCK or 3.3ns
tRRD_L(1K)	4 nCK or 5.3ns	4 nCK or 4.9ns
tRRD_S(2K)	4 nCK or 5.3ns	4 nCK or 5.3ns
tRRD_L(2K)	4 nCK or 6.4ns	4 nCK or 6.4ns
tWTR_S	2 nCK or 2.5ns	2 nCK or 2.5ns
tWTR_L	4 nCK or 7.5ns	4 nCK or 7.5ns

NOTE 1 Refer to Timing Tables for actual specification values, these shown for reference only and are not verified to be correct.
NOTE 2 Timings with both nCK and ns require both to be satisfied; that is, the larger time of the two cases need to be satisfied.

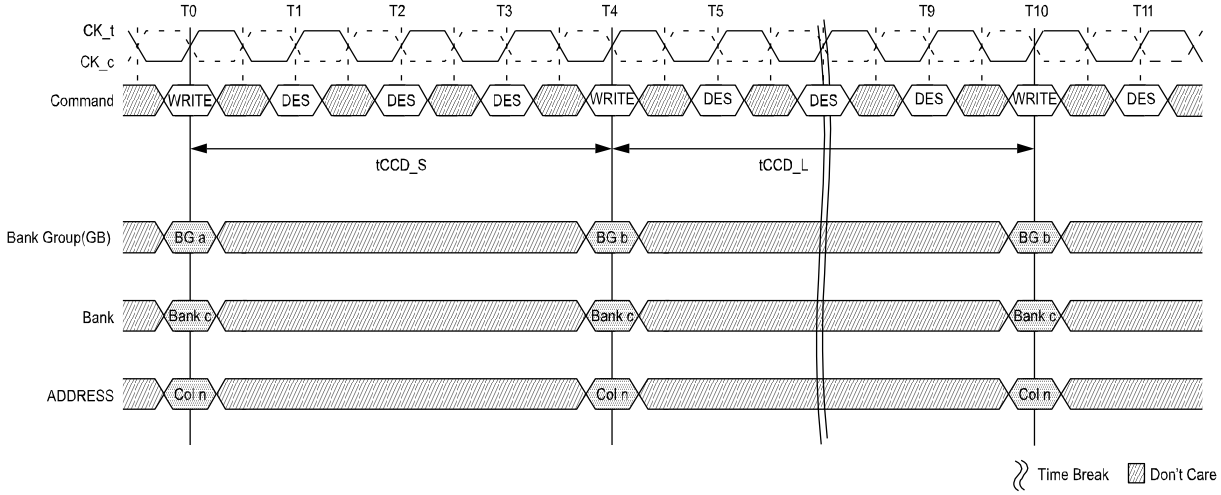
READ Burst tCCD_S and tCCD_L Examples



NOTE 1 tCCD_S; $\overline{CAS}$-to-$\overline{CAS}$ delay (short). Applies to consecutive $\overline{CAS}$ to different bank groups (i.e., T0 to T4).

NOTE 2 tCCD_L; $\overline{CAS}$-to-$\overline{CAS}$ delay (long). Applies to consecutive $\overline{CAS}$ to the same bank group (i.e., T4 to T10).

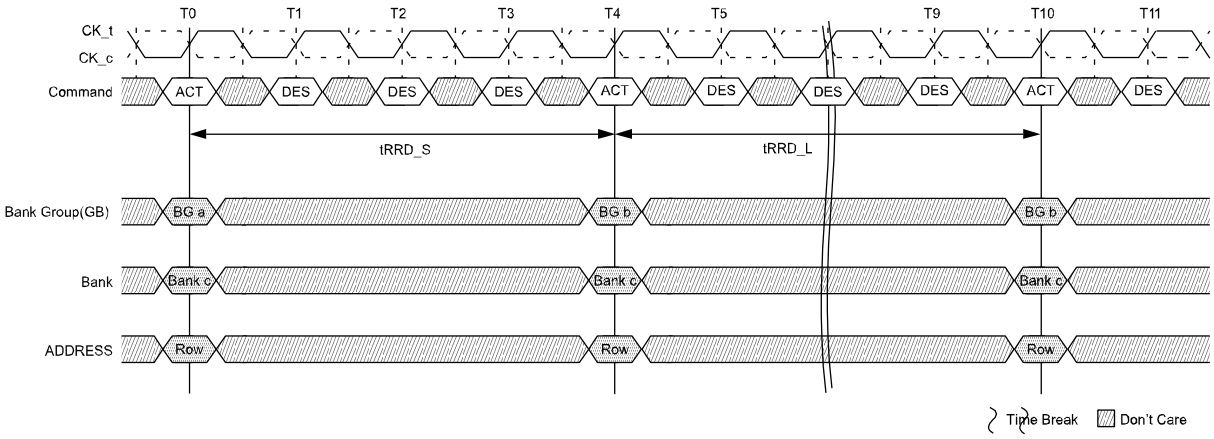
Write Burst tCCD_S and tCCD_L Examples



NOTE 1 tCCD_S; $\overline{CAS}$-to-$\overline{CAS}$ delay (short). Applies to consecutive $\overline{CAS}$ to different bank groups (i.e., T0 to T4).

NOTE 2 tCCD_L; $\overline{CAS}$-to-$\overline{CAS}$ delay (long). Applies to consecutive $\overline{CAS}$ to the same bank group (i.e., T4 to T10).

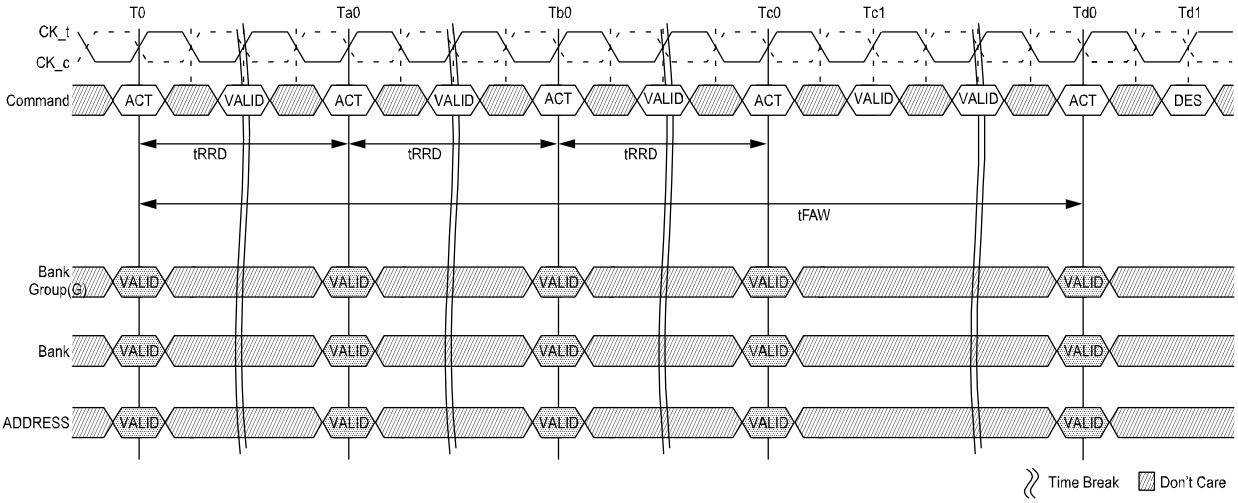
tRRD Timing



NOTE 1 tRRD_S; ACTIVATE-to-ACTIVATE command period (short); applies to consecutive ACTIVATE commands to different bank groups (i.e., T0 and T4) .

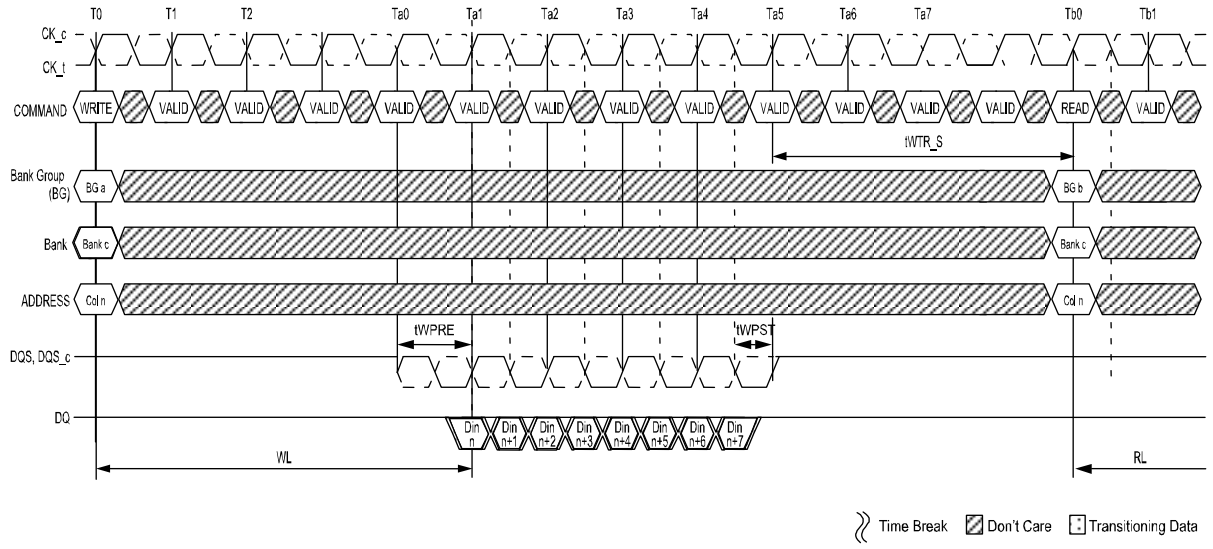
NOTE 2 tRRD_L; ACTIVATE-to-ACTIVATE command period (long); applies to consecutive ACTIVATE commands to the different banks in the same bank group (i.e., T4 and T10).

tFAW Timing



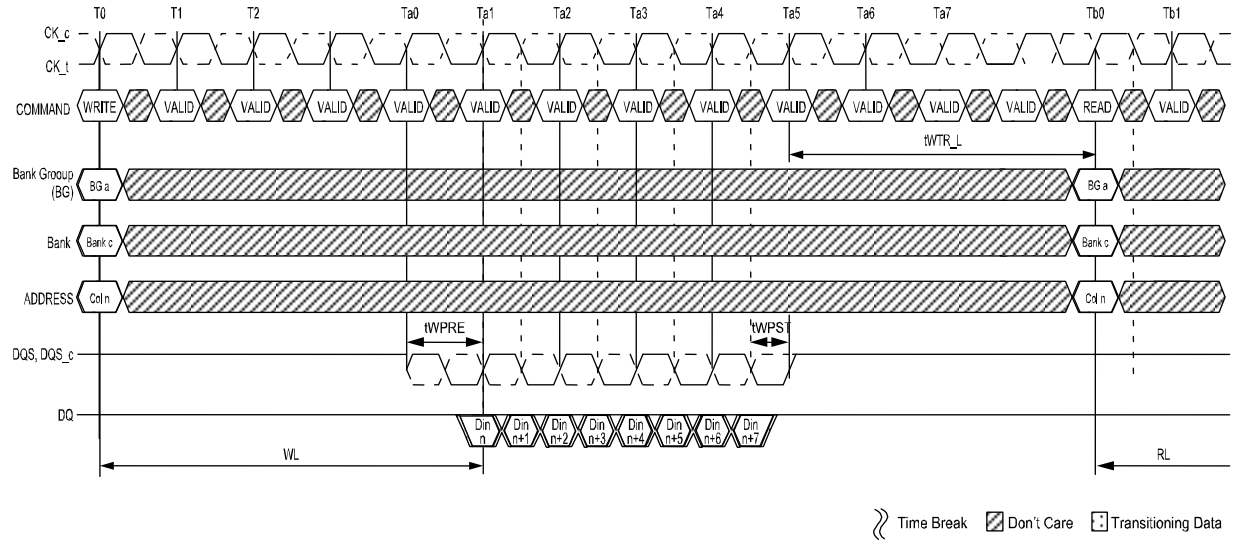
NOTE 1 tFAW : Four activate window :

tWTR_S Timing (WRITE-to-READ, Different Bank Group, CRC and DM Disabled)



NOTE 1 tWTR_S: delay from start of internal write transaction to internal READ command to a different bank group.

tWTR_L Timing (WRITE-to-READ, Same Bank Group, CRC and DM Disabled)



NOTE 1 tWTR_L: delay from start of internal write transaction to internal READ command to the same bank group.

Read Operation

Read Timing Definitions

Read timings are shown below and are applicable in normal operation mode, i.e. when the DLL is enabled and locked.

Rising data strobe edge parameters:

• tDQSCK MIN/MAX describes the allowed range for a rising data strobe edge relative to CK, $\overline{CK}$.

• tDQSCK is the actual position of a rising strobe edge relative to CK, $\overline{CK}$.

• tQSH describes the DQS, $\overline{DQS}$ differential output HIGH time.

• tDQSQ describes the latest valid transition of the associated DQ pins.

• tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

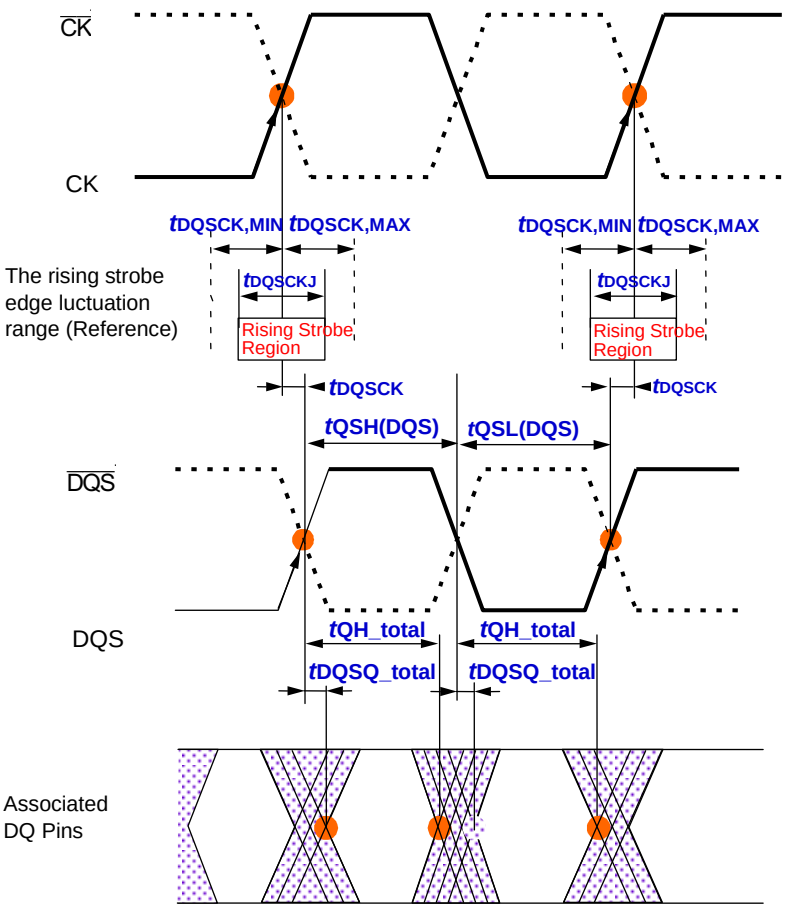
• tQSL describes the DQS, $\overline{DQS}$ differential output LOW time.

• tDQSQ describes the latest valid transition of the associated DQ pins.

• tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.

READ Timing Definition



READ Timing – Clock to Data Strobe Relationship

The clock to data strobe relationship is shown below and is applicable in normal operation mode, i.e. when the DLL is enabled and locked. Rising data strobe edge parameters:

• tDQSCK MIN/MAX describes the allowed range for a rising data strobe edge relative to CK, $\overline{CK}$.

• tDQSCK is the actual position of a rising strobe edge relative to CK, $\overline{CK}$.

• tQSH describes the data strobe high pulse width.

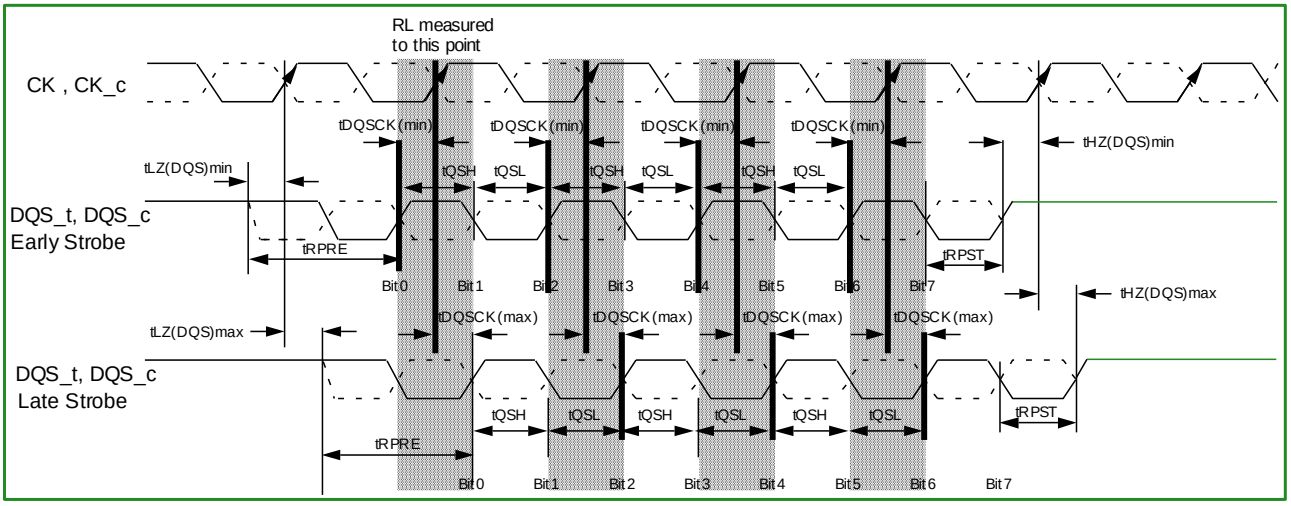
• tHZ(DQS) DQS strobe going to high, non-drive level; detailed in postamble section.

Falling data strobe edge parameters:

• tQSL describes the data strobe low pulse width.

• tLZ(DQS) DQS strobe going to low, initial drive level; detailed in preamble section

Clock to Data Strobe Relationship



NOTE 1 Within a burst, the rising strobe edge will be vary within tDQSCKj with a fixed and constant VDD. However, when the device, voltage, and temperature variation are incorporated,the rising strobe edge will be vary between tDQSCK(MIN) and tDQSCK(MAX).

NOTE 2 Notwithstanding Note 1, a rising strobe edge with tDQSCK (MAX) at T(n) can not be immediately followed by a rising strobe edge with tDQSCK (MIN) at T(n+1) because other timing relationships (tQSH, tQSL) exist: if tDQSCK(n+1) < 0: tDQSCK(n) < 1.0 tCK - (tQSH (MIN) + tQSL (MIN) - | tDQSCK(n+1) |

NOTE 3 The DQS, $\overline{DQS}$ differential output HIGH time is defined by tQSH and the DQS, DQS# differential output LOW time is defined by tQSL.

NOTE 4 Likewise,tLZ(DQS) MIN and tHZ(DQS) MIN are not tied to tDQSCK (MIN) (early strobe case) and tLZ(DQS) MAX and tHZ(DQS) MAX are not tied to tDQSCK (MAX) (late strobe case).

NOTE 5 The minimum pulse width of read preamble is defined by tRPRE (MIN).

NOTE 6 The maximum read postamble is bound by tDQSCK (MIN) plus tQSH (MIN) on the left side and tHZDSQ (MAX) on the right side.

NOTE 7 The minimum pulse width of read postamble is defined by tRPST (MIN).

NOTE 8 The maximum read preamble is bound by tLZDQS (MIN) on the left side and tDQSCK (MAX) on the right side.

READ Timing – Data Strobe to Data Relationship

The data strobe to data relationship is shown below and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

• tDQSQ describes the latest valid transition of the associated DQ pins.

• tQH describes the earliest invalid transition of the associated DQ pins.

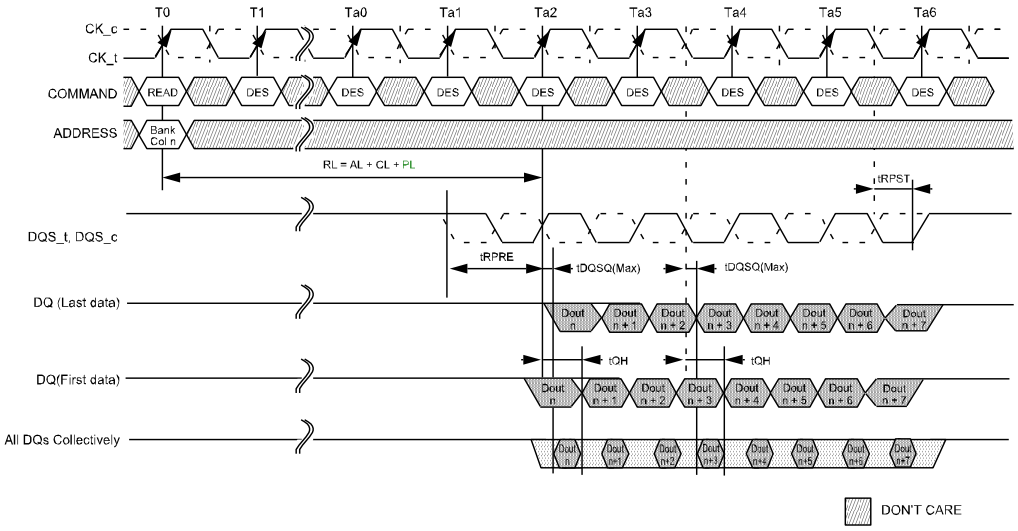
Falling data strobe edge parameters:

• tDQSQ describes the latest valid transition of the associated DQ pins.

• tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.

Data Strobe to Data Relationship



NOTE 1 BL = 8, RL = 11 (AL = 0, CL = 1) , Premable = 1CK

NOTE 2 DOUTn = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0.

NOTE 5 Output timings are referenced to VDDQ, and DLL on for locking.

NOTE 6 tDQSQ defines the skew between DQS, $\overline{DQS}$ to data and does not define DQS, $\overline{DQS}$ to clock.

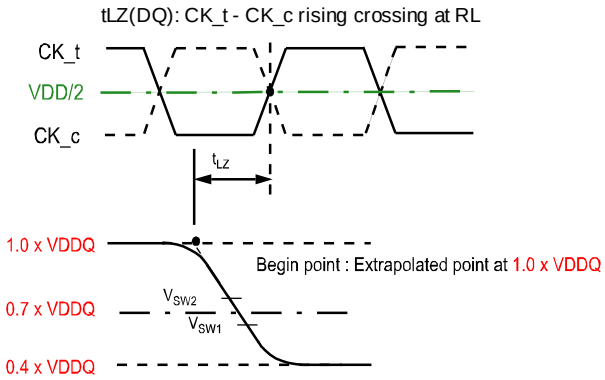
NOTE 7 Early data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

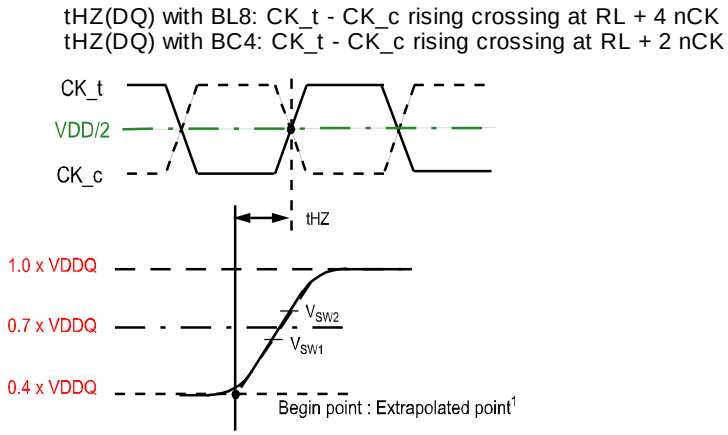
tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ).

The figure below shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as singled ended.

tLZ(DQ) and tHZ(DQ) method for calculating transitions and begin points



tLZ(DQ) begin point is above-mentioned extrapolated point.



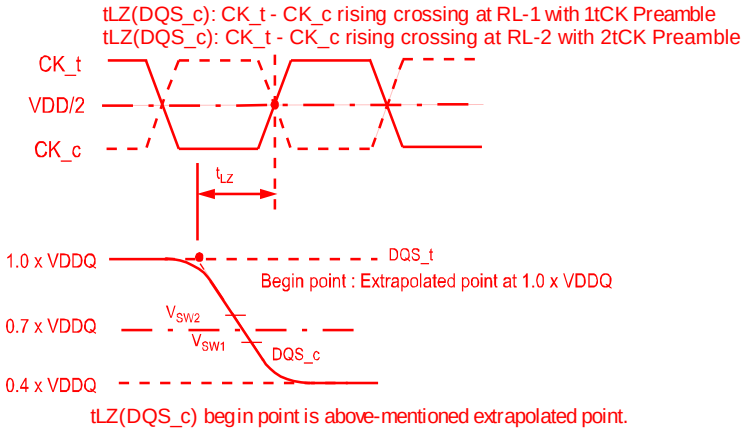
tHZ(DQ) is begin point is above-mentioned extrapolated point.

NOTE 1 Extrapolated point (Low Level) = VDDQ/(50+34) X 34
= VDDQ x 0.40
- A driver impedance : RZQ/7(34ohm)
- An effective test load : 50 ohm to VTT = VDDQ

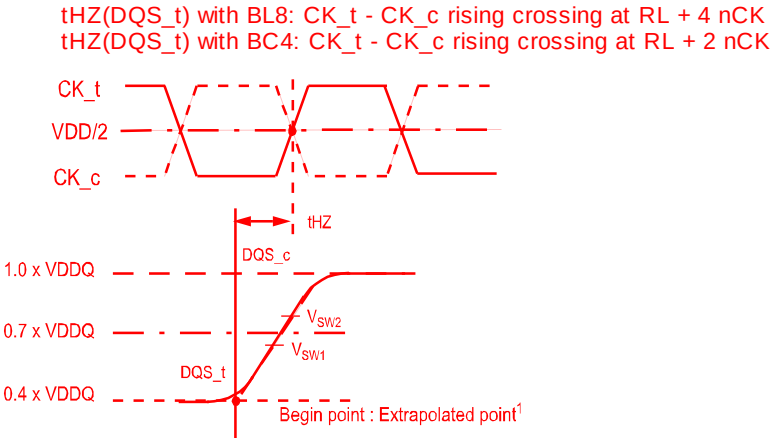
Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1 [V]	Vsw2 [V]
tLZ(DQ)	DQ low-impedance time from CK, $\overline{CK}$	(0.70 – 0.04) x VDDQ	(0.70 + 0.04) x VDDQ
tHZ(DQ)	DQ high-impedance time from CK, $\overline{CK}$	(0.70 – 0.04) x VDDQ	(0.70 + 0.04) x VDDQ

tLZ($\overline{DQS}$) and tHZ(DQS) method for calculating transitions and begin points



tLZ(DQS_c) begin point is above-mentioned extrapolated point.



tHZ(DQS_t) begin point is above-mentioned extrapolated point.

NOTE 1 Extrapolated point (Low Level) = VDDQ/(50+34) X 34
= VDDQ x 0.40
- A driver impedance : RZQ/7(34ohm)
- An effective test load : 50 ohm to VTT = VDDQ

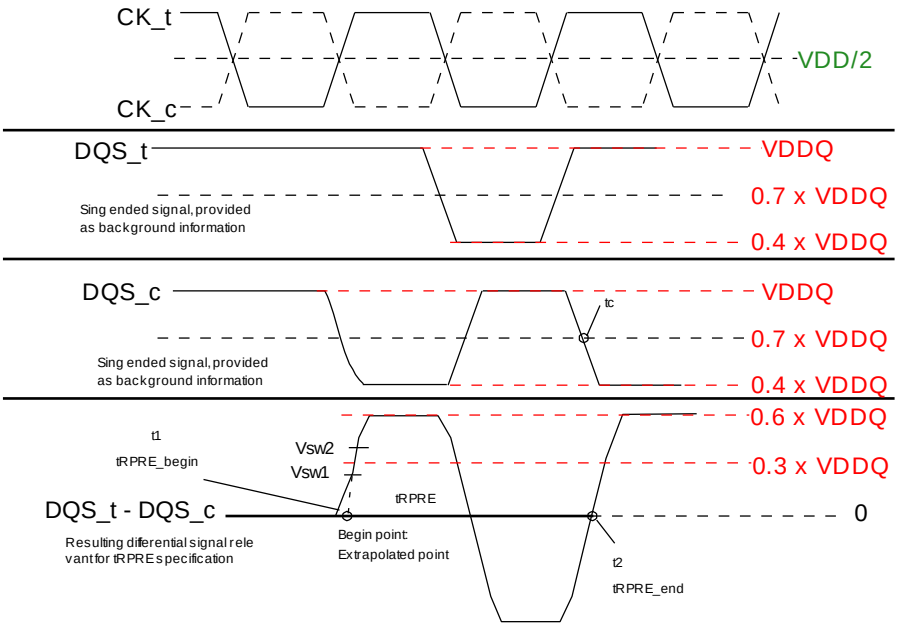
Reference Voltage for tLZ($\overline{DQS}$), tHZ(DQS) Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1 [V]	Vsw2 [V]
tLZ($\overline{DQS}$)	$\overline{DQS}$ low-impedance time from CK, $\overline{CK}$	(0.70 – 0.04) x VDDQ	(0.70 + 0.04) x VDDQ
tHZ(DQS)	DQS high-impedance time from CK, $\overline{CK}$	(0.70 – 0.04) x VDDQ	(0.70 + 0.04) x VDDQ

tRPRE Calculation

The method for calculating differential pulse widths for tRPRE is shown in figure below

tRPRE Method for Calculating Transitions and Endpoints



NOTE 1 Low Level of DQS and $\overline{DQS}$ = VDDQ/(50+34) x 34 = VDDQ x 0.40

- A driver impedance : RZQ/7(34Ω)
- An effective test load : 50 Ωto VTT = VDDQ

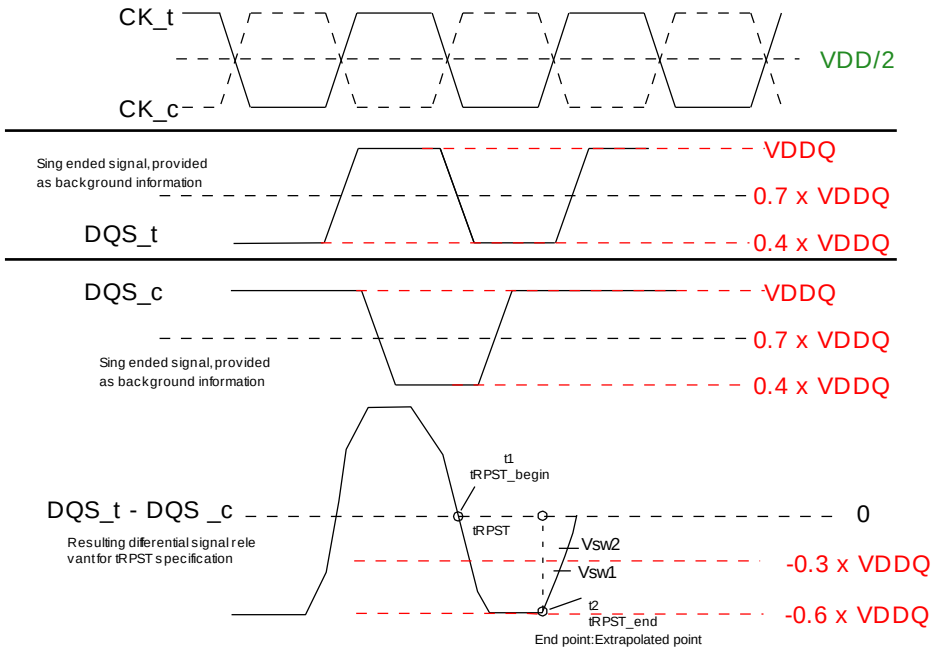
Reference Voltage for tRPRE Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1 [V]	Vsw2 [V]
tRPRE	DQS, $\overline{DQS}$ differential READ Preamble	(0.30 – 0.04) x VDDQ	(0.30 + 0.04) x VDDQ

tRPST Calculation

The method for calculating differential pulse widths for tRPST is shown in figure below

tRPST Method for Calculating Transitions and Endpoints



NOTE 1 Low Level of DQS and $\overline{DQS}$ = VDDQ/(50+34) x 34 = VDDQ x 0.40

- A driver impedance : RZQ/7(34 Ω)
- An effective test load : 50 Ω to VTT = VDDQ

Reference Voltage for tRPST Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1 [V]	Vsw2 [V]
tRPST	DQS, $\overline{DQS}$ differential READ Postamble	(-0.30 – 0.04) x VDDQ	(-0.30 + 0.04) x VDDQ

READ Burst Operation

DDR4 READ command supports bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF when OTF is enabled:

• A12 = 0, BC4 (BC4 = burst chop)

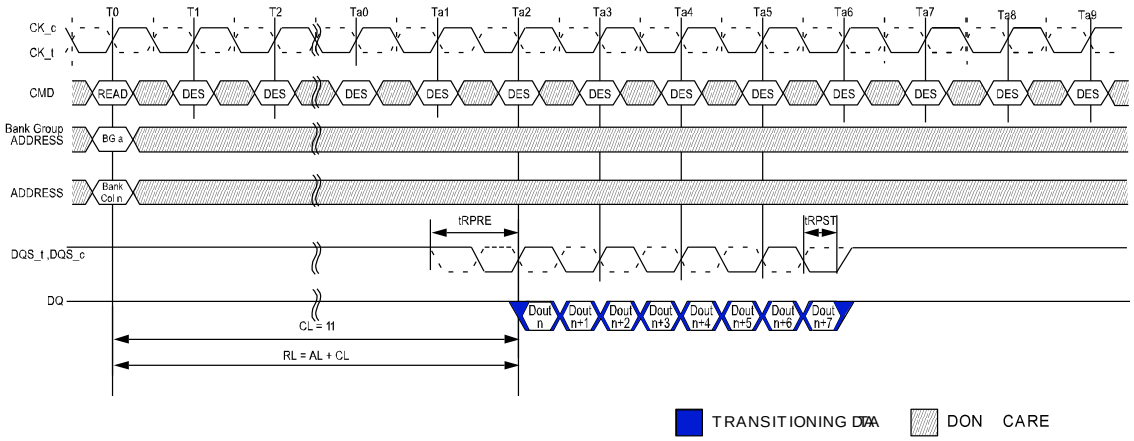
• A12 = 1, BL8

Read commands can issue precharge automatically with a read with auto-precharge command (RDA); and is enabled by A10 high.

• Read command with A10 = 0 (RD) performs standard Read, bank remains active after read burst.

• Read command with A10 = 1 (RDA) performs Read with auto-precharge, back goes in to precharge after read burst.

READ Burst Operation RL = 11 (AL = 0, CL = 11, BL8)



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK

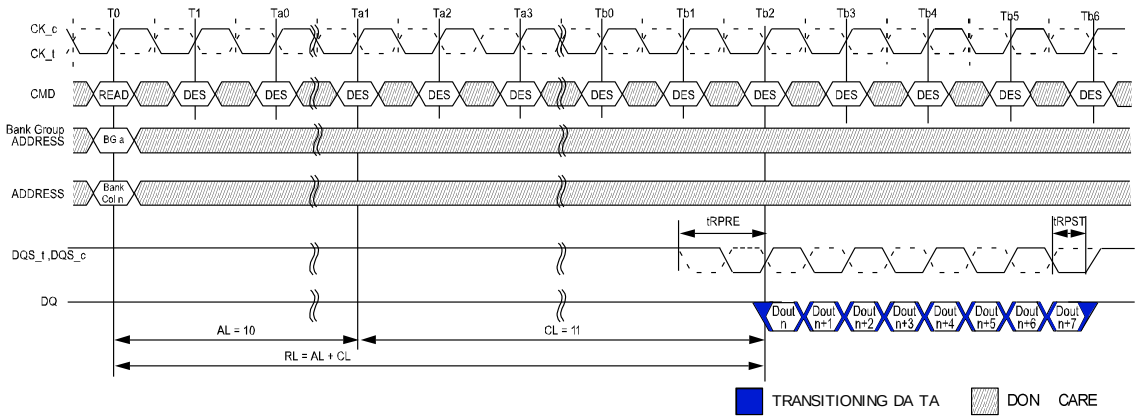
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable

READ Burst Operation RL = 21 (AL = 10, CL = 11, BL8)



NOTE 1 BL = 8, RL = 21, AL = (CL-1), CL = 11, Preamble = 1tCK

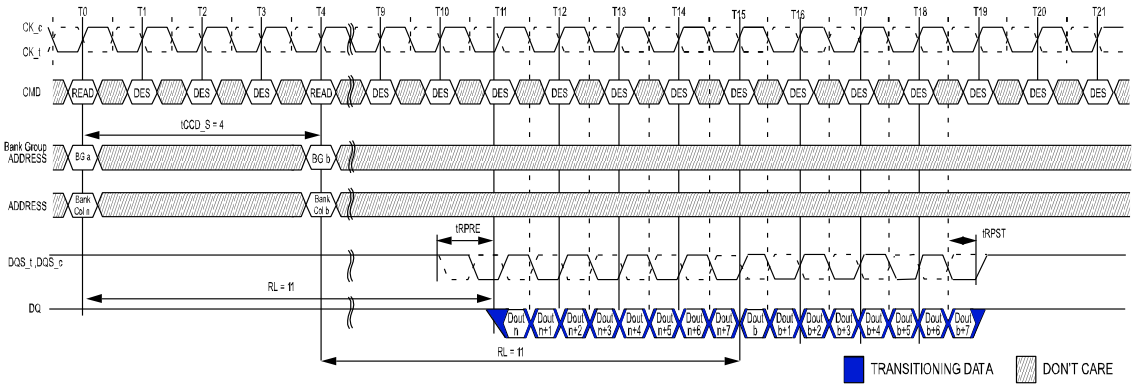
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable

Consecutive READ (BL8) with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK

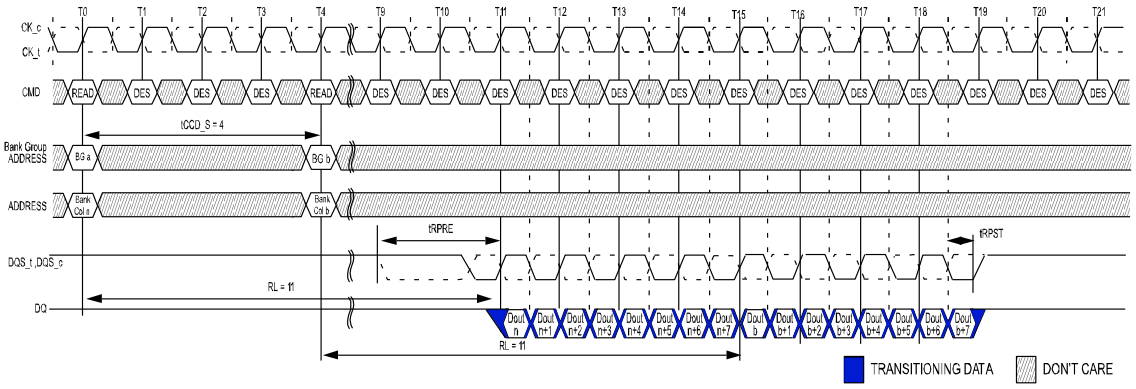
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable

Consecutive READ (BL8) with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 2tCK

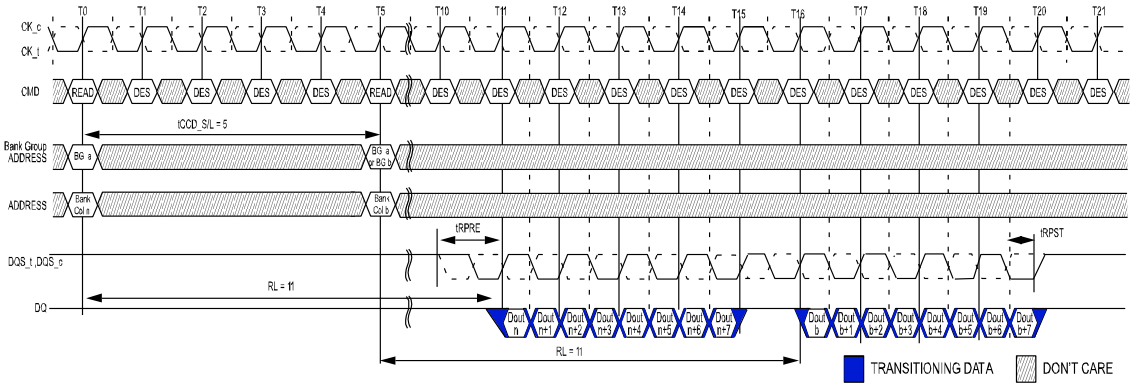
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A:0 = 0:1] and A12 = 1 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable

Nonconsecutive READ (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK, tCCD_S/L = 5

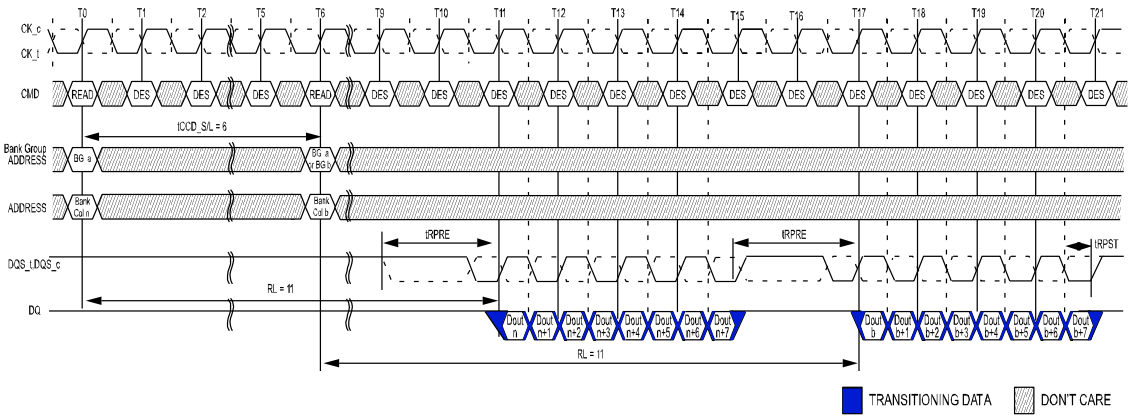
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T5.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable

Nonconsecutive READ (BL8) with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 2tCK, tCCD_S/L = 6

NOTE 2 DOUT n (or b) = data-out from column n (or column b).

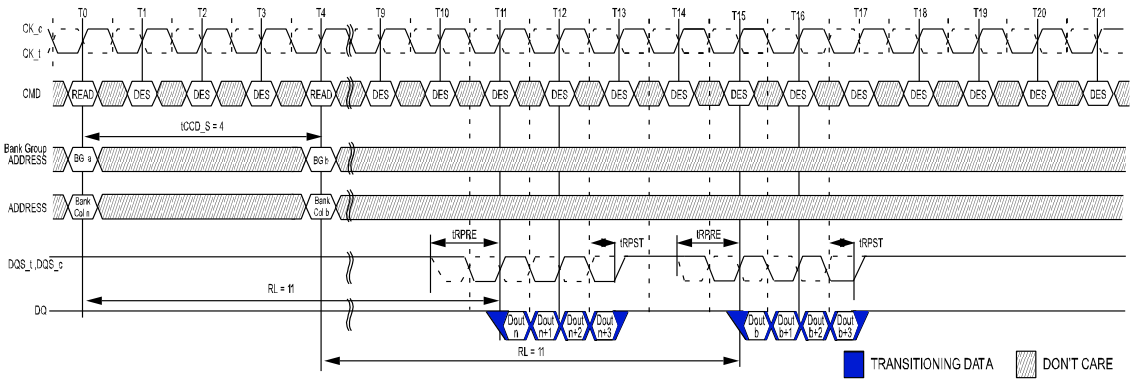
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T6.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable

NOTE 6 tCCD_S/L=5 isn't allowed in 2tCK preamble mode.

READ (BC4) to READ (BC4) with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK

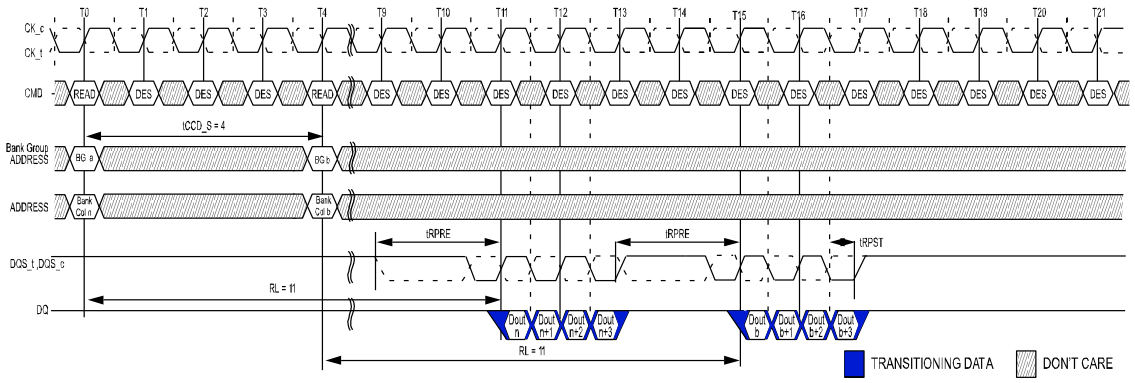
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable

READ (BC4) to READ (BC4) with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 2tCK

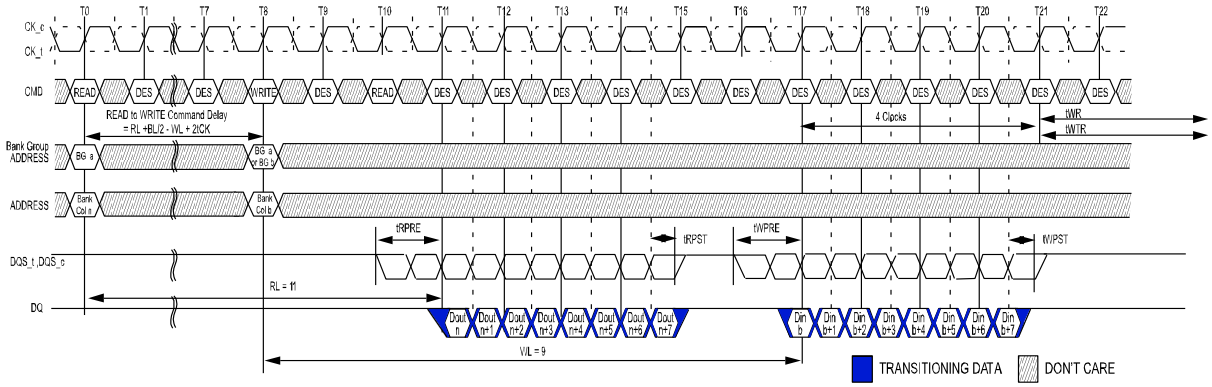
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable

READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK

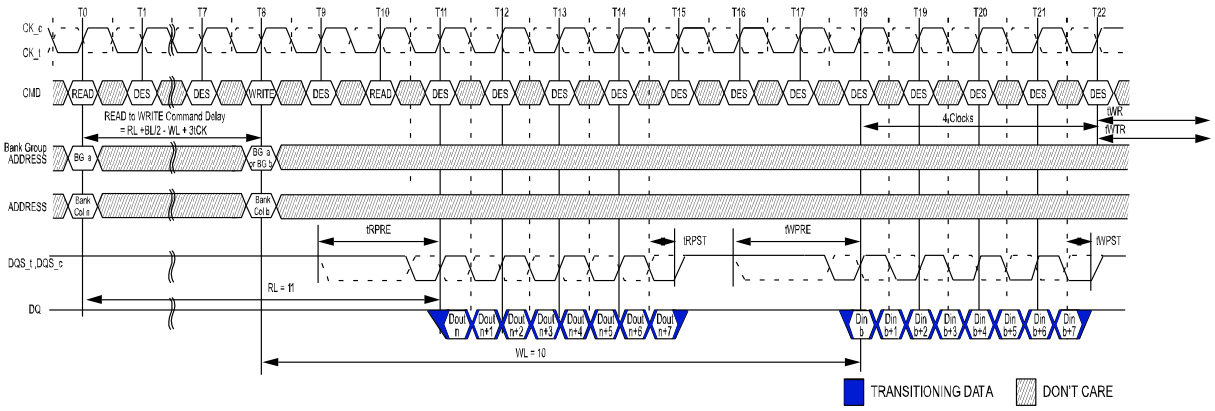
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

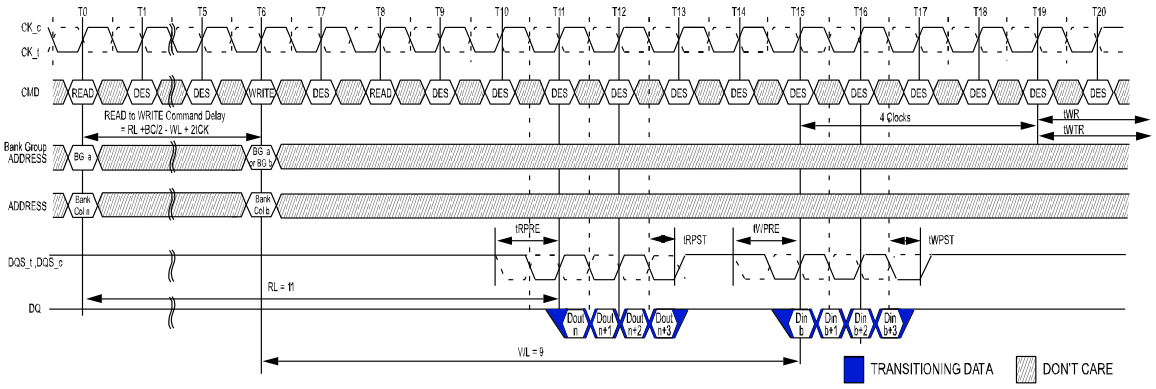
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK

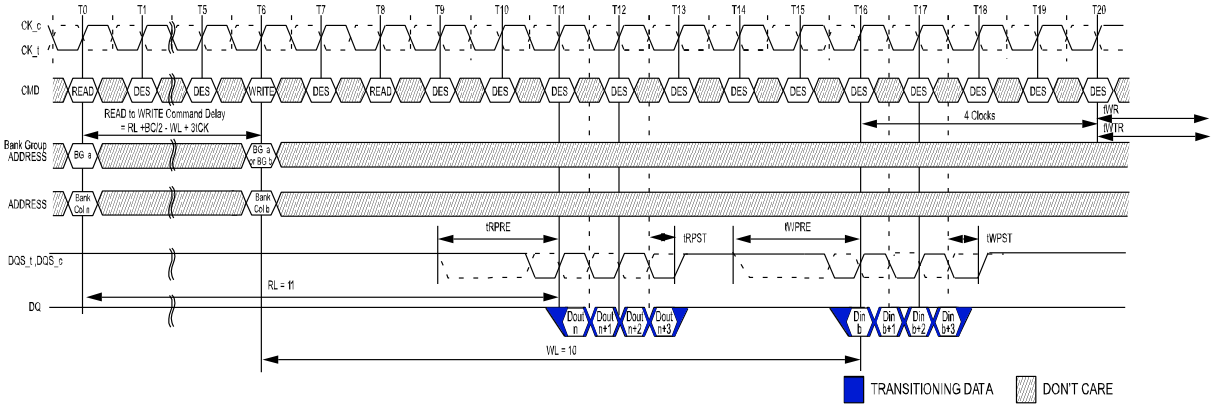
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4(OTF) setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and WRITE command at T6.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

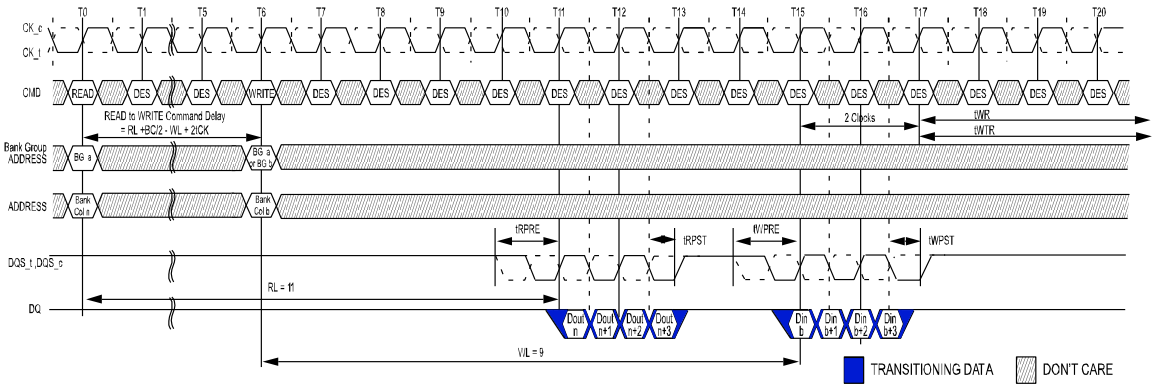
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4(OTF) setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and WRITE command at T6.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK

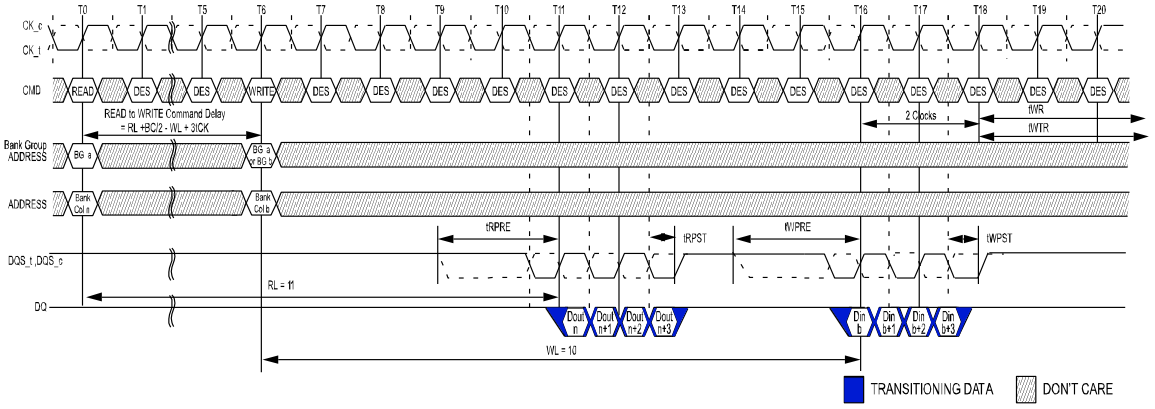
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4(Fixed) setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) Fixed to WRITE (BC4) Fixed with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

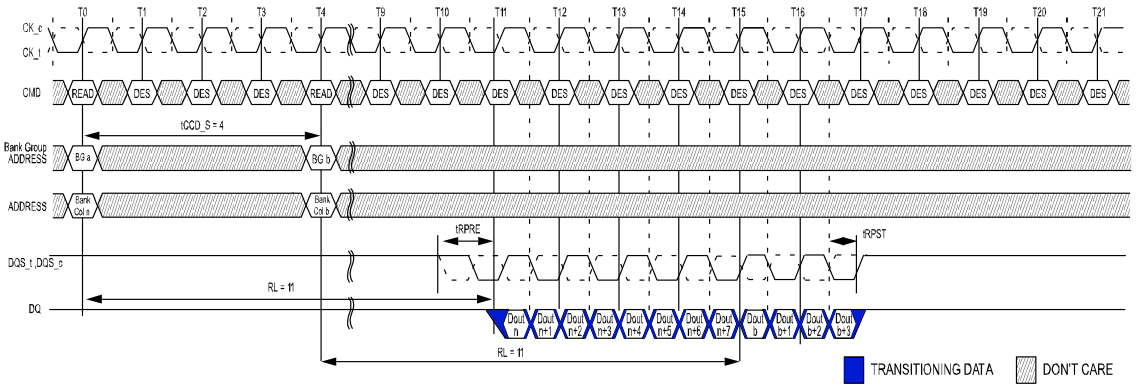
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4(Fixed) setting activated by MR0[A1:A0 = 1:0].

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to READ (BC4) OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL =0, CL = 11 ,Preamble = 1tCK

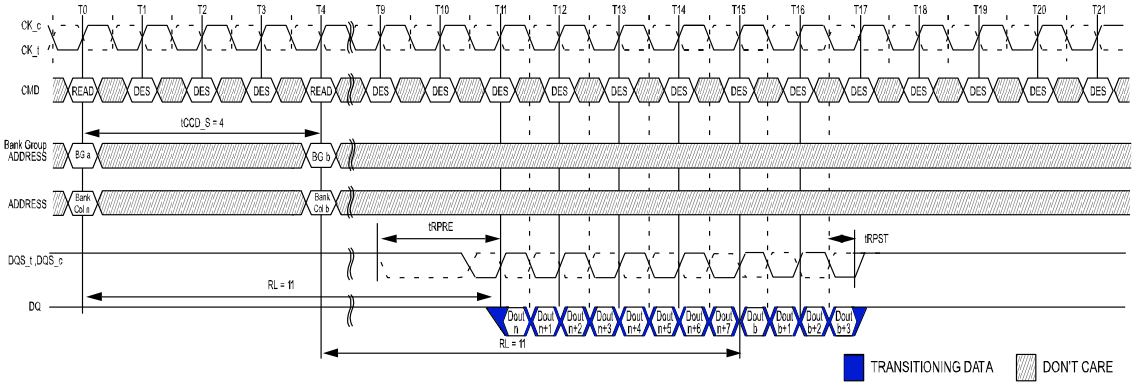
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable.

READ (BL8) to READ (BC4) OTF with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL =0, CL = 11 ,Preamble = 2tCK

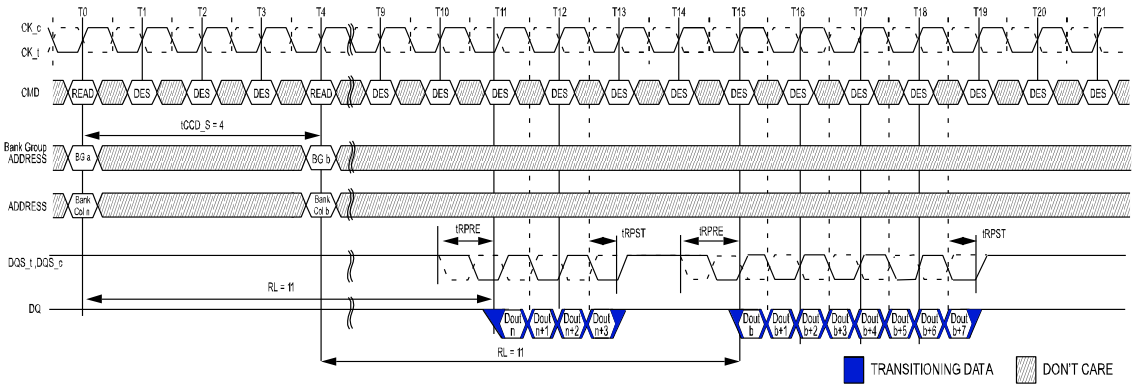
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable.

READ (BC4) to READ (BL8) OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL =0, CL = 11 ,Preamble = 1tCK

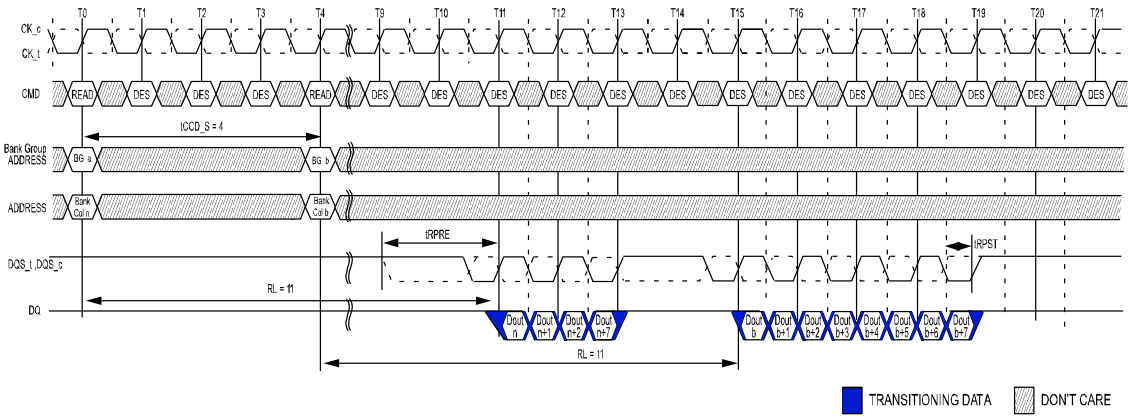
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable.

READ (BC4) to READ (BL8) OTF with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL =0, CL = 11 ,Preamble = 2tCK

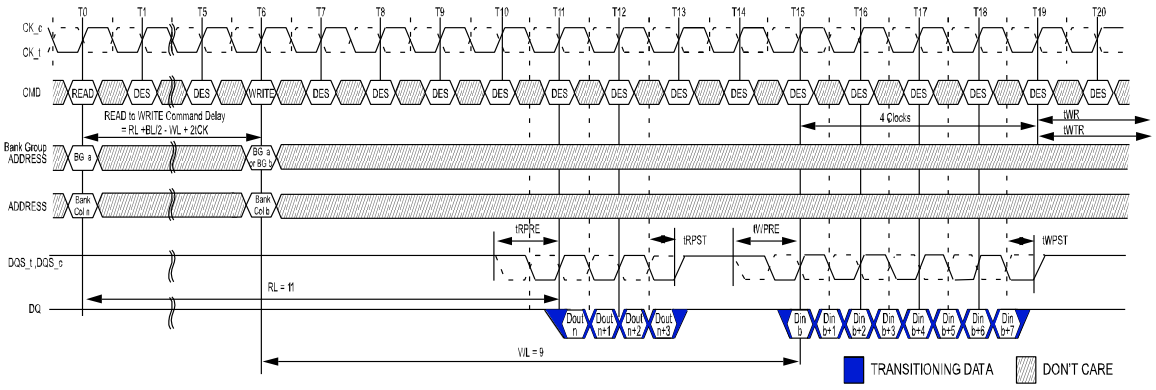
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable.

READ (BC4) to WRITE (BL8) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK

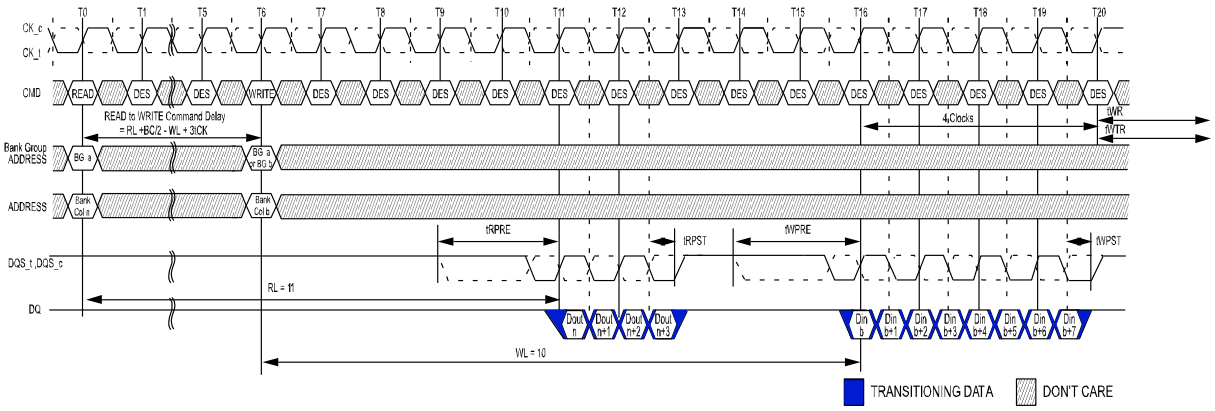
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T6.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) to WRITE (BL8) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

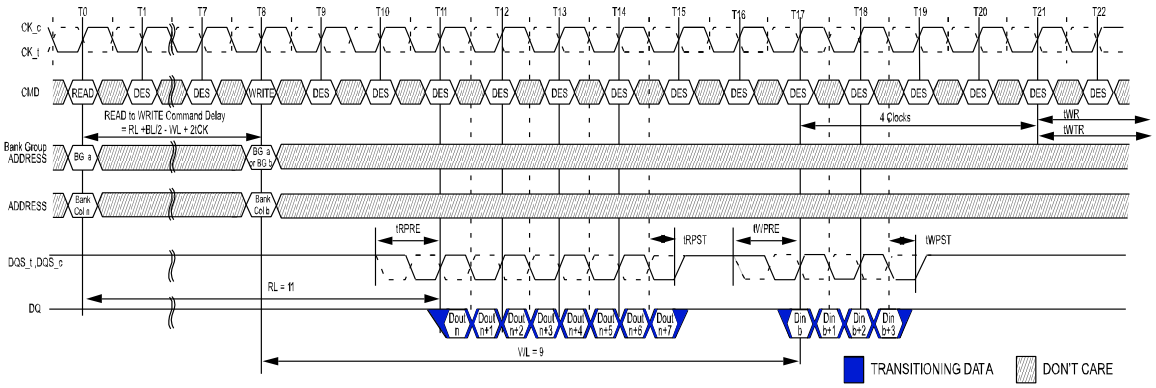
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T6.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK

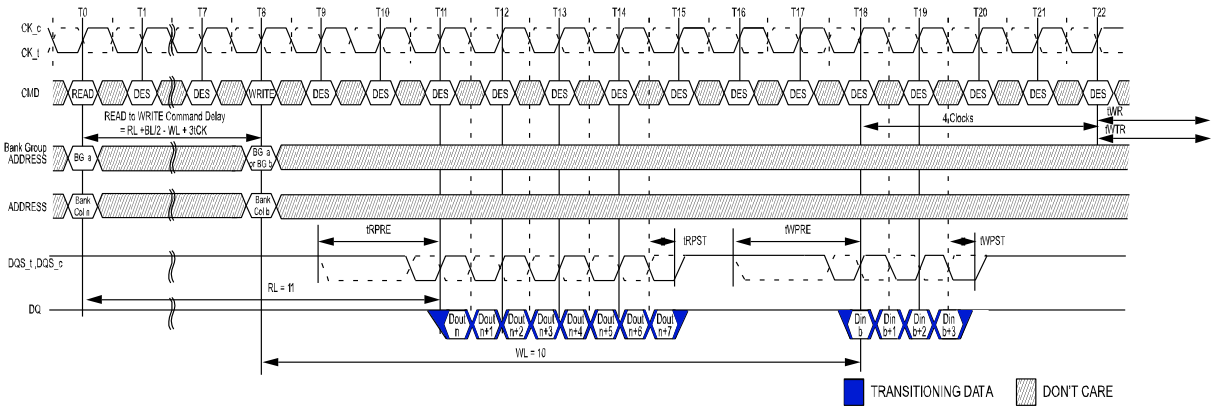
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T8.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T8.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

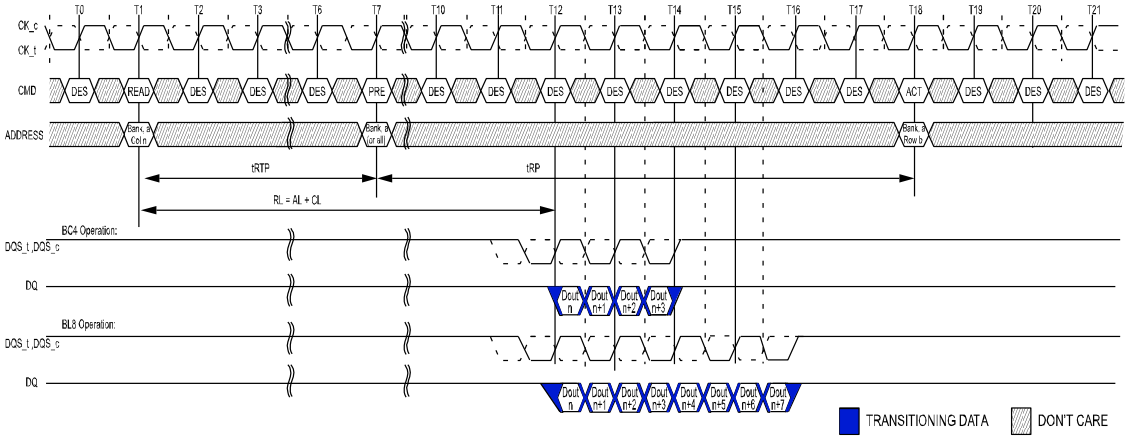
Burst Read Operation followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to AL + tRTP with tRTP being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by tRTP.min, A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The minimum RAS precharge time (tRP.MIN) has been satisfied from the clock at which the precharge begins.

2. The minimum RAS cycle time (tRC.MIN) from the previous bank activation has been satisfied.

READ to PRECHARGE with 1tCK Preamble



NOTE 1 BL = 8, RL = 11(CL = 11 , AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11

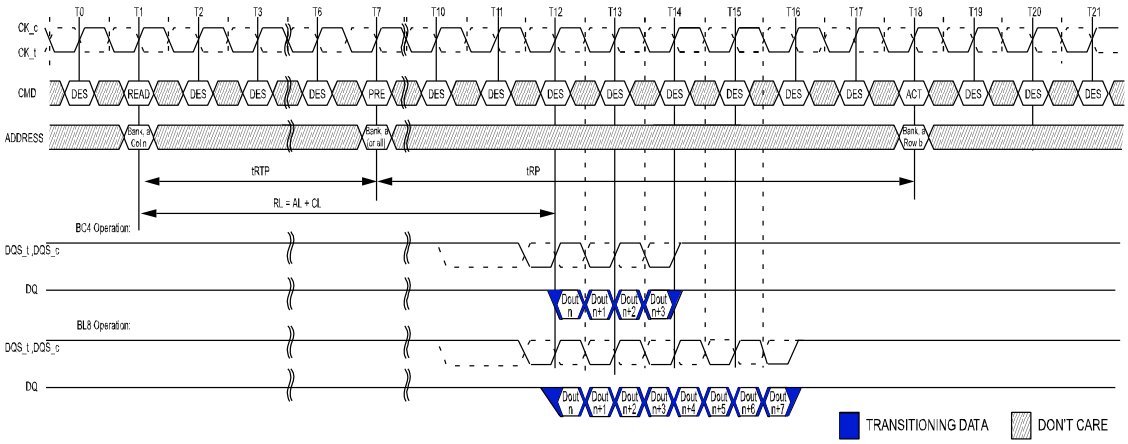
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable.

READ to PRECHARGE with 2tCK Preamble



NOTE 1 BL = 8, RL = 11(CL = 11 , AL = 0), Preamble = 2tCK, tRTP = 6, tRP = 11

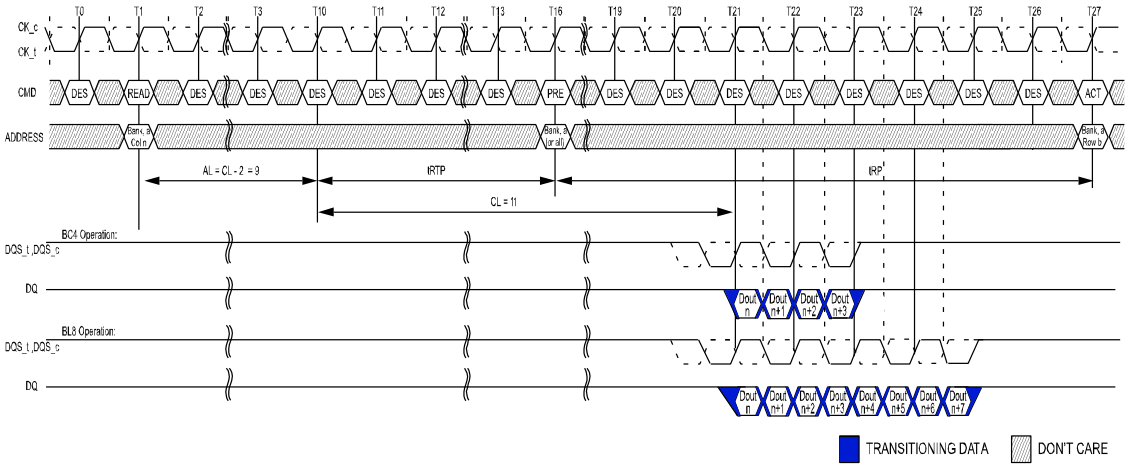
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable.

READ to PRECHARGE with Additive Latency and 1tCK Preamble



NOTE 1 BL = 8, RL = 20 (CL = 11 , AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11

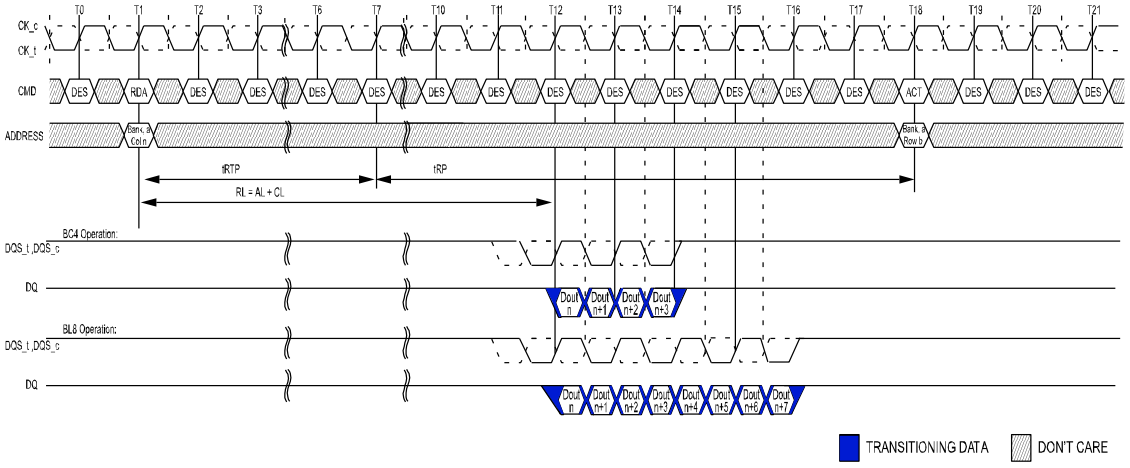
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 The example assumes tRAS. MIN is satisfied at Precharge command time(T16) and that tRC. MIN is satisfied at the next Active command time(T27).

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable.

READ with Auto Precharge and 1tCK Preamble



NOTE 1 BL = 8, RL = 11 (CL = 11 , AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11

NOTE 2 DOUT n = data-out from column n.

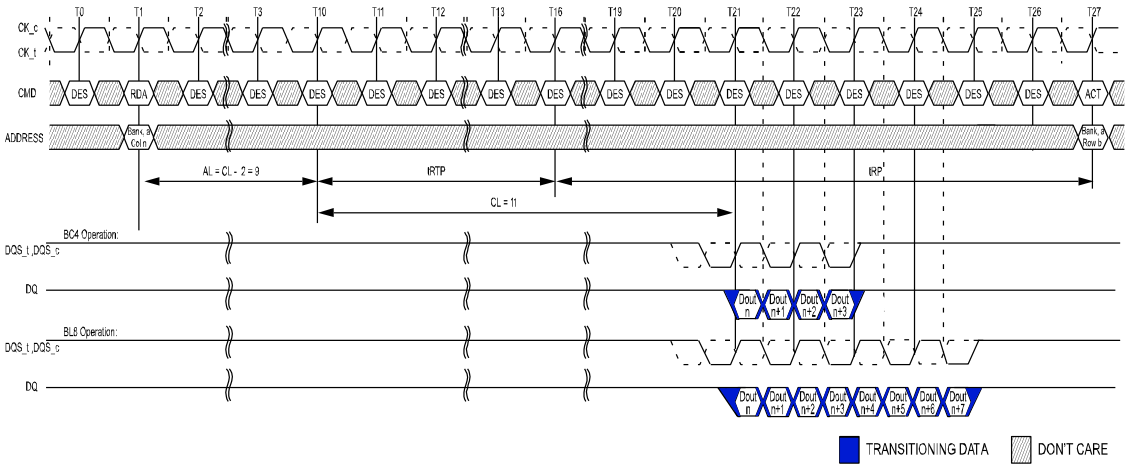
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 tRTP = 6 setting activated by MR0[A11:9 = 001]

NOTE 5 The example assumes tRC. MIN is satisfied at the next Active command time(T18).

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable.

READ with Auto Precharge, Additive Latency and 1tCK Preamble



NOTE 1 BL = 8, RL = 20 (CL = 11 , AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11

NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

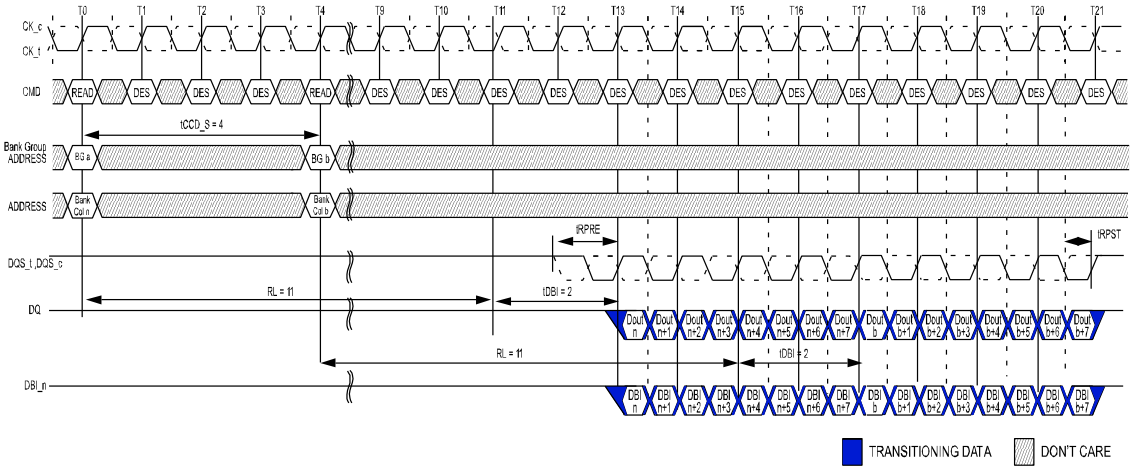
NOTE 4 tRTP = 6 setting activated by MR0[A11:9 = 001]

NOTE 5 The example assumes tRC. MIN is satisfied at the next Active command time(T27).

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable.

Burst Read Operation with Read DBI (Data Bus Inversion)

Consecutive READ (BL8) with 1tCK Preamble and DBI in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK, tDBI = 2tCK

NOTE 2 DOUT n (or b) = data-out from column n (or column b).

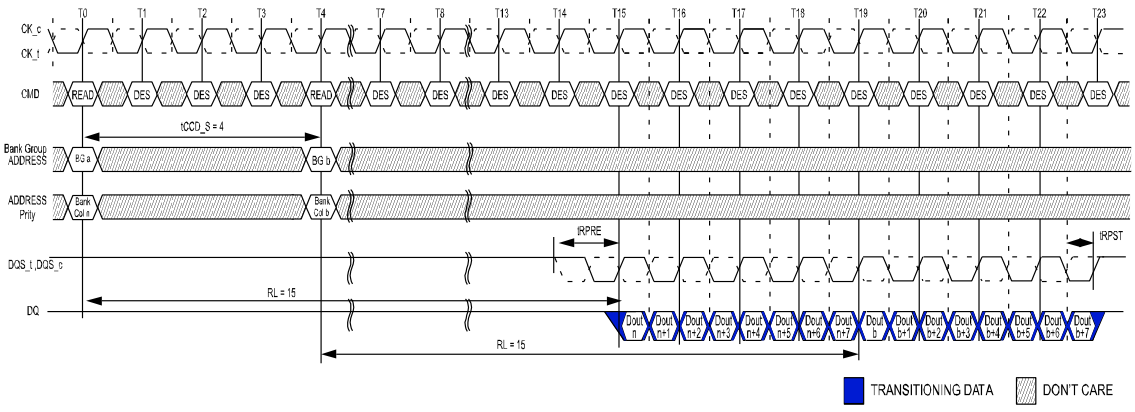
NOTE 3 DES commands are shown for ease of illustrat:ion; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 00] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Enable.

Burst Read Operation with Command/Address Parity

Consecutive READ (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Preamble = 1tCK

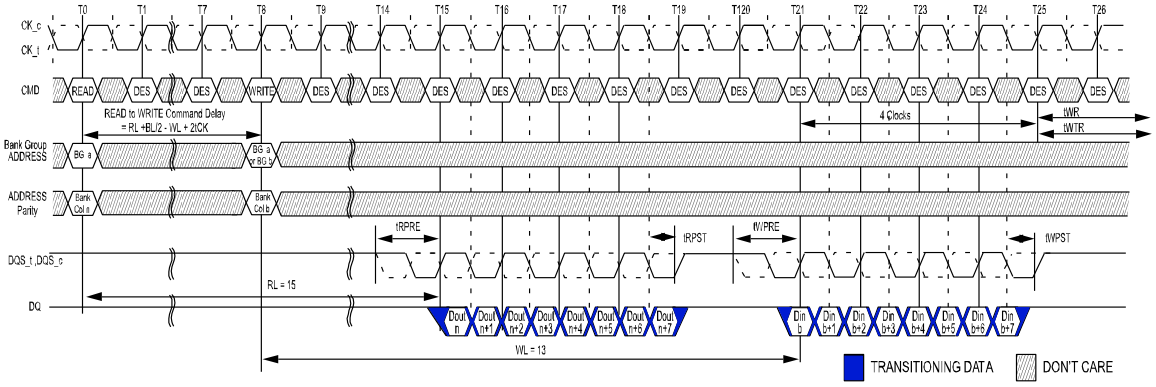
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.

NOTE 5 CA Parity =Enable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable.

READ (BL8) to WRITE (BL8) with 1tCK Preamble and CA parity in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Read Preamble = 1tCK, CWL=9, AL=0, PL=4, (WL=CWL+AL+PL=13), Write Preamble = 1tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

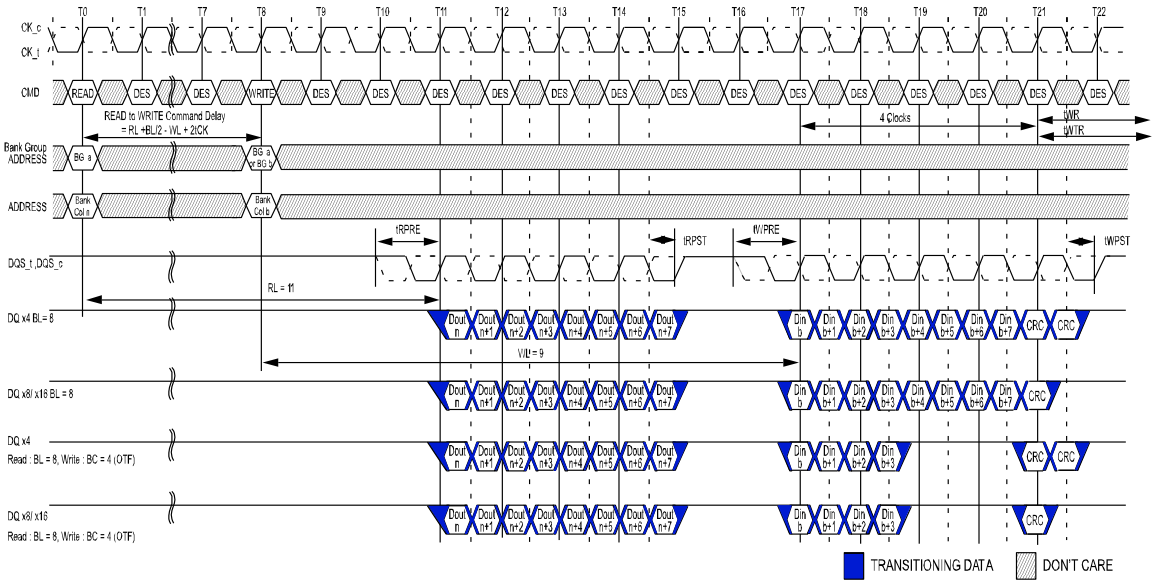
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.

NOTE 5 CA Parity = Enable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Read to Write with Write CRC

READ (BL8) to WRITE (BL8 or BC4:OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8 (or BC = 4 : OTF for Write), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble = 1tCK

NOTE 2 DOUT n = data-out from column n . DIN b = data-in to column b.

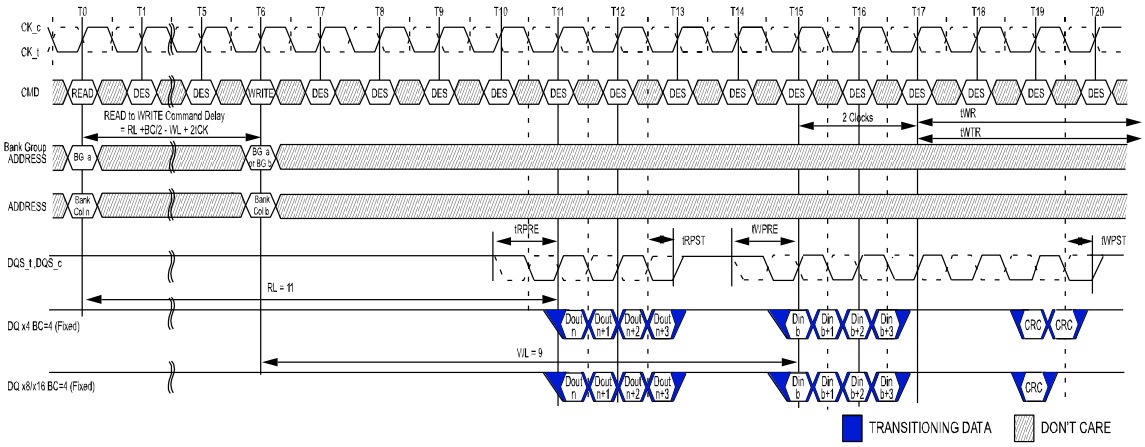
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.

NOTE 5 BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during Write command at T8.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

READ (BC4:Fixed) to WRITE (BC4:Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BC = 4 (Fixed), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble = 1tCK

NOTE 2 DOUT n = data-out from column n . DIN b = data-in to column b.

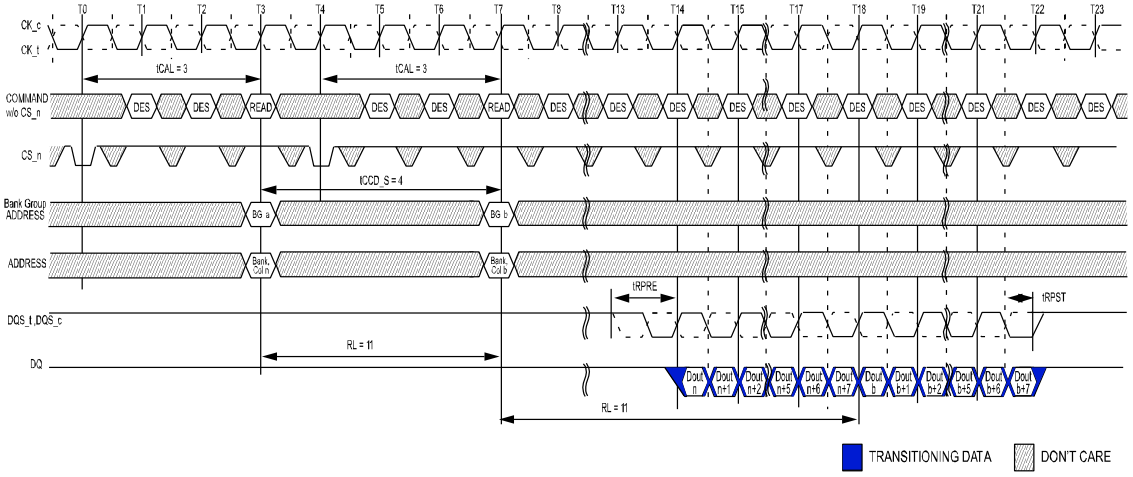
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

Read to Read with $\overline{CS}$ to CA Latency

Consecutive READ (BL8) with CAL(3) and 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8 ,AL = 0, CL = 11, CAL = 3, Preamble = 1tCK

NOTE 2 DOUT n (or b) = data-out from column n (or column b).

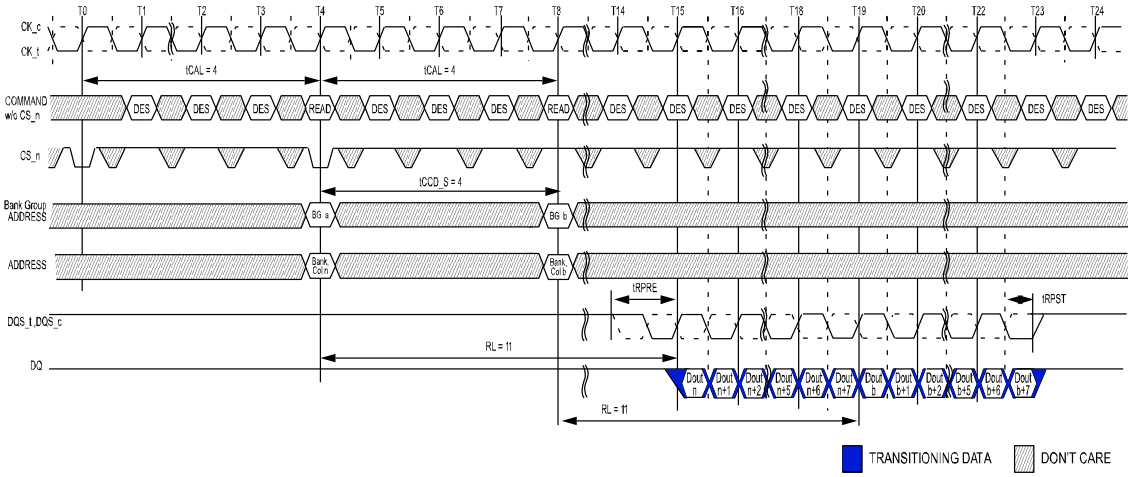
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T3 and T7.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Enable, Read DBI = Disable.

NOTE 6 Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/ address bus as when CAL is disabled.

Consecutive READ (BL8) with CAL(4) and 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8 ,AL = 0, CL = 11, CAL = 4, Preamble = 1tCK

NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4 and T8.

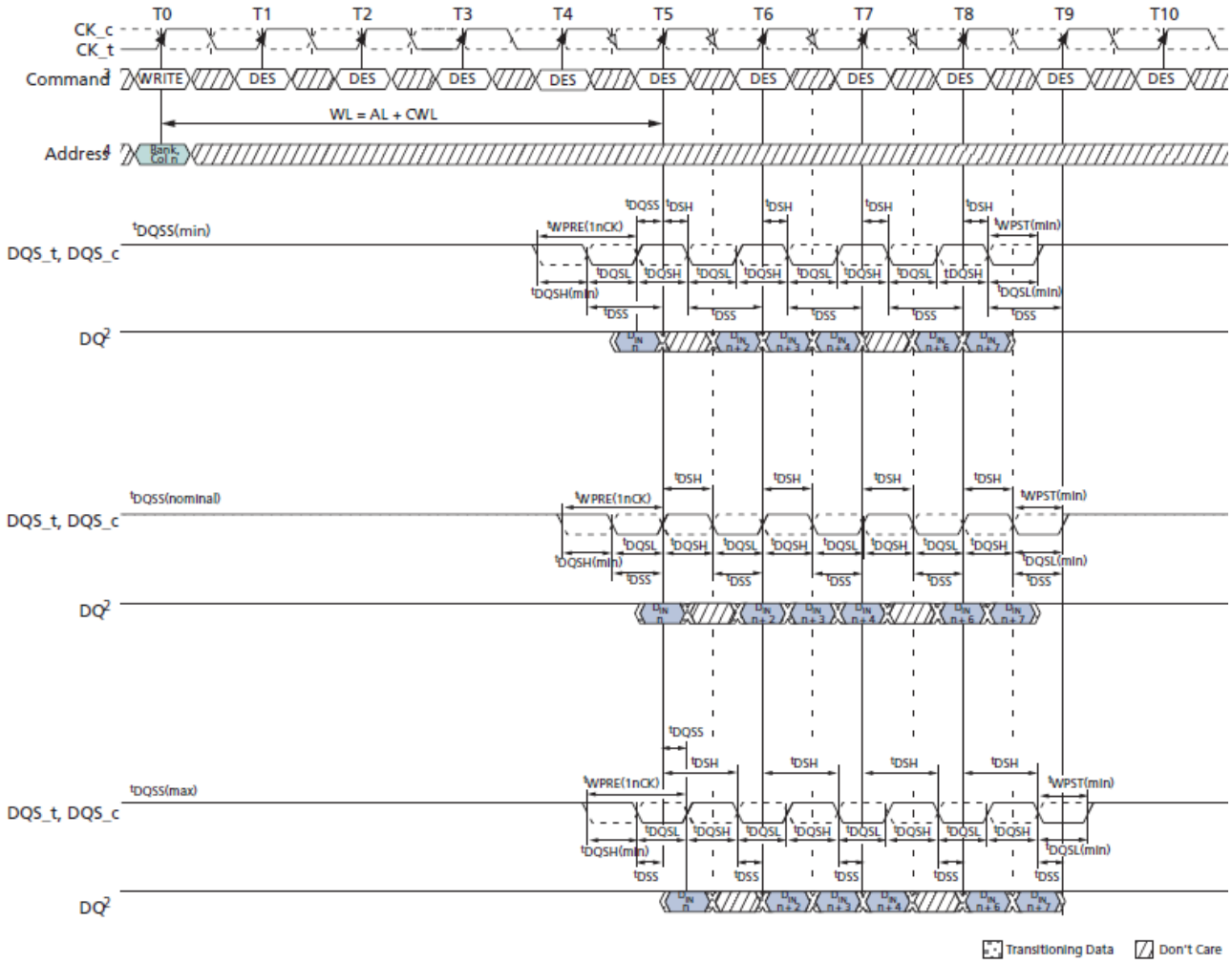
NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Enable, Read DBI = Disable.

NOTE 6 Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/ address bus as when CAL is disabled.

WRITE Operation

Write Timing Definitions

Write timings are shown below and are applicable in normal operation mode, i.e. when the DLL is enabled and locked.



NOTE 1 BL8, WL = 5 (AL = 0, CWL = 5).

NOTE 2 DINn = data-in from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.

NOTE 5 tDQSS must be met at each rising clock edge.

WRITE Timing – Clock to Data Strobe Relationship

The clock to data strobe relationship is shown below and is applicable in normal operation mode, i.e. when the DLL is enabled and locked.

Rising data strobe edge parameters:

• tDQSSMIN to tDQSSMaxdescribes the allowed range for a rising data strobe edge relative to CK, $\overline{CK}$.

• tDQSS is the actual position of a rising strobe edge relative to CK, $\overline{CK}$.

• tDQSH describes the data strobe high pulse width.

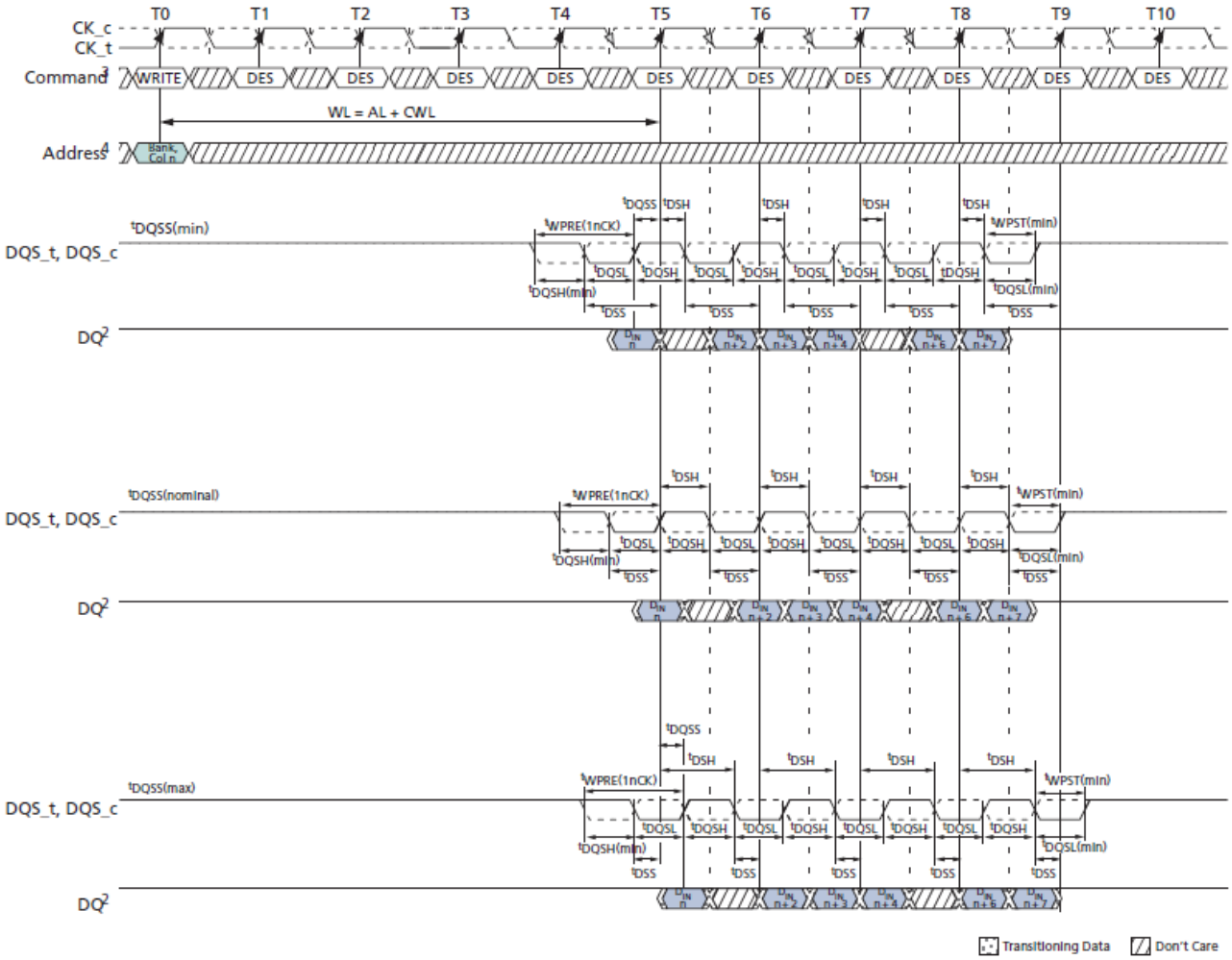
• tWPST strobe going to high, non-drive level; detailed in postamble section.

Falling data strobe edge parameters:

• tDQSL describes the data strobe low pulse width.

• tWPRE strobe going to low, initial drive level; detailed in preamble section

Clock to Data Strobe Relationship



NOTE 1 Within a burst, the rising strobe edge will be vary within tDQSCKj with a fixed and constant VDD. However, when the device, voltage, and temperature variation are incorporated,the rising strobe edge will be vary between tDQSCK(MIN) and tDQSCK(MAX).

NOTE 2 Notwithstanding Note 1, a rising strobe edge with tDQSCK (MAX) at T(n) can not be immediately followed by a rising strobe edge with tDQSCK (MIN) at T(n+1) because other timing relationships (tQSH, tQSL) exist: if tDQSCK(n+1) < 0: tDQSCK(n) < 1.0 tCK - (tQSH (MIN) + tQSL (MIN) - | tDQSCK(n+1) |

NOTE 3 The DQS, $\overline{DQS}$ differential output HIGH time is defined by tQSH and the DQS, $\overline{DQS}$ differential output LOW time is defined by tQSL.

NOTE 4 Likewise,tLZ(DQS) MIN and tHZ(DQS) MIN are not tied to tDQSCK (MIN) (early strobe case) and tLZ(DQS) MAX and tHZ(DQS) MAX are not tied to tDQSCK (MAX) (late strobe case).

NOTE 5 The minimum pulse width of read preamble is defined by tRPRE (MIN).

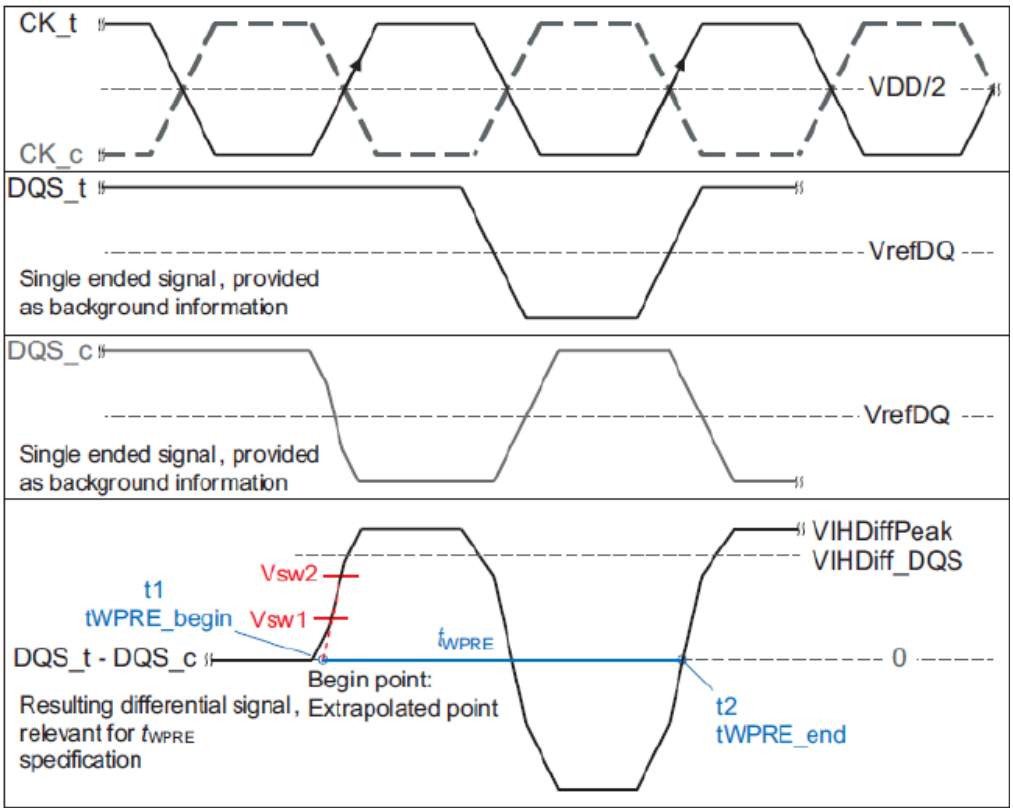
NOTE 6 The maximum read postamble is bound by tDQSCK (MIN) plus tQSH (MIN) on the left side and tHZDSQ (MAX) on the right side.

NOTE 7 The minimum pulse width of read postamble is defined by tRPST (MIN).

NOTE 8 The maximum read preamble is bound by tLZDQS (MIN) on the left side and tDQSCK (MAX) on the right side.

tWPRE Calculation

Method for calculating tWPRE transitions and endpoints



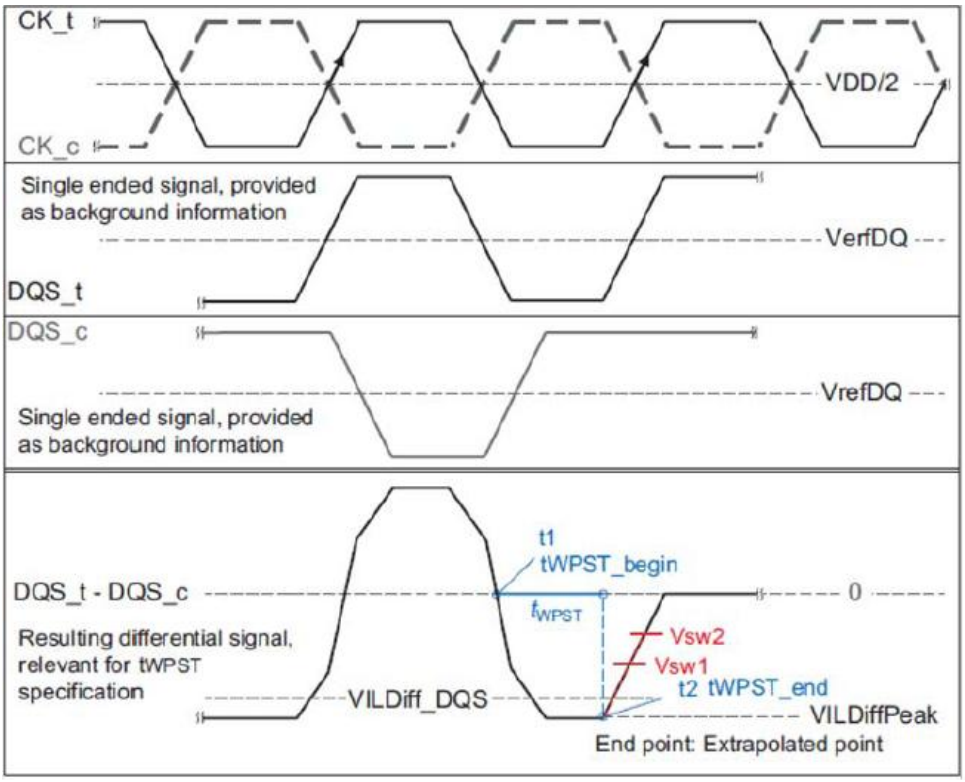
Reference Voltage for tWPRE Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1[V]	Vsw2[V]
tWPRE	DQS, $\overline{DQS}$ differential WRITE Preamble	VIHDiff_DQS x 0.1	VIHDiff_DQS x 0.9

NOTE 1 The method for calculating differential pulse widths for tWPRE2 is same as tWPRE.

tWPST Calculation

Method for calculating tWPST transitions and endpoints



Reference Voltage for tWPST Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1[V]	Vsw2[V]
tWPST	DQS, $\overline{DQS}$ differential WRITE Postamble	VILDiff_DQS x 0.9	VILDiff_DQS x 0.1

Timing Parameters by Speed Grade

Symbol	Parameter	DDR4-2133		DDR4-2400		Unit
		Min	Max	Min	Max	
tWPRE	DQS, $\overline{DQS}$ differential WRITE Preamble (1tCK Preamble)	0.9	–	0.9	–	tCK(avg)
tWPRE2	DQS, $\overline{DQS}$ differential WRITE Preamble (2tCK Preamble)	–	–	–	–	tCK(avg)
tWPST	DQS, $\overline{DQS}$ differential WRITE Postamble	TBD	–	TBD	–	tCK(avg)
tDQSL	DQS, $\overline{DQS}$ differential input low pulse width	0.46	0.54	0.46	0.54	tCK(avg)
tDQSH	DQS, $\overline{DQS}$ differential input high pulse width	0.46	0.54	0.46	0.54	tCK(avg)
tDQSH2PRE	DQS, $\overline{DQS}$ differential input high pulse width at 2tCK Preamble	–	–			tCK(avg)
tDQSS	DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge(1tCK Preamble)	-0.27	-0.27	-0.27	-0.27	tCK(avg)
tDSS	DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	0.18	–	0.18	–	tCK(avg)
tDSH	DQS, $\overline{DQS}$ falling edge hold time from CK, $\overline{CK}$ rising edge	0.18	–	0.18	–	tCK(avg)

WRITE Burst Operation

The following write timing diagrams are to help understanding of each write parameter's meaning and are just examples. The details of the definition of each parameter will be defined separately. In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.

DDR4 WRITE command supports bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF when OTF is enabled:

• A12 = 0, BC4 (BC4 = burst chop)

• A12 = 1, BL8

Write commands can issue precharge automatically with a Write with auto-precharge command (WRA); and is enabled by A10 high.

• Write command with A10 = 0 (WR) performs standard Write, bank remains active after write burst.

• Write command with A10 = 1 (WRA) performs Write with auto-precharge, back goes in to precharge after write burst.

Data mask (DM) function is supported for the x8 and x16 configurations only (not supported on x4). The DM function shares a common pin with the $\overline{DBI}$ and TDQS functions.

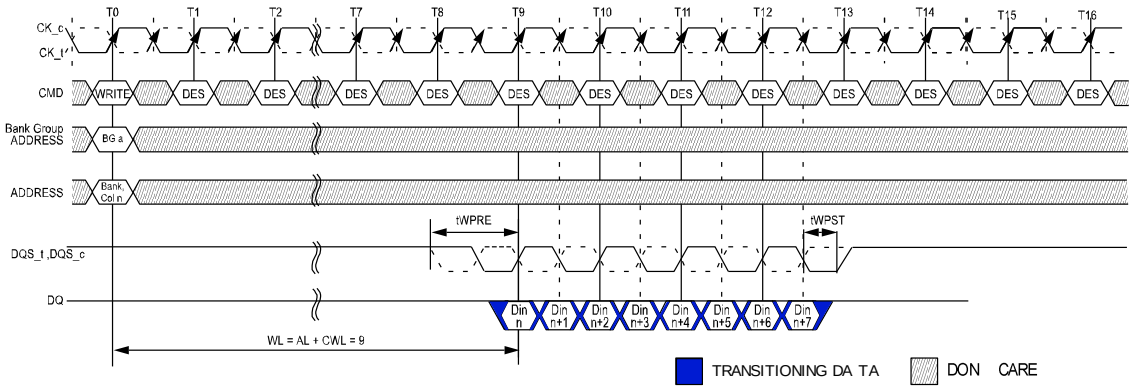
The DM function only applies to WRITE operations and cannot be enabled at the same time the DBI function is enabled.

• If $\overline{DM}$ is sampled LOW on a given byte lane, the DRAM masks the write data received on the DQ inputs.

• If $\overline{DM}$ is sampled HIGH on a given byte lane, the DRAM does not mask the data and writes this data into the DRAM core.

• If CRC Write is enabled, then DM enabled (via MRS), will selected between Write CRC non-Persistent Mode (DM disabled) and Write CRC Persistent Mode (DM enabled).

WRITE Burst Operation, WL = 9 (AL = 0, CWL = 9, BL8)



NOTE 1 BL8, WL = 0, AL = 0, CWL = 9, Preamble = 1 tCK.

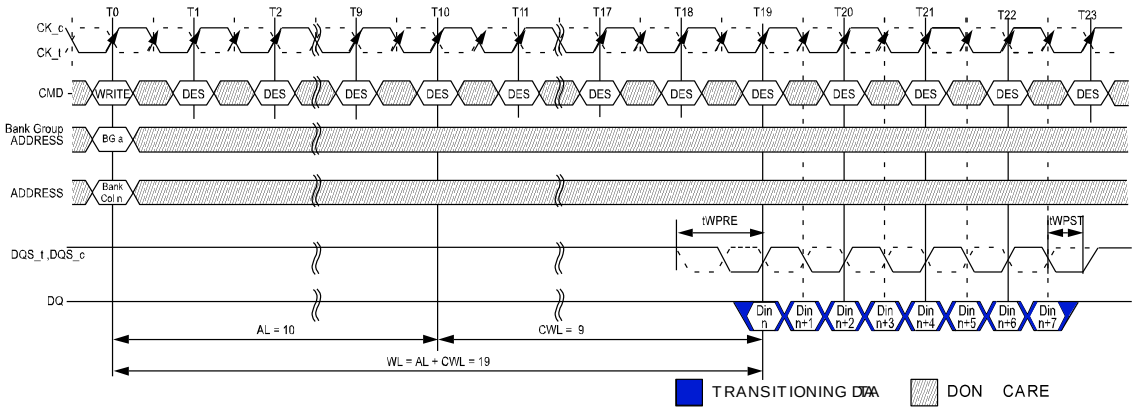
NOTE 2 DINn = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.

NOTE 5 C/A Parity = Disable, $\overline{CS}$ to C/A Latency = Disable, Read DBI = Disable.

WRITE Burst Operation, WL = 19 (AL = 10, CWL = 9, BL8)



NOTE 1 BL8, WL = 19, AL = 10 (CL - 1), CWL = 9, Preamble = 1 tCK.

NOTE 2 DINn = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

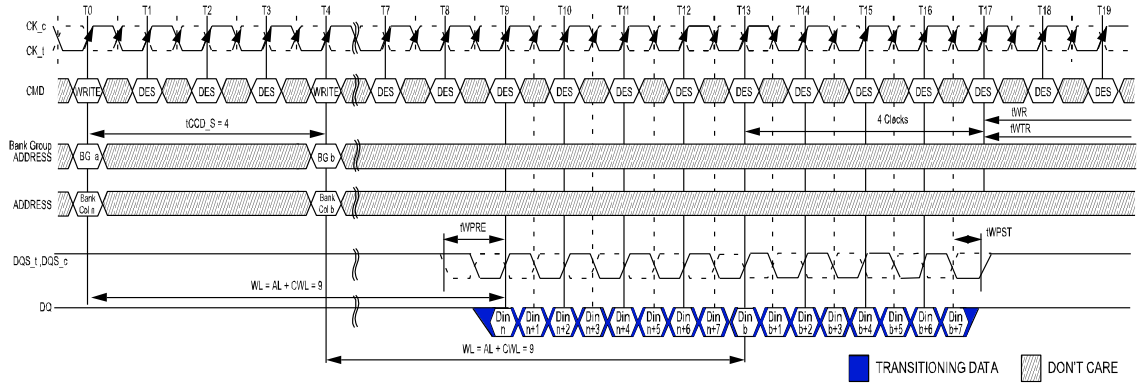
NOTE 4 BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.

NOTE 5 C/A Parity = Disable, $\overline{CS}$ to C/A Latency = Disable, Read DBI = Disable.

WRITE Operation Followed by another WRITE Operation

Various Burst Read examples are shown below.

Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group



NOTE 1 BL8, AL = 0, CWL = 9, Preamble = 1 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

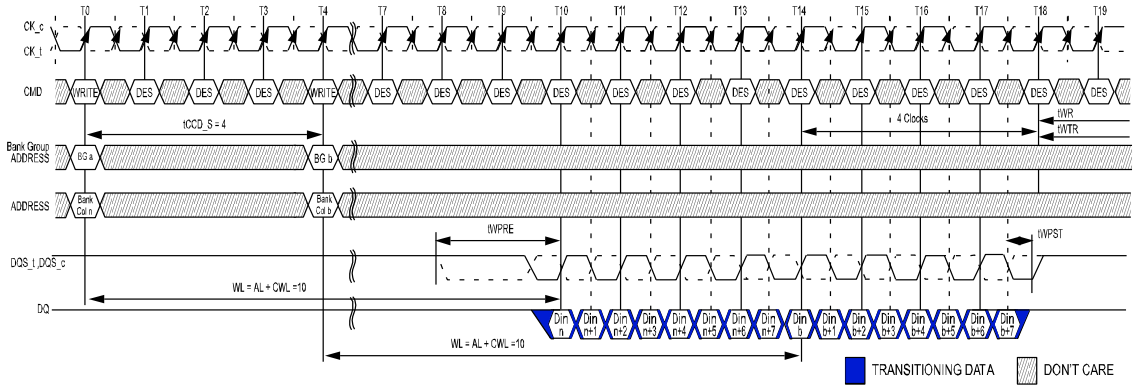
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write DBI = disable, Write CRC = disable.

NOTE6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

Consecutive WRITE (BL8) with 2tCK Preamble in Different Bank Group



NOTE 1 BL8, AL = 0, CWL = 9+1=10[7], Preamble = 2 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

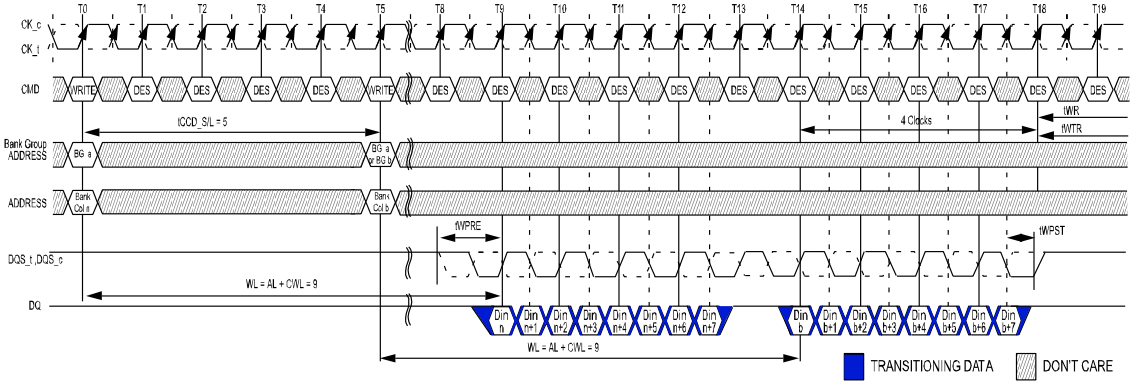
NOTE 4 BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write DBI = disable, Write CRC = disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

NOTE 7 When operating in 2tCK Write Preamble Mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

Nonconsecutive WRITE (BL8) with 1 tCK Preamble in Same or Different Bank Group



NOTE 1 BL8, AL = 0, CWL = 9, Preamble = 1 tCK, tCCD_S/L = 5 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

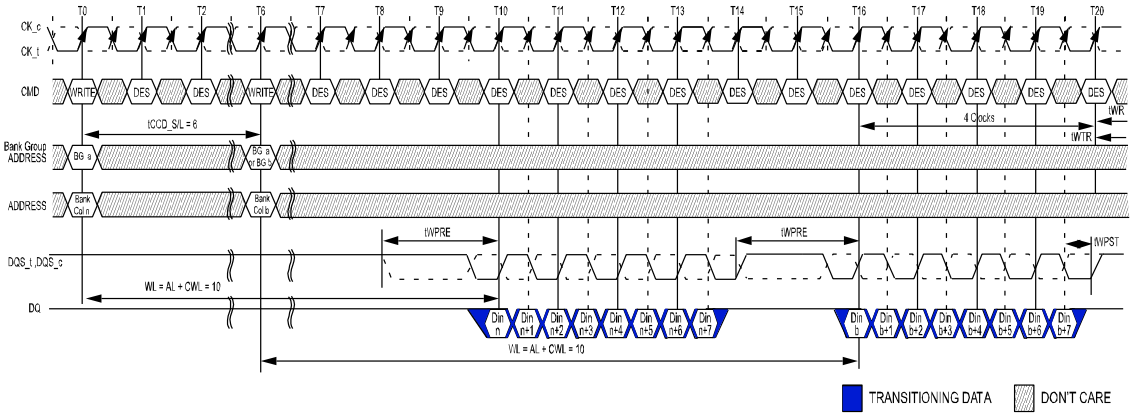
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T5.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write DBI = disable, Write CRC = disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

Nonconsecutive WRITE (BL8) with 2 tCK Preamble in Same or Different Bank Group



NOTE 1 BL8, AL = 0, CWL = 9+1=10[8], Preamble = 2 tCK, tCCD_S/L = 6 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T6.

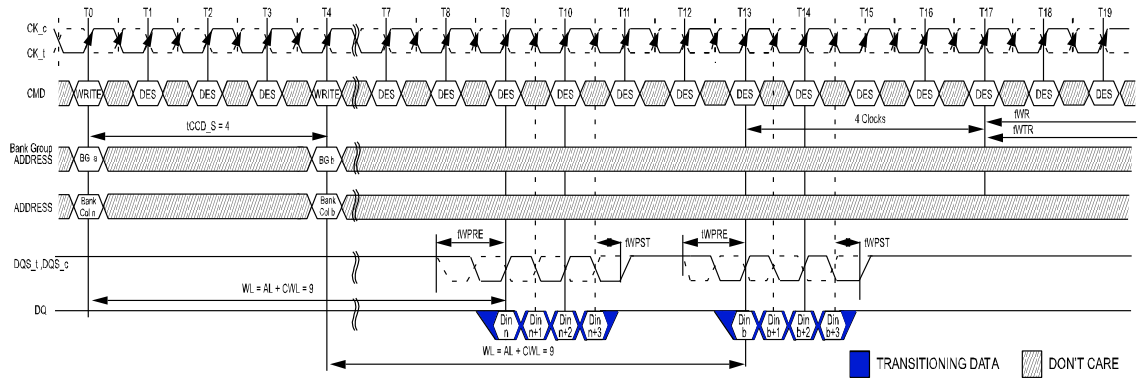
NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write DBI = disable, Write CRC = disable.

NOTE 6 tCCD_S/L = 5 isn't allowed in 2tCK preamble mode.

NOTE 7 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

NOTE 8 When operating in 2tCK Write Preamble Mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

WRITE (BC4) OTF to WRITE (BC4) OTF with 1 tCK Preamble in Different Bank Group



NOTE 1 BC4, AL = 0, CWL = 9, Preamble = 1 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

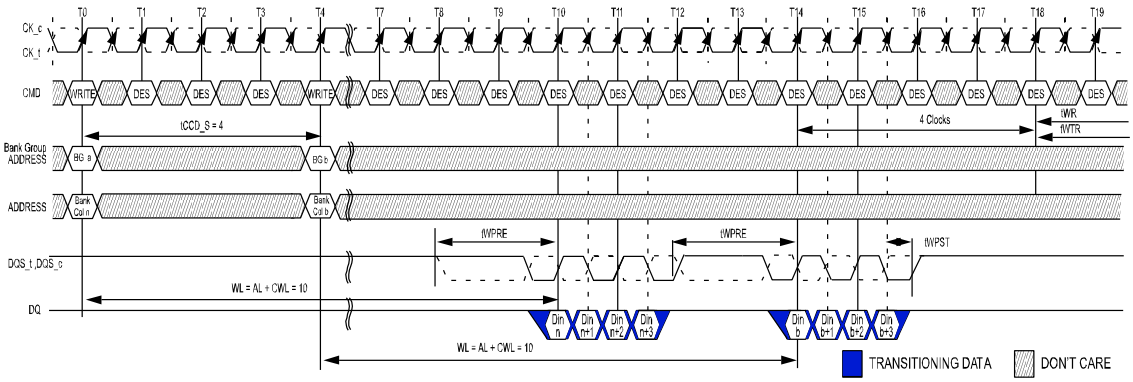
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T4.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write DBI = disable, Write CRC = disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

WRITE (BC4) OTF to WRITE (BC4) OTF with 2 tCK Preamble in Different Bank Group



NOTE 1 BC4, AL = 0, CWL = 9+1=10[7], Preamble = 2 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

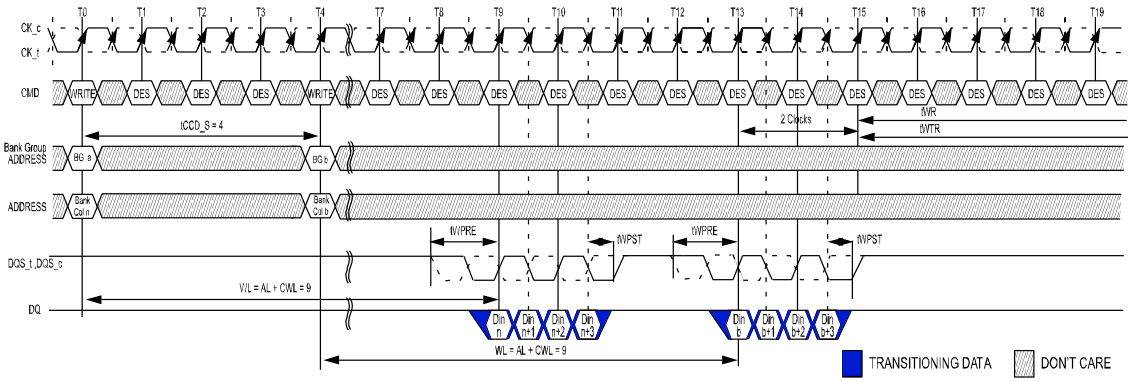
NOTE 4 BC4 setting activated by MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write DBI = disable, Write CRC = disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

NOTE 7 When operating in 2tCK Write Preamble Mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1 tCK Preamble in Different Bank Group



NOTE 1 BC4, AL = 0, CWL = 9, Preamble = 1 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

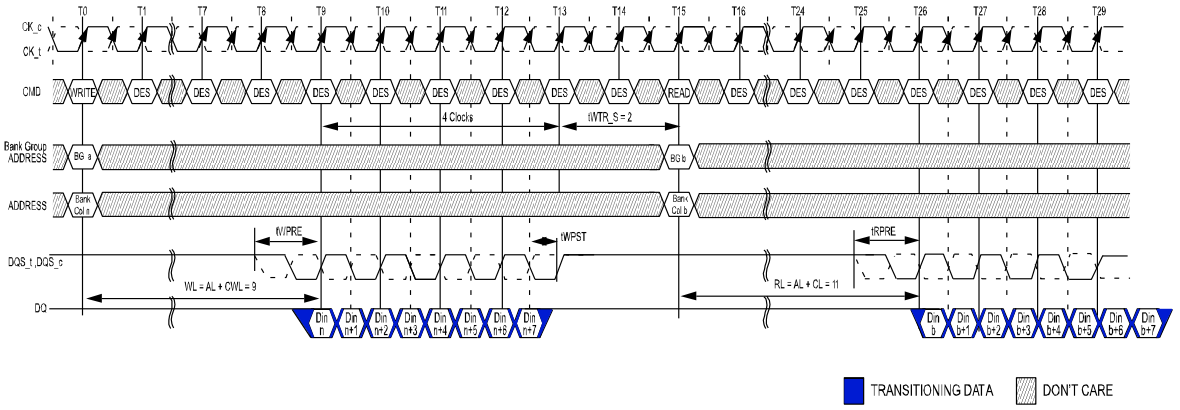
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T4.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write DBI = disable, Write CRC = disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T15.

WRITE (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BL=8/BC=4, AL =0, CL = 9, Preamble = 1 tCK

NOTE 2 DIN n (or b) = data-in from column n (or column b).

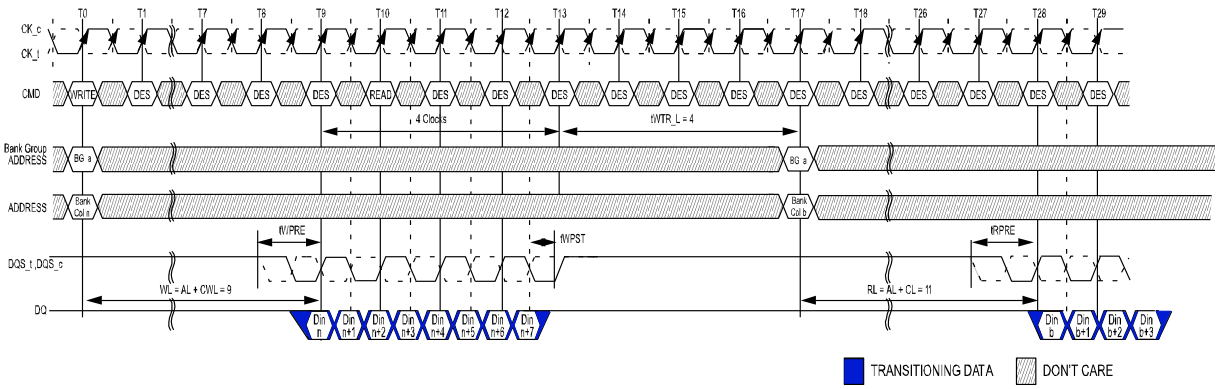
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during WRITE command at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T4.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Read DBI = disable, Write CRC = disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

WRITE (BL8) to READ (BL8) with 1tCK Preamble in Same Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

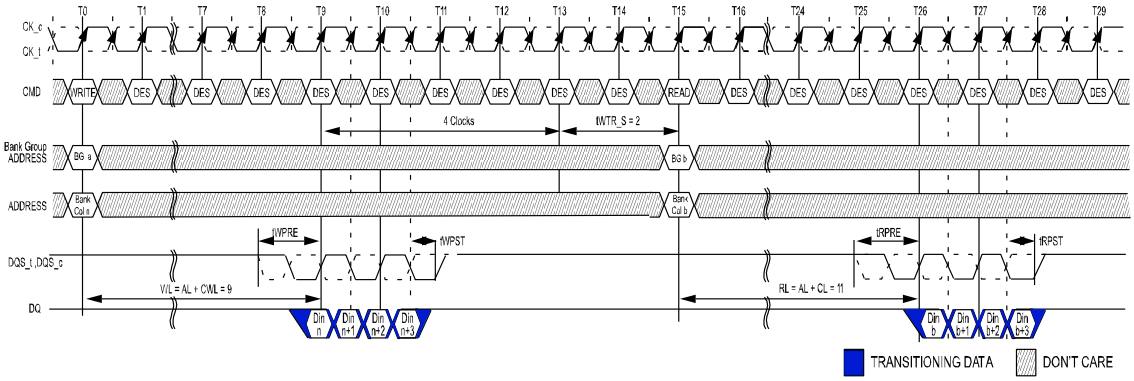
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and READ command at T17.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4)OTF to READ (BC4)OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

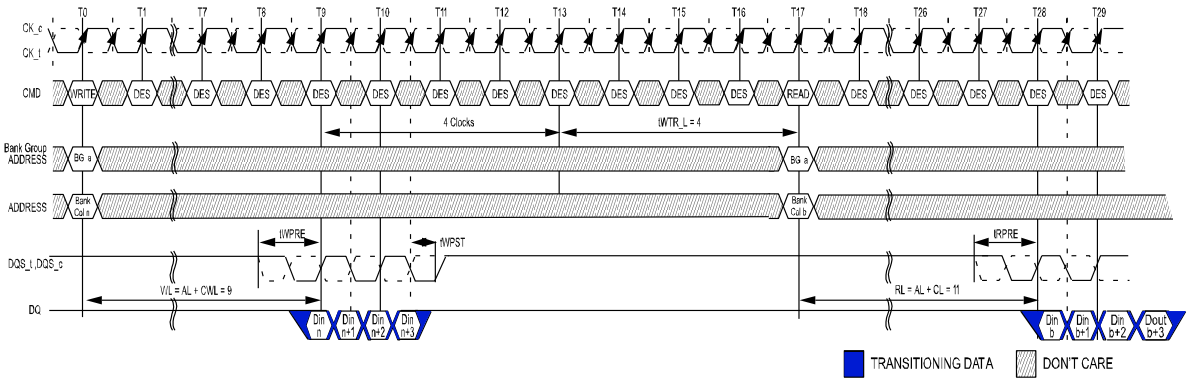
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and READ command at T15.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4)OTF to READ (BC4)OTF with 1tCK Preamble in Same Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

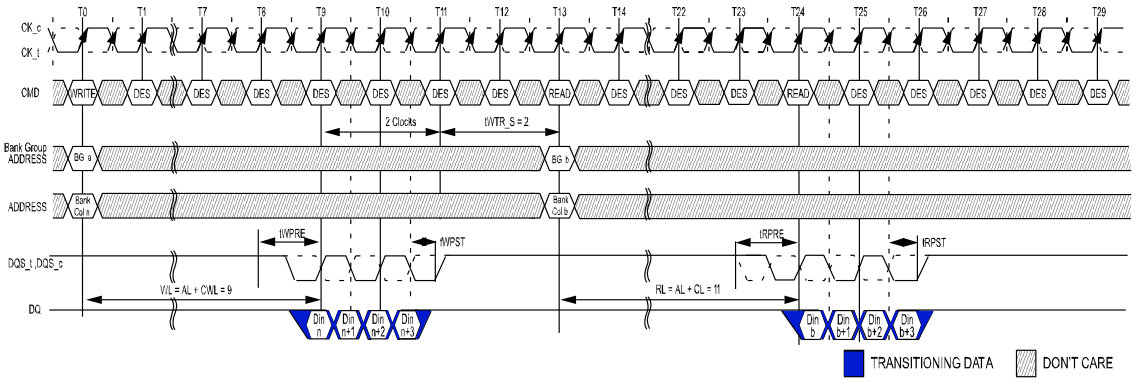
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and READ command at T17.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4)Fixed to READ (BC4)Fixed with 1tCK Preamble in Different Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

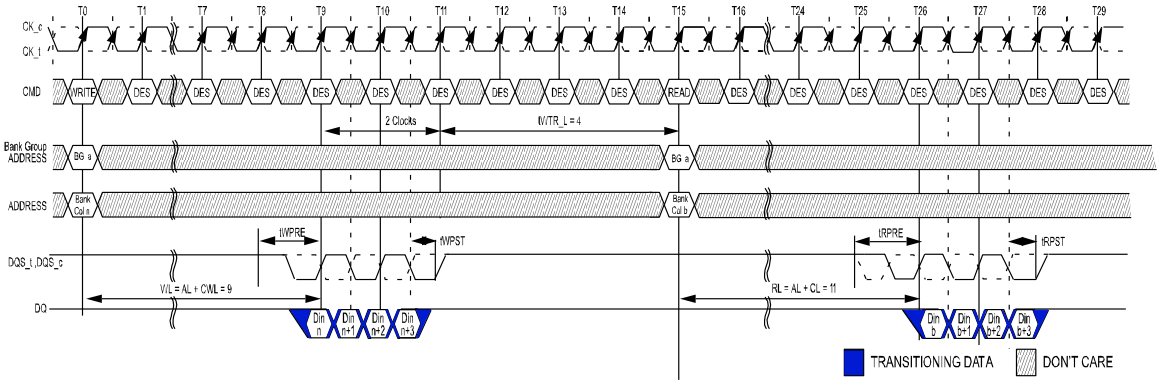
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T11.

WRITE (BC4)Fixed to READ (BC4)Fixed with 1tCK Preamble in Same Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

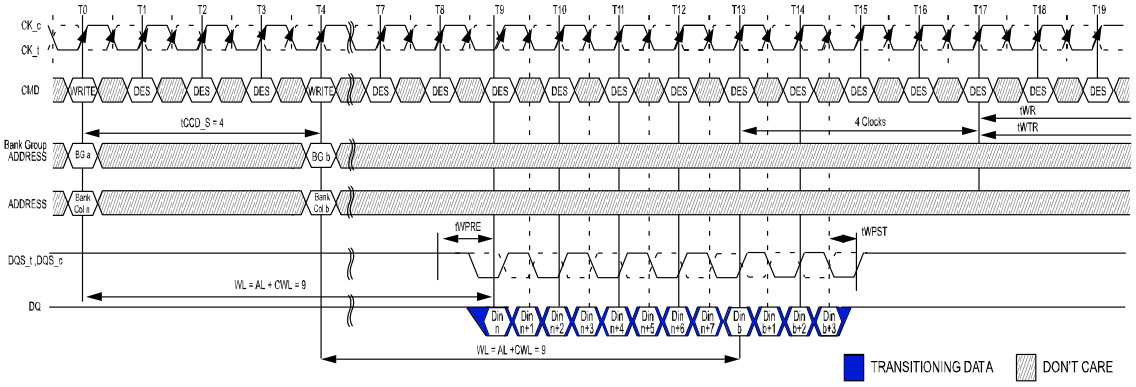
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T11.

WRITE (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n (or b) = data-in to column n (or column b).

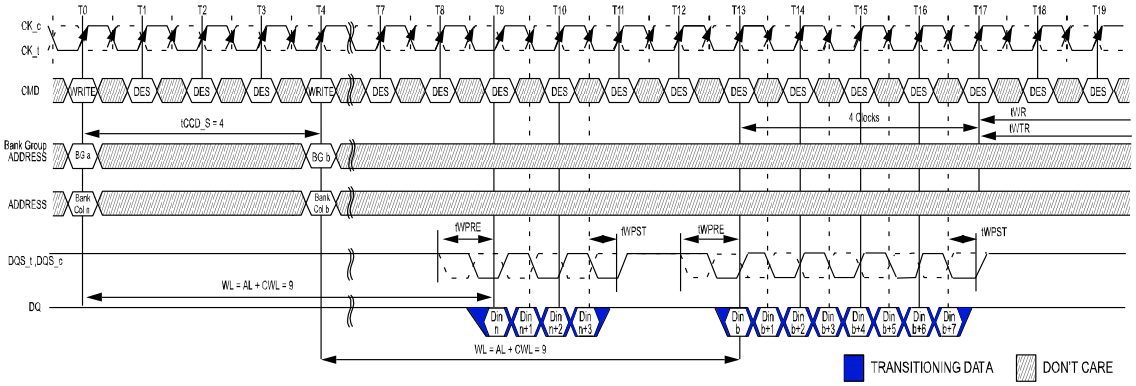
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17

WRITE (BC4) OTF to WRITE (BL8) with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n (or b) = data-in to column n (or column b).

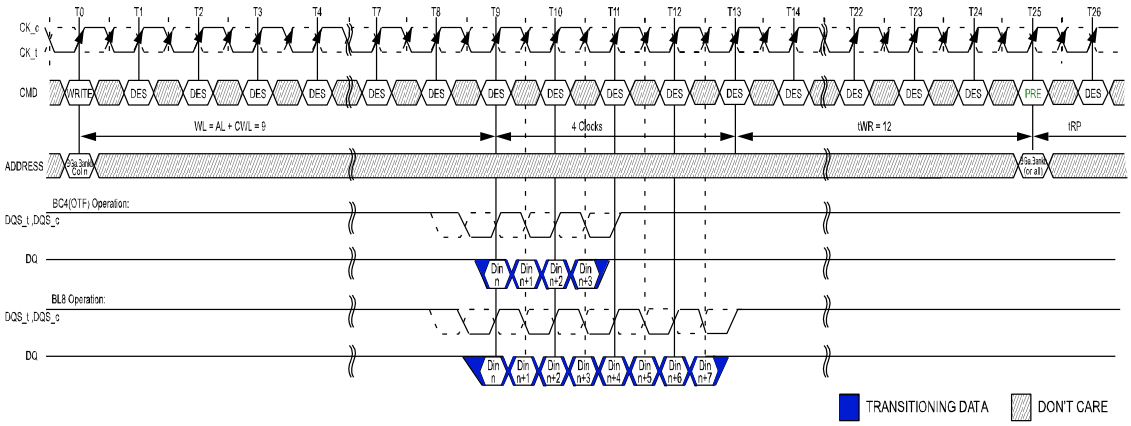
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17

WRITE (BL8/BC4) OTF to PRECHARGE Operation with 1tCK Preamble



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tWR = 12

NOTE 2 DIN n = data-in to column n.

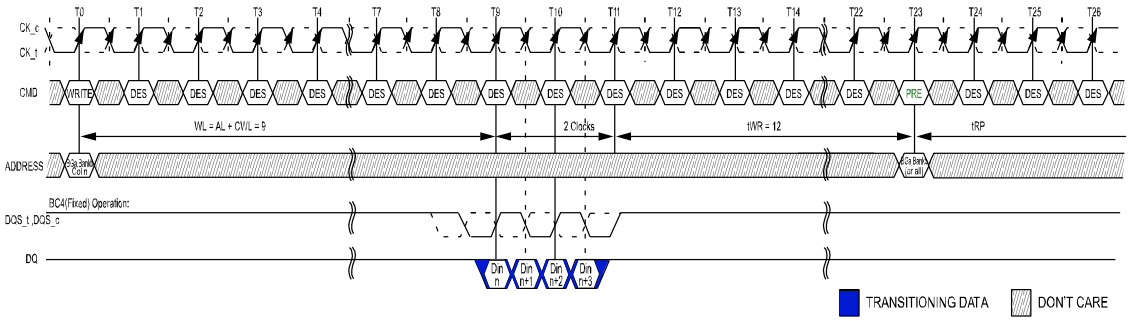
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0. BL8 setting activated by MR0[A1:A0 = 0:0] or MR0[A1:0 = 01] and A12 =1 during WRITE command at T0.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BC4) Fixed to PRECHARGE Operation with 1tCK Preamble



NOTE 1 BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tWR = 12

NOTE 2 DIN n = data-in to column n.

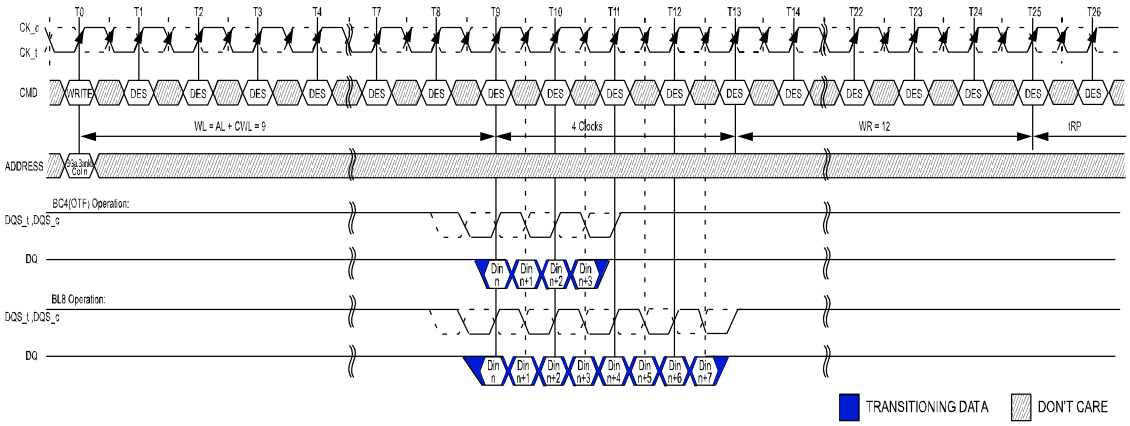
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BL8/BC4) OTF with Auto PRECHARGE Operation and 1tCK Preamble



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, WR = 12

NOTE 2 DIN n = data-in to column n.

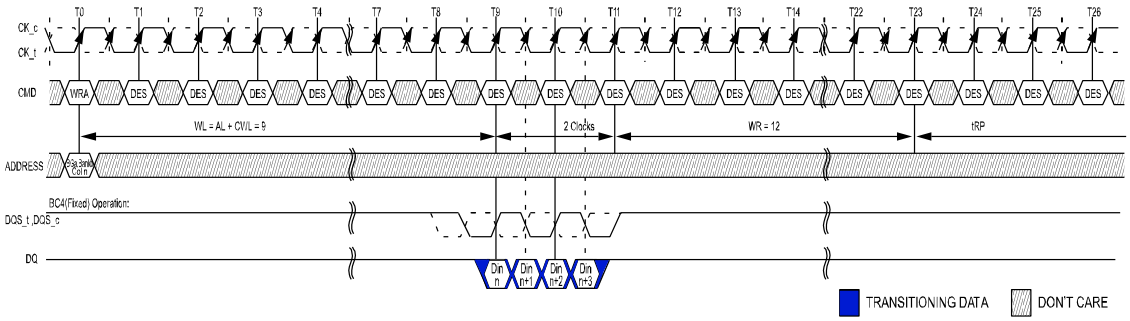
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 =1 during WRITE command at T0.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (WR) is referenced from the first rising clock edge after the last write data shown at T13. WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BC4) Fixed with Auto PRECHARGE Operation and 1tCK Preamble



NOTE 1 BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, WR = 12

NOTE 2 DIN n = data-in to column n.

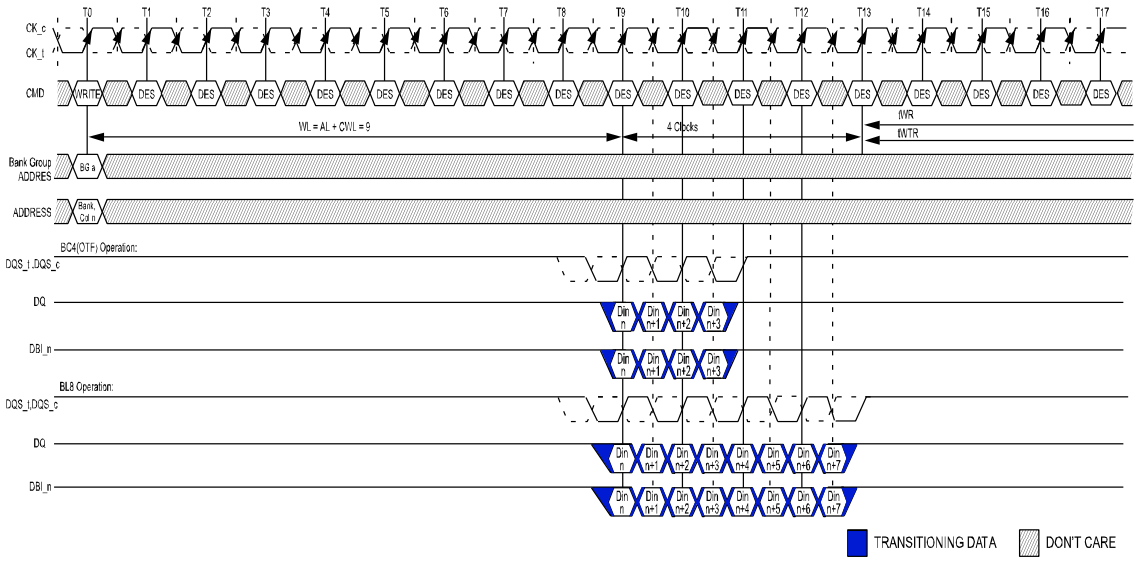
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11. WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BL8/BC4) OTF with 1tCK Preamble and DBI



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n.

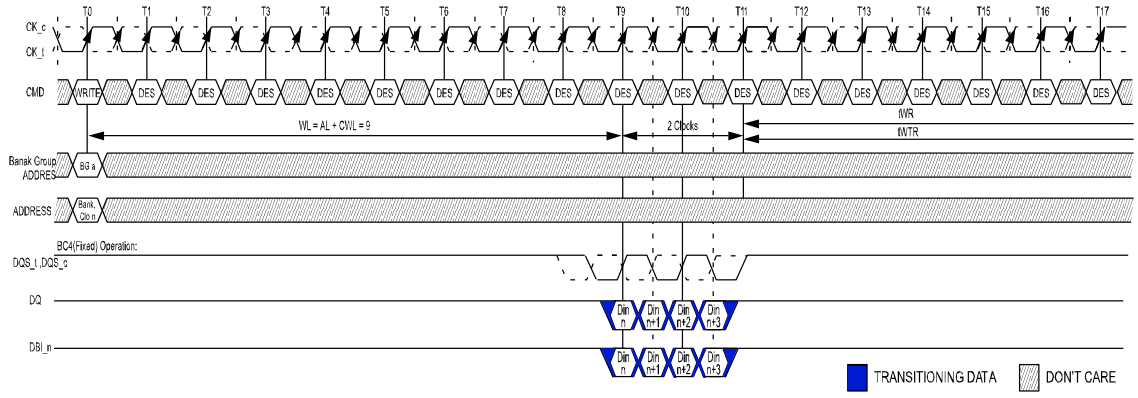
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Enable, CRC = Disable.

NOTE 6 The write recovery time (tWR_DBI) and write timing parameter (tWTR_DBI) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4) Fixed with 1tCK Preamble and DBI



NOTE 1 BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n.

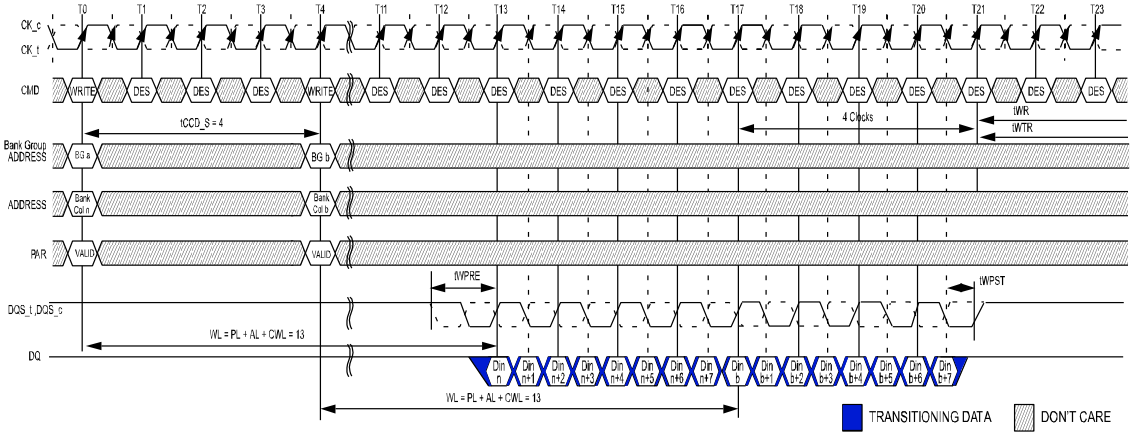
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0].

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Enable, CRC = Disable.

NOTE 6 The write recovery time (tWR_DBI) and write timing parameter (tWTR_DBI) are referenced from the first rising clock edge after the last write data shown at T11.

Consecutive WRITE (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, PL = 4, Preamble = 1tCK

NOTE 2 DIN n (or b) = data-in to column n(or column b).

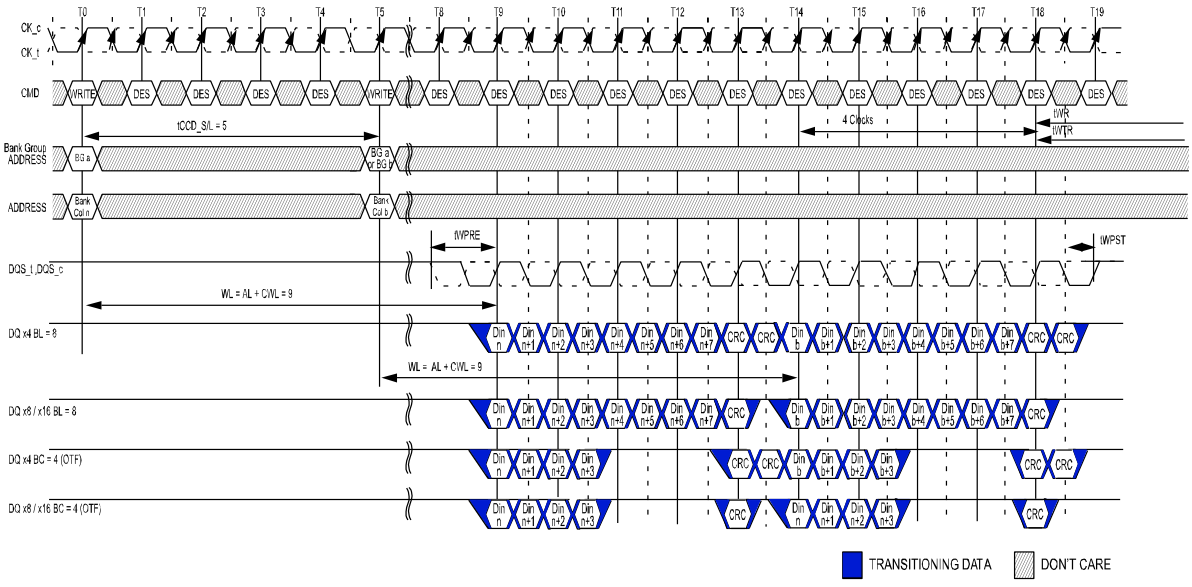
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0 and T4.

NOTE 5 CA Parity = Enable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.

Consecutive WRITE (BL8/BC4) OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8/BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5

NOTE 2 DIN n (or b) = data-in to column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

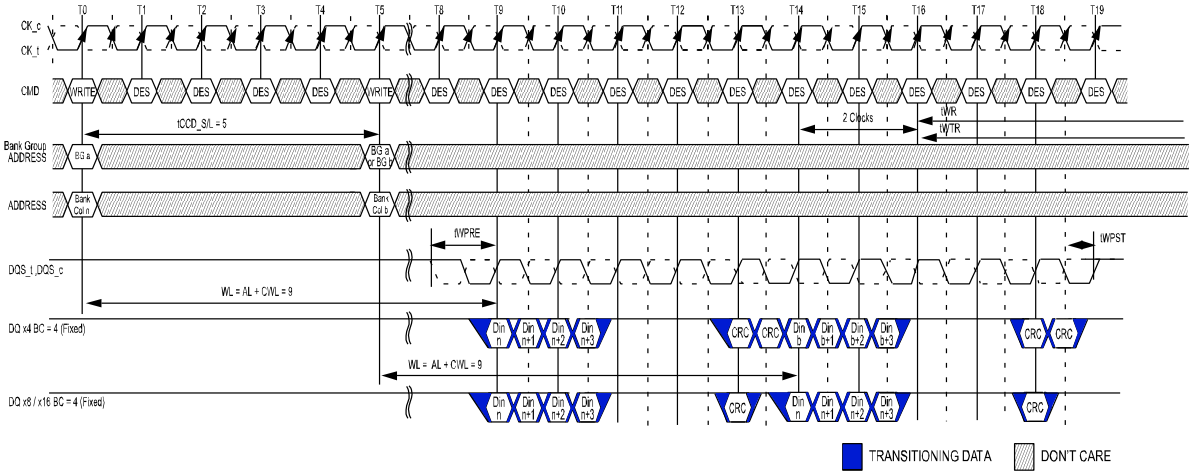
NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0 and T5.

NOTE 5 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T5.

NOTE 6 C/A Parity = Disable, $\overline{CS}$ to C/A Latency = Disable, Write DBI = Disable, Write CRC = Enable.

NOTE 7 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18

Consecutive WRITE (BC4)Fixed with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5

NOTE 2 DIN n (or b) = data-in to column n(or column b).

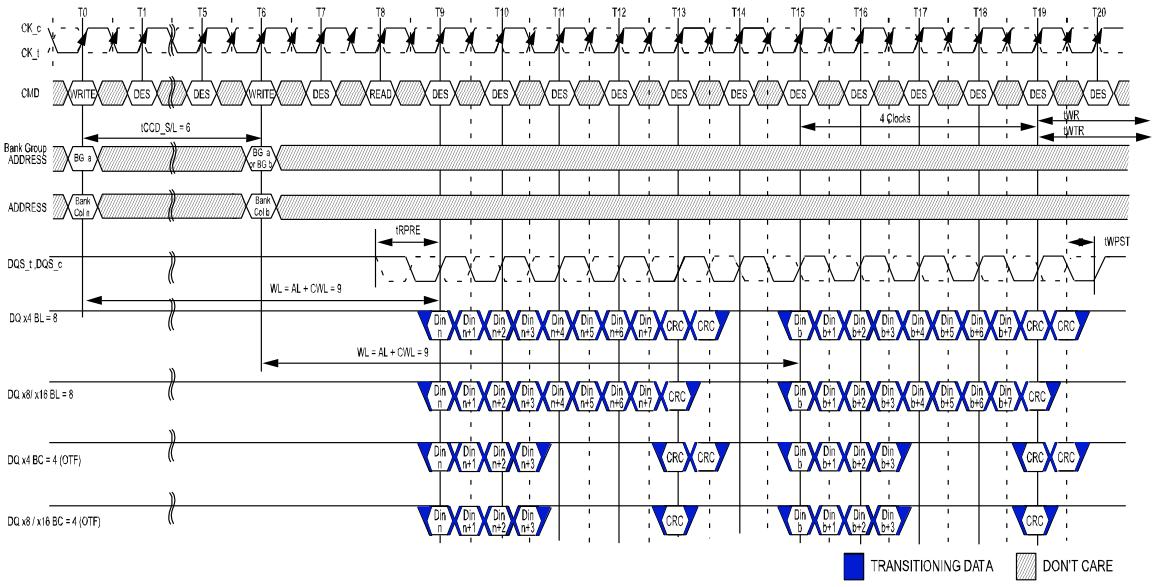
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0[A1:A0 = 1:0] at T0 and T5.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T16.

Nonconsecutive WRITE (BL8/BC4) OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 6

NOTE 2 DIN n (or b) = data-in to column n(or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

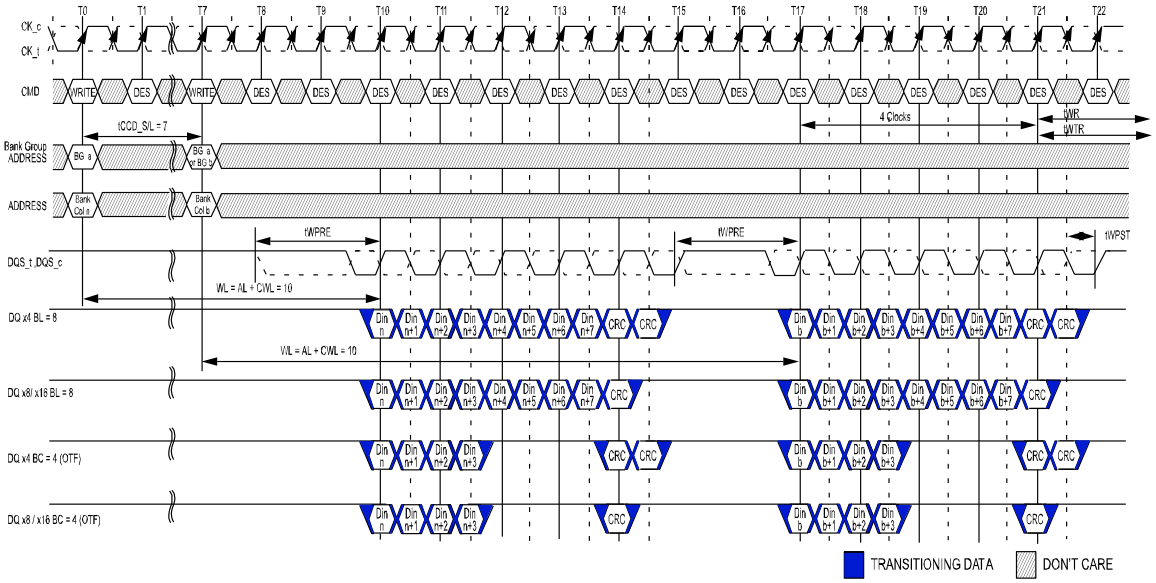
NOTE 4 BL8 setting activated by either MR0[A1A:0 = 0:0] or MR0[A1A:0 = 0:1] and A12 =1 during WRITE command at T0 and T6.

NOTE 5 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0 and T6.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.

NOTE 7 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T19.

Nonconsecutive WRITE (BL8/BC4) OTF with 2tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9 + 1 = 109, Preamble = 2tCK, tCCD_S/L = 7

NOTE 2 DIN n (or b) = data-in to column n(or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0 and T7.

NOTE 5 BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0 and T7.

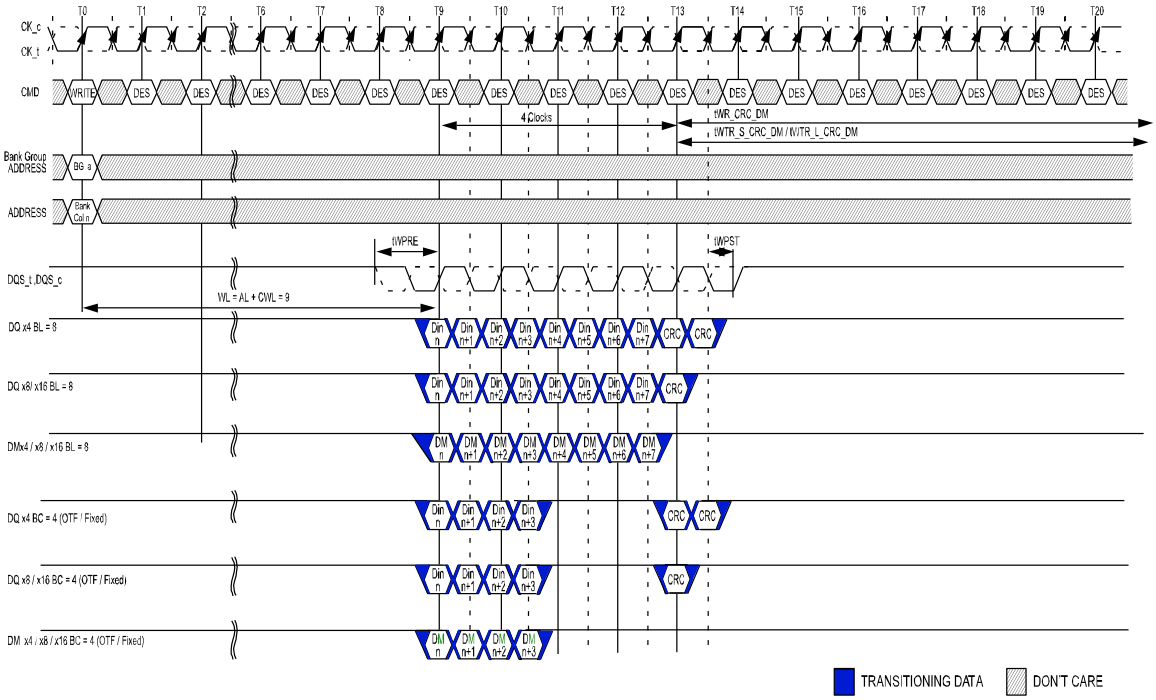
NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.

NOTE 7 tCCD_S/L = 6 isn't allowed in 2tCK preamble mode.

NOTE 8 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.

NOTE 9 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode

WRITE (BL8/BC4)OTF/Fixed with 1tCK Preamble and Write CRC and DM in Same or Different Bank Group



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.

NOTE 5 BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable, DM = Enable.

NOTE 7 The write recovery time (tWR_CRC_ DM) and write timing parameter (tWR_S_CRC_ DM/tWR_L_CRC_ DM) are referenced from the first rising clock edge after the last write data shown at T13.

ZQ Calibration Commands

ZQ Calibration command is used to calibrate DRAM RON and ODT values. The device needs a longer time to calibrate the output driver and on-die termination circuits at initialization and a relatively smaller time to perform periodic calibrations.

The ZQCL command is used to perform the initial calibration during the power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM and, once calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM IO, which is reflected as an updated output driver and on-die termination values. The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET are allowed a timing period of tZQoper.

The ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the Output Driver and ODT Voltage and Temperature Sensitivity tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the device is subjected to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the temperature and voltage sensitivities.

For example, if TSens = 1.5% / ^{o}C, VSens = 0.15% / mV, Tdriftrate = 1^{o}C / sec and Vdriftrate = 15 mV /sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

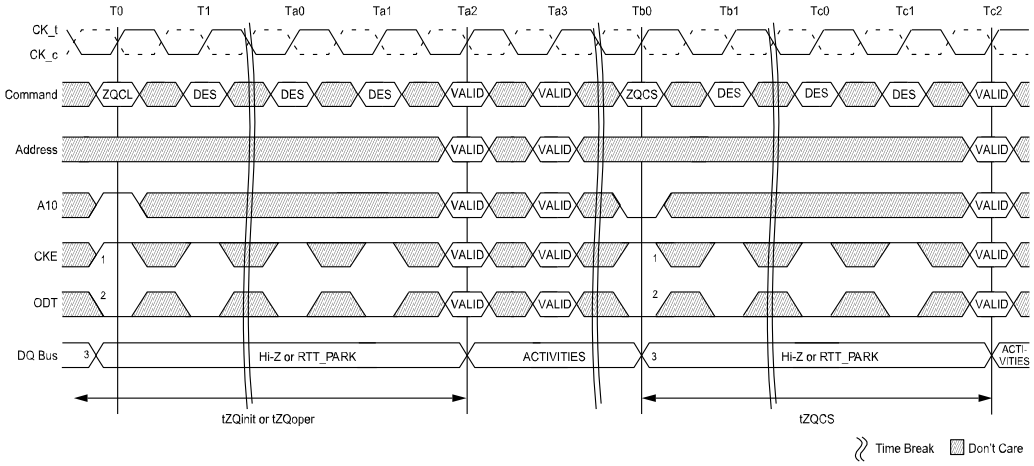
No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the device should disable the ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon self refresh exit, the device will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for a ZQ calibration command (short or long) after self refresh exit is tXSF.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between the devices.

ZQ Calibration Timing



NOTE 1 CKE must be continuously registered HIGH during the calibration procedure.

NOTE 2 On-die termination must be disabled via the ODT signal or MRS during the calibration procedure or the DRAM will automatically disable Rtt.

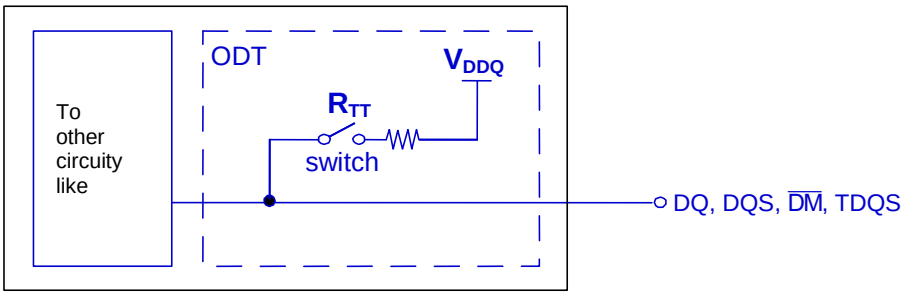
NOTE 3 All devices connected to the DQ bus should be High Z during the calibration procedure.

On-Die Termination (ODT)

On-die termination (ODT) is a feature of the DDR4 SDRAM that enables the DRAM to change termination resistance for each DQ, DQS, $\overline{DQS}$, and $\overline{DM}$ for x4 and x8 configuration (and DQS, $\overline{TDQS}$, for x8 configuration, when enabled via A11 = 1 in MR1) via the ODT control pin or WRITE command or default parking value with MR setting. For x16 configuration, ODT is applied to each UDQ, LDQ, LDQS, $\overline{LDQS}$, UDQS, $\overline{UDQS}$, $\overline{UDM}$ and $\overline{LDM}$ signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document.

The ODT feature is turned off and not supported in self refresh mode.

Functional Representation of ODT



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information. The value of RTT is determined by the settings of mode register bits (see Mode Register). The ODT pin will be ignored if the mode register MR1 is programmed to disable RTT_NOM [MR1[9,6,2] = 0,0,0] and in self refresh mode.

ODT Mode Register and ODT State Table

The ODT mode of the DDR4 device has four states: data termination disable, RTT_NOM, RTT_WR and RTT_PARK. The ODT mode is enabled if any of MR1[10,9,8] (RTT_NOM), MR2[11:9] (RTT_WR), or MR5[8:6] (RTT_PARK) are non-zero. When enabled, the value of RTT is determined by the settings of these bits.

RTT control of each RTT condition is possible with WR/RD command and ODT pin.

• RTT_WR: The rank that is being written to provide termination regardless of ODT pin status (either HIGH or LOW).

• RTT_NOM: DRAM turns ON RTT_NOM if it sees ODT asserted (except when ODT is disabled by MR1).

• RTT_PARK: Default parked value set via MR5 to be enabled and ODT pin is driven LOW.

• The Termination State Table below shows various interactions.

The RTT values have the following priority:

• Data termination disable

• RTT_WR

• RTT_NOM

• RTT_PARK

Termination State Table

RTT_PARK MR5[8:6]	RTT_NOM MR1[10:8]	ODT pin	DRAM termination state	Note
Enabled	Enabled	HIGH	RTT_NOM	1,2
		LOW	RTT_PARK	1,2
	Disabled	Don't care	RTT_PARK	1,2,3
Disabled	Enabled	HIGH	RTT_NOM	1,2
		LOW	Hi-Z	1,2
	Disabled	Don't care	Hi-Z	1,2,3

NOTE 1 When a READ command is executed, DRAM termination state will be High-Z for defined period independent of ODT pin and MR setting of RTT_PARK/RTT_NOM. This is described in the ODT During Read section.

NOTE 2 If RTT_WR is enabled, RTT_WR will be activated by WRITE command for defined period time independent of ODT pin and MR setting of RTT_PARK /RTT_NOM. This is described in the Dynamic ODT section.

NOTE 3 If RTT_NOM MR is disabled, ODT receiver power will be turned off to save power.

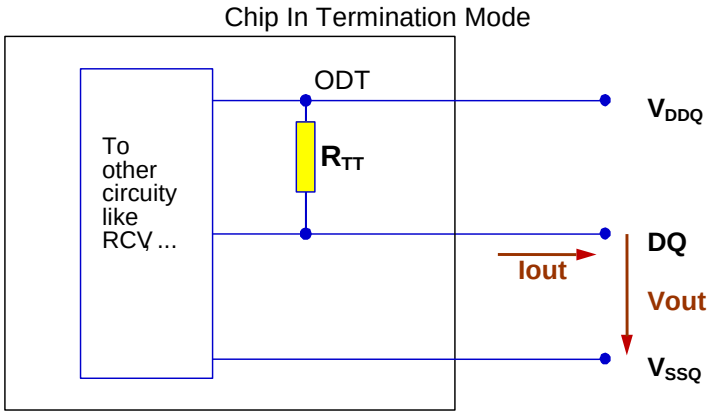
On-die termination effective resistances are defined and can be selected by any or all of the following options:

- MR1[10:8] (R_{TT}_NOM) - Disable, 240Ω, 120Ω, 80Ω, 60Ω, 48Ω, 40Ω, and 34Ω.
- MR2[11:9] (R_{TT}_WR) - Disable, 240Ω,120Ω, and 80Ω.
- MR5[8:6] (R_{TT}_PARK) - Disable, 240Ω, 120Ω, 80Ω, 60Ω, 48Ω, 40Ω, and 34Ω.

ODT is applied to the following inputs:

- X4: DQs, $\overline{DM}$, DQS, and DQS inputs.
- X8: DQs, $\overline{DM}$, DQS, $\overline{DQS}$, TDQS, and $\overline{TDQS}$ inputs.
- X16: DQs, $\overline{LDM}$, $\overline{UDM}$, LDQS, $\overline{LDQS}$, UDQS, and $\overline{UDQS}$ inputs.

ODT Definition of Voltages and Currents



Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes include the following:

• Any bank active with CKE HIGH

• Refresh with CKE HIGH

• Idle mode with CKE HIGH

• Active power-down mode (regardless of MR1 bit A10)

• Precharge power-down mode

In synchronous ODT mode, RTT_NOM will be turned on DODTLon clock cycles after ODT is sampled HIGH by a rising clock edge and turned off DODTLoff clock cycles after ODT is registered LOW by a rising clock edge. The ODT latency is determined by the programmed values for: CWL (CAS Write Latency), AL (additive Latency), and PL (Parity Latency) as well as the programmed state of the preamble.

ODT Latency and Posted ODT

In synchronous ODT mode, the ODT latencies are summarized in the table below. For details, refer to the latency definitions.

ODT Latency at DDR4-2133/-2400/-2666/-3200

Symbol	Parameter	1 tCK Preamble	2 tCK Preamble	Unit
DODTLon	Direct ODT turn on Latency	CWL + AL + PL – 2 CK	CWL + AL + PL – 3 CK	tCK
DODTLoff	Direct ODT turn off Latency	CWL + AL + PL – 2 CK	CWL + AL + PL – 3 CK	
RODTLoff	Read command to internal ODT turn off Latency	CWL + AL + PL – 2 CK	CWL + AL + PL – 3 CK	
RODTLon4	Read command to RTT_PARK turn on Latency in BC4-fixed	RODTLoff + 4	RODTLoff + 5	
RODTLon8	Read command to RTT_PARK turn on Latency in BC4/BL8-OTF	RODTLoff + 6	RODTLoff + 7	

NOTE 1 Applicable when WRITE CRC is disabled.

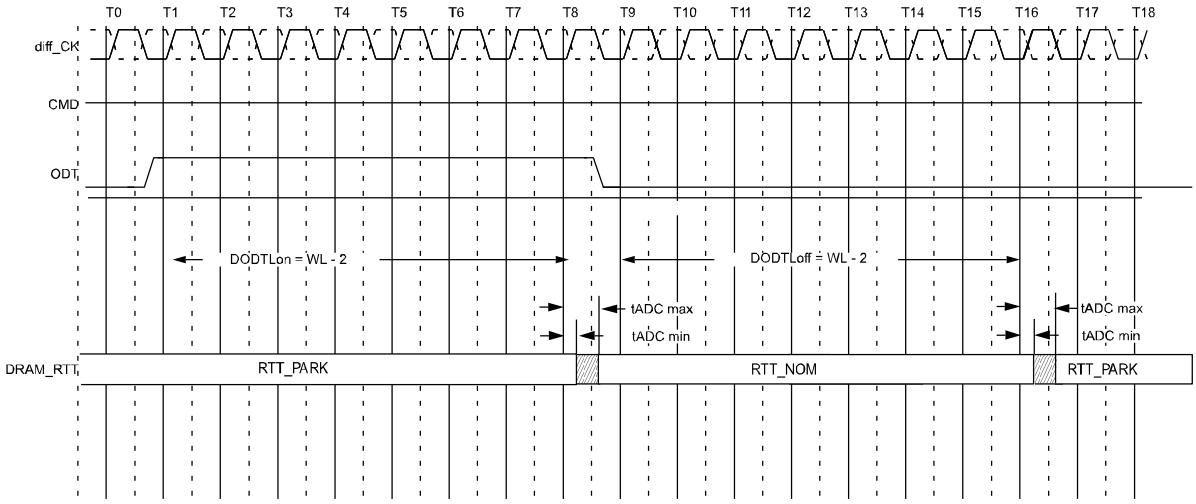
Timing Parameters

In synchronous ODT mode, the following parameters apply:

• DODTLon, DODTLoff, RODTLoff, RODTLon4, RODTLon8, tADC (MIN) (MAX).

• tADC (MIN) and tADC (MAX) are minimum and maximum RTT change timing skew between different termination values. These timing parameters apply to both the synchronous ODT mode and the data termination disable mode. When ODT is asserted, it must remain HIGH until minimum ODTH4 (BC = 4) or ODTH8 (BL = 8) is satisfied. If Write CRC Mode or 2 tCK Preamble Mode is enabled, ODTH should be adjusted to account for these. ODTH is measured from ODT first registered HIGH to ODT first registered LOW or from the registration of a WRITE command.

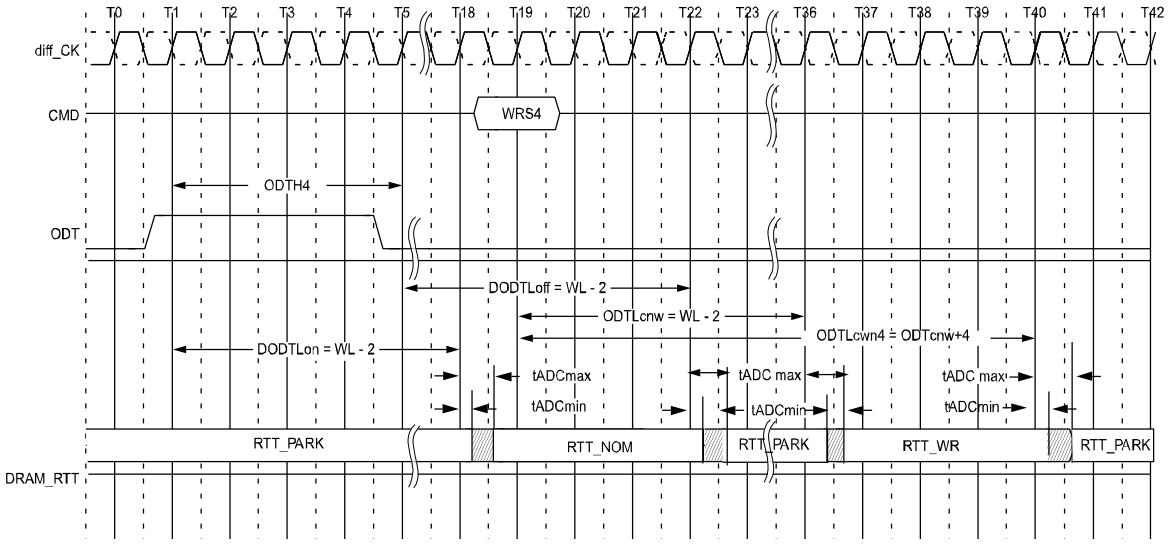
Synchronous ODT Timing with BL8



NOTE 1 Example for CWL = 9, AL = 0, PL = 0; DODTLon = AL + PL +CWL - 2 = 7; DODTLoff = AL + PL + CWL - 2 = 7.

NOTE 2 ODT must be held HIGH for at least ODTH8 after assertion (T1).

Synchronous ODT with BC4



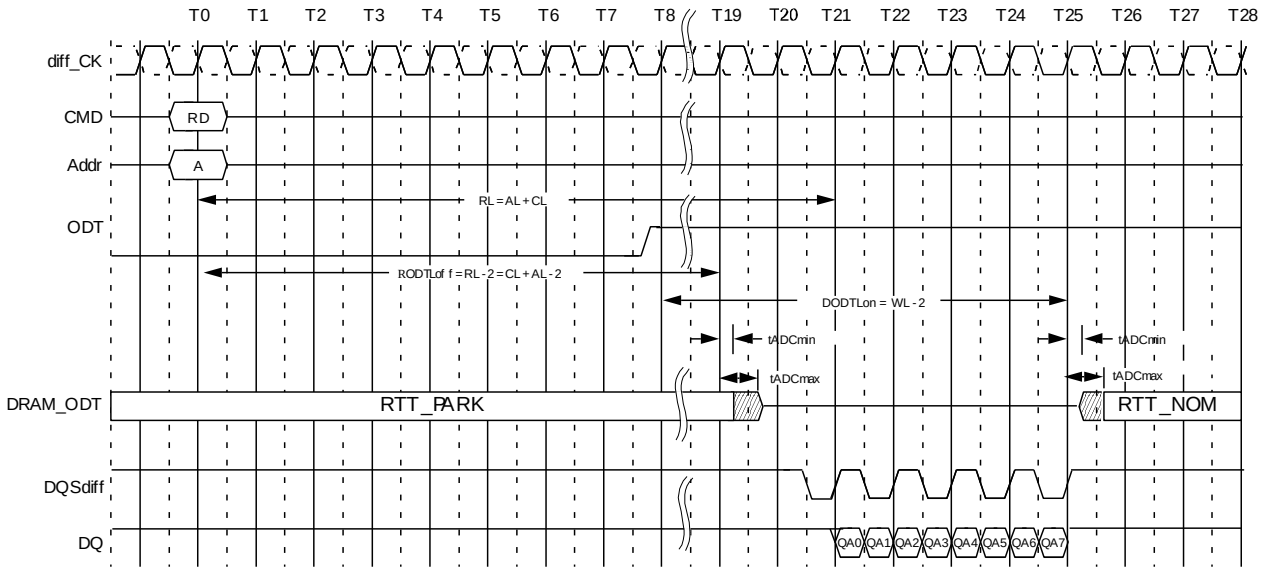
NOTE 1 Example for CWL = 9, AL = 10, PL = 0; DODTLon/off = AL + PL+ CWL - 2 = 17; ODTcnw = AL + PL+ CWL - 2 = 17.

NOTE 2 ODT must be held HIGH for at least ODTH4 after assertion (T1).

ODT During Reads

Because the DRAM cannot terminate with R_{TT} and drive with R_{ON} at the same time; R_{TT} may nominally not be enabled until the end of the postamble as shown in the example below. At cycle T25, the device turns on the termination when it stops driving, which is determined by tHZ. If the DRAM stops driving early (that is, tHZ is early), then tADC (MIN) timing may apply. If the DRAM stops driving late (that is, tHZ is late), then the DRAM complies with tADC (MAX) timing.

ODT During Reads



NOTE 1 Example for CL = 11; PL = 0, AL = CL - 1 = 10; RL = PL +AL + CL = 21; CWL= 9; DODTLon = PL + AL + CWL - 2 = 17; DODTLoff = PL + AL + CWL - 2 = 17;1tCK preamble

Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the device can be changed without issuing an MRS command. This requirement is supported by the dynamic ODT feature, described below.

Functional Description

The dynamic ODT mode is enabled if bit A9 or A10 of MR2 is set to 1.

- Three RTT values are available: RTT_NOM, RTT_WR, and RTT_PARK.
  - The value for RTT_NOM is preselected via bits MR1[10:8].
  - The value for RTT_WR is preselected via bits MR2[11:9].
  - The value for RTT_PARK is preselected via bits MR5[8:6].
- During operation without WRITE commands, the termination is controlled as follows:
  - Nominal termination strength RTT_NOM or RTT_PARK is selected.
  - RTT_NOM on/off timing is controlled via ODT pin and latencies DODTLon and DODTLoff; and RTT_PARK is on when ODT is LOW.
- When a WRITE command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
  - Latency ODTLcnw after the WRITE command, termination strength RTT_WR is selected.
  - Latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the WRITE command, termination strength RTT_WR is deselected. One or two clocks will be added into or subtracted from ODTLcwn8 and ODTLcwn4, depending on Write CRC Mode and/or 2 tCK preamble enablement.

The following table shows latencies and timing parameters which are relevant for the on-die termination control in dynamic ODT mode. The dynamic ODT feature is not supported in DLL-off mode. MRS command must be used to set RTT_WR, MR2[11:9] = 000, to disable dynamic ODT externally.

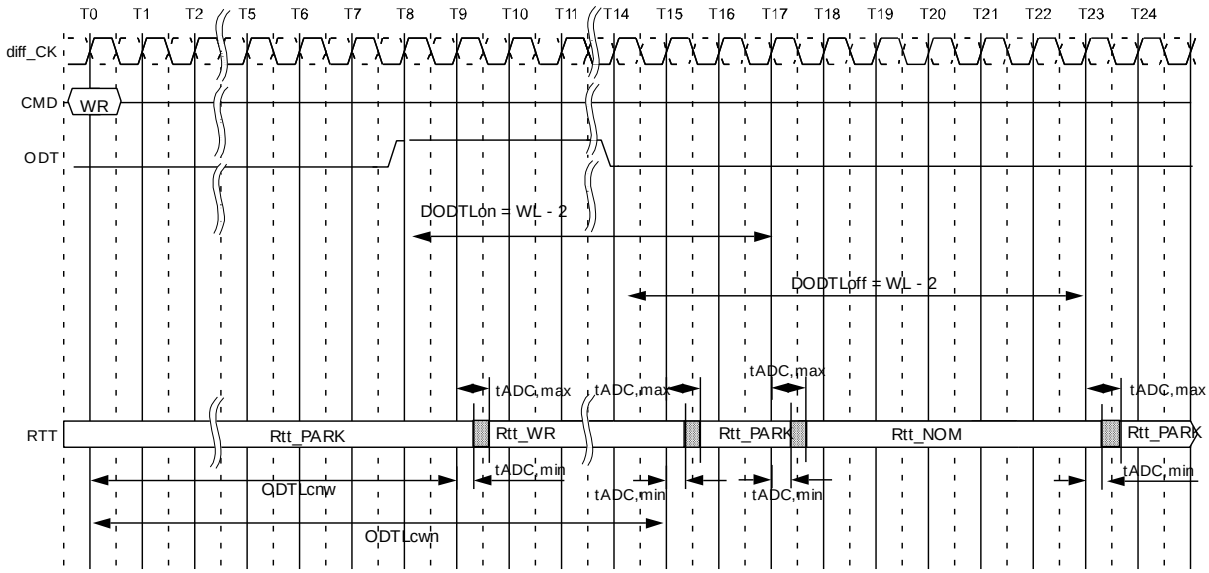
Dynamic ODT Latencies and Timing (1 tCK Preamble Mode and CRC Disabled)

Name and Description	Abbr.	Defined from	Define to	Definition for all DDR4 speed bins	Unit
ODT Latency for changing from RTT_PARK/RTT_NOM to RTT_WR	**ODTLcnw**	Registering external write command	Change RTT strength from RTT_PARK/RTT_NOM to RTT_WR	ODTLcnw = WL - 2	tCK
ODT Latency for change from RTT_WR to RTT_PARK/RTT_NOM (BL = 4)	**ODTLcwn4**	Registering external write command	Change RTT strength from RTT_WR to RTT_PARK/RTT_NOM	ODTLcwn4 = 4 + ODTLcnw	tCK
ODT Latency for change from RTT_WR to RTT_PARK/RTT_NOM (BL = 8)	**ODTLcwn8**	Registering external write command	Change RTT strength from RTT_WR to RTT_PARK/RTT_NOM	ODTLcwn8 = 6 + ODTLcnw	tCK(avg)
RTT change skew	**tADC**	ODTLcnw ODTLcwn	RTT valid	tADC(min) = 0.3 tADC(max) = 0.7	tCK(avg)

Dynamic ODT Latencies and Timing with Preamble Mode and CRC Mode Matrix

Symbol	1tck Preamble		2tck Preamble		Unit
	CRC off	CRC on	CRC off	CRC on	
ODTLcnw	WL - 2	WL - 2	WL - 3	WL - 3	tCK
ODTLcwn4	ODTLcnw +4	ODTLcnw +7	ODTLcnw +5	ODTLcnw +8	
ODTLcwn8	ODTLcnw +6	ODTLcnw +7	ODTLcnw +7	ODTLcnw +8	

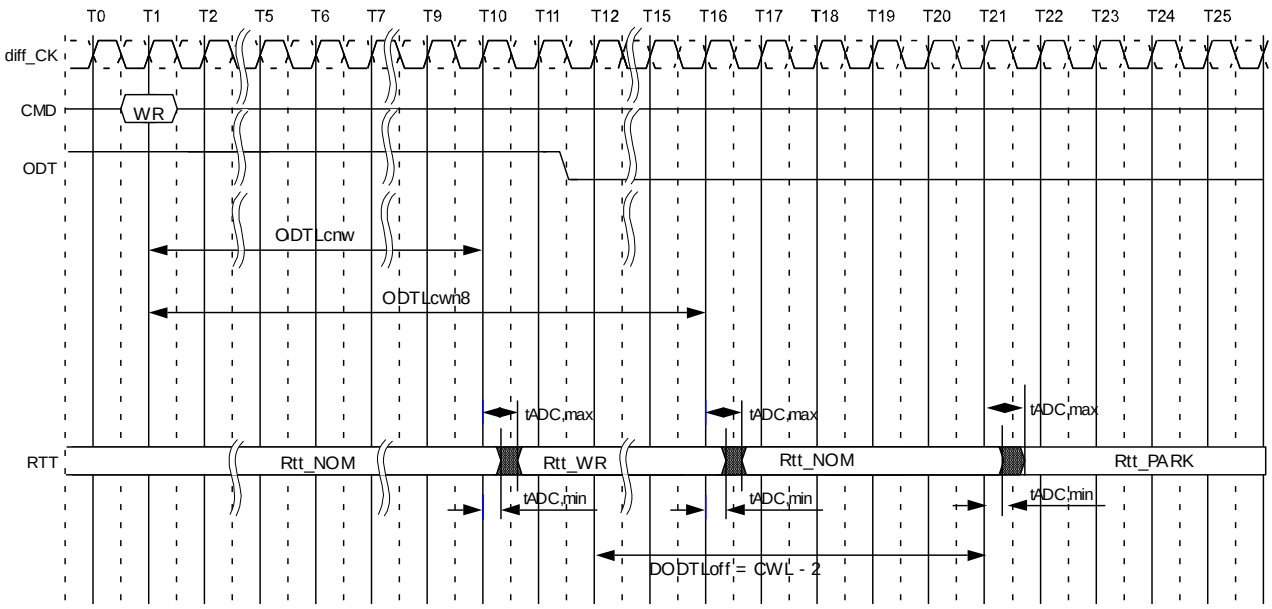
Dynamic ODT (1t CK Preamble; CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled)



NOTE 1 ODTLcnw = WL - 2 (1 tCK preamble) or WL - 3 (2 tCK preamble).

NOTE 2 If BC4 then ODTLcwn = WL+4 if CRC disabled or WL+5 if CRC enabled; If BL8 then ODTLcwn = WL+6 if CRC disabled or WL+7 if CRC enabled.

Dynamic ODT Overlapped with RTT_NOM (CL=14, CWL=11, BL=8, AL=0, CRC Disabled)



NOTE 1 Behavior with WR command issued while ODT is being registered HIGH.

Asynchronous ODT Mode

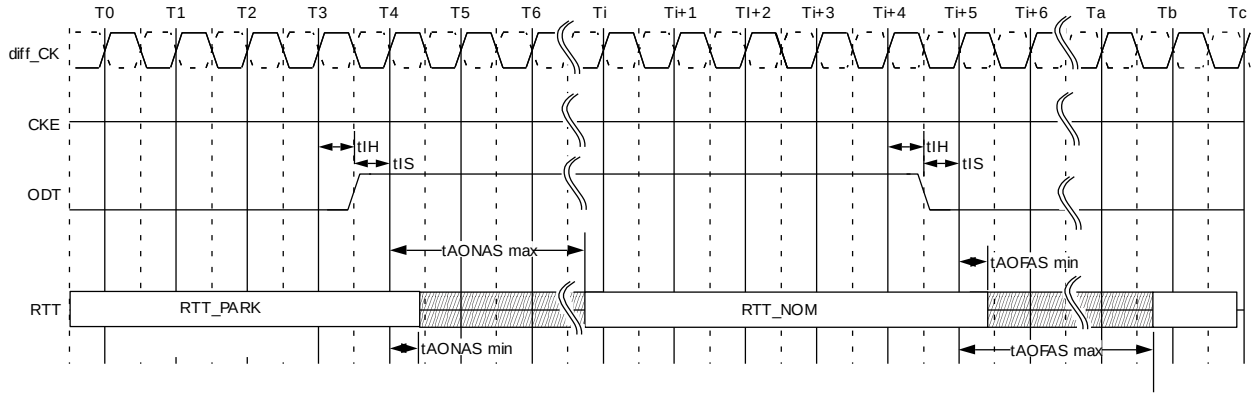
Asynchronous ODT mode is selected when DRAM runs in DLL off mode. In asynchronous ODT timing mode, the internal ODT command is *not* delayed by either Additive Latency (AL) or the Parity Latency (PL) relative to the external ODT signal (RTT_NOM).

In asynchronous ODT mode, two timing parameters apply: tAONAS (MIN/MAX), tAOFAS (MIN/MAX).

RTT_NOM turn-on time

- Minimum RTT_NOM turn-on time (tAONAS (MIN) is the point in time when the device termination circuit leaves RTT_PARK and ODT resistance begins to turn on.
- Maximum RTT_NOM turn-on time (tAONAS [MAX]) is the point in time when the ODT resistance has reached RTT_NOM.
- tAONAS (MIN) and tAONAS (MAX) are measured from ODT being sampled HIGH. RTT_NOM turn-off time
- Minimum RTT_NOM turn-off time (tAOFAS [MIN]) is the point in time when the device's termination circuit starts to leave RTT_NOM.
- Maximum RTT_NOM turn-off time (tAOFAS [MAX]) is the point in time when the on die termination has reached RTT_PARK.
- tAOFAS (MIN) and tAOFAS (MAX) are measured from ODT being sampled LOW.

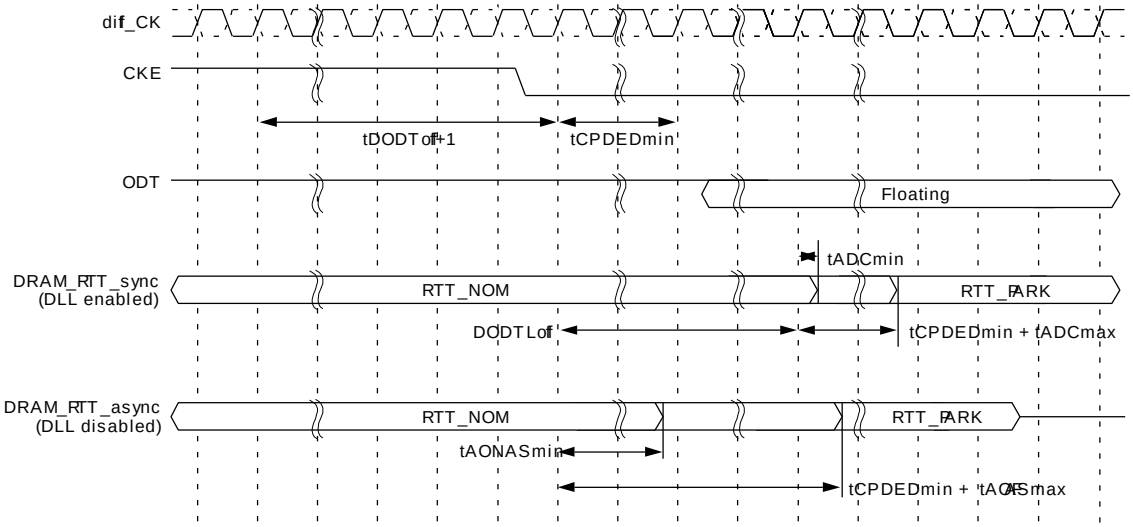
Asynchronous ODT Timings with DLL Off



ODT buffer disabled mode for Power down

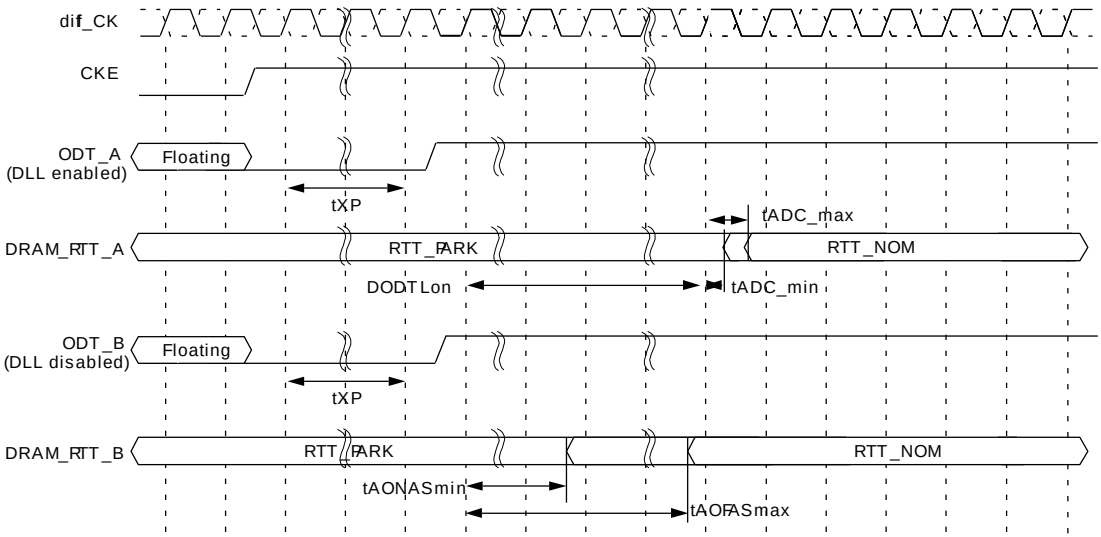
DRAM does not provide Rtt_NOM termination during power down when ODT input buffer deactivation mode is enabled in MR5 bit A5. To account for DRAM internal delay on CKE line to disable the ODT buffer and block the sampled output, the host controller must continuously drive ODT to either low or high when entering power down. The ODT signal may be floating after tCPDEDmin has expired. In this mode, RTT_NOM termination corresponding to sampled ODT at the input after CKE is first registered low (and tANPD before that) may not be provided. tANPD is equal to (WL-1) and is counted backwards from PDE.

ODT timing for power down entry with ODT buffer disable mode



When exit from power down, along with CKE being registered high, ODT input signal must be re-driven and maintained low until tXP is met.

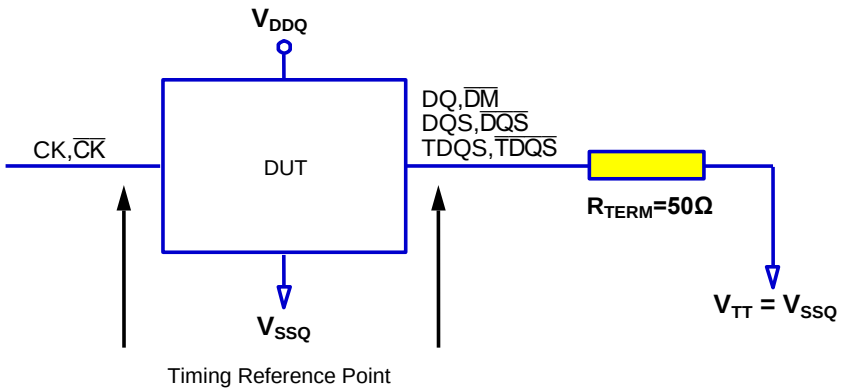
ODT timing for power down exit with ODT buffer disable mode



ODT Timing Definitions

The reference load for ODT timings is different than the reference load used for timing measurements.

ODT Timing Reference Load



ODT Timing Definitions and Waveforms

Definitions for tADC, tAONAS and tAOFAS are provided in the Table and measurement reference settings are provided in the subsequent. The tADC for the Dynamic ODT case and Read Disable ODT cases are represented by tADC of Direct ODT Control case.

ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition
tADC	Rising edge of CK, CK defined by the end point of **DODTLoff**	Extrapolated point at V_{RTT_NOM}
	Rising edge of CK, CK defined by the end point of **DODTLon**	Extrapolated point at V_{SSQ}
	Rising edge of CK - CK defined by the end point of **ODTLcnw**	Extrapolated point at V_{RTT_NOM}
	Rising edge of CK - CK defined by the end point of **ODTLcwn4** or **ODTLcwn8**	Extrapolated point at V_{SSQ}
tAONAS	Rising edge of CK, CK with ODT being first registered high	Extrapolated point at V_{SSQ}
tAOFAS	Rising edge of CK, CK with ODT being first registered low	Extrapolated point at V_{RTT_NOM}

Reference Settings for ODT Timing Measurements

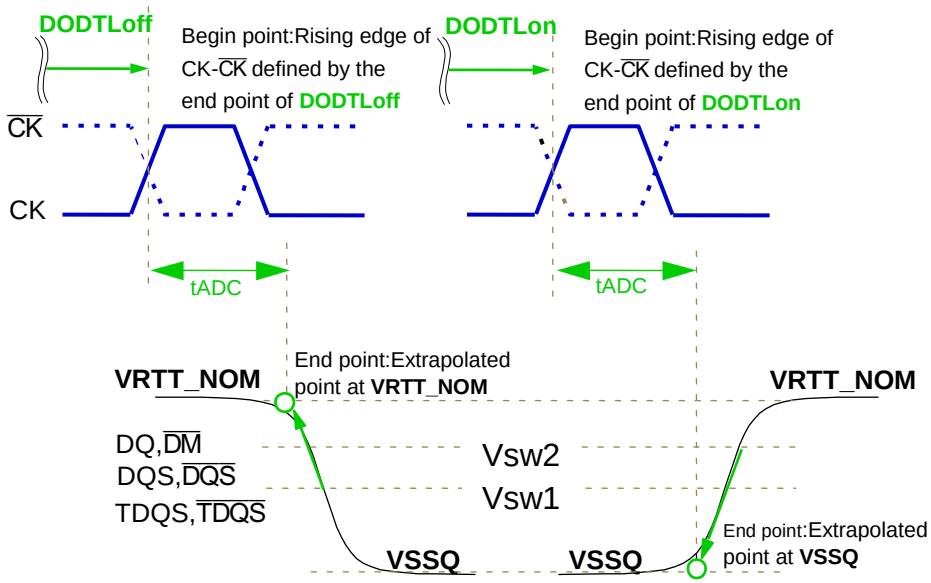
Measured Parameter	RTT_PARK	RTT_NOM	RTT_WR	Vsw1	Vsw2	Note
tADC	Disable	$R_{ZQ}/7$	–	0.20V	0.40V	1,2
	–	$R_{ZQ}/7$	Hi-Z	0.20V	0.40V	1,3
tAONAS	Disable	$R_{ZQ}/7$	–	0.20V	0.40V	1,2
tAOFAS	Disable	$R_{ZQ}/7$	–	0.20V	0.40V	

NOTE 1 MR setting is as follows.
- MR1 A10=1, A9=1, A8=1 (RTT_NOM_Setting)
- MR5 A8=0 , A7=0, A6=0 (RTT_PARK Setting)
- MR2 A11=0, A10=1, A9=1 (RTT_WR Setting)

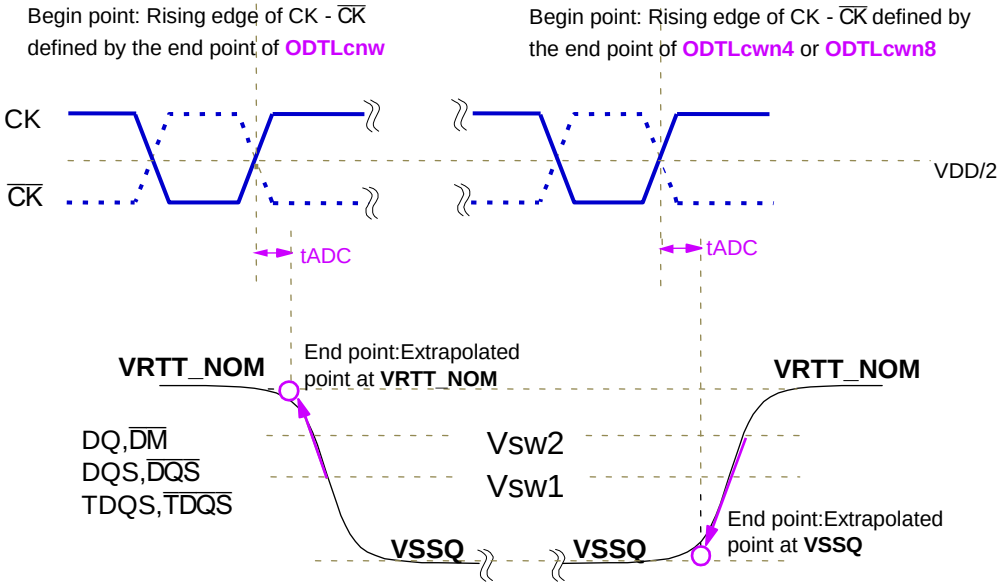
NOTE 2 ODT state change is controlled by ODT pin.

NOTE 3 ODT state change is controlled by Write Command.

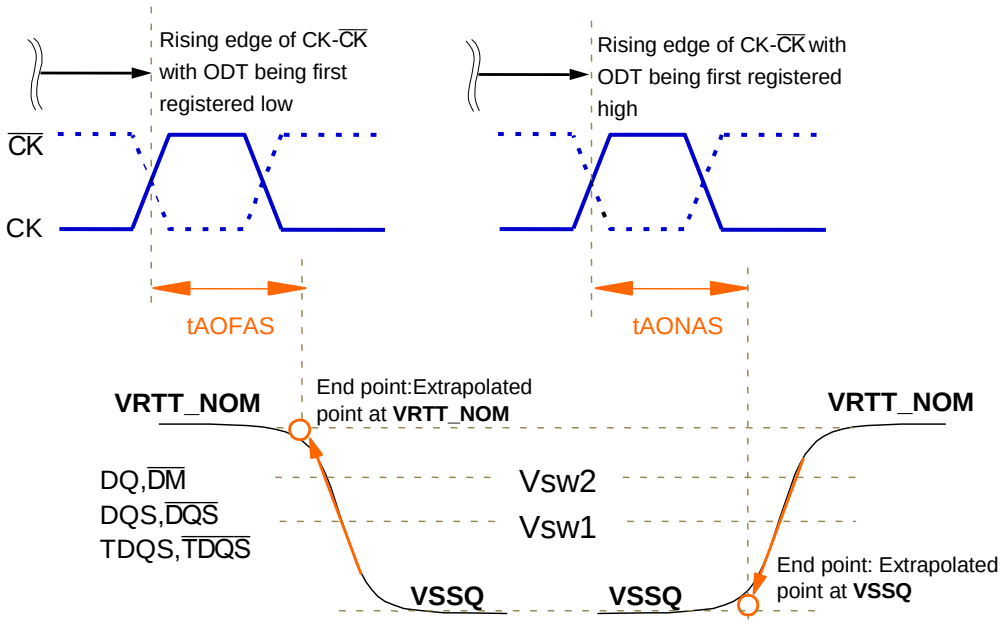
Definition of tADC at Direct ODT Control



Definition of tADC at Dynamic ODT Control



Definition of tAOFAS and tAONAS



Absolute Maximum DC Ratings

Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Symbol	Parameter	Min	Max	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3	1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3	1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3	3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3	1.5	V	1,3,5
T_{STG}	Storage Temperature	-55	100	°C	1,2

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51- 2 standard.

NOTE 3 VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV

NOTE 4 VPP must be equal or greater than VDD/VDDQ at all times.

NOTE 5 Refer to overshoot area above 1.5 V.

AC and DC Operating Conditions

Supply Operating Conditions

Recommended Supply Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP		2.375	2.5	2.75	V	3

NOTE 1 Under all conditions VDDQ must be less than or equal to VDD.

NOTE 2 VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

NOTE 3 The DC bandwidth is limited to 20MHz

AC and DC Single-Ended Input Measurement Levels ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ Input Levels (CMOS)

Symbol	Parameter	Min	Max	Unit	NOTE
VIH(AC)_RESET	AC Input High Voltage	0.8 x VDD	VDD	V	6
VIH(DC)_RESET	DC Input High Voltage	0.7 x VDD	VDD	V	2
VIL(DC)_RESET	DC Input Low Voltage	VSS	0.3 x VDD	V	1
VIL(AC)_RESET	AC Input Low Voltage	VSS	0.2 x VDD	V	7
TR_RESET	Rising time	–	1.0	µs	4
tPW_RESET	RESET pulse width	1.0	–	µs	3,5

NOTE 1 After $\overline{\text{RESET}}$ is registered LOW, $\overline{\text{RESET}}$ level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, the DRAM may not be reset.

NOTE 2 Once $\overline{\text{RESET}}$ is registered HIGH, $\overline{\text{RESET}}$ level must be maintained above VIH(DC)_RESET, otherwise, operation will be uncertain until it is reset by asserting $\overline{\text{RESET}}$ signal LOW.

NOTE 3 $\overline{\text{RESET}}$ is destructive to data contents

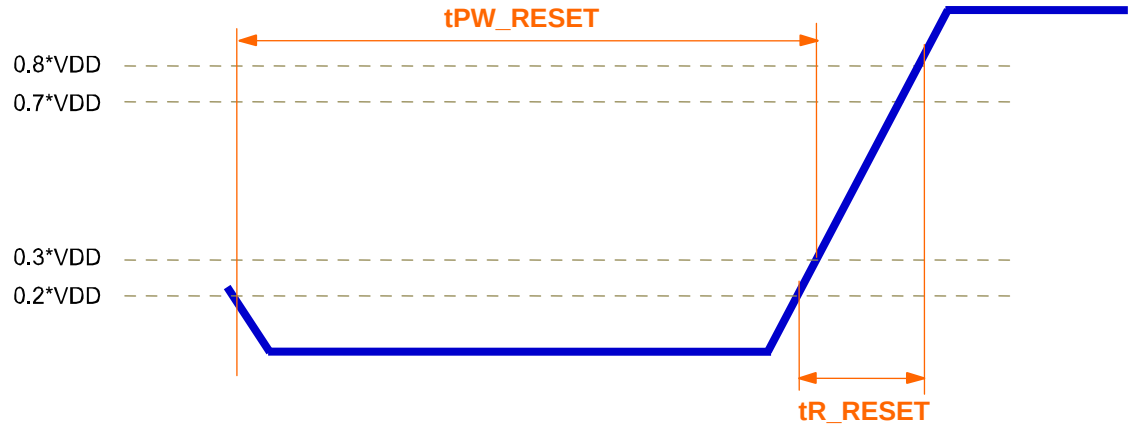
NOTE 4 No slope reversal(ringback) requirement during its level transition from Low to High.

NOTE 5 This definition is applied only “Reset Procedure at Power Stable”.

NOTE 6 Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.

NOTE 7 Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

CT Type-D Input Slew Rate Definition



Command/Address Input Levels

Command and Address Input Levels: DDR4-2133 through DDR4-2400

Symbol	Parameter	DDR4-2133/2400		DDR4-2666/3200		Unit	NOTE
		Min	Max	Min	Max		
VIH.CA(DC75)	DC input logic high	VREFCA + 0.075	VDD	TBD	TBD	V	
VIL.CA(DC75)	DC input logic low	VSS	VREFCA - 0.075	TBD	TBD	V	
VIH.CA(AC100)	AC input logic high	VREFCA + 0.1	NOTE 2	TBD	TBD	V	1
VIL.CA(AC100)	AC input logic low	NOTE 2	VREFCA - 0.1	TBD	TBD	V	1
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 x VDD	0.51 x VDD	TBD	TBD	V	2,3

NOTE 1 Refer to “Overshoot and Undershoot Specifications”.

NOTE 2 The ac peak noise on VREF may not allow VREF to deviate from VREFCA(DC) by more than ±1% VDD (for reference: approx. ± 12 mV).

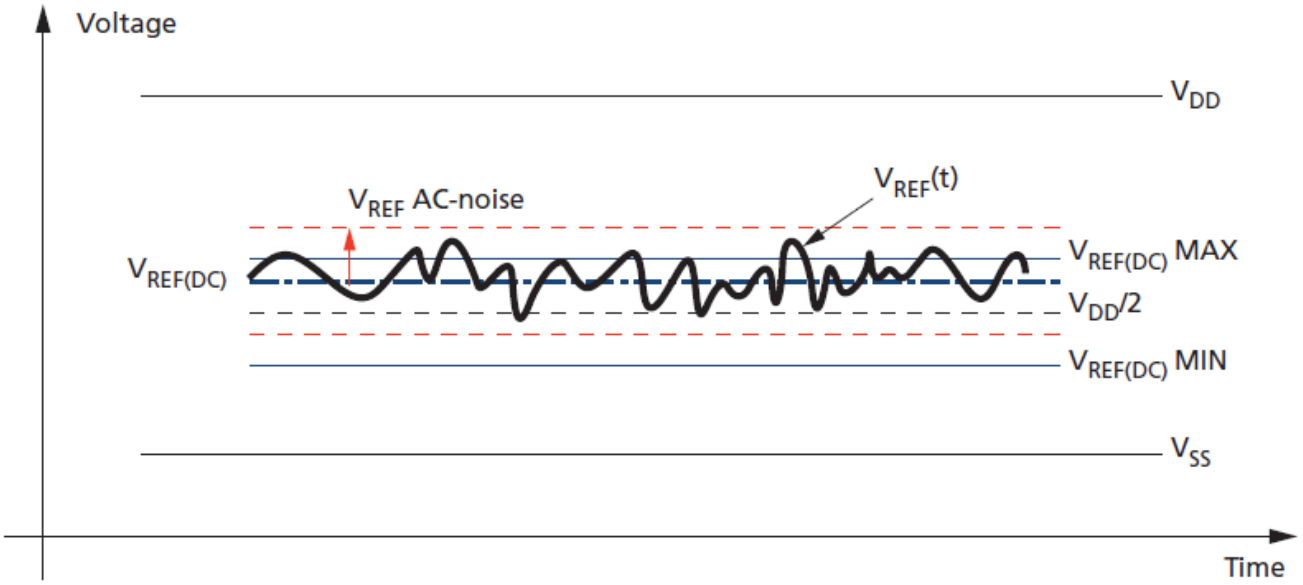
NOTE 3 For reference : approx. VDD/2 ± 12mV.

AC and DC Input Measurement Levels: VREF Tolerances

VREFCA is to be supplied to the DRAM and equal to VDD/2. The VREFCA is a reference supply input and therefore does not draw biasing current.

The DC-tolerance limits and AC-noise limits for the reference voltages VREFCA are illustrated in figure below. The figure shows a valid reference voltage VRef(t) as a function of time (VRef stands for VREFCA). VRef (DC) is the linear average of VRef(t) over a very long period of time (e.g., 1 sec). This average has to meet the min/max requirements. Furthermore VRef(t) may temporarily deviate from VRef(DC) by no more than +/- 1% VDD for the AC-noise limit.

VREFDQ Voltage Range

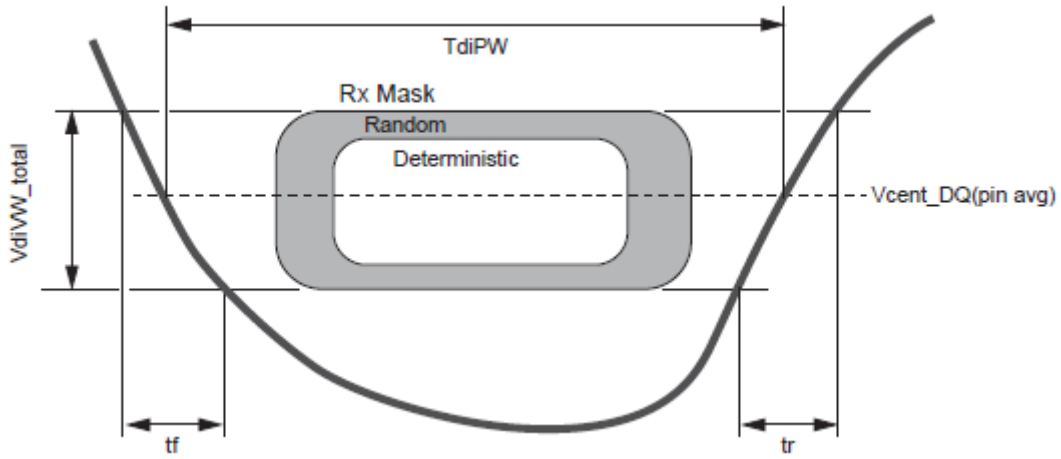


The voltage levels for setup and hold time measurements are dependent on VRef. “VRef ” shall be understood as VRef(DC), as defined in above figure. This clarifies that DC-variations of VRef affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VRef(DC) deviations from the optimum position within the data-eye of the input signals. This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VRef AC-noise. Timing and voltage effects due to AC-noise on VRef up to the specified limit (+/-1% of VDD) are included in DRAM timings and their associated deratings.

Data Receiver Input Requirements

The Write Timing section "Data Strobe to Data Relationship" details the Data receiver Rx mask operation to which the following parameters are applicable for. The figure below defines the measurement points for the Rx mask input slew rates, applicable on a per input basis.

DQ TdIPW and SRIN_dIVW definitions.



NOTE 1 SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

DQ Input Receiver Specifications

Symbol	Parameter	DDR4-2133		DDR4-2400		DDR4-2666/3200		Unit	NOTE
		Min.	Max.	Min.	Max.	Min.	Max.		
VdIVW_total	Rx Mask voltage - p-p total	–	136 [12]	–	TBD	–	TBD	mV	1,2,4,6
VdIVW_dV	Rx Mask voltage - deterministic	–	136	–	TBD	–	TBD	mV	1,5,13
TdIVW_total	Rx timing window total	–	0.2 [12]	–	TBD	–	TBD	UI	1,2,4,6
TdIVW_dj	Rx deterministic timing	–	0.2	–	TBD	–	TBD	UI	1,5, 13
VIHL_AC	DQ AC input swing pk-pk	186	–	TBD	–	TBD	–	mV	7
TdIPW	DQ input pulse width	0.58	TBD	TBD		TBD		UI	8
Tdqs_off	DQ to DQS Setup offset	–	TBD	–	TBD	–	TBD	UI	9
Tdqh_off	DQ to DQS Hold offset	–	TBD	–	TBD	–	TBD	UI	9
Tdqs_dd_off	DQ to DQ Setup offset	–	TBD	–	TBD	–	TBD	UI	10
Tdqh_dd_off	DQ to DQ Hold offset	–	TBD	–	TBD	–	TBD	UI	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	TBD	9	TBD	TBD	TBD	TBD	V/ns	11

NOTE 1 Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(pin avg). The data Rx mask is applied per bit and should include voltage and temperature drift terms. The design specification is BER <1e-16 and how this varies for lower BER is tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tbd).

NOTE 2 Rx mask voltage AC swing peak-peak requirement over TdIVW_total with at least half of TdIVW_total(max) above Vcent_DQ(pin avg) and at least half of TdIVW_total(max) below Vcent_DQ(pin avg).

NOTE 3 Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels centered around Vcent_DQ(pin avg).

NOTE 4 Defined over the DQ internal Vref range 1.

NOTE 5 Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method tbd

NOTE 6 Overshoot and Undershoot Specifications tbd.

NOTE 7 DQ input pulse signal swing into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin avg)

NOTE 8 DQ minimum input pulse width defined at the Vcent_DQ(pin avg).

NOTE 9 DQ to DQS setup or hold offset defined within byte from DRAM ball to DRAM internal latch; tDQS and tDQH are the minimum DQ setup and hold per DQ pin; each is equal to one-half of TdIVW_total(max).

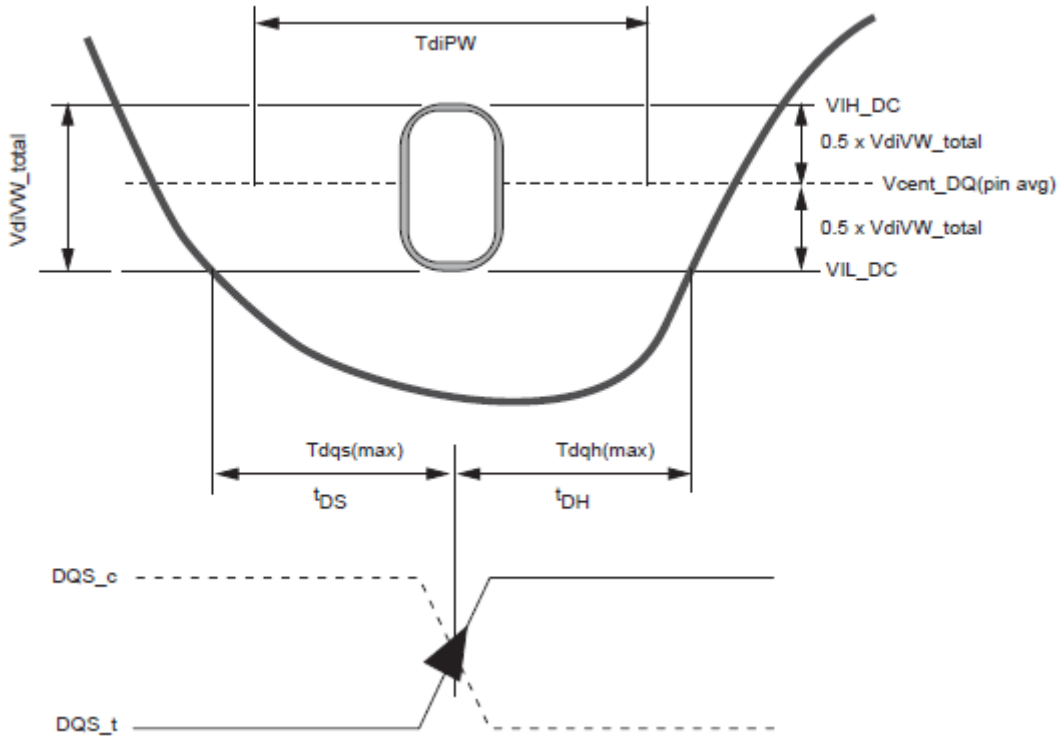
NOTE 10 DQ to DQ setup or hold delta offset within byte. Defined as the static difference in Tdqs_off(max) and Tdqs_off(min) or Tdqh(max) – Tdqh(min) for a given component, from DRAM ball to DRAM internal latch.

NOTE 11 Input slew rate over VdIVW Mask centered at Vcent_DQ(pin avg). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within tbd V/ns of each other.

NOTE 12 The total timing and voltage terms(tdIVW_total & VdIVWtotal) are valid for any BER lower {lower fail rate} than the spec.

NOTE 13 VdIVW_total - VdIVW_dV and TdIVW_total - TdIVW_dj define the difference between random and deterministic fail mask. When VdIVW_total - VdIVW_dV = 0 and TdIVW_total - TdIVW_dj = 0, random error is assumed to be zero.

Rx Mask to tDS/tDH Conversion



Connectivity Test (CT) Mode Input Levels

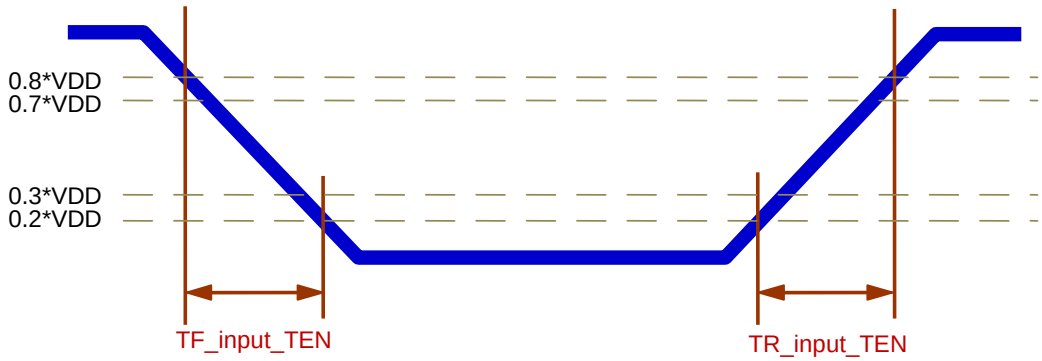
CMOS rail to rail Input Levels for TEN

Symbol	Parameter	Min	Max	Unit	NOTE
$VIH_{(AC)\_TEN}$	TEN AC Input High Voltage	0.8 x VDD	VDD	V	1
$VIH_{(DC)\_TEN}$	TEN DC Input High Voltage	0.7 x VDD	VDD	V	
$VIL_{(DC)\_TEN}$	TEN DC Input Low Voltage	VSS	0.3 x VDD	V	
$VIL_{(AC)\_TEN}$	TEN AC Input Low Voltage	VSS	0.2 x VDD	V	2
$TF_{\_input\_TEN}$	TEN Input signal Falling time	–	10	ns	
$TR_{\_input\_TEN}$	TEN Input signal Rising time	–	10	ns	

NOTE 1 Overshoot should not exceed the Vin Absolute Maximum Ratings.

NOTE 2 Undershoot should not exceed the Vin Absolute Maximum Ratings.

TEN Input Slew Rate Definition



CT Type-A Input Levels ($\overline{CS}$, Address, ODT, CKE, CK, $\overline{CK}$, PAR)

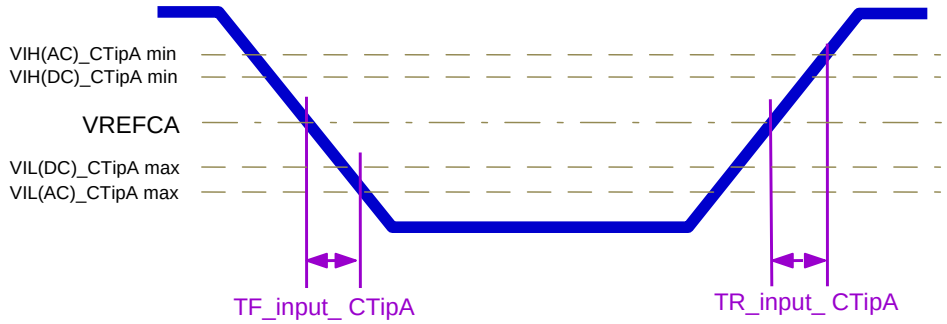
Symbol	Parameter	Min	Max	Unit	Notes
$VIH_{(AC)\_CTipA}$	CTipA AC Input High Voltage	VREFCA + 0.2	NOTE 1	V	
$VIH_{(DC)\_CTipA}$	CTipA DC Input High Voltage	VREFCA + 0.15	VDD	V	
$VIL_{(DC)\_CTipA}$	CTipA DC Input Low Voltage	VSS	VREFCA - 0.15	V	
$VIL_{(AC)\_CTipA}$	CTipA AC Input Low Voltage	NOTE 1	VREFCA - 0.2	V	
$TF_{\_input\_CTipA}$	CTipA Input signal Falling time	–	5	ns	
$TR_{\_input\_CTipA}$	CTipA Input signal Rising time	–	5	ns	

NOTE 1 Refer to "Overshoot and Undershoot Specifications".

NOTE 2 CT Type-A inputs: $\overline{CS}$, BG0-1, BA0-1, A0-A9, A10/AP, A11, A12/$\overline{BC}$, A13, $\overline{WE}$/A14, $\overline{CAS}$/A15, $\overline{RAS}$/A16, CKE, $\overline{ACT}$, ODT, CK, $\overline{CK}$, PAR .

NOTE 3 VREFCA = 0.5 x VDD

CT Type-A Input Slew Rate Definition



CT Type-B Input Levels ($\overline{DM}/\overline{DBI}$, $\overline{LDM}/\overline{LDBI}$, $\overline{UDM}/\overline{UDBI}$)

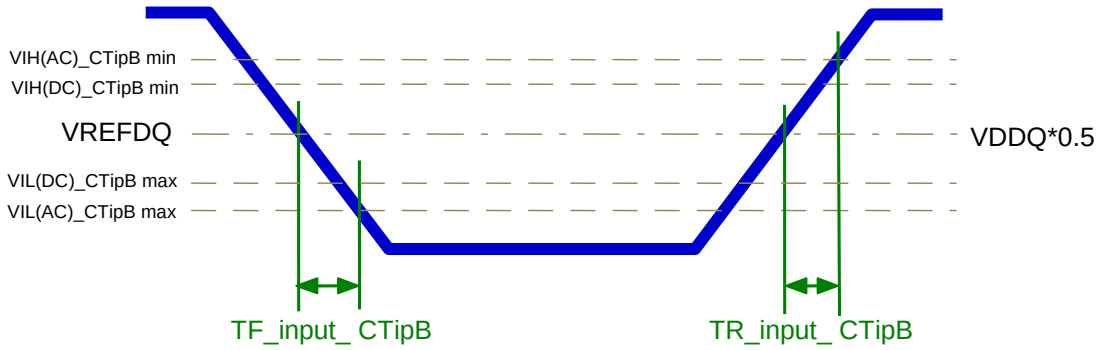
Symbol	Parameter	Min	Max	Unit	Notes
$V_{IH(AC)\_CTipB}$	CTipB AC Input High Voltage	VREFDQ + 0.3	Note 2	V	1
$V_{IH(DC)\_CTipB}$	CTipB DC Input High Voltage	VREFDQ + 0.2	VDDQ	V	1
$V_{IL(DC)\_CTipB}$	CTipB DC Input Low Voltage	VSSQ	VREFDQ - 0.2	V	1
$V_{IL(AC)\_CTipB}$	CTipB AC Input Low Voltage	Note 2	VREFDQ - 0.3	V	1
$TF_{\_input\_CTipB}$	CTipB Input signal Falling time	–	5	ns	1
$TR_{\_input\_CTipB}$	CTipB Input signal Rising time	–	5	ns	1

NOTE 1 Refer to “Overshoot and Undershoot Specifications”.

NOTE 2 CT Type-B inputs: $\overline{DM}/\overline{DBI}$, $\overline{LDM}/\overline{LDBI}$ and $\overline{UDM}/\overline{UDBI}$.

NOTE 3 VREFDQ should be 0.5 x VDD

CT Type-B Input Slew Rate Definition



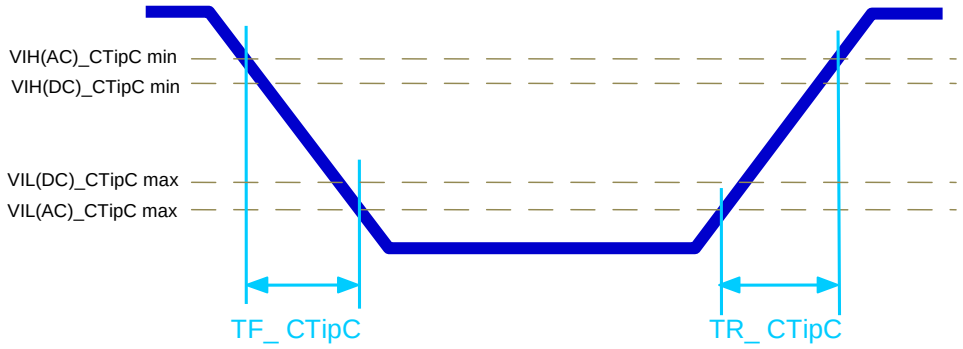
CT Type-C Input Levels ($\overline{ALERT}$)

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IH(AC)\_CTipC}$	CTipC AC Input High Voltage	0.8 x VDD	VDD	V	1
$V_{IH(DC)\_CTipC}$	CTipC DC Input High Voltage	0.7 x VDD	VDD	V	
$V_{IL(DC)\_CTipC}$	CTipC DC Input Low Voltage	VSS	0.3 x VDD	V	
$V_{IL(AC)\_CTipC}$	CTipC AC Input Low Voltage	VSS	0.2 x VDD	V	2
T_{F_CTipC}	CTipC Falling time	–	10	ns	
T_{R_CTipC}	CTipC Rising time	–	10	ns	

NOTE 1 Refer to “Overshoot and Undershoot Specifications”.

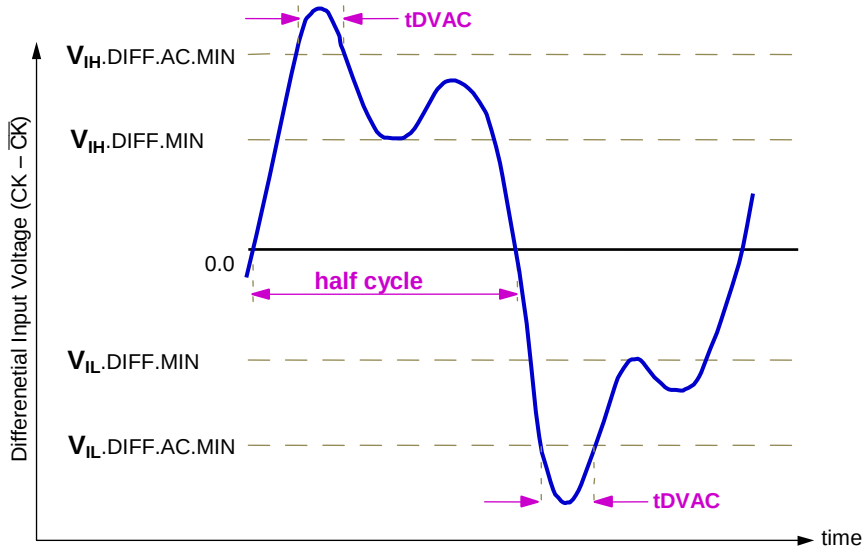
NOTE 2 CT Type-C inputs: $\overline{ALERT}$.

CT Type-C Input Slew Rate Definition



AC and DC Logic Input Levels for Differential Signals

Differential signal definition



NOTE 1 Differential signal rising edge from VIL_DIFF(MAX) to VIH_DIFF_AC(MIN) must be monotonic slope.

NOTE 2 Differential signal falling edge from VIH_DIFF(MIN) to VIL_DIFF_AC(MAX) must be monotonic slope.

Differential Input Swing Requirements for CK - $\overline{CK}$

Symbol	Parameter	DDR4 -2133		DDR4 -2400/2666/3200		Unit	NOTE
		Min	Max	Min	Max		
VIH_{diff}	differential input high	+0.150	NOTE 3	TBD	NOTE 3	V	1
VIL_{diff}	differential input low	NOTE 3	-0.150	NOTE 3	TBD	V	1
$VIH_{diff(AC)}$	differential input high ac	2 x (VIH(AC) - VREF)	NOTE 3	2 x (VIH(AC) - VREF)	NOTE 3	V	2
$VIL_{diff(AC)}$	differential input low ac	NOTE 3	2 x (VIL(AC) - VREF)	NOTE 3	2 x (VIL(AC) - VREF)	V	2

NOTE 1 Used to define a differential signal slew-rate.

NOTE 2 For CK - $\overline{CK}$ use VIH(AC) and VIL(AC) of ADD/CMD and VREFCA.

NOTE 3 These values are not defined; however, the differential signals (CK, $\overline{CK}$) need to be within the respective limits, VIH(DC) max and VIL(DC) min for single-ended signals as well as the limitations for overshoot and undershoot.

Minimum Time AC time tDVAC for CK

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(AC)| = 200mV		tDVAC [ps] @ |VIH/Ldiff(AC)| = TBDmV	
	Min	Max	Min	Max
> 4.0	120	–	TBD	–
4.0	115	–	TBD	–
3.0	110	–	TBD	–
2.0	105	–	TBD	–
1.8	100	–	TBD	–
1.6	95	–	TBD	–
1.4	90	–	TBD	–
1.2	85	–	TBD	–
1.0	80	–	TBD	–
< 1.0	80	–	TBD	–

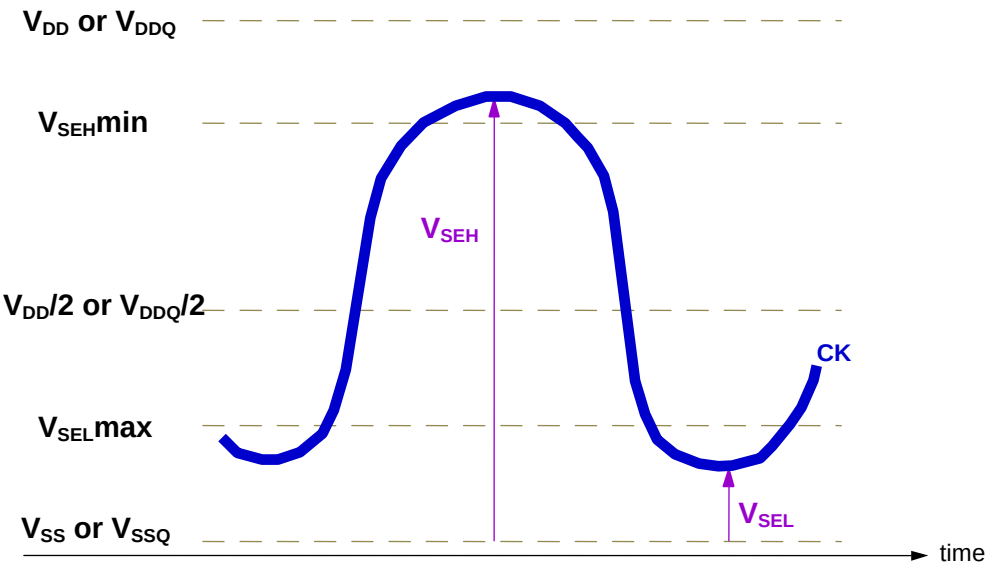
NOTE 1 Below VIL(AC)

Single-ended requirements for CK differential signals

Each individual component of a differential signal (CK, $\overline{CK}$) has also to comply with certain requirements for single-ended signals. CK and $\overline{CK}$ have to reach approximately VSEHmin / VSELmax , approximately equal to the ac-levels $V_{IH(AC)}$ and $V_{IL(AC)}$ for ADD/CMD signals in every half-cycle. The applicable ac-levels for ADD/CMD might be different per speed-bin etc. e.g., if a value other than 100mV is used for ADD/CMD $V_{IH(AC)}$ and $V_{IL(AC)}$ signals, then these ac-levels apply also for the single-ended signals CK and $\overline{CK}$.

While ADD/CMD signal requirements are with respect to V_{REFCA}, the single-ended components of differential signals have a requirement with respect to V_{DD} / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended requirement for CK



Single-Ended Requirements for CK

Symbol	Parameter	DDR4-2133		DDR4-2400/2666/3200		Unit	NOTE
		Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for CK , $\overline{CK}$	(VDD/2)+0.100	NOTE 3	TBD	NOTE 3	V	1,2
V_{SEL}	Single-ended low-level for CK , $\overline{CK}$	NOTE 3	(VDD/2)-0.100	NOTE 3	TBD	V	1,2

NOTE 1 For CK - $\overline{CK}$ use VIH(AC) and VIL(AC) of ADD/CMD and VREFCA.

NOTE 2 ADDR/CMD VIH(AC) and VIL(AC) based on VREFCA.

NOTE 3 These values are not defined; however, the differential signals (CK, $\overline{CK}$) need to be within the respective limits, VIH(DC) max and VIL(DC) min for single-ended signals as well as the limitations for overshoot and undershoot.

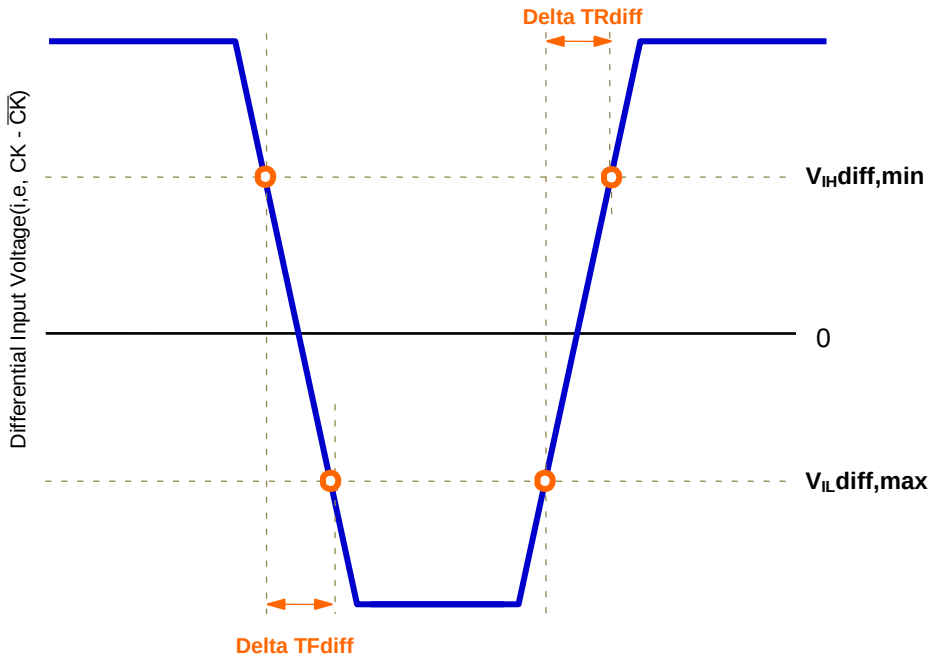
Slew Rate Definitions for CK Differential Input Signals

CK Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge(CK - $\overline{CK}$)	$VIL_{,diff,max}$	$VIH_{,diff,min}$	[$VIH_{,diff,min}$ – $VIL_{,diff,max}$] /ΔTRdiff
Differential input slew rate for falling edge(CK - $\overline{CK}$)	$VIH_{,diff,min}$	$VIL_{,diff,max}$	[$VIH_{,diff,min}$ – $VIL_{,diff,max}$] /ΔTFdiff

NOTE 1 The differential signal CK - $\overline{CK}$ must be monotonic between these thresholds.

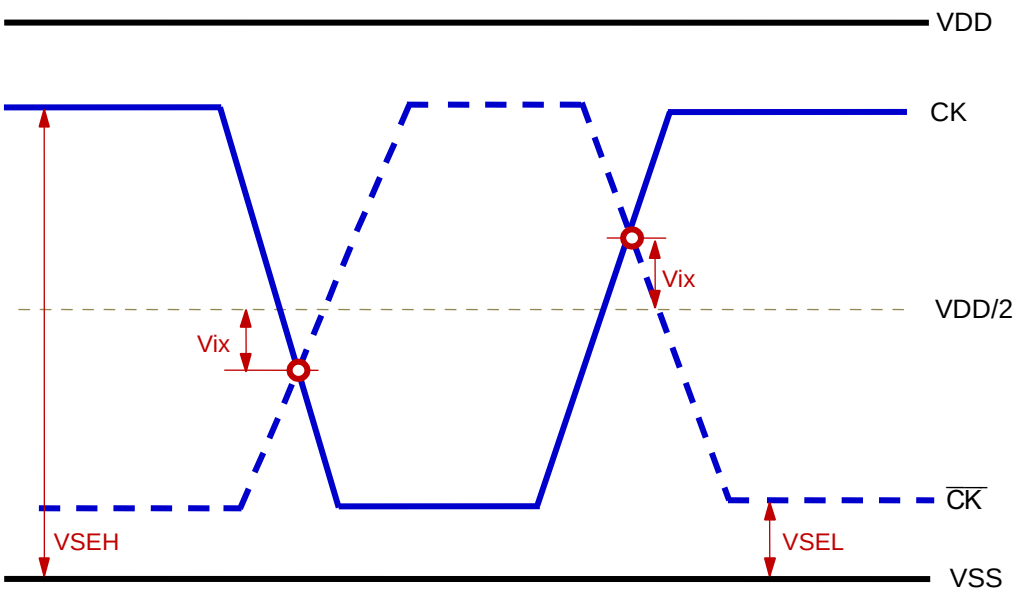
Differential Input Slew Rate Definition for CK, $\overline{CK}$



CK Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signal CK, $\overline{CK}$ must meet the requirements shown below. The differential input cross point voltage $V_{IX(CK)}$ is measured from the actual cross point of true and complement signals to the midlevel between V_{DD} and V_{SS}.

VIX(CK) Definition



Cross Point Voltage For CK Differential Input Signals

Symbol	Parameter	DDR4-2133			
		Min		Max	
–	Area of VSEH, VSEL	VSEL≦ VDD/2 - 145 mV	VDD/2 - 145 mV ≦VSEL≦ VDD/2 - 100 mV	VDD/2 + 100 mV ≦VSEH≦ VDD/2 + 145 mV	VDD/2 + 145 mV ≦VSEH
$V_{IX(CK)}$	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{CK}$	-120 mV	- (VDD/2 - VSEL) + 25 mV	(VSEH - VDD/2) - 25 mV	120 mV

NOTE 1 Extended range for VIX(CK) is only allowed if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL/VSEH of at least VDD/2 ±250mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 4V/ns.

NOTE 2 The relation between Vix(CK) Min/Max and VSEL/VSEH should satisfy following:

(VDD/2) + VIX(CK) Min) - VSEL ≥ 25mV

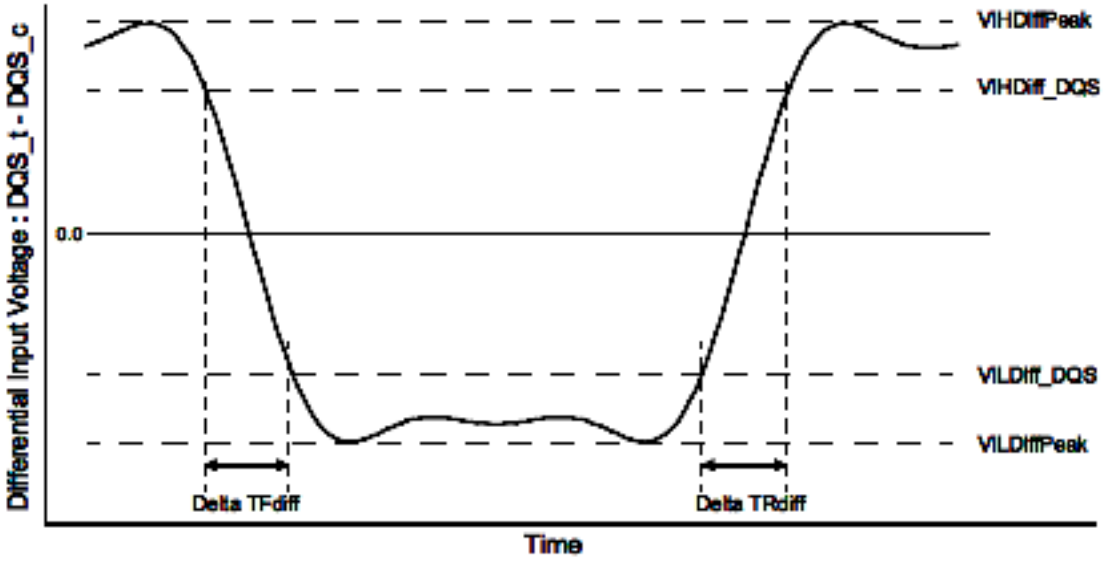
VSEH - ((VDD/2) + IX(CK) Max) ≥ 25mV

Slew Rate Definitions for DQS Differential Input Signals

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge(DQS - $\overline{DQS}$)	VIL_{Diff_DQS}	VIH_{Diff_DQS}	$\lvert VIL_{Diff\_DQS} - VIH_{Diff\_DQS}\rvert$ / ΔTRdiff
Differential input slew rate for falling edge(DQS - $\overline{DQS}$)	VIH_{Diff_DQS}	VIL_{Diff_DQS}	$\lvert VIL_{Diff\_DQS} - VIH_{Diff\_DQS}\rvert$ / ΔTFdiff

NOTE 1 The differential signal DQS - $\overline{DQS}$ must be monotonic between these thresholds.

Differential Input Slew Rate and Input Level Definition for DQS - $\overline{DQS}$



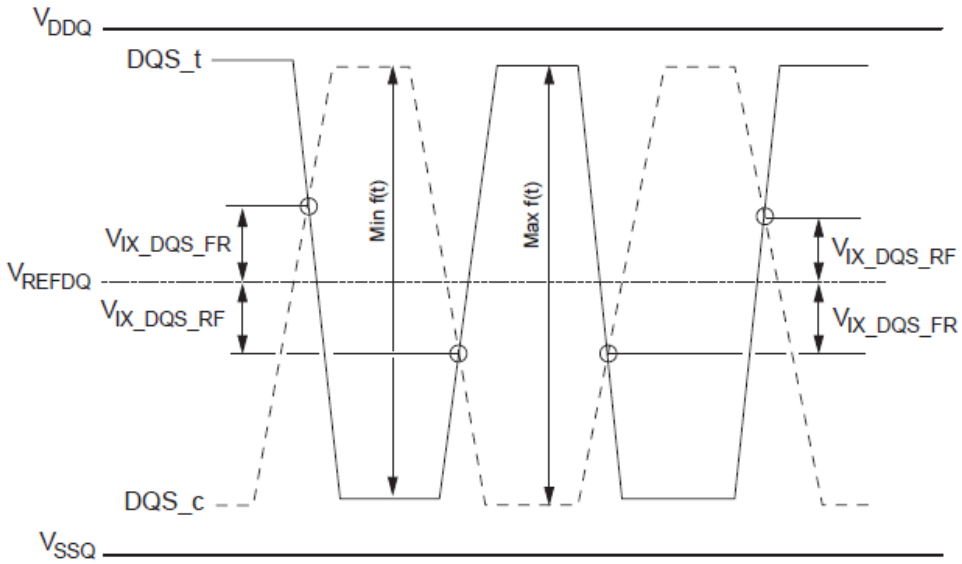
Differential Input Slew Rate and Input Levels for DQS - $\overline{DQS}$

Symbol	Parameter	DDR4-2133		DDR4-2400		DDR4-2666/3200		Unit
		Min	Max	Min	Max	Min	Max	
VIH_{Diff_DQS}	Differntial Input High	136	–	TBD	TBD	TBD	TBD	mV
VIL_{Diff_DQS}	Differntial Input Low	–	–136	TBD	TBD	TBD	TBD	mV
$VIH_{DiffPeak}$	VIH.DIFF.Peak Voltage	186	NOTE 2	TBD	TBD	TBD	TBD	mV
$VIL_{DiffPeak}$	VIL.DIFF.Peak Voltage	NOTE 2	–186	TBD	TBD	TBD	TBD	mV
SR_{Idiff}	Differential Intput Slew Rate	TBD	18	TBD	TBD	TBD	TBD	V/ns

DQS Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signal DQS, $\overline{DQS}$ must meet the requirements shown below. The differential input cross point voltage $V_{IX(DQS)}$ is measured from the actual cross point of true and complement signals to the midlevel between V_{DD} and V_{SS}.

VIX(DQS) Definition



Cross Point Voltage For Differential Input Signals DQS

Symbol	Parameter	DDR4-2133		DDR4-2400		DDR4-2666/3200		Unit	NOTE
		Min.	Max.	Min.	Max.	Min.	Max.		
Vix_DQS_ratio	DQS Differential input crosspoint voltage ratio	–	25	–	25	TBD	TBD	%	1,2,3

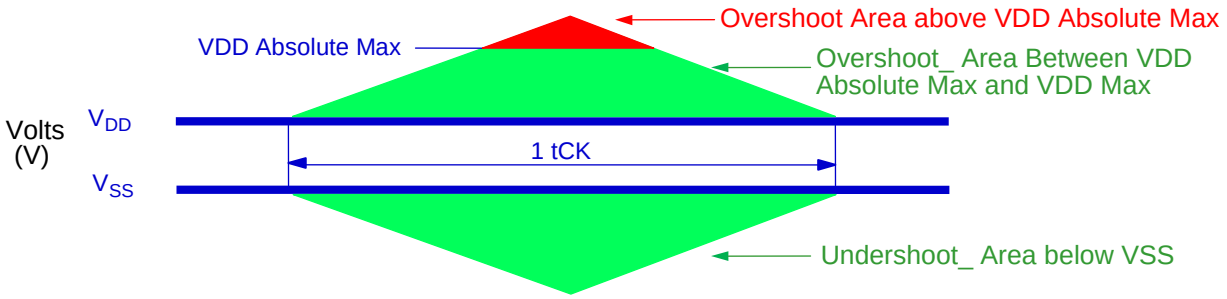
NOTE 1 The base level of Vix_DQS_FR/RF is VREFDQ that is the internal setting value that was determined by VREF Training.
NOTE 2 MIN(f(t)) = VIL_DIFF_Peak.
NOTE 3 MAX(f(t))= VIH_DIFF_Peak.
NOTE 4 Vix_DQS_FR = MIN(f(t)) x VIX_DQS_ratio.
NOTE 5 Vix_DQS_RF = MAX(f(t)) x VIX_DQS_ratio.

Overshoot and Undershoot Specifications

Address, Command, and Control Overshoot and Undershoot Specifications

Parameter	Specification				Unit
	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	
Address and control pins (A0-A13,A17,BG[1:0],BA[1:0],$\overline{ACT}$,$\overline{RAS}$/A16,$\overline{CAS}$/A15,$\overline{WE}$/A14,$\overline{CS}$,CKE,ODT)					
Maximum peak amplitude above VDD Absolute Max allowed for overshoot area	0.06	0.06	TBD	TBD	V
Delta value between VDD Absolute Max and VDD Max allowed for overshoot area	0.24	0.24	TBD	TBD	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	TBD	TBD	V/ns
Maximum overshoot area per 1tCK Above Absolute Max	0.0062	0.0055	TBD	TBD	V/ns
Maximum overshoot area per 1tCK Between Absolute Max and VDD Max	0.1914	0.1699	TBD	TBD	V/ns
Maximum undershoot area per 1tCK Below VSS	0.1984	0.1762	TBD	TBD	V/ns

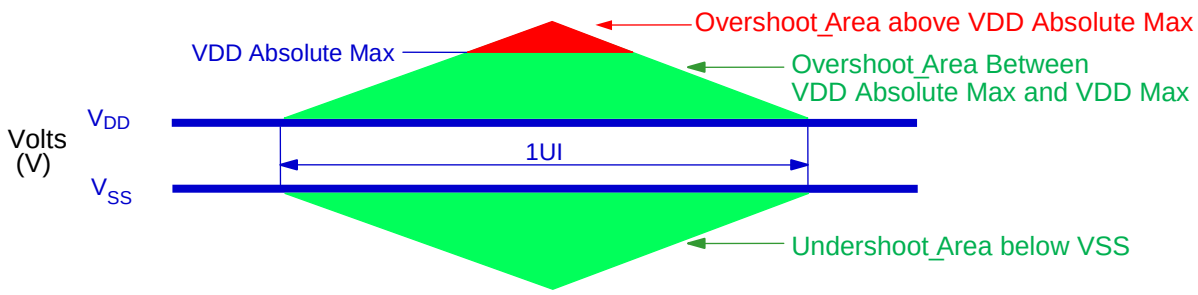
ADDR, CMD, CNTL Overshoot and Undershoot Definition



Clock Overshoot and Undershoot Specifications

Parameter	Specification				Unit
	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	
Clock (CK, $\overline{CK}$)					
Maximum peak amplitude above VDD Absolute Max allowed for overshoot area	0.06	0.06	TBD	TBD	V
Delta value between VDD Absolute Max and VDD Max allowed for overshoot area	0.24	0.24	TBD	TBD	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	TBD	TBD	V/ns
Maximum overshoot area per 1UI Above Absolute Max	0.0028	0.0025	TBD	TBD	V/ns
Maximum overshoot area per 1UI Between Absolute Max and VDD Max	0.0844	0.0750	TBD	TBD	V/ns
Maximum undershoot area per 1UI Below VSS	0.0858	0.0762	TBD	TBD	V/ns

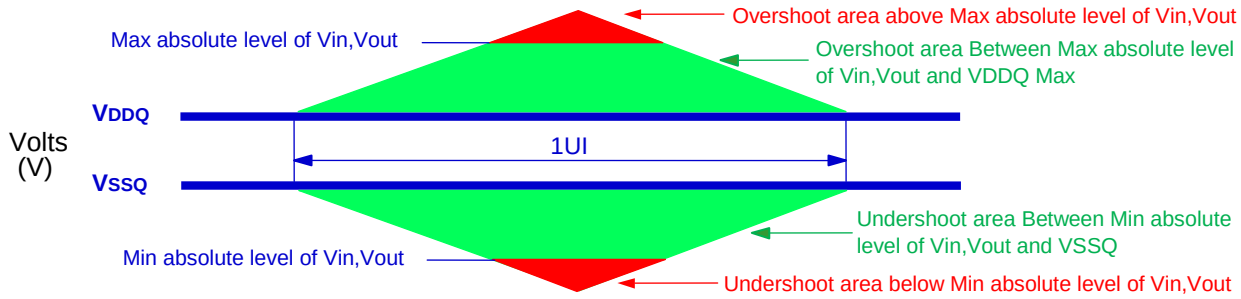
CK Overshoot and Undershoot Definition



Data, Strobe, and Mask Overshoot and Undershoot Specifications

Parameter	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	Unit
Data, Strobe and Mask (DQ, DQS, $\overline{DQS}$, $\overline{DM}$, $\overline{DBI}$, TDQS, $\overline{TDQS}$)					
Maximum peak amplitude above Max absolute level of Vin,Vout	0.16	0.16	TBD	TBD	V
Overshoot area Between Max Absolute level of Vin,Vout and VDDQ Max	0.24	0.24	TBD	TBD	V
Undershoot area Between Min absolute level of Vin,Vout and VSSQ	0.30	0.30	TBD	TBD	V
Maximum peak amplitude below Min absolute level of Vin,Vout	0.10	0.10	TBD	TBD	V
Maximum overshoot area per 1UI Above Max absolute level of Vin,Vout	0.0113	0.0100	TBD	TBD	V/ns
Maximum overshoot area per 1UI Between Max absolute level of Vin,Vout and VDDQ Max	0.0788	0.0700	TBD	TBD	V/ns
Maximum undershoot area per 1UI Between Min absolute level of Vin,Vout and VSSQ	0.0788	0.0700	TBD	TBD	V/ns
Maximum undershoot area per 1UI Below Min absolute level of Vin,Vout	0.0113	0.0100	TBD	TBD	V/ns

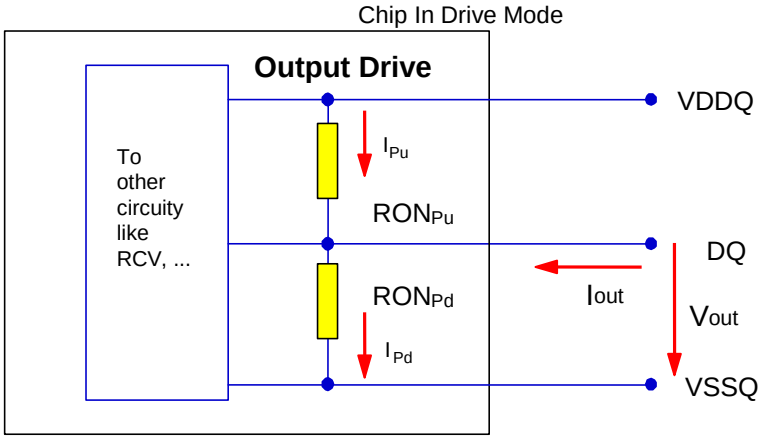
Data, Strobe, and Mask Overshoot and Undershoot Definition



AC and DC Output Measuremnt Levels

Output Driver DC Electrical Characteristics

The DDR4 driver supports two Ron values. These Ron values are referred as strong mode (low Ron - 34Ω) and weak mode (high Ron - 48Ω). A functional representation of the output buffer is shown in the figure below.



The output driver impedance, *RON,* is determined by the value of the external reference resistor RZQ as follows: RON(34) = RZQ/7, or RON(48) = RZQ/5 . This provides either a nominal 34.3Ω ±10% or 48Ω ±10% with nominal RZQ = 240 Ω

$$RON_{Pu} = \frac{VDDQ - Vout}{|\ Iout\ |}$$ under the condition that RON_{Pd} is off

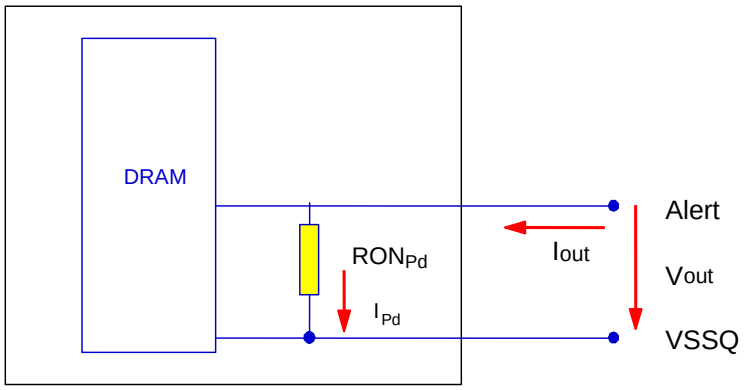
$$RON_{Pd} = \frac{Vout}{|\ Iout\ |}$$ under the condition that RON_{Pu} is off

$\overline{\text{ALERT}}$ Output Drive Characteristic

Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\ Iout\ |}$$ under the condition that RON_{Pu} is off

Alert Driver

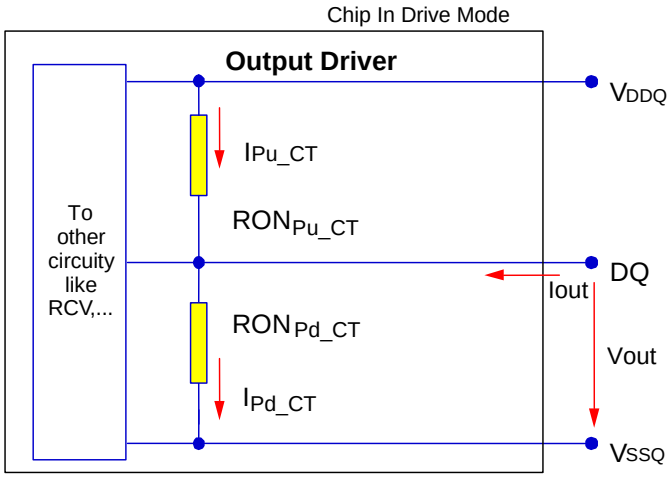


Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied Test Output Pin during Connectivity Test (CT) Mode.

The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ} - V_{OUT}}{|Iout|} \qquad RON_{Pd\_C} = \frac{V_{OUT}}{|Iout|}$$



Single-Ended AC & DC Output Levels

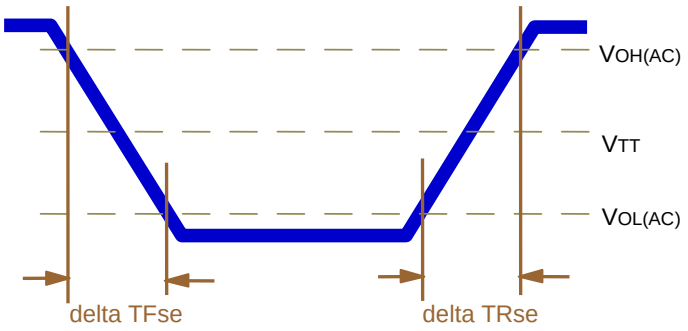
Symbol	Parameter		DDR4-2133/2400/2666/3200	Units	NOTE
$VOH_{(DC)}$	DC output high measurement level	For IV curve linearity	1.1 x VDDQ	V	
$VOM_{(DC)}$	DC output mid measurement level		0.8 x VDDQ	V	
$VOL_{(DC)}$	DC output low measurement level		0.5 x VDDQ	V	
$VOH_{(AC)}$	AC output high measurement level	For output SR	(0.7 + 0.15) x VDDQ	V	1
$VOL_{(AC)}$	AC output low measurement level		(0.7 - 0.15) x VDDQ	V	1

NOTE 1 The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of 50Ω to VTT = VDDQ.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals.

Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single ended output slew rate for rising edge	$VOL_{(AC)}$	$VOH_{(AC)}$	$[VOH_{(AC)}-VOL_{(AC)}] / \Delta TRse$
Single ended output slew rate for falling edge	$VOH_{(AC)}$	$VOL_{(AC)}$	$[VOH_{(AC)}-VOL_{(AC)}] / \Delta TFse$



Single-Ended Output Slew Rate

Symbol	Parameter	DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SRQse	Single ended output slew rate	4	9	4	9	TBD	TBD	TBD	TBD	V/ns

For RON = RZQ/7

NOTE 1 SR = slew rate; Q = query output; se = single-ended signals

NOTE 2 In two cases a maximum slew rate of 12V/ns applies for a single DQ signal within a byte lane.

- Case 1 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from high-to-low or low-to-high) while all remaining DQ signals in the same byte lane are static (they stay at either high or low).
- Case 2 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies.

Differential Outputs

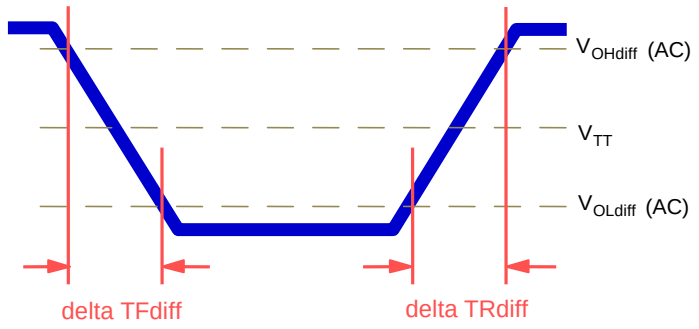
Symbol	Parameter	DDR4-2133/2400/2666/3200	Units
$VOH_{diff(AC)}$	AC differential output high measurement level (for output SR)	+0.3 x VDDQ	V
$VOL_{diff(AC)}$	AC differential output low measurement level (for output SR)	-0.3 x VDDQ	V

NOTE 1 The swing of ± 0.3 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of 50Ω to VTT = VDDQ at each differential output.

NOTE 2 Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL,diff(AC) and VOH,diff(AC) for differential signals.

Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	$VOL_{diff(AC)}$	$VOH_{diff(AC)}$	$[VOH_{,diff(AC)}-VOL_{,diff(AC)}] / \Delta TRdiff$
Differential output slew rate for falling edge	$VOH_{diff(AC)}$	$VOL_{diff(AC)}$	$[VOH_{,diff(AC)}-VOL_{,diff(AC)}] / \Delta TFdiff$



Differential Output Slew Rate

For RON = RZQ/7

Symbol	Parameter	DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SRQdiff	Differential output slew rate	8	18	8	18	TBD	TBD	TBD	TBD	V/ns

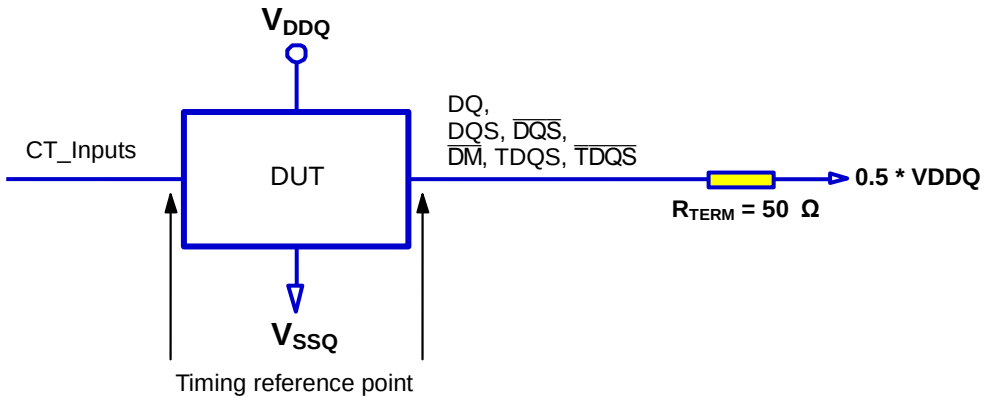
NOTE 1 SR = slew rate; Q = query output; se = single-ended signals

Connectivity Test Mode Output Levels

Symbol	Parameter		DDR4-2133/2400/2666/3200	Units	NOTE
$VOH_{(DC)}$	DC output high measurement level	For IV curve linearity	1.1 x VDDQ	V	
$VOM_{(DC)}$	DC output mid measurement level		0.8 x VDDQ	V	
$VOL_{(DC)}$	DC output low measurement level		0.5 x VDDQ	V	
$VOB_{(DC)}$	DC output below measurement level		0.2 x VDDQ	V	
$VOH_{(AC)}$	AC output high measurement level	For output SR	VTT + (0.1 x VDDQ)	V	1
$VOL_{(AC)}$	AC output below measurement level		VTT - (0.1 x VDDQ)	V	1

NOTE 1 Driver impedance of RZQ/7 and an effective test load of 50Ω to VTT = VDDQ.

Test Load for Connectivity Test Mode Timing



Symbol	Parameter	DDR4-2133/ 2400/2666/3200		Unit
		Min	Max	
TF_{output_CT}	Output signal Falling time	–	10	ns/V
TR_{output_CT}	Output signal Rising time	–	10	ns/V

Speed Bin

DDR4-2133 Speed Bins and Operating Conditions

Speed Bin				DDR4-2133P		DDR4-2133R		Unit	Notes
CL-nRCD-nRP				15-15-15		16-16-16			
Parameter			Symbol	Min	Max	Min	Max		
Internal read command to first data			tAA	14.06[14] (13.50)[5,12]	18.00	15.00	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) +3nCK	tAA(min) + 3nCK	tAA(max) +3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.06 (13.50)[5,12]	–	15.00	–	ns	12
PRE command period			tRP	14.06 (13.50)[5,12]	–	15.00	–	ns	12
ACT to PRE command period			tRAS	33	9 x tREFI	33	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	47.06 (46.50)[5,12]	–	48.00	–	ns	12
	Normal	Read DBI							
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5 (Optional)[5,12]	1.6	Reserved		ns	1,2,3,4,11,14
	CL = 10	CL = 12	tCK(AVG)	Reserved		1.5	1.6	ns	1,2,3,11
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	Reserved		ns	1,2,3,4,7
				(Optional)[5,12]				ns	1,2,3,7
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	Reserved		ns	1,2,3,4,7
				(Optional)[5,12]					
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.938	<1.071	0.938	<1.071	ns	1,2,3
Supported CL Settings				(9),(11),12,(13),14,15,16		10,12,14,16		nCK	13,14
Supported CL Settings with read DBI				(11),(13),14,(15),16,18,19		12,14,16,19		nCK	
Supported CWL Settings				9,10,11,12,14		9,10,11,12,14		nCK	

DDR4-2400 Speed Bins and Operating Conditions

Speed Bin				DDR4-2400R		DDR4-2400U		Unit	Notes
CL-nRCD-nRP				16-16-16		18-18-18			
Parameter			Symbol	Min	Max	Min	Max		
Internal read command to first data			tAA	13.32	18.00	15.00	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) +3nCK	tAA(min) + 3nCK	tAA(max) +3nCK	ns	12
ACT to internal read or write delay time			tRCD	13.32	–	15.00	–	ns	12
PRE command period			tRP	13.32	–	15.00	–	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	45.32	–	47.00	–	ns	12
	Normal	Read DBI							
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5 (Optional)[5,12]	1.6	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	Reserved		1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	Reserved		ns	1,2,34,8
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	Reserved		ns	1,2,3,4,8
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	Reserved		ns	1,2,3,4,8
	CL = 16	CL = 19	tCK(AVG)	0.938	<1.071	0.938	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.833	<0.938	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.938	0.833	<0.938	ns	1,2,3
Supported CL Settings				(9),11,12,13,14,15,16,18		10,12,14,16,18		nCK	13
Supported CL Settings with read DBI				(11),13,14,15,16,18,19,21		12,14,16,19,21		nCK	
Supported CWL Settings				9,10,11,12,14,16		9,10,11,12,14,16		nCK	

Speed Bin Table Note

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

NOTE 1 The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

NOTE 2 tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.

NOTE 3 tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.

NOTE 4 'Reserved' settings are not allowed. User must program a different value.

NOTE 5 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.

NOTE 6 Reserved for DDR4-1866 speed bin.

NOTE 7 Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 8 Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 9 Reserved for DDR4-2666 speed bin.

NOTE 10 Reserved for DDR4-3200 speed bin.

NOTE 11 Reserved for DDR4-1600 speed bin.

NOTE 12 Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.

NOTE 13 CL number in parentheses, it means that these numbers are optional.

NOTE 14 DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).

Input / Output Capacitance

Silicon pad I/O Capacitance

Symbol	Parameter	DDR4-2133		DDR4-2400/2666		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
C_{IO}	Input/output capacitance	0.7	1.4	0.7	1.3	TBD	TBD	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS and $\overline{DQS}$	0	0.05	0	0.05	TBD	TBD	pF	1,2,3,5
C_{CK}	Input capacitance, CK and $\overline{CK}$	0.2	0.8	0.2	0.7	TBD	TBD	pF	1,3
C_{DCK}	Input capacitance delta CK and $\overline{CK}$	0	0.05	0	0.05	TBD	TBD	pF	1,3,4
C_{I}	Input capacitance(CTRL, ADD, CMD pins)	0.2	0.8	0.2	0.7	TBD	TBD	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta(All CTRL pins)	-0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta(All ADD/ CMD pins)	-0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of $\overline{ALERT}$	0.5	1.5	0.5	1.5	TBD	TBD	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	0.5	2.3	0.5	2.3	TBD	TBD	pF	1,3,12
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	TBD	TBD	pF	1,3,13

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure TBD.

NOTE 2 DQ, $\overline{DM}$, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$. Although the DM, TDQS and $\overline{TDQS}$ pins have different functions, the loading matches DQ and DQS.

NOTE 3 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.

NOTE 4 Absolute value CK - $\overline{CK}$.

NOTE 5 Absolute value of CIO(DQS)-CIO($\overline{DQS}$) .

NOTE 6 CI applies to ODT, $\overline{CS}$, CKE, A0-A17, BA0-BA1, BG0-BG1, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, $\overline{ACT}$ and PAR.

NOTE 7 CDI CTRL applies to ODT, $\overline{CS}$ and CKE.

NOTE 8 CDI_CTRL = CI(CTRL)-0.5*(CI(CK)+CI($\overline{CK}$))

NOTE 9 CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CK)+CI($\overline{CK}$)) .

NOTE 10 CDI_ADD_ CMD applies to, A0-A17, BA0-BA1, BG0-BG1,$\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, $\overline{ACT}$ and PAR.

NOTE 11 CDIO = CIO(DQ,$\overline{DM}$)-0.5*(CIO(DQS)+CIO($\overline{DQS}$)) .

NOTE 12 Maximum external load capacitance on ZQ pin: TBD pF.

NOTE 13 TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

DRAM package electrical specifications

Symbol	Parameter	DDR4-2133/2400		DDR4-2666/3200		Unit	Notes
		Min	Max	Min	Max		
Z_{IO}	Input/output Zpkg	45	85	TBD	TBD	Ω	1,2,4,5,10,11
T_{dIO}	Input/output Pkg Delay	14	42	TBD	TBD	ps	1,3,4,5,11
L_{io}	Input/Output Lpkg	-	3.3	TBD	TBD	nH	11, 12
C_{io}	Input/Output Cpkg	-	0.78	TBD	TBD	pF	11, 13
Z_{IO} DQS	DQS, $\overline{DQS}$ Zpkg	45	85	TBD	TBD	Ω	1,2,5,10,11
T_{dIO} DQS	DQS, $\overline{DQS}$ Pkg Delay	14	42	TBD	TBD	ps	1,3,5,10,11
L_{io} DQS	DQS Lpkg	-	3.3	TBD	TBD	nH	11, 12
C_{io} DQS	DQS Cpkg	-	0.78	TBD	TBD	pF	11, 13
DZ_{DIO} DQ	Delta Zpkg DQS, $\overline{DQS}$	-	10	TBD	TBD	Ω	1,2,5,7,10
DT_{dDIO} DQS	Delta Delay DQS, $\overline{DQS}$	-	5	TBD	TBD	ps	1,3,5,7,10
Z_I CTRL	Input- CTRL pins Zpkg	50	90	TBD	TBD	Ω	1,2,5,9,10,11
T_{dI}_CTRL	Input- CTRL pins Pkg Delay	14	42	TBD	TBD	ps	1,3,5,9,10,11
L_i CTRL	Input CTRL Lpkg	-	3.4	TBD	TBD	nH	11, 12
C_i CTRL	Input CTRL Cpkg	-	0.7	TBD	TBD	pF	11, 13
Z_{IADD} CMD	Input- CMD ADD pins Zpkg	50	90	TBD	TBD	Ω	1,2,5,8,10,11
T_{dIADD} CMD	Input- CMD ADD pins Pkg Delay	14	45	TBD	TBD	ps	1,3,5,8,10,11
L_i ADD CMD	Input CMD ADD Lpkg	-	3.6	TBD	TBD	nH	11, 12
C_i ADD CMD	Input CMD ADD Cpkg	-	0.74	TBD	TBD	pF	11, 13
Z_{CK}	CK, $\overline{CK}$ Zpkg	50	90	TBD	TBD	Ω	1,2,5,10,11
T_{dCK}	CK, $\overline{CK}$ Pkg Delay	14	42	TBD	TBD	ps	1,3,5,10,11
L_i CLK	Input CLK Lpkg	-	3.4	TBD	TBD	nH	11, 12
C_i CLK	Input CLK Cpk	-	0.7	TBD	TBD	pF	11, 13
DZ_{DCK}	Delta Zpkg CK, $\overline{CK}$	-	10	TBD	TBD	Ω	1,2,5,6,10
DT_{dCK}	Delta Delay CK, $\overline{CK}$	-	5	TBD	TBD	ps	1,3,5,6,10
Z_O ZQ	ZQ Zpkg	40	100	TBD	TBD	Ω	1,2,5,10,11
T_{dO} ZQ	ZQ Delay	20	90	TBD	TBD	ps	1,3,5,10,11
Z_O ALERT	ALERT Zpkg	40	100	TBD	TBD	Ω	1,2,5,10,11
T_{dO} ALERT	ALERT Delay	20	55	TBD	TBD	ps	1,3,5,10,11

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The package parasitic(L & C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, VSSQ shorted with all other signal pins floating. The inductance is measured with VDD, VDDQ, VSS and VSSQ shorted and all other signal pins shorted at the die side(not pin). Measurement procedure TBD.

NOTE 2 Package only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where:

Zpkg (total per pin) = $\sqrt{Lpkg / Cpkg}$

NOTE 3 Package only delay(Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where:

Tdpkg (total per pin) =$\sqrt{Lpkg \times Cpkg}$

NOTE 4 Z & Td IO applies to DQ, $\overline{DM}$, DQS, $\overline{DQS}$, TDQS and $\overline{TDQS}$.

NOTE 5 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.

NOTE 6 Absolute value of ZCK-Z$\overline{CK}$ for impedance(Z) or absolute value of TdCK-Td$\overline{CK}$ for delay(Td).

NOTE 7 Absolute value of ZIO(DQS)-ZIO($\overline{DQS}$) for impedance(Z) or absolute value of TdIO(DQS)-TdIO($\overline{DQS}$) for delay(Td) .

NOTE 8 ZI & Td ADD CMD applies to A0-A13,A17, $\overline{ACT}$ BA0-BA1, BG0-BG1, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and $\overline{PAR}$.

NOTE 9 ZI & Td CTRL applies to ODT, $\overline{CS}$ and CKE.

NOTE 10 This table applies to monolithic X4 and X8 devices.

NOTE 11 Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.

NOTE 12 It is assumed that Lpkg can be approximated as Lpkg = Zo x Td.

NOTE 13 It is assumed that Cpkg can be approximated as Cpkg = Td / Zo.

IDD and IDDQ Specification Parameters and Test conditions

I_{DD}, I_{PP} and I_{DDQ} Measurement Conditions

In this chapter, I_{DD}, I_{PP} and I_{DDQ} measurement conditions such as test load and patterns are defined and setup and test load for I_{DD}, I_{PP} and I_{DDQ} measurements are also described here.

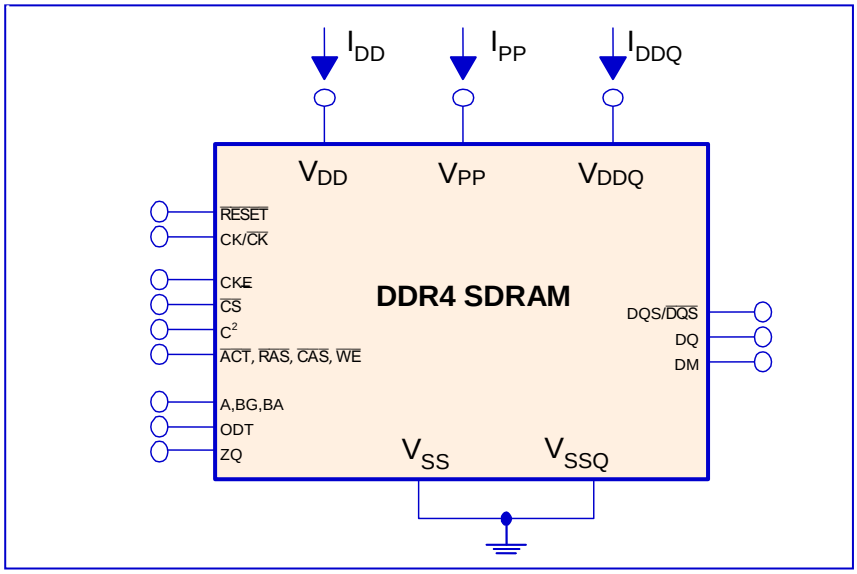
- I_{DD} currents (such as I_{DD0}, I_{DD0A}, $I_{DD}1$, I_{DD1A}, I_{DD2N}, I_{DD2NA}, I_{DD2NL}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3NA}, I_{DD3P}, I_{DD4R}, I_{DD4RA}, I_{DD4W}, I_{DD4WA}, I_{DD5B}, I_{DD5F2}, I_{DD5F4}, I_{DD6N}, I_{DD6E}, I_{DD6R}, I_{DD6A}, I_{DD7} and I_{DD8}) are measured as time-averaged currents with all V_{DD} balls of the DDR4 SDRAM under test tied together. Any I_{PP} or I_{DDQ} current is not included in I_{DD} currents.
- I_{PP} currents have the same definition as I_{DD} except that the current on the V_{PP} supply is measured.
- I_{DDQ} currents (such as I_{DDQ2NT} and I_{DDQ4R}) are measured as time-averaged currents with all V_{DDQ} balls of the DDR4 SDRAM under test tied together. Any I_{DD} current is not included in I_{DDQ} currents.

  Attention: I_{DDQ} values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power. In DRAM module application, I_{DDQ} cannot be measured separately since V_{DD} and V_{DDQ} are using one merged-power layer in Module PCB.

For I_{DD}, I_{PP} and I_{DDQ} measurements, the following definitions apply:

- "0" and "LOW" is defined as $V_{IN} <= V_{ILAC(max)}$.
- "1" and "HIGH" is defined as $V_{IN} >= V_{IHAC(min)}$.
- "MID-LEVEL" is defined as inputs are $V_{REF} = V_{DD} / 2$.
- Timings used for I_{DD}, I_{PP} and I_{DDQ} Measurement-Loop Patterns are described.
- Basic I_{DD}, I_{PP} and I_{DDQ} Measurement Conditions are described.
- Detailed I_{DD}, I_{PP} and I_{DDQ} Measurement-Loop Patterns are described.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
  - $R_{ON} = R_{ZQ}/7$ (34 Ω in MR1);
  - $R_{TT\_NOM} = R_{ZQ/6}$ (40 Ω in MR1);
  - $R_{TT\_WR} = R_{ZQ/2}$ (120 Ω in MR2);
  - R_{TT_PARK} = Disable;
  - Qoff = 0B (Output Buffer enabled) in MR1;
  - TDQS disabled in MR1;
  - CRC disabled in MR2;
  - CA parity feature disabled in MR5;
  - Gear down mode disabled in MR3;
  - Read/Write DBI disabled in MR5;
  - DM disabled in MR5
- Attention: The I_{DD}, I_{PP} and I_{DDQ} Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {$\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$} := {HIGH, LOW, LOW, LOW, LOW}
- Define D# = {$\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$} := {HIGH, HIGH, HIGH, HIGH, HIGH}

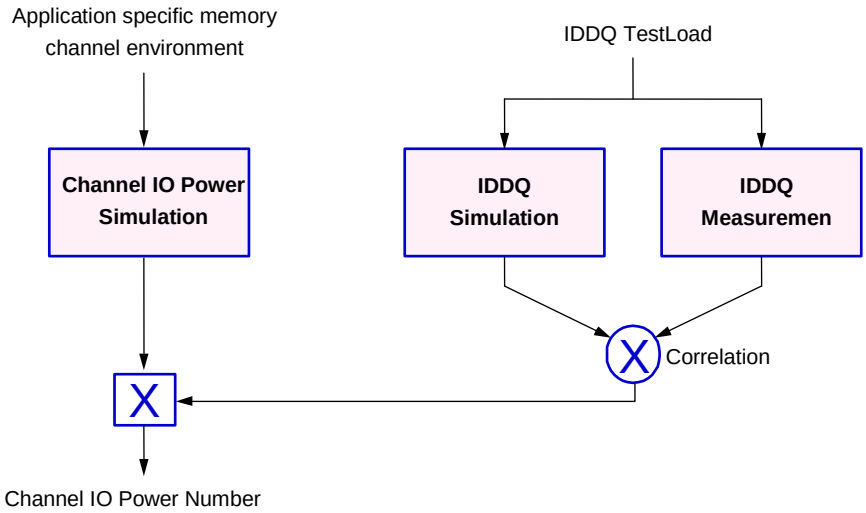
Measurement Setup and Test Load for I_{DDx}, I_{DDPx} and I_{DDQx}



NOTE 1 DIMM level Output test load condition may be different from above.

NOTE 2 For information only.

Correlation: Simulated Channel I/O Power to Actual Channel I/O Power



Timings used for I_{DD}, I_{PP} and I_{DDQ} Measurement-Loop Patterns

Symbol		DDR4-2133		DDR4-2400		Unit
		15-15-15	16-16-16	16-16-16	18-18-18	
tCK		0.938		0.833		ns
CL		15	16	16	18	nCK
CWL		14	14	16	16	nCK
nRCD		15	16	16	18	nCK
nRC		51	52	55	57	nCK
nRAS		36		39		nCK
nRP		15	16	16	18	nCK
nFAW	x4	16		16		nCK
	x8	23		26		nCK
	x16	32		36		nCK
nRRDS	x4	4		4		nCK
	x8	4		4		nCK
	x16	6		7		nCK
nRRDL	x4	6		6		nCK
	x8	6		6		nCK
	x16	7		8		nCK
tCCD_S		4		4		nCK
tCCD_L		6		6		nCK
tWTR_S		3		3		nCK
tWTR_L		8		9		nCK
nRFC 4Gb		278		313		nCK

NOTE IDD spec is defined for 1.2V part herein and it's TBD for 1.35V part.

Basic IDD, IPP, and IDDQ Measurement Conditions

Symbol	Description
I_{DD0}	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD loop table; **Data IO:** VDDQ; **$\overline{DM}$:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD loop table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD loop table;
I_{DD0A}	**Operating One Bank Active-Precharge Current (AL=CL-1)** **AL = CL-1,** **Other conditions:** see IDD0
I_{PP0}	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0**
I_{DD1}	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling according to IDD loop table; **$\overline{DM}$:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD loop table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD loop table;
I_{DD1A}	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** **AL = CL-1,** **Other conditions:** see IDD1
I_{PP1}	**Operating One Bank Active-Read-Precharge IPP Current** **Same condition with IDD1**
I_{DD2N}	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD loop table; **Data IO:** VDDQ; **$\overline{DM}$:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD loop table;

Symbol	Description
I_{DD2NA}	**Precharge Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD2N
I_{PP2N}	**Precharge Standby IPP Current** **Same condition with IDD2N**
I_{DD2NT}	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD loop table; **Data IO: VSSQ**; $\overline{DM}$**:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according to IDD loop table; **Pattern Details:** see IDD loop table;
I_{DDQ2NT} **(Optional)**	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
I_{DD2NL}	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled[3]
I_{DD2NG}	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled[3,5]
I_{DD2ND}	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled[3]
I_{DD2N_par}	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled[3]
I_{DD2P}	**Precharge Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; $\overline{DM}$**:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
I_{PP2P}	**Precharge Power-Down IPP Current** **Same condition with IDD2P**
I_{DD2Q}	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; $\overline{DM}$**:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0

Symbol	Description
I_{DD3N}	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD loop table; **Data IO:** VDDQ; $\overline{DM}$**:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD loop table;
I_{DD3NA}	**Active Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD3N
I_{PP3N}	**Active Standby IPP Current** **Same condition with IDD3N**
I_{DD3P}	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; $\overline{DM}$**:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers2; **ODT Signal:** stable at 0
I_{PP3P}	**Active Power-Down IPP Current** **Same condition with IDD3P**
I_{DD4R}	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: see IDD timing Table; **BL:** 8[2]; **AL:** 0; $\overline{CS}$: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD loop table; **Data IO:** seamless read data burst with different data between one burst and the next one according to IDD loop table; $\overline{DM}$: stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see IDD loop table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD loop table;
I_{DD4RA}	**Operating Burst Read Current (AL=CL-1)** **AL = CL-1,** **Other conditions:** see IDD4R
I_{DD4RB}	**Operating Burst Read Current with Read DBI** **Read DBI enabled[3],** **Other conditions:** see IDD4R
I_{PP4R}	**Operating Burst Read IPP Current** **Same condition with IDD4R**

Symbol	Description
I_{DDQ4R} (Optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
I_{DDQ4RB} (Optional)	**Operating Burst Read IDDQ Current with Read DBI** Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
I_{DD4W}	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD loop table; **Data IO:** seamless write data burst with different data between one burst and the next one according to IDD loop table; $\overline{DM}$**:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see IDD loop table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** see IDD loop table;
I_{DD4WA}	**Operating Burst Write Current (AL=CL-1)** **AL = CL-1,** **Other conditions:** see IDD4W
I_{DD4WB}	**Operating Burst Write Current with Write DBI** **Write DBI enabled[3],** **Other conditions:** see IDD4W
I_{DD4WC}	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3],** **Other conditions:** see IDD4W
I_{DD4W_par}	**Operating Burst Write Current with CA Parity** **CA Parity enabled[3],** **Other conditions:** see IDD4W
I_{PP4W}	**Operating Burst Write IPP Current** **Same condition with IDD4W**
I_{DD5B}	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD loop table; **Data IO:** VDDQ; $\overline{DM}$**:** stable at 1; **Bank Activity:** REF command every nRFC (see IDD loop table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD loop table;
I_{PP5B}	**Burst Refresh Write IPP Current (1X REF)** **Same condition with IDD5B**
I_{DD5F2}	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions:** see IDD5B
I_{PP5F2}	**Burst Refresh Write IPP Current (2X REF)** **Same condition with IDD5F2**
I_{DD5F4}	**Burst Refresh Current (4X REF)** **tRFC=tRFC_x4, Other conditions:** see IDD5B
I_{PP5F4}	**Burst Refresh Write IPP Current (4X REF)** **Same condition with IDD5F4**

Symbol	Description
I_{DD6N}	**Self Refresh Current: Normal Temperature Range** ***T*CASE:** 0 - 85°C; **Low Power Array Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK and $\overline{CK}$: LOW; **CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **$\overline{DM}$:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6N}	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N**
I_{DD6E}	**Self-Refresh Current: Extended Temperature Range** ***T*CASE:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK and $\overline{CK}$: LOW; **CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **$\overline{DM}$**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6E}	**Self Refresh IPP Current: Extended Temperature Range Same condition with IDD6E**
I_{DD6R}	**Self-Refresh Current: Reduced Temperature Range** ***T*CASE:** 0 - 45°C; **Low Power Array Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK and $\overline{CK}$: LOW; **CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **$\overline{DM}$**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6R}	**Self Refresh IPP Current: Reduced Temperature Range** **Same condition with IDD6R**
I_{DD6A}	**Auto Self-Refresh Current** ***T*CASE:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Auto[4]; **CKE:** Low; **External clock:** Off; CK and $\overline{CK}$: LOW; **CL**: see IDD timing Table; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **$\overline{DM}$**:stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6A}	**Auto Self-Refresh IPP Current** **Same condition with IDD6A**

Symbol	Description
I_{DD7}	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: see IDD timing Table; **BL:** 8[1]; **AL:** CL-1; $\overline{CS}$: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD loop table; **Data IO:** read data bursts with different data between one burst and the next one according to IDD loop table; $\overline{DM}$: stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see IDD loop table; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD loop table;
I_{PP7}	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7**
I_{DD8}	**Maximum Power Down Current**
I_{PP8}	**Maximum Power Down IPP Current** **Same condition with IDD8**

NOTE 1 Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].

NOTE 2 Output Buffer Enable:
- set MR1 [A12 = 0] : Qoff = Output buffer enabled
- set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
RTT_NOM enable:
- set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6
RTT_WR enable:
- set MR2 [A10:9 = 01] : RTT_WR = RZQ/2
RTT_PARK disable:
- set MR5 [A8:6 = 000]

NOTE 3 CAL enabled :
- set MR4 [A8:6 =010] : 2133MT/s
- set MR4 [A8:6 =011] : 2400MT/s
Gear Down mode enabled :
- set MR3 [A3 = 1] : 1/4 Rate
DLL disabled :
- set MR1 [A0 = 0]
CA parity enabled :
- set MR5 [A2:0 = 001] : 2133MT/s
- set MR5 [A2:0 = 010] : 2400MT/s
Read DBI enabled :
- set MR5 [A12 = 1]
Write DBI enabled :
- set :MR5 [A11 = 1]

NOTE 4 Low Power Array Self Refresh (LP ASR) :
- set MR2 [A7:6 = 00] : Normal
- set MR2 [A7:6 = 01] : Reduced Temperature range
- set MR2 [A7:6 = 10] : Extended Temperature range
- set MR2 [A7:6 = 11] : Auto Self Refresh

NOTE 5 IDD2NG should be measured after sync pulse(NOP) input.

I_{DD0}, I_{DD0A} and I_{PP0} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3,4	D_#, D_#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	–
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	**PRE**	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	–
			…	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 1 instead																
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	3*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	5*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	7*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	8*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	10*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	11*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	12*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	13*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	14*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	15*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

NOTE 1 DQS, $\overline{DQS}$ are VDDQ.

NOTE 2 DBG1 is a don't care for x16 devices.

NOTE 3 DQ signals are VDDQ.

NOTE 4 For x4 and x8 only.

I_{DD1}, I_{DD1A} and I_{PP1} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3,4	D_#, D_#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	–
			…	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
			nRCD -AL	**RD**	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
				repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	**PRE**	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	–
			…	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC + 0	**ACT**	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	0	3[b]	3	0	0	0	7	F	0	
			…	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																
			1*nRC + nRCD - AL	**RD**	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			1*nRC + Nras	**PRE**	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	
			…	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	3*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	5*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	7*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	8*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	10*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	11*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	12*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	13*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	14*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	15*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

NOTE 1 DQS, $\overline{DQS}$ are used according to RD Commands, otherwise VDDQ.

NOTE 2 BG1 is don't care for x16 device.

NOTE 3 C[2:0] are used only for 3DS device.

NOTE 4 Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

I_{DD2N}, I_{DD2NA}, I_{DD2NL}, I_{DD2NG}, I_{DD2ND}, I_{DD2N_par}, I_{PP2}, I_{DD3N}, I_{DD3NA} and I_{DD3P} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	–
			3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	–
		1	4-7	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 1 instead															
		2	8-11	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 3 instead															
		4	16-19	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead															
		5	20-23	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 2 instead															
		6	24-27	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead															
		7	28-31	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 0 instead															
		8	32-35	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead															For x4 and x8 only
		9	36-39	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1 instead															
		10	40-43	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead															
		11	44-47	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3 instead															
		12	48-51	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead															
		13	52-55	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead															
		14	56-59	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead															
		15	60-63	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0 instead															

NOTE 1 DQS, $\overline{DQS}$ are VDDQ.

NOTE 2 BG1 is don't care for x16 device.

NOTE 3 C[2:0] are used only for 3DS device.

NOTE 4 DQ signals are VDDQ.

I_{DD2NT} and I_{DDQ2NT} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	–
			3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	–
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 1, BA[1:0] = 1 instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 3, BA[1:0] = 0 instead																

NOTE 1 DQS, $\overline{DQS}$ are VDDQ.

NOTE 2 BG1 is don't care for x16 device

NOTE 3 C[2:0] are used only for 3DS device

NOTE 4 DQ signals are VDDQ.

I_{DD4R}, I_{DD4RA}, I_{DD4RB} and I_{DDQ4R} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**RD**	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2,3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	–
		1	4	**RD**	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			6,7	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	–
		2	8-11	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 0 instead																

NOTE 1 DQS, $\overline{DQS}$ are used according to RD Commands, otherwise VDDQ.

NOTE 2 BG1 is don't care for x16 device

NOTE 3 C[2:0] are used only for 3DS device

NOTE 4 Burst Sequence driven on each DQ signal by Read Command.

I_{DD4W}, I_{DD4WA}, I_{DD4WB} and I_{DD4W_par} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**WR**	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	–
			2,3	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
		1	4	**WR**	0	1	1	0	1	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	–
			6,7	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
		2	8-11	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 0 instead																

NOTE 1 DQS, $\overline{DQS}$ are used according to WR Commands, otherwise VDDQ.

NOTE 2 BG1 is don't care for x16 device

NOTE 3 C[2:0] are used only for 3DS device

NOTE 4 Burst Sequence driven on each DQ signal by Write Command.

I_{DD4WC} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**WR**	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC
			1,2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	–
			3,4	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
			5	**WR**	0	1	1	0	1	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC
			6,7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	–
			8,9	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
		2	10-14	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 2 instead															
		3	15-19	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 3 instead																
		4	20-24	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 1 instead																
		5	25-29	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 2 instead																
		6	30-34	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 3 instead																
		7	35-39	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 0 instead																
		8	40-44	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	45-49	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 1 instead																
		10	50-54	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 2 instead																
		11	55-59	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 3 instead																
		12	60-64	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 1 instead																
		13	65-69	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 2 instead																
		14	70-74	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 3 instead																
		15	70-74	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 0 instead																

NOTE 1 DQS, $\overline{DQS}$ are VDDQ.

NOTE 2 BG1 is don't care for x16 device.

NOTE 3 C[2:0] are used only for 3DS device.

NOTE 4 Burst Sequence driven on each DQ signal by Write Command.

I_{DD5B} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	–
			4	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	–
			4-7	repeat pattern 1...4, use BG[1:0]2 = 1, BA[1:0] = 1 instead																
			8-11	repeat pattern 1...4, use BG[1:0]2 = 0, BA[1:0] = 2 instead																
			12-15	repeat pattern 1...4, use BG[1:0]2 = 1, BA[1:0] = 3 instead																
			16-19	repeat pattern 1...4, use BG[1:0]2 = 0, BA[1:0] = 1 instead																
			20-23	repeat pattern 1...4, use BG[1:0]2 = 1, BA[1:0] = 2 instead																
			24-27	repeat pattern 1...4, use BG[1:0]2 = 0, BA[1:0] = 3 instead																
			28-31	repeat pattern 1...4, use BG[1:0]2 = 1, BA[1:0] = 0 instead																
			32-35	repeat pattern 1...4, use BG[1:0]2 = 2, BA[1:0] = 0 instead																For x4 and x8 only
			36-39	repeat pattern 1...4, use BG[1:0]2 = 3, BA[1:0] = 1 instead																
			40-43	repeat pattern 1...4, use BG[1:0]2 = 2, BA[1:0] = 2 instead																
			44-47	repeat pattern 1...4, use BG[1:0]2 = 3, BA[1:0] = 3 instead																
			48-51	repeat pattern 1...4, use BG[1:0]2 = 2, BA[1:0] = 1 instead																
			52-55	repeat pattern 1...4, use BG[1:0]2 = 3, BA[1:0] = 2 instead																
			56-59	repeat pattern 1...4, use BG[1:0]2 = 2, BA[1:0] = 3 instead																
			60-63	repeat pattern 1...4, use BG[1:0]2 = 3, BA[1:0] = 0 instead																
		2	64 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																

NOTE 1 DQS, $\overline{DQS}$ are VDDQ.

NOTE 2 BG1 is don't care for x16 device.

NOTE 3 C[2:0] are used only for 3DS device.

NOTE 4 DQ signals are VDDQ.

I_{DD7} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	**RDA**	0	1	1	0	1	0		0	0	0	0	1	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	–
			…	repeat pattern 2...3 until nRRD - 1, if nRCD > 4. Truncate if necessary																
		1	nRRD	**ACT**	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	–
			nRRD + 1	**RDA**	0	1	1	0	1	0		1	1	0	0	1	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			…	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRCD > 4. Truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 2 instead																
		3	3*nRRD	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 3 instead																
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 1 instead																
		6	nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 2 instead																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 3 instead																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 0 instead																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																
		10	2*nFAW	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 0 instead																For x4 and x8 only
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 1 instead																
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 2 instead																
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 3 instead																
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																
		15	3*nFAW	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 1 instead																
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 2 instead																
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 3 instead																
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 0 instead																
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																

NOTE 1 DQS, $\overline{DQS}$ are VDDQ.

NOTE 2 BG1 is don't care for x16 device.

NOTE 3 C[2:0] are used only for 3DS device.

NOTE 4 Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

IDD6 Descriptions

Symbol	Temperature Range	NOTE
I_{DD6N}	0 - 85 °C	3,4
I_{DD6E}	0 - 95 °C	4,5,6
I_{DD6R}	0 - 45 °C	4,6,9
I_{DD6A}	0 °C ~ Ta	4,6,7,8
	Tb ~ Ty	4,6,7,8
	Tz ~ TOPERmax	4,6,7,8

NOTE 1 Some IDD currents are higher for x16 organization due to larger page-size architecture.

NOTE 2 Max values for IDD currents considering worst case conditions of process, temperature and voltage.

NOTE 3 Applicable for MR2 settings A6=0 and A7=0.

NOTE 4 Supplier data sheets include a max value for IDD6.

NOTE 5 Applicable for MR2 settings A6=0 and A7=1. IDD6E is only specified for devices which support the Extended Temperature Range feature.

NOTE 6 Refer to the supplier data sheet for the value specification method (e.g. max, typical) for IDD6E and IDD6A

NOTE 7 Applicable for MR2 settings A6=1 and A7=0. IDD6A is only specified for devices which support the Auto Self Refresh feature.

NOTE 8 The number of discrete temperature ranges supported and the associated Ta - Tz values are supplier/design specific. Temperature ranges are specified for all supported values of TOPER. Refer to supplier data sheet for more information.

NOTE 9 Applicable for MR2 settings MR2 [A7:A6 = 01] : Reduced Temperature range. IDD6R is verified by design and characterization, and may not be subject to production test

I_{DD}, I_{DDQ} and I_{PP} Specification

Symbol	Description	DDR4-2133 X16	DDR4-2400 X16	Unit
I_{DD0}	Operating One Bank Active-Precharge Current (AL=0)	95	100	mA
I_{DD0A}	Operating One Bank Active-Precharge Current (AL=CL-1)	100	105	mA
I_{PP0}	Operating One Bank Active-Precharge IPP Current	2.5	2.5	mA
I_{DD1}	Operating One Bank Active-Read-Precharge Current (AL=0)	100	105	mA
I_{DD1A}	Operating One Bank Active-Read-Precharge Current (AL=CL-1)	105	110	mA
I_{PP1}	Operating One Bank Active-Read-Precharge IPP Current	2.5	2.5	mA
I_{DD2N}	Precharge Standby Current (AL=0)	85	85	mA
I_{DD2NA}	Precharge Standby Current (AL=CL-1)	90	90	mA
I_{PP2N}	Precharge Standby IPP Current	2	2	mA
I_{DD2NT}	Precharge Standby ODT Current	120	125	mA
I_{DDQ2NT}	Precharge Standby ODT IDDQ Current	20	25	mA
I_{DD2NL}	Precharge Standby Current with CAL enabled	70	75	mA
I_{DD2NG}	Precharge Standby Current with Gear Down mode enabled	120	125	mA
I_{DD2ND}	Precharge Standby Current with DLL disabled	70	75	mA
I_{DD2N_par}	Precharge Standby Current with CA parity enabled	120	125	mA
I_{DD2P}	Precharge Power-Down Current	60	60	mA
I_{PP2P}	Precharge Power-Down IPP Current	2	2	mA
I_{DD2Q}	Precharge Quiet Standby Current	65	70	mA
I_{DD3N}	Active Standby Current	105	110	mA
I_{DD3NA}	Active Standby Current (AL=CL-1)	110	115	mA
I_{PP3N}	Active Standby IPP Current	2	2	mA
I_{DD3P}	Active Power-Down Current	75	80	mA
I_{PP3P}	Active Power-Down IPP Current	2	2	mA
I_{DD4R}	Operating Burst Read Current	270	280	mA
I_{DD4RA}	Operating Burst Read Current (AL=CL-1)	270	280	mA
I_{DD4RB}	Operating Burst Read Current with Read DBI	270	280	mA
I_{PP4R}	Operating Burst Read IPP Current	2	2	mA
I_{DDQ4R}	Operating Burst Read IDDQ Current	70	80	mA
I_{DDQ4RB}	Operating Burst Read IDDQ Current with Read DBI	70	80	mA
I_{DD4W}	Operating Burst Write Current	310	320	mA
I_{DD4WA}	Operating Burst Write Current (AL=CL-1)	320	330	mA
I_{DD4WB}	Operating Burst Write Current with Write DBI	310	320	mA
I_{DD4WC}	Operating Burst Write Current with Write CRC	300	310	mA

Symbol	Description	DDR4-2133 X16	DDR4-2400 X16	Unit
I_{DD4W_par}	Operating Burst Write Current with CA Parity	330	340	mA
I_{PP4W}	Operating Burst Write IPP Current	2	2	mA
I_{DD5B}	Burst Refresh Current (1X REF)	210	220	mA
I_{PP5B}	Burst Refresh Write IPP Current (1X REF)	30	30	mA
I_{DD5F2}	Burst Refresh Current (2X REF)	200	210	mA
I_{PP5F2}	Burst Refresh Write IPP Current (2X REF)	28	28	mA
I_{DD5F4}	Burst Refresh Current (4X REF)	190	200	mA
I_{PP5F4}	Burst Refresh Write IPP Current (4X REF)	26	26	mA
I_{DD6N}	Self Refresh Current: Normal Temperature Range	30	30	mA
I_{PP6N}	Self Refresh IPP Current: Normal Temperature Range	2.5	2.5	mA
I_{DD6E}	Self-Refresh Current: Extended Temperature Range	28	28	mA
I_{PP6E}	Self Refresh IPP Current: Extended Temperature Range	2	2	mA
I_{DD6R}	Self-Refresh Current: Reduced Temperature Range	25	25	mA
I_{PP6R}	Self Refresh IPP Current: Reduced Temperature Range	2	2	mA
I_{DD6A}	Auto Self-Refresh Current	30	30	mA
I_{PP6A}	Auto Self-Refresh IPP Current	2.5	2.5	mA
I_{DD7}	Operating Bank Interleave Read Current	300	310	mA
I_{PP7}	Operating Bank Interleave Read IPP Current	15	15	mA
I_{DD8}	Maximum Power Down Current	—	—	mA
I_{PP8}	Maximum Power Down IPP Current	—	—	mA

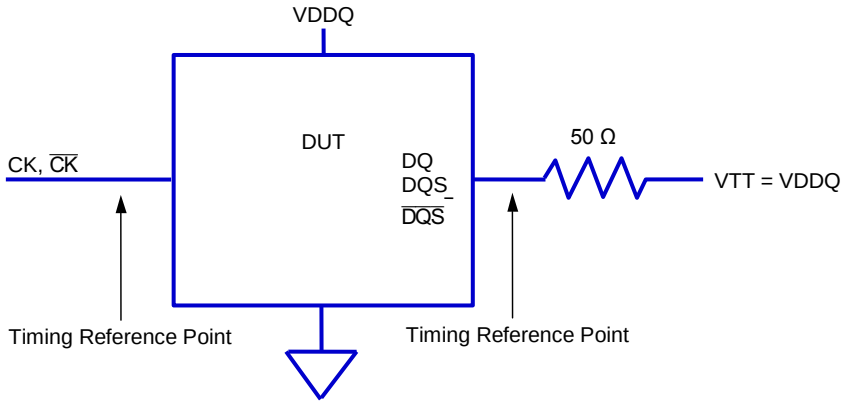
NOTE IDD spec is defined for 1.2V part herein and it's TBD for 1.35V part.

Electrical Characteristics & AC Timing

Reference Load for AC Timing and Output Slew Rate

The effective reference load of 50Ω to V_{TT} = V_{DDQ} and driver impedance of RZQ/7 for each output was used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined.

Parameter	Symbol		2Gb	4Gb	8Gb	16Gb	Units
Average periodic refresh interval	tREFI	0°C≤TCASE ≤85°C	7.8	7.8	7.8	TBD	µs
		85°C≤TCASE ≤95°C	3.9	3.9	3.9	TBD	µs

Timing Parameters by Speed Grade

DDR4-2133

Speed		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	**tCK (DLL_OFF)**	8	–	ns	22
Average Clock Period	**tCK(avg)**	0.938	<1.071	ns	35,36
Average high pulse width	**tCH(avg)**	0.48	0.52	tCK(avg)	
Average low pulse width	**tCL(avg)**	0.48	0.52	tCK(avg)	
Absolute Clock Period	**tCK(abs)**	Min: tCK(avg)min+tJIT(per)min_tot Max: tCK(avg)max+ tJIT(per)max_tot		tCK(avg)	
Absolute clock HIGH pulse width	**tCH(abs)**	0.45	–	tCK(avg)	23
Absolute clock LOW pulse width	**tCL(abs)**	0.45	–	tCK(avg)	23
Clock Period Jitter- total	**JIT(per)_tot**	-47	47	ps	23
Clock Period Jitter- deterministic	**JIT(per)_dj**	-23	23	ps	26
Clock Period Jitter during DLL locking period	**tJIT(per, lck)**	-38	38	ps	
Cycle to Cycle Period Jitter	**tJIT(cc)_total**	94		ps	25
Cycle to Cycle Period Jitter deterministic	**tJIT(cc)_dj**	47		ps	26
Cycle to Cycle Period Jitter during DLL locking period	**tJIT(cc, lck)**	75		ps	
Duty Cycle Jitter	**tJIT(duty)**	TBD	TBD	ps	
Cumulative error across 2 cycles	**tERR(2per)**	-69	69	ps	
Cumulative error across 3 cycles	**tERR(3per)**	-82	82	ps	
Cumulative error across 4 cycles	**tERR(4per)**	-91	91	ps	
Cumulative error across 5 cycles	**tERR(5per)**	-98	98	ps	
Cumulative error across 6 cycles	**tERR(6per)**	-104	104	ps	
Cumulative error across 7 cycles	**tERR(7per)**	-109	109	ps	
Cumulative error across 8 cycles	**tERR(8per)**	-113	113	ps	
Cumulative error across 9 cycles	**tERR(9per)**	-117	117	ps	
Cumulative error across 10 cycles	**tERR(10per)**	-120	120	ps	
Cumulative error across 11 cycles	**tERR(11per)**	-123	123	ps	
Cumulative error across 12 cycles	**tERR(12per)**	-126	126	ps	
Cumulative error across 13 cycles	**tERR(13per)**	-129	129	ps	
Cumulative error across 14 cycles	**tERR(14per)**	-131	131	ps	
Cumulative error across 15 cycles	**tERR(15per)**	-133	133	ps	
Cumulative error across 16 cycles	**tERR(16per)**	-135	135	ps	
Cumulative error across 17 cycles	**tERR(17per)**	-137	137	ps	
Cumulative error across 18 cycles	**tERR(18per)**	-139	139	ps	
Cumulative error across n = 13, 14 . . .49, 50 cycles	**tERR(nper)**	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)		ps	
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	**tIS(base)**	80	–	ps	
Command and Address setup time to CK, $\overline{CK}$ referenced to Vref levels	**tIS(Vref)**	180	–	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to Vih(dc) / Vil(dc) levels	**tIH(base)**	105	–	ps	
Command and Address hold time to CK, $\overline{CK}$ referenced to Vref levels	**tIH(Vref)**	180	–	ps	
Control and Address Input pulse width for each input	**tIPW**	460	–	ps	
Command and Address Timing					
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank group	**tCCD_L**	6	–	nCK	34

Speed		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max		
$\overline{CAS}$ to $\overline{CAS}$ command delay for different bank group	**tCCD_S**	4	–	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	**tRRD_S(2K)**	Max(4nCK,5.3ns)	–	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	**tRRD_S(1K)**	Max(4nCK,3.7ns)	–	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	**tRRD_S(1/2K)**	Max(4nCK,3.7ns)	–	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	**tRRD_L(2K)**	Max(4nCK,6.4ns)	–	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	**tRRD_L(1K)**	Max(4nCK,5.3ns)	–	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	**tRRD_L(1/2K)**	Max(4nCK,5.3ns)	–	nCK	
Four activate window for 2KB page size	**tFAW_2K**	Max(28nCK,30ns)	–	ns	
Four activate window for 1KB page size	**tFAW_1K**	Max(20nCK,21ns)	–	ns	
Four activate window for 1/2KB page size	**tFAW_1/2K**	Max(16nCK,15ns)	–	ns	
Delay from start of internal write transaction to internal read command for different bank group	**tWTR_S**	max(2nCK,2.5ns)	–		
Delay from start of internal write transaction to internal read command for same bank group	**tWTR_L**	max(4nCK,7.5ns)	–		
Internal READ Command to PRECHARGE Command delay	**tRTP**	max(4nCK,7.5ns)	–		
WRITE recovery time	**tWR**	15	–	ns	
Write recovery time when CRC and DM are enabled	**tWR_CRC_DM**	tWR+max(5nCK,3.75ns)	–	ns	
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	**tWTR_S_CRC_DM**	tWTR_S+max(5nCK,3.75ns)	–	ns	
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	**tWTR_L_CRC_DM**	tWTR_L+max(5nCK,3.75ns)	–	ns	
DLL locking time	**tDLLK**	768	–	nCK	
Mode Register Set command cycle time	**tMRD**	8	–	nCK	
Mode Register Set command update delay	**tMOD**	max(24nCK,15ns)	–		
Multi-Purpose Register Recovery Time	**tMPRR**	1	–	nCK	
Multi Purpose Register Write Recovery Time	**tWR_MPR**	tMOD (min)+ AL + PL	–	–	
Auto precharge write recovery + precharge time	**tDAL(min)**	Programmed WR + roundup (tRP / tCK(avg))		nCK	
$\overline{CS}$ to Command Address Latency					
$\overline{CS}$ to Command Address Latency	**tCAL**	4	–	nCK	
DRAM Data Timing					
DQS,$\overline{DQS}$ to DQ skew, per group, per access	**tDQSQ**	–	TBD	tCK(avg)/2	13,18
DQS,$\overline{DQS}$ to DQ Skew deterministic, per group, per access	**tDQSQ**	–	TBD	tCK(avg)/2	14,16, 18
DQ output hold time from DQS,$\overline{DQS}$	**tQH**	TBD	–	tCK(avg)/2	13,17,18
DQ output hold time deterministic from DQS,$\overline{DQS}$	**tQH**	TBD	–	UI	14,16. 18
DQS,$\overline{DQS}$ to DQ Skew total, per group, per access; DBI enabled	**tDQSQ**	–	TBD	UI	13,19
DQ output hold time total from DQS,$\overline{DQS}$; DBI enabled	**tQH**	TBD	–	UI	13,19
DQ to DQ offset , per group, per access referenced to DQS,$\overline{DQS}$	**tDQSQ**	TBD	TBD	UI	15,16

Speed		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max		
Data Strobe Timing					
DQS,$\overline{DQS}$ differential READ Preamble (2 clock preamble)	**tRPRE**	0.9	TBD	tCK	
DQS,$\overline{DQS}$ differential READ Postamble	**tRPST**	TBD	TBD	tCK	
DQS,$\overline{DQS}$ differential output high time	**tQSH**	0.4	–	tCK	
DQS,$\overline{DQS}$ differential output low time	**tQSL**	0.4	–	tCK	
DQS,$\overline{DQS}$ differential WRITE Preamble	**tWPRE**	0.9	–	tCK	
DQS,$\overline{DQS}$ differential WRITE Postamble	**tWPST**	TBD	TBD	tCK	
DQS and $\overline{DQS}$ low-impedance time (Referenced from RL-1)	**tLZ(DQS)**	-360	180	ps	
DQS and $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	**tHZ(DQS)**	–	180	ps	
DQS,$\overline{DQS}$ differential input low pulse width	**tDQSL**	0.46	0.54	tCK	
DQS,$\overline{DQS}$ differential input high pulse width	**tDQSH**	0.46	0.54	tCK	
DQS,$\overline{DQS}$ rising edge to CK,$\overline{CK}$ rising edge (1 clock preamble)	**tDQSS**	-0.27	0.27	tCK	
DQS,$\overline{DQS}$ falling edge setup time to CK,$\overline{CK}$ rising edge	**tDSS**	0.18	–	tCK	
DQS,$\overline{DQS}$ falling edge hold time from CK,$\overline{CK}$ rising edge	**tDSH**	0.18	–	tCK	
MPSM Timing					
Command path disable delay upon MPSM entry	**tMPED**	Min: tMOD(min) +tCPDED(min)			
Valid clock requirement after MPSM entry	**tCKMPE**	Min: tMOD(min) +tCPDED(min)			
Valid clock requirement before MPSM exit	**tCKMPX**	Min: tCKSRX(min)			
Exit MPSM to commands not requiring a locked DLL	**tXMP**	TBD	–		
Exit MPSM to commands requiring a locked DLL	**tXMPDLL**	Min: tXMP(min) + tXSDLL(min)			
CS setup time to CKE	**tMPX_S**	TBD	–		
CS hold time to CKE	**tMPX_H**	TBD	–		
Calibration Timing					
Power-up and RESET calibration time	**tZQinit**	1024	–	nCK	
Normal operation Full calibration time	**tZQoper**	512	–	nCK	
Normal operation Short calibration time	**tZQCS**	128	–	nCK	
Reset/Self Refresh Timing					
Exit Reset from CKE HIGH to a valid command	**tXPR**	Max: max(5nCK,tRFC(min)+10ns)			
Exit Self Refresh to commands not requiring a locked DLL	**tXS**	Min: tRFC(min)+10ns			
SRX to commands not requiring a locked DLL in Self Refresh ABORT	**tXS_ABORT(min)**	Min: tRFC4(min)+10ns			
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	**tXS_FAST(min)**	Min: tRFC4(min)+10ns			
Exit Self Refresh to commands requiring a locked DLL	**tXSDLL**	Min: tDLLK(min)			
Minimum CKE low width for Self refresh entry to exit timing	**tCKESR**	Min: tCKE(min)+1nCK			
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	**tCKESR_PAR**	Min: tCKE(min)+1nCK+PL			
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	**tCKSRE**	Min: max(5nCK,10ns)			
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	**tCKSRE_PAR**	Min: max(5nCK,10ns)+PL			
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	**tCKSRX**	Min: max(5nCK,10ns)			

Speed		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max		
Power Down Timing					
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	**tXP**	Min: max(4nCK,6ns)			
CKE minimum pulse width	**tCKE**	Min: max (3nCK,5ns)			31,32
Command pass disable delay	**tCPDED**	4	–	nCK	
Power Down Entry to Exit Timing	**tPD**	tCKE(min)	9xtREFI		6
Timing of ACT command to Power Down entry	**tACTPDEN**	2	–	nCK	7
Timing of PRE or PREA command to Power Down entry	**tPRPDEN**	2	–	nCK	7
Timing of RD/RDA command to Power Down entry	**tRDPDEN**	RL+4+1	–	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	**tWRPDEN**	WL+4+(tWR/tCK(avg))		nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	**tWRAPDEN**	WL+4+WR+1	–		5
Timing of WR command to Power Down entry (BC4MRS)	**tWRPBC4DEN**	WL+2+(tWR/tCK(avg))	–		4
Timing of WRA command to Power Down entry (BC4MRS)	**tWRAPBC4DEN**	WL+2+WR+1	–		5
Timing of REF command to Power Down entry	**tREFPDEN**	2	–	nCK	7
Timing of MRS command to Power Down entry	**tMRSPDEN**	tMOD(min)	–		
PDA Timing					
Mode Register Set command cycle time in PDA mode	**tMRD_PDA**	max(16nCK,10ns)			
Mode Register Set command update delay in PDA mode	**tMOD_PDA**	tMOD			
ODT Timing					
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	**tAONAS**	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	**tAOFAS**	1.0	9.0	ns	
RTT dynamic change skew	**tADC**	0.3	0.7	tCK(avg)	
Write Leveling Timing					
First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed	**tWLMRD**	40	–	nCK	
DQS/$\overline{DQS}$ delay after write leveling mode is programmed	**tWLDQSEN**	25	–	nCK	
Write leveling setup time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	**tWLS**	0.13	–	tCK(avg)	
Write leveling hold time from rising DQS/$\overline{DQS}$ crossing to rising CK/$\overline{CK}$ crossing	**tWLH**	0.13	–	tCK(avg)	
Write leveling output delay	**tWLO**	0	9.5	ns	
Write leveling output error	**tWLOE**	0	2	ns	
CA Parity Timing					
Commands not guaranteed to be executed during this time	**tPAR_UNKNOWN**	–	PL		
Delay from errant command to $\overline{ALERT}$ assertion	**tPAR_ALERT_ON**	–	PL+6ns		
Pulse width of $\overline{ALERT}$ signal when asserted	**tPAR_ALERT_PW**	56	128	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	**tPAR_ALERT_RSP**	–	57	nCK	
Parity Latency	**PL**	4		nCK	
CRC Error Reporting					
CRC error to $\overline{ALERT}$ latency	**tCRC_ALERT**	3	13	ns	

Speed		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max		
CRC $\overline{\text{ALERT}}$ pulse width	**CRC_ALERT_PW**	6	10	nCK	
tREFI					
tRFC1 (min)	2Gb	160	–	ns	34
	4Gb	260	–	ns	34
	8Gb	350	–	ns	34
	16Gb	TBD	–	ns	34
tRFC2 (min)	2Gb	110	–	ns	34
	4Gb	160	–	ns	34
	8Gb	260	–	ns	34
	16Gb	TBD	–	ns	34
tRFC4 (min)	2Gb	90	–	ns	34
	4Gb	110	–	ns	34
	8Gb	160	–	ns	34
	16Gb	TBD	–	ns	34

Timing Parameters by Speed Bin for DDR4-2400 to DDR4-3200

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	–	8	–	8	–	ns	22
Average Clock Period	tCK(avg)	0.833	<0.938	0.750	<0.833	0.625	<0.750	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min: tCK(avg)min+tJIT(per)min_tot Max: tCK(avg)max+ tJIT(per)max_tot						tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	–	0.45	–	0.45	–	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	–	0.45	–	0.45	–	tCK(avg)	23
Clock Period Jitter- total	JIT(per)_tot	-42	42	- 0.1	0.1	- 0.1	0.1	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-21	21	TBD	TBD	TBD	TBD	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-33	33	TBD	TBD	TBD	TBD	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_total	83		TBD		TBD		ps	25
Cycle to Cycle Period Jitter deterministic	tJIT(cc)_dj	42		TBD		TBD		ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	67		TBD		TBD		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-61	61	TBD	TBD	TBD	TBD	ps	
Cumulative error across 3 cycles	tERR(3per)	-73	73	TBD	TBD	TBD	TBD	ps	
Cumulative error across 4 cycles	tERR(4per)	-81	81	TBD	TBD	TBD	TBD	ps	
Cumulative error across 5 cycles	tERR(5per)	-87	87	TBD	TBD	TBD	TBD	ps	
Cumulative error across 6 cycles	tERR(6per)	-92	92	TBD	TBD	TBD	TBD	ps	
Cumulative error across 7 cycles	tERR(7per)	-97	97	TBD	TBD	TBD	TBD	ps	
Cumulative error across 8 cycles	tERR(8per)	-101	101	TBD	TBD	TBD	TBD	ps	
Cumulative error across 9 cycles	tERR(9per)	-104	104	TBD	TBD	TBD	TBD	ps	
Cumulative error across 10 cycles	tERR(10per)	-107	107	TBD	TBD	TBD	TBD	ps	
Cumulative error across 11 cycles	tERR(11per)	-110	110	TBD	TBD	TBD	TBD	ps	
Cumulative error across 12 cycles	tERR(12per)	-112	112	TBD	TBD	TBD	TBD	ps	
Cumulative error across 13 cycles	tERR(13per)	-114	114	TBD	TBD	TBD	TBD	ps	
Cumulative error across 14 cycles	tERR(14per)	-116	116	TBD	TBD	TBD	TBD	ps	
Cumulative error across 15 cycles	tERR(15per)	-118	118	TBD	TBD	TBD	TBD	ps	
Cumulative error across 16 cycles	tERR(16per)	-120	120	TBD	TBD	TBD	TBD	ps	
Cumulative error across 17 cycles	tERR(17per)	-122	122	TBD	TBD	TBD	TBD	ps	
Cumulative error across 18 cycles	tERR(18per)	-124	-124	TBD	TBD	TBD	TBD	ps	
Cumulative error across n = 13, 14 . . .49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)						ps	
Command and Address setup time to CK,$\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIS(base)	62	–	TBD	–	TBD	–	ps	
Command and Address setup time to CK,$\overline{CK}$ referenced to Vref levels	tIS(Vref)	162	–	TBD	–	TBD	–	ps	
Command and Address hold time to CK,$\overline{CK}$ referenced to Vih(dc) / Vil(dc) levels	tIH(base)	87	–	TBD	–	TBD	–	ps	
Command and Address hold time to CK,$\overline{CK}$ referenced to Vref levels	tIH(Vref)	162	–	TBD	–	TBD	–	ps	
Control and Address Input pulse width for each input	tIPW	410	–	TBD	–	TBD	–	ps	
Command and Address Timing									
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank group	tCCD_L	6	–	TBD	–	TBD	–	nCK	34
$\overline{CAS}$ to $\overline{CAS}$ command delay for different bank group	tCCD_S	4	–	4	–	TBD	–	nCK	34

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	–	TBD	–	TBD	–	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK, 3.3ns)	–	TBD	–	TBD	–	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK, 3.3ns)	–	TBD	–	TBD	–	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	–	TBD	–	TBD	–	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 4.9ns)	–	TBD	–	TBD	–	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK, 4.9ns)	–	TBD	–	TBD	–	nCK	
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	–	TBD	–	TBD	–	ns	
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)	–	TBD	–	TBD	–	ns	
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 13ns)	–	TBD	–	TBD	–	ns	
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max (2nCK, 2.5ns)	–	TBD	–	TBD	–		
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK, 7.5ns)	–	TBD	–	TBD	–		
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	–	TBD	–	TBD	–		
WRITE recovery time	tWR	15	–	TBD	–	TBD	–	ns	
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (5nCK,3.75ns)	–	TBD	–	TBD	–	ns	
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max(5nCK, 3.75ns)	–	TBD	–	TBD	–	ns	
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max(5nCK, 3.75ns)	–	TBD	–	TBD	–	ns	
DLL locking time	tDLLK	768	–	TBD	–	TBD	–	nCK	
Mode Register Set command cycle time	tMRD	8	–	TBD	–	TBD	–	nCK	
Mode Register Set command update delay	tMOD	max(24nCK, 15ns)	–	TBD	–	TBD	–		
Multi-Purpose Register Recovery Time	tMPRR	1	–	TBD	–	TBD	–	nCK	
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	–	TBD	–	TBD	–	–	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))						nCK	
$\overline{CS}$ to Command Address Latency									
$\overline{CS}$ to Command Address Latency	tCAL	5	–	TBD	–	TBD	–	nCK	
DRAM Data Timing									
DQS,$\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	–	TBD	–	TBD	–	TBD	tCK(avg)/2	13,18
DQS,$\overline{DQS}$ to DQ Skew deterministic, per group, per access	tDQSQ	–	TBD	–	TBD	–	TBD	tCK(avg)/2	14,16, 18
DQ output hold time from DQS,$\overline{DQS}$	tQH	TBD	–	TBD	–	TBD	–	tCK(avg)/2	13,17,18
DQ output hold time deterministic from DQS,$\overline{DQS}$	tQH	TBD	–	TBD	–	TBD	–	tCK(avg)/2	14,16. 18
DQS,$\overline{DQS}$ to DQ Skew total, per group, per access; DBI enabled	tDQSQ	–	TBD	–	TBD	–	TBD	tCK(avg)/2	13,19
DQ output hold time total from DQS,$\overline{DQS}$; DBI enabled	tQH	TBD	–	TBD	–	TBD	–	tCK(avg)/2	13,19
DQ to DQ offset , per group, per access referenced to DQS,$\overline{DQS}$	tDQSQ	TBD	TBD	TBD	TBD	TBD	TBD	tCK(avg)/2	15,16

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Data Strobe Timing									
DQS,$\overline{DQS}$ differential READ Preamble (2 clock preamble)	**tRPRE**	0.9	TBD	TBD	TBD	TBD	TBD	tCK	
DQS,$\overline{DQS}$ differential READ Postamble	**tRPST**	TBD	TBD	TBD	TBD	TBD	TBD	tCK	
DQS,$\overline{DQS}$ differential output high time	**tQSH**	0.4	–	TBD	TBD	TBD	TBD	tCK	
DQS,$\overline{DQS}$ differential output low time	**tQSL**	0.4	–	TBD	TBD	TBD	TBD	tCK	
DQS,$\overline{DQS}$ differential WRITE Preamble	**tWPRE**	0.9	–	TBD	TBD	TBD	TBD	tCK	
DQS,$\overline{DQS}$ differential WRITE Postamble	**tWPST**	TBD	TBD	TBD	TBD	TBD	TBD	tCK	
DQS and $\overline{DQS}$ low-impedance time (Referenced from RL-1)	**tLZ(DQS)**	-300	150	TBD	TBD	TBD	TBD	ps	
DQS and $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	**tHZ(DQS)**	–	150	TBD	TBD	TBD	TBD	ps	
DQS,$\overline{DQS}$ differential input low pulse width	**tDQSL**	0.46	0.54	TBD	TBD	TBD	TBD	tCK	
DQS,$\overline{DQS}$ differential input high pulse width	**tDQSH**	0.46	0.54	TBD	TBD	TBD	TBD	tCK	
DQS,$\overline{DQS}$ rising edge to CK,$\overline{CK}$ rising edge (1 clock preamble)	**tDQSS**	-0.27	0.27	TBD	TBD	TBD	TBD	tCK	
DQS,$\overline{DQS}$ falling edge setup time to CK,$\overline{CK}$ rising edge	**tDSS**	0.18	–	TBD	TBD	TBD	TBD	tCK	
DQS,$\overline{DQS}$ falling edge hold time from CK,$\overline{CK}$ rising edge	**tDSH**	0.18	–	TBD	TBD	TBD	TBD	tCK	
MPSM Timing									
Command path disable delay upon MPSM entry	**tMPED**	tMOD(min) +tCPDED(min)	–	TBD	–	TBD	–		
Valid clock requirement after MPSM entry	**tCKMPE**	tMOD(min) +tCPDED(min)	–	TBD	–	TBD	–		
Valid clock requirement before MPSM exit	**tCKMPX**	tCKSRX(min)		TBD		TBD			
Exit MPSM to commands not requiring a locked DLL	**tXMP**	TBD		TBD		TBD			
Exit MPSM to commands requiring a locked DLL	**tXMPDLL**	tXMP(min) + tXSDLL(min)		TBD		TBD			
CS setup time to CKE	**tMPX_S**	TBD	–	TBD	–	TBD	–		
CS hold time to CKE	**tMPX_H**	TBD	–	TBD	–	TBD	–		
Calibration Timing									
Power-up and RESET calibration time	**tZQinit**	1024	–	TBD	–	TBD	–	nCK	
Normal operation Full calibration time	**tZQoper**	512	–	TBD	–	TBD	–	nCK	
Normal operation Short calibration time	**tZQCS**	128	–	TBD	–	TBD	–	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid command	**tXPR**	Max(5nCK,tRFC(min)+10ns)	–	TBD	–	TBD	–		
Exit Self Refresh to commands not requiring a locked DLL	**tXS**	tRFC(min)+ 10ns	–	TBD	–	TBD	–		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	**tXS_ABORT(min)**	tRFC4(min)+ 10ns	–	TBD	–	TBD	–		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	**tXS_FAST(min)**	tRFC4(min)+ 10ns	–	TBD	–	TBD	–		
Exit Self Refresh to commands requiring a locked DLL	**tXSDLL**	tDLLK(min)	–	TBD	–	TBD	–		
Minimum CKE low width for Self refresh entry to exit timing	**tCKESR**	tCKE(min)+ 1nCK	–	TBD	–	TBD	–		
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	**tCKESR_PAR**	tCKE(min)+ 1nCK+PL	–	tCKE(min)+ 1nCK+PL	–	tCKE(min)+ 1nCK+PL	–		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	**tCKSRE**	max (5nCK,10ns)	–	TBD	–	TBD	–		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	**tCKSRE_PAR**	max (5nCK,10ns)+ PL	–	TBD	–	TBD	–		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	**tCKSRX**	max (5nCK,10ns)	–	TBD	–	TBD	–		

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Power Down Timing									
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	**tXP**	max (4nCK,6ns)	–	TBD	–	TBD	–		
CKE minimum pulse width	**tCKE**	max (3nCK,5ns)	–	TBD	–	TBD	–		31,32
Command pass disable delay	**tCPDED**	4	–	TBD	–	TBD	–	nCK	
Power Down Entry to Exit Timing	**tPD**	tCKE(min)	9xtREFI	TBD	–	TBD	–		6
Timing of ACT command to Power Down entry	**tACTPDEN**	2	–	TBD	–	TBD	–	nCK	7
Timing of PRE or PREA command to Power Down entry	**tPRPDEN**	2	–	TBD	–	TBD	–	nCK	7
Timing of RD/RDA command to Power Down entry	**tRDPDEN**	RL+4+1	–	TBD	–	TBD	–	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	**tWRPDEN**	WL+4+(tWR/ tCK(avg))	–	TBD	–	TBD	–	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	**tWRAPDEN**	WL+4+WR+1	–	TBD	–	TBD	–		5
Timing of WR command to Power Down entry (BC4MRS)	**tWRPBC4DEN**	WL+2+(tWR/ tCK(avg))	–	TBD	–	TBD	–		4
Timing of WRA command to Power Down entry (BC4MRS)	**tWRAPBC4DEN**	WL+2+WR+1	–	TBD	–	TBD	–		5
Timing of REF command to Power Down entry	**tREFPDEN**	1	–	TBD	–	TBD	–	nCK	7
Timing of MRS command to Power Down entry	**tMRSPDEN**	tMOD(min)	–	TBD	–	TBD	–		
PDA Timing									
Mode Register Set command cycle time in PDA mode	**tMRD_PDA**	max(16nCK, 10ns)		TBD	–	TBD	–		
Mode Register Set command update delay in PDA mode	**tMOD_PDA**	tMOD		TBD	–	TBD	–		
ODT Timing									
Asynchronous RTT turn-on delay (Power- Down with DLL frozen)	**tAONAS**	1.0	9.0	TBD	TBD	TBD	TBD	ns	
Asynchronous RTT turn-off delay (Power- Down with DLL frozen)	**tAOFAS**	1.0	9.0	TBD	TBD	TBD	TBD	ns	
RTT dynamic change skew	**tADC**	0.3	0.7	TBD	TBD	TBD	TBD	tCK(avg)	
Write Leveling Timing									
First DQS/$\overline{\text{DQS}}$ rising edge after write leveling mode is programmed	**tWLMRD**	40	–	TBD	TBD	TBD	TBD	nCK	
DQS/$\overline{\text{DQS}}$ delay after write leveling mode is programmed	**tWLDQSEN**	25	–	TBD	TBD	TBD	TBD	nCK	
Write leveling setup time from rising CK/$\overline{\text{CK}}$ crossing to rising DQS/$\overline{\text{DQS}}$ crossing	**tWLS**	0.13	–	TBD	TBD	TBD	TBD	tCK(avg)	
Write leveling hold time from rising DQS/$\overline{\text{DQS}}$ crossing to rising CK/$\overline{\text{CK}}$ crossing	**tWLH**	0.13	–	TBD	TBD	TBD	TBD	tCK(avg)	
Write leveling output delay	**tWLO**	0	9.5	TBD	TBD	TBD	TBD	ns	
Write leveling output error	**tWLOE**	0	2	0	2	0	2	ns	
CA Parity Timing									
Commands not guaranteed to be executed during this time	**tPAR_UNKNOWN**	–	PL	–	TBD	–	TBD		
Delay from errant command to $\overline{\text{ALERT}}$ assertion	**tPAR_ALERT_ON**	–	PL+6ns	–	TBD	–	TBD		
Pulse width of $\overline{\text{ALERT}}$ signal when asserted	**tPAR_ALERT_PW**	72	144	TBD	TBD	TBD	TBD	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	**tPAR_ALERT_RSP**	–	64	TBD	TBD	TBD	TBD	nCK	
Parity Latency	**PL**	5		TBD		TBD		nCK	

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
CRC Error Reporting									
CRC error to $\overline{\text{ALERT}}$ latency	**tCRC_ALERT**	3	13	TBD	TBD	TBD	TBD	ns	
CRC $\overline{\text{ALERT}}$ pulse width	**CRC_ALERT_PW**	6	10	TBD	TBD	TBD	TBD	nCK	
Geardown timing									
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	**tXPR_GEAR**	–		TBD		TBD			
CKE High Assert to Gear Down Enable time(T2/CKE)	**tXS_GEAR**	–		TBD		TBD			
MRS command to Sync pulse time(T3)	**tSYNC_GEAR**	–	–	TBD	–	TBD	–		
Sync pulse to First valid command(T4)	**tCMD_GEAR**	–		TBD		TBD			27
Geardown setup time	**tGEAR_setup**	–	–	2	–	2	–	nCK	27
Geardown hold time	**tGEAR_hold**	–	–	2	–	2	–	nCK	
tREFI									
tRFC1 (min)	2Gb	160	–	160	–	160	–	ns	34
	4Gb	260	–	260	–	260	–	ns	34
	8Gb	350	–	350	–	350	–	ns	34
	16Gb	TBD	–	TBD	–	TBD	–	ns	34
tRFC2 (min)	2Gb	110	–	110	–	110	–	ns	34
	4Gb	160	–	160	–	160	–	ns	34
	8Gb	260	–	260	–	260	–	ns	34
	16Gb	TBD	–	TBD	–	TBD	–	ns	34
tRFC4 (min)	2Gb	90	–	90	–	90	–	ns	34
	4Gb	110	–	110	–	110	–	ns	34
	8Gb	160	–	160	–	160	–	ns	34
	16Gb	TBD	–	TBD	–	TBD	–	ns	34

NOTE 1 Start of internal write transaction is defined as follows : For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.

NOTE 2 A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.

NOTE 3 Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

NOTE 4 tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.

NOTE 5 WR in clock cycles as programmed in MR0.

NOTE 6 tREFI depends on TOPER.

NOTE 7 CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

NOTE 8 For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied

NOTE 9 When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.

NOTE 10 When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.

NOTE 11 When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.

NOTE 12 The max values are system dependent.

NOTE 13 DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.

NOTE 14 The deterministic component of the total timing. Measurement method TBD.

NOTE 15 DQ to DQ static offset relative to strobe per group. Measurement method TBD.

NOTE 16 This parameter will be characterized and guaranteed by design.

NOTE 17 When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example TBD.

NOTE 18 DRAM DBI mode is off.

NOTE 19 DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.

NOTE 20 tQSL describes the instantaneous differential output low pulse width on DQS - $\overline{\text{DQS}}$, as measured from on falling edge to the next consecutive rising edge.

NOTE 21 tQSH describes the instantaneous differential output high pulse width on DQS - $\overline{\text{DQS}}$, as measured from on falling edge to the next consecutive rising edge.

NOTE 22 There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI.

NOTE 23 tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

NOTE 24 tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

NOTE 25 Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.

NOTE 26 The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.

NOTE 27 This parameter has to be even number of clocks.

NOTE 28 When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.

NOTE 29 When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.

NOTE 30 When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.

NOTE 31 After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).

NOTE 32 After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).

NOTE 33 Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

NOTE 34 Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.

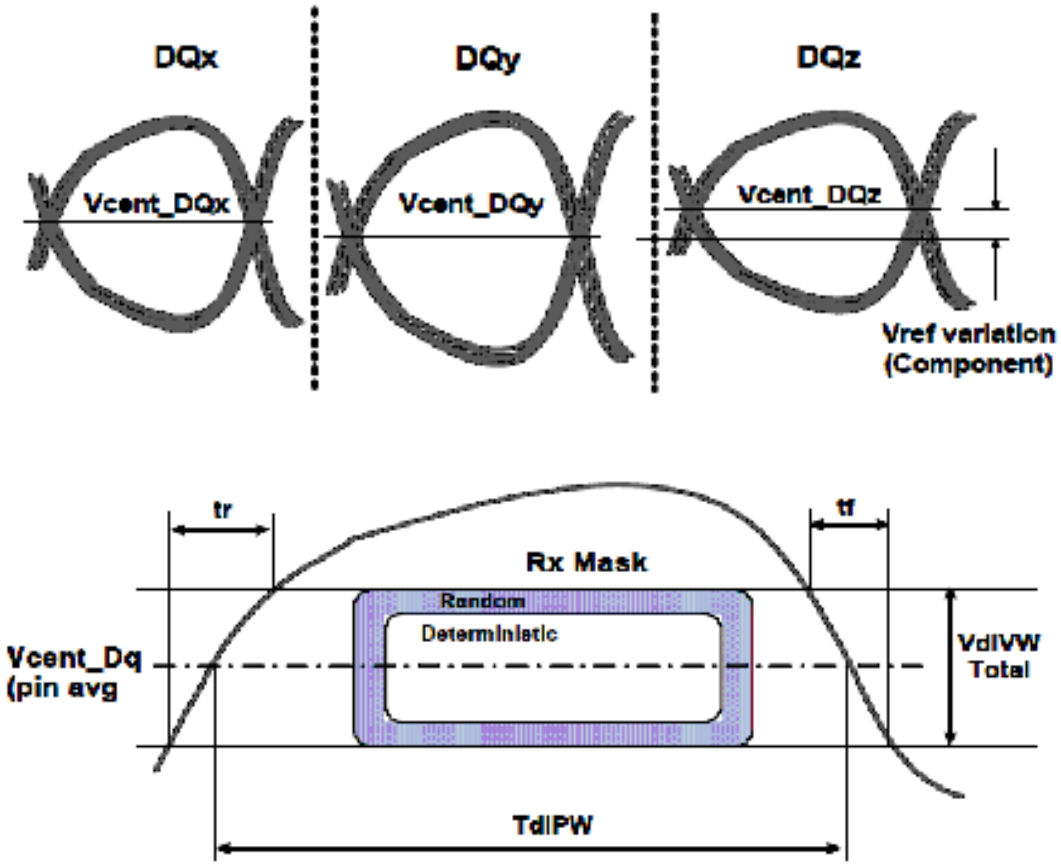
NOTE 35 This parameter must keep consistency with Speed-Bin Tables.

NOTE 36 Reserved for DDR4-1600 speed bin.

The DQ input receiver compliance mask for voltage and timing

The DQ input receiver uses a compliance mask (Rx) for voltage and timing as shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye. The TdiVW_total and VidVW_total define the absolute maximum mask and incorporates the Deterministic and Random components of the Rx mask. The TdiVW_dj and VidVW_dv define the Deterministic portion of the Rx mask.

Rx Compliance Mask



NOTE 1 SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

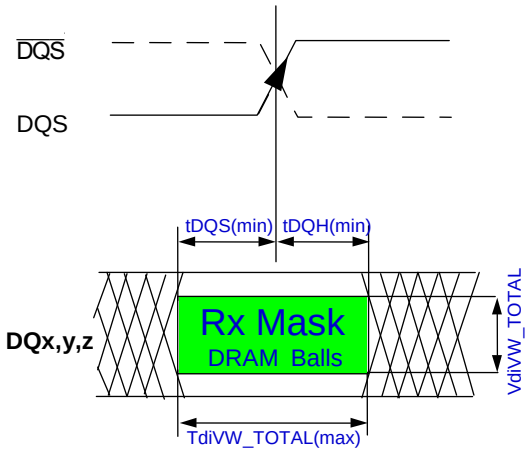
DQ TdIPW and SRIN_dIVW definition (for each input pulse)

Vcent_DQ(pin avg) is defined as the midpoint between the largest V_{REFDQ} voltage level and the smallest V_{REFDQ} voltage level across all DQ pins for a given DRAM. Each DQ pin's V_{REFDQ} is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in below. This means a DRAM's level variation is accounted for within the DRAM Rx mask. The DRAM V_{REFDQ} level will be set by the system to account for Ron and ODT settings.

DQ to DQS Timings at DRAM Balls

DQS, DQS Data-in at DRAM ball

Minimum Data-Eye / Maximum Rx Mask



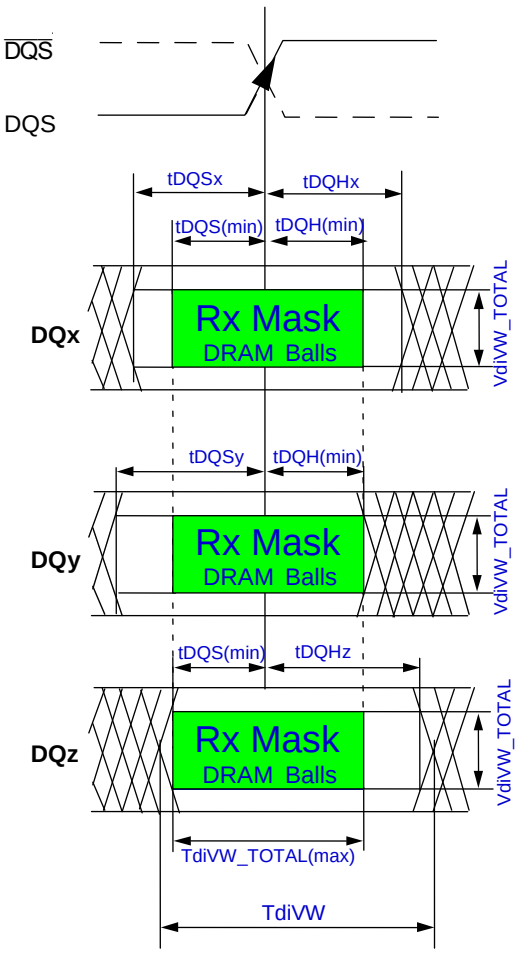
$$\frac{TdiVW\_TOTAL(max)}{2} = tDQS(min)^{*} = tDQH(min)^{*}$$

*NOTE: tDQS(min) and tDQH(min) are not new timing parameters, they are derived from the value of Tdivw_TOTAL(max)

NOTE: DQx represents an optimally centered input
DQy represents earliest valid transiining input
DQz represents latest valid transitioning input

DQS, DQS Data-in at DRAM ball

non Minimum Data-Eye / Maximum Rx Mask

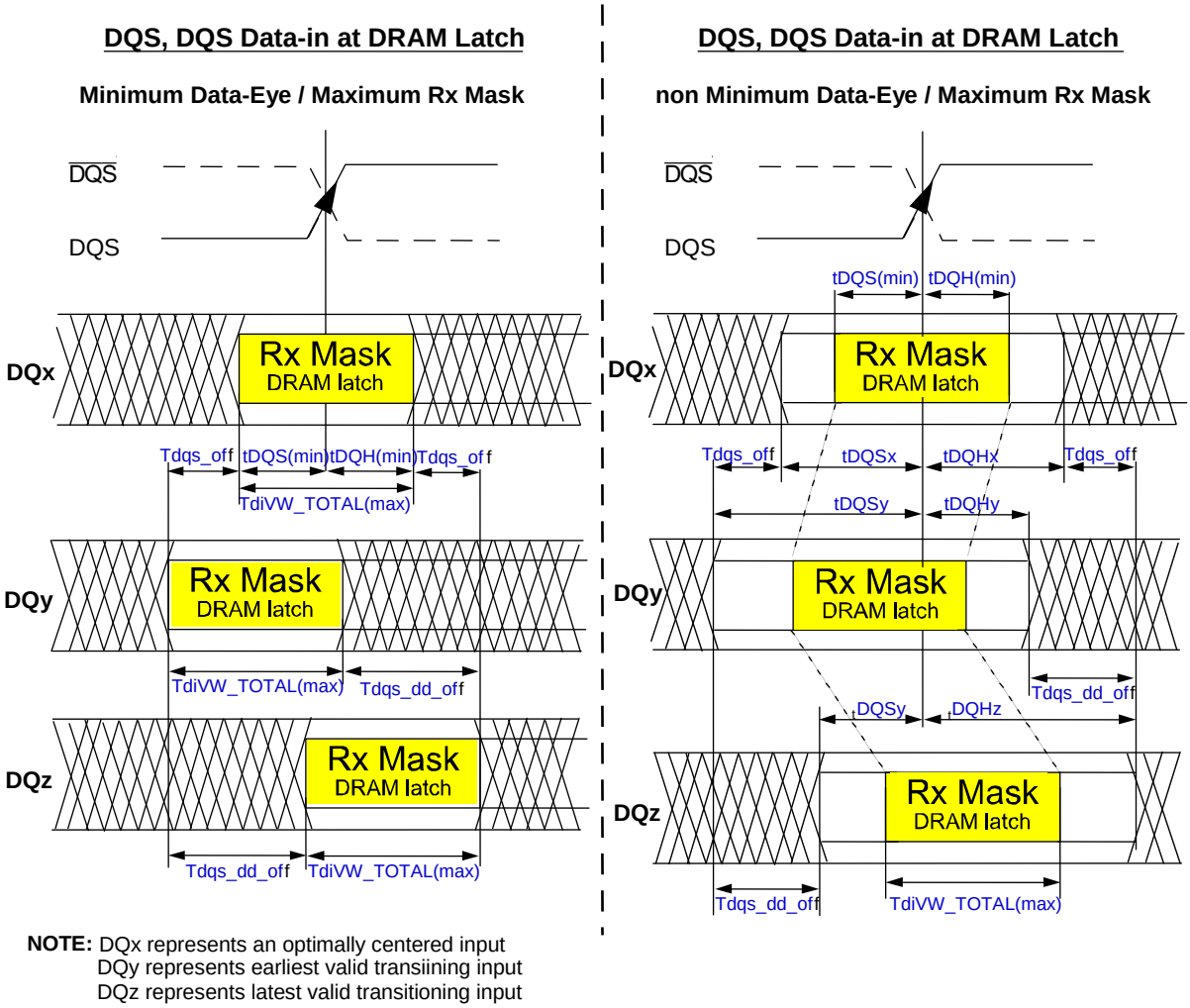


All of the timing terms in Figure 189 are measured at the VdIVW_total voltage levels centered around Vcent_DQ(pin avg) and are referenced to the DQS_t/DQS_c center aligned to the DQ per pin.

The DQ inputs relationship between each other and DQS for voltage and timing are shown in the two figures below. The figure below shows the data-eye vs Rx mask concept.

The timing terms in the figure below are measured at the VdIVW_total voltage levels centered around Vcent_DQ(pin avg). For illustrative purpose, the DQs are refer-enced to the DQS/$\overline{DQS}$ center aligned to the DQ per pin however the DRAM can capture the data input mask any where within the TdiVW_total+Tdqs_off+Tdqh_off region.

DQ to DQS Timings at DRAM latch



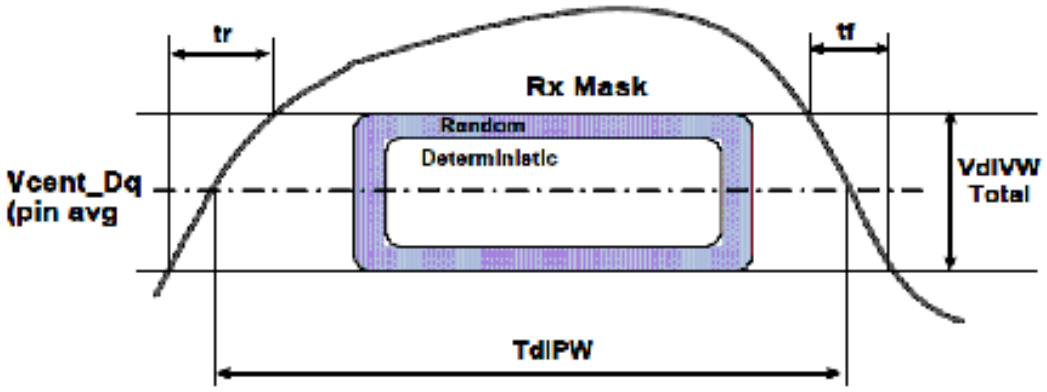
NOTE: DQx represents an optimally centered input
DQy represents earliest valid transiining input
DQz represents latest valid transitioning input

The timing terms in the figure below are measured at the VdIVW_total voltage levels centered around Vcent_DQ(pin avg) and are referenced to the DQS/$\overline{DQS}$ center aligned. Typical view assumes DQx, DQy, and DQz edges are aligned at DRAM balls.

The DDR4 DRAM's input receivers are expected to capture the input data somewhere in the TdiVW_total+Tdqs_off+Tdqh_off window provided the Rx mask is not encroached.

This means the DRAM controller will have to train to utilize the Rx specifications to its maximum benefit. If the DRAM controller does not train the data input buffers, then the worst case limits have to be used to determine a classical minimum tDS and tDH values.

DQ TdIPW and SRIN_dIVW definition (for each input pulse)



NOTE 1 SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

DRAM DQs In Receive Mode

Symbol	Parameter	DDR4-2133		DDR4-2400		DDR4-2666/ 3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
VdIVW_total	Rx Mask voltage - p-p total	–	136[12]	–	TBD	–	TBD	mV	1,2,4,6
VdIVW_dV	Rx Mask voltage - deterministic	–	136	–	TBD	–	TBD	mV	1,5,13
TdIVW_total	Rx timing window total	–	0.2[12]	–	TBD	–	TBD	UI	1,2,4,6
TdIVW_dj	Rx deterministic timing	–	0.2	–	TBD	–	TBD	UI	1,5, 13
VIHL_AC	DQ AC input swing pk-pk	186	–	TBD	–	TBD	–	mV	
TdIPW	DQ input pulse width	0.58	TBD	TBD		TBD		UI	
Tdqs_off	DQ to DQS Setup offset	–	TBD	–	TBD	–	TBD	UI	
Tdqh_off	DQ to DQS Hold offset	–	TBD	–	TBD	–	TBD	UI	
Tdqs_dd_off	DQ to DQ Setup offset	–	TBD	–	TBD	–	TBD	UI	
Tdqh_dd_off	DQ to DQ Hold offset	–	TBD	–	TBD	–	TBD	UI	
SRIN_dIVW	Input Slew Rate over VdIVW_total	TBD	9	TBD	TBD	TBD	TBD	V/ns	

UI=TCK(avg)min/2

NOTE 1 Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(pin avg). The data Rx mask is applied per bit and should include voltage and temperature drift terms. The design specification is BER <1e-16 and how this varies for lower BER is tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tbd).

NOTE 2 Rx mask voltage AC swing peak-peak requirement over TdIVW_total with at least half of TdIVW_total(max) above Vcent_DQ(pin avg) and at least half of TdIVW_total(max) below Vcent_DQ(pin avg).

NOTE 3 Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels centered around Vcent_DQ(pin avg).

NOTE 4 Defined over the DQ internal Vref range 1.

NOTE 5 Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method tbd

NOTE 6 Overshoot and Undershoot Specifications tbd.

NOTE 7 DQ input pulse signal swing into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin avg)

NOTE 8 DQ minimum input pulse width defined at the Vcent_DQ(pin avg).

NOTE 9 DQ to DQS setup or hold offset defined within byte from DRAM ball to DRAM internal latch; tDQS and tDQH are the minimum DQ setup and hold per DQ pin; each is equal to one-half of TdIVW_total(max).

NOTE 10 DQ to DQ setup or hold delta offset within byte. Defined as the static difference in Tdqs_off(max) and Tdqs_off(min) or Tdqh(max) – Tdqh(min) for a given component, from DRAM ball to DRAM internal latch.

NOTE 11 Input slew rate over VdIVW Mask centered at Vcent_DQ(pin avg). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within tbd V/ns of each other.

NOTE 12 The total timing and voltage terms(tdIVW_total & VdIVWtotal) are valid for any BER lower {lower fail rate} than the spec.

NOTE 13 VdIVW_total - VdIVW_dV and TdIVW_total - TdIVW_dj define the difference between random and deterministic fail mask. When VdIVW_total - VdIVW_dV = 0 and TdIVW_total - TdIVW_dj = 0, random error is assumed to be zero.

Function Matrix By Organization

(V:Supported, Blank:Not supported)

Functions	X4	X8	X16
Write Leveling	V	V	V
Temperature controlled Refresh	V	V	V
Low Power Auto Self Refresh	V	V	V
Fine Granularity Refresh	V	V	V
Multi Purpose Register	V	V	V
Data Mask		V	V
Data Bus Inversion		V	V
TDQS		V	
ZQ calibration	V	V	V
DQ Vref Training	V	V	V
Per DRAM Addressability	V	V	V
Mode Register Readout	V	V	V
CAL	V	V	V
WRITE CRC	V	V	V
CA Parity	V	V	V
Control Gear Down Mode	V	V	V
Programmable Preamble	V	V	V
Maximum Power Down Mode	V	V	
Boundary Scan Mode			V
Additive Latency	V	V	V

Function Matrix By Speed

(V:Supported, Blank:Not supported)

Functions	DDR4-2133	DDR4-2400	DDR4-2666/3200
Write Leveling	V	V	V
Temperature controlled Refresh	V	V	V
Low Power Auto Self Refresh	V	V	V
Fine Granularity Refresh	V	V	V
Multi Purpose Register	V	V	V
Data Mask	V	V	V
Data Bus Inversion	V	V	V
TDQS	V	V	V
ZQ calibration	V	V	V
DQ Vref Training	V	V	V
Per DRAM Addressability	V	V	V
Mode Register Readout	V	V	V
CAL	V	V	V
WRITE CRC	V	V	V
CA Parity	V	V	V
Control Gear Down Mode			V
Programmable Preamble (= 2tCK)		V	V
Maximum Power Down Mode	V	V	V
Boundary Scan Mode	V	V	V

Revision History

Version	Page	Modified	Description	Released
1.0	-	-	Preliminary Release.	12/2013
1.1	P1,2,4	-	1. Add X8 PN and 78ball info. 2. Remove 1866 PN. 2. Modify 2133 offering: 2133 15-15-15 (was: 2133 14-14-14)	03/2014
	P52	-	Add notes to the table for Auto Self Refresh.	
	All	-	1. Adjust the format of timing diagram slightly. 2. Remove 1600, 1866, 2133 14-14-14, 2400 15-15-15 specs.	
1.2	-	-	Official Release.	05/2014
1.3	P3	Part Number Guide	Simplify Part Number Guide.	07/2014
	P94	Logic Equations	Modify equations.	
	P240,257,258	IDD, IDDQ and IPP Specification	Add NOTE ”IDD spec is defined for 1.2V part herein and it's TBD for 1.35V part”.	

http://www.nanya.com/