HD66729

(Low-power 105 x 68-dot Graphics LCD Controller/Driver)

HITACHI

Preliminary
Rev 0.4a
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Description

The HD66729, 105-by-68 dot-matrix graphics LCD controller and driver LSI, displays graphics. It can be configured to drive a dot-matrix liquid-crystal display under the control of a microprocessor connected via a clock-synchronized serial or 4/8-bit bus. The HD66729 has a partial display mode that selects and drives part of the display area by using a low-duty ratio, a centering display mode that places the LCD drive position at the center of the screen, a smooth vertical-scroll display mode and a double-height display mode for the remaining bit-map areas. It continuously displays several of the graphics icons so that the user can easily access a variety of information.

The HD66729 has a booster to generate a quintuple LCD drive voltage from a single 1.8-V power supply and voltage-followers to decrease the direct current flow in the LCD drive bleeder resistors. Combining these hardware functions with software functions such as standby and sleep, enables fine power control. The HD66729 is suitable for any portable battery-driven product requiring long-term driving capabilities, including cellular phones, pagers, and electronic wallets.

Features

- Control and drive of a 105 × 68-dot-matrix graphics LCD enabling quintuple power boosting from a single 1.8-V power supply
- Partial-display and centering-display modes in which a part of the display area is selected and driven by using a low-duty ratio
- Fixed display of several graphics icons (pictograms) at the top of the screen
- Low-power operation support:
  - Vcc = 1.8 to 5.5 V (low voltage)
  - V_{LCD} = 4.0 to 13.0 V (liquid crystal drive voltage)
  - Double, triple, quadruple, or quintuple booster for liquid crystal drive voltage
  - 64-step contrast adjuster and voltage followers to decrease direct current flow in the LCD drive bleeder-resistors
  - Power-save functions such as the standby mode and sleep mode supported
  - Programmable drive duty ratios and bias values displayed on LCD
- High-speed clock-synchronized serial interface (serial transfer rate: 5 MHz max.)
- High-speed 4-/8-bit bus interface capability
- 105-segment × 68-common liquid crystal display driver

- Duty ratio and drive bias (selectable by program)
- Vertical smooth scroll
- Partial smooth scroll control (fixed display of graphics icons)
- Vertical double-height display by each display line
- Black-and-white reversed display
- No wait time for instruction execution and RAM access
- Internal R-C oscillation and hardware reset
- n-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Shift change of segment and common driver

Table 1 Progammable Display Sizes and Duty Ratios

		Graphics Display				
Duty Ratio	Optimum Drive Bias	Bit Map	13 x 13-dot Font Width	16 x 16-dot Font Width	17 x 17-dot Font Width	7 x 8-dot Font Width
1/16	1/5	105 x 16 dots	1 line x 8 characters	1 line x 6 characters	1 line x 6 characters	2 lines x 15 characters
1/24	1/6	105 x 24 dots	1 line x 8 characters	1.5 lines x 6 characters	1 line x 6 characters	3 lines x 15 characters
1/32	1/7	105 x 32 dots	2 lines x 8 characters	2 lines x 6 characters	1 line x 6 characters	4 lines x 15 characters
1/40	1/7	105 x 40 dots	3 lines x 8 characters	2.5 lines x 6 characters	2 lines x 6 characters	5 lines x 15 characters
1/48	1/8	105 x 48 dots	3 lines x 8 characters	3 lines x 6 characters	2.5 lines x 6 characters	6 lines x 15 characters
1/56	1/8	105 x 56 dots	4 lines x 8 characters	3.5 lines x 6 characters	3 lines x 6 characters	7 lines x 15 characters
1/64	1/9	105 x 64 dots	5 lines x 8 characters	4 lines x 6 characters	3.5 lines x 6 characters	8 lines x 15 characters
1/68	1/9	105 x 68 dots	5 lines x 8 characters	4 lines x 6 characters	4 lines x 6 characters	9 lines x 15 characters

<Target values>

Total Current Consumption Characteristics (Vcc = 2.0 V, TYP Conditions, LCD Drive Power Current Included)

Character Display Dot Size	Duty Ratio	R-C Oscillation Frequency	Frame Frequency	Total Power Consumption: Normal Display Operation: Internal Logic	LCD Power	Total*	Sleep Mode	Standby Mode
105 x 16 dots	1/16	75 kHz	73 Hz	(22 µA)	(8 µA)	Double (38 µA)	(8 µA)	0.1 µA
105 x 16 dots	1/24	75 kHz	73 Hz	(22 µA)	(8 µA)	Triple (46 µA)	(8 µA)	
105 x 32 dots	1/32	75 kHz	73 Hz	(25 µA)	(8 µA)	Triple (49 µA)	(8 µA)	
105 x 40 dots	1/40	75 kHz	73 Hz	(25 µA)	(8 µA)	Triple (49 µA)	(8 µA)	
105 x 48 dots	1/48	75 kHz	74 Hz	(25 µA)	(8 µA)	Triple (49 µA)	(8 µA)	
105 x 56 dots	1/56	75 kHz	74 Hz	(30 µA)	(8 µA)	Quadruple (62 µA)	(8 µA)	
105 x 64 dots	1/64	75 kHz	73 Hz	(30 µA)	(8 µA)	Quadruple (62 µA)	(8 µA)	
105 x 68 dots	1/68	75 kHz	69 Hz	(30 µA)	(8 µA)	Quintuple (70 µA)	(8 µA)	

Note : When a double, triple, quadruple, or quintuple booster is used:
the total power consumption = Internal logic current + LCD power current x 2 (double booster),
the total power consumption = Internal logic current + LCD power current x 3 (triple booster),
the total power consumption = Internal logic current + LCD power current x 4 (quadruple booster), and
the total power consumption = Internal logic current + LCD power current x 5 (quintuple booster)

Type Name

Types	External Dimensions	Operation Voltages
HD66729TB0	Bending TCP	1.8 V to 5.5 V
HCD66729BP	Au-bumped chip	

LCD Display Example

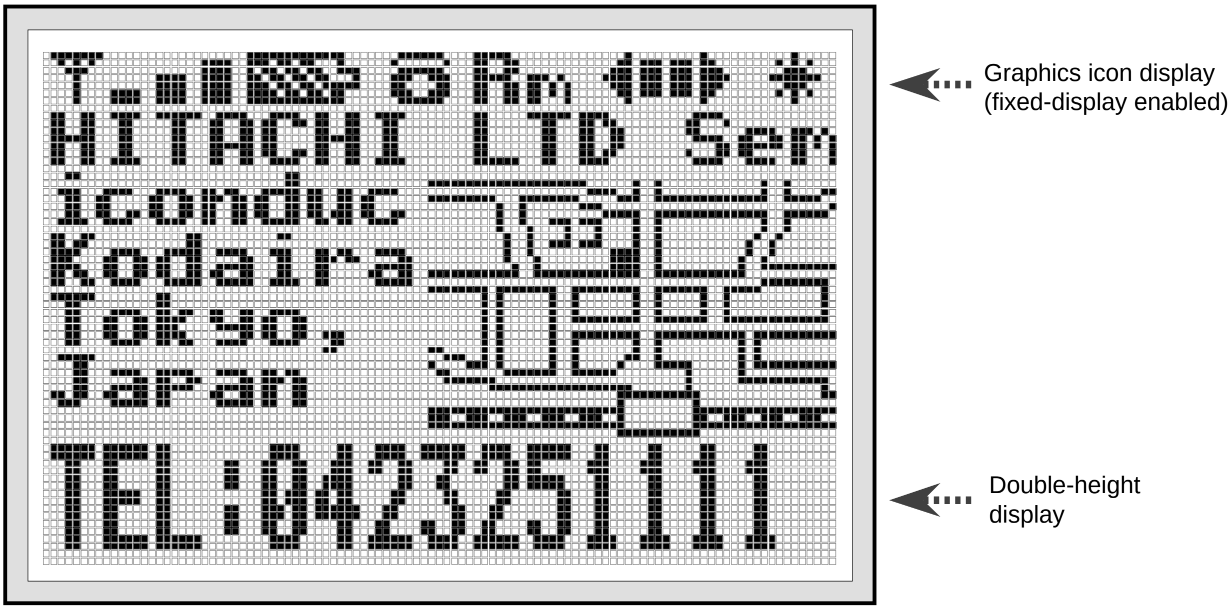


Figure 1 LCD Display Example

- 1/68 duty
- Graphics display area: 105 x 68 dots (dot matrix)
- Graphics-icon display at the top of the screen

LCD Family Comparison

Items	HD66705U	HD66717	HD66727
Character display sizes	12 characters x 2 lines	12 characters x 4 lines	12 characters x 4 lines
Graphic display sizes	—	—	—
Multiplexing icons	40	40	40
Annunciator	Static: 10	Static: 10	Static: 12
Key scan control	—	—	4 x 8
LED control ports	—	—	3
General output ports	—	—	3
Operating power voltages	2.4 V to 5.5 V	2.4 V to 5.5 V	2.4 V to 5.5 V
Liquid crystal drive voltages	3 V to 9 V	3 V to 13 V	3 V to 13 V
Serial bus	Clock-synchronized serial	I2C, Clock-synchronized serial	I2C, Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	—
Liquid crystal drive duty ratios	1/10, 18	1/10, 18, 26, 34	1/10, 18, 26, 34
Liquid crystal drive biases	1/4	1/4, 1/6	1/4, 1/6
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Double or triple	Double or triple	Double or triple
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated	Incorporated	Incorporated
Horizontal smooth scroll	—	—	—
Vertical smooth scroll	Raster-row unit	Raster-row unit	Raster-row unit
Double-height display	Yes	Yes	Yes
DDRAM	60 x 8	60 x 8	60 x 8
CGROM	9,600	9,600	11,520
CGRAM	32 x 5	32 x 5	32 x 6
SEGRAM	8 x 5	8 x 5	8 x 6
No. of CGROM fonts	240	240	240
No. of CGRAM fonts	4	4	4
Font sizes	5 x 8	5 x 8	5 x 8, 6 x 8
Bit map area	—	—	—
R-C oscillation resistor/ oscillation frequency	External resistor (40, 80 kHz)	External resistor (40-160 kHz)	External resistor (40-160 kHz)
Reset function	External	External	External
Low power control	Partial display off Oscillation off Liquid crystal power off	Partial display off Oscillation off Liquid crystal power off	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt
SEG/COM direction switching	SEG only	SEG only	SEG, COM
TCP package	TCP-153	TCP-153	TCP-158
Bare chip	Yes	Yes	Yes
Bumped chip	Yes	Yes	Yes
No. of pins	153	153	158
Chip sizes	9.69 x 2.73	10.88 x 2.89	11.39 x 2.89
Pad intervals	120 µm	120 µm	120 µm

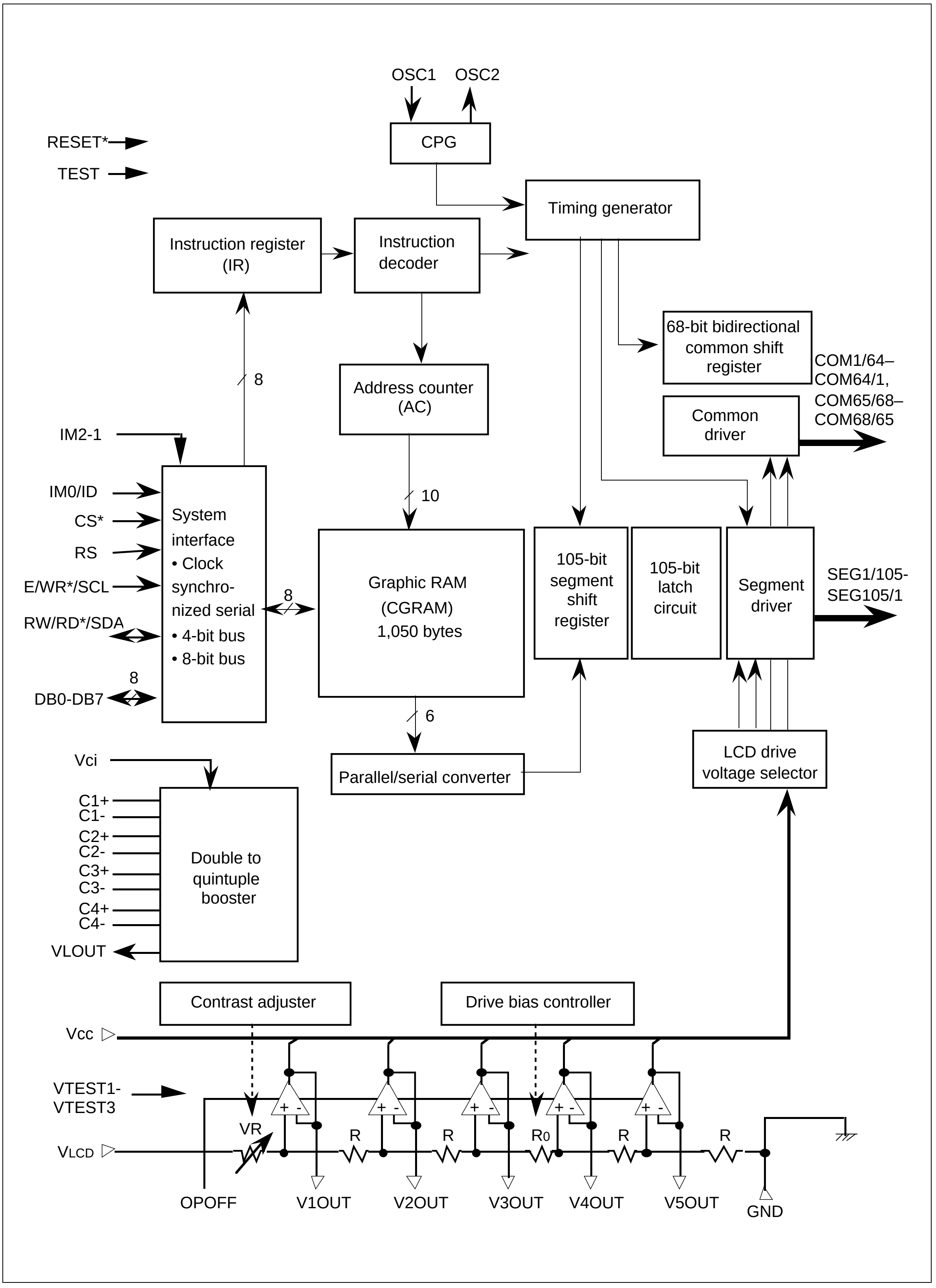
LCD Family Comparison (cont)

Items	HD66724	HD66725	HD66726
Character display sizes	12 characters x 3 lines	16 characters x 3 lines	16 characters x 5 lines
Graphic display sizes	72 x 26 dots	96 x 26 dots	96 x 42 dots
Multiplexing icons	144	192	192
Annunciator	1/2 duty: 144	1/2 duty: 192	1/2 duty: 192
Key scan control	8 x 4	8 x 4	8 x 4
LED control ports	—	—	—
General output ports	3	3	3
Operating power voltages	1.8 V to 5.5 V	1.8 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	2.2 V to 6 V	2.2 V to 6 V	4.5 V to 11 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	4 bits, 8 bits
Liquid crystal drive duty ratios	1/2, 10, 18, 26	1/2, 10, 18, 26	1/2, 10, 18, 26, 34, 42
Liquid crystal drive biases	1/4 to 1/6.5	1/4 to 1/6.5	1/2 to 1/8
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Single, double or triple	Single, double, or triple	Single, double, triple, or quadruple
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated	Incorporated	Incorporated
Horizontal smooth scroll	3-dot unit	3-dot unit	—
Vertical smooth scroll	Raster-row unit	Raster-row unit	Raster-row unit
Double-height display	Yes	Yes	Yes
DDRAM	80 x 8	80 x 8	80 x 8
CGROM	20,736	20,736	20,736
CGRAM	384 x 8	384 x 8	480 x 8
SEGRAM	72 x 8	96 x 8	96 x 8
No. of CGROM fonts	240 + 192	240 + 192	240 + 192
No. of CGRAM fonts	64	64	64
Font sizes	6 x 8	6 x 8	6 x 8
Bit map areas	72 x 26	96 x 26	96 x 42
R-C oscillation resistor/ oscillation frequency	External resistor, incorporated (32 kHz)	External resistor, incorporated (32 kHz)	External resistor, (50 kHz)
Reset function	External	External	External
Low power control	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt
SEG/COM direction switching	SEG, COM	SEG, COM	SEG, COM
TCP package	TCP-146	TCP-170	TCP-188
Bare chip	—	—	Yes
Bumped chip	Yes	Yes	Yes
No. of pins	146	170	188
Chip sizes	10.34 x 2.51	10.97 x 2.51	13.13 x 2.51
Pad intervals	80 µm	80 µm	100 µm

LCD Family Comparison (cont)

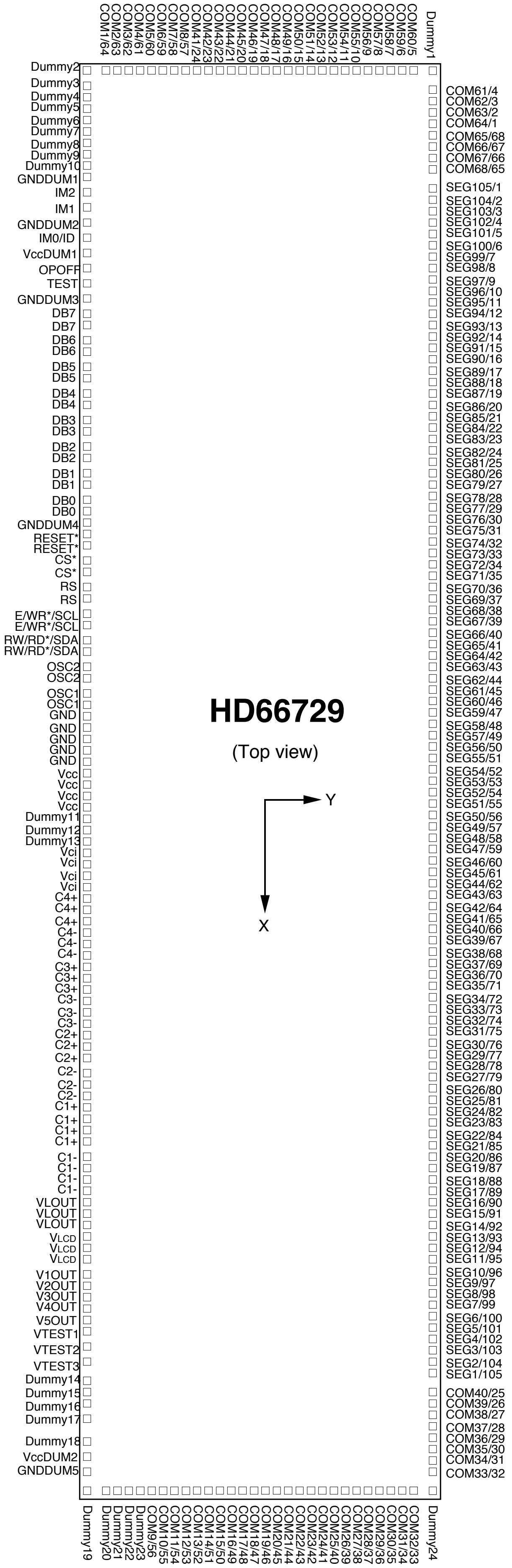
Items	HD66728	(Under development) HD66729	(Under WS) HD66741
Character display sizes	16 characters x 10 lines	—	—
Graphic display sizes	112 x 80 dots	105 x 68 dots	128 x 80 dots
Multiplexing icons	—	—	—
Annunciator	—	—	—
Key scan control	8 x 4	—	—
LED control ports	—	—	—
General output ports	3	—	3
Operating power voltages	1.8 V to 5.5 V	1.8 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	4.5 V to 15 V	4.0 V to 13 V	4.5 V to 15 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	4 bits, 8 bits
Liquid crystal drive duty ratios	1/8, 16, 24, 32, 40, 1/48, 56, 64, 72, 80	1/8, 16, 24, 32, 40, 1/48, 56, 64, 68	1/8, 16, 24, 32, 40, 1/48, 56, 64, 72, 80
Liquid crystal drive biases	1/4 to 1/10	1/4 to 1/9	1/4 to 1/10
Liquid crystal drive waveforms	B, C	B, C	B, C
Liquid crystal voltage booster	Triple, quadruple, or quintuple	Double, triple, quadruple, or quintuple	Triple, quadruple, or quintuple
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated	Incorporated	Incorporated
Horizontal smooth scroll	—	—	—
Vertical smooth scroll	Raster-row unit	Raster-row unit	Raster-row unit
Double-height display	Yes	Yes	Yes
DDRAM	160 x 8	—	—
CGROM	20,736	—	—
CGRAM	1,120 x 8	1,050 x 8	1,280 x 8
SEGRAM	—	—	—
No. of CGROM fonts	240 + 192	—	—
No. of CGRAM fonts	64	—	—
Font sizes	6 x 8	—	—
Bit map areas	112 x 80	105 x 68	128 x 80
R-C oscillation resistor/ oscillation frequency	External resistor (70–90 kHz)	External resistor (75 kHz)	External resistor (70–90 kHz)
Reset function	External	External	External
Low power control	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Oscillation off Liquid crystal power off	Partial display off Oscillation off Liquid crystal power off
SEG/COM direction switching	SEG, COM	SEG, COM	SEG, COM
TCP package	TCP-243	TCP-213	TCP-254
Bare chip	—	—	—
Bumped chip	Yes	Yes	Yes
No. of pins	243	213	243
Chip sizes	13.67 x 2.78	12.23 x 2.52	14.30 x 2.78
Pad intervals	70 µm	70 µm	70 µm

HD66729 Block Diagram



HD66729 Pad Arrangement

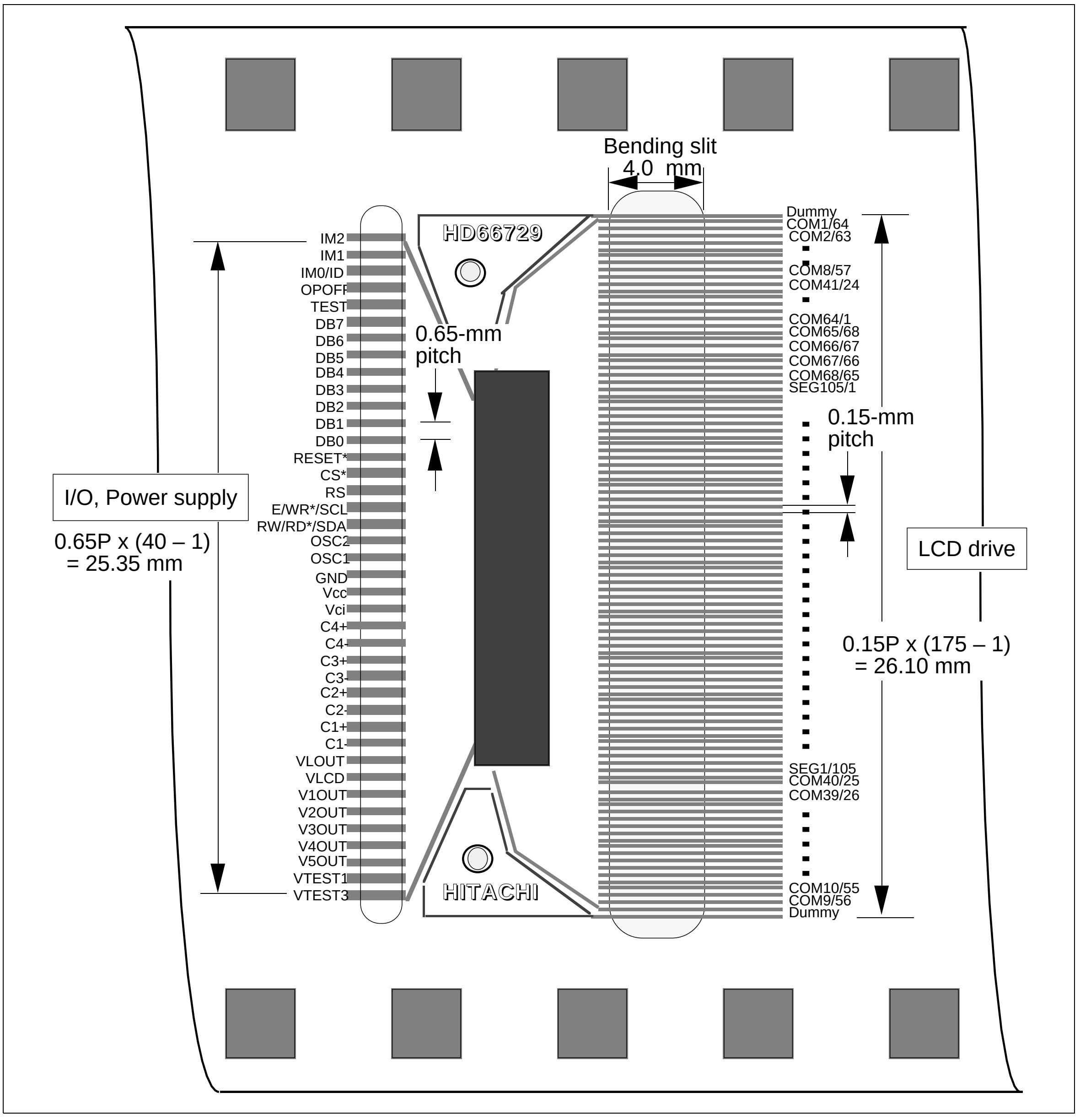
- Chip size: 12.23 mm X 2.52 mm
- Pad coordinates: Pad center
- Coordinate origin: Chip center
- Au bump size: 50 µm x 70 µm
- Au bump pitch: 70 µm (min.)
- Au bump height: 20 µm (typ.)



HD66729 Pad Coordinate

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1	Dummy2	-5915	-1146	74	C3+	1364	-1135	147	COM37 / 28	5455	1106	220	SEG70 / 36	-1640	1135
2	Dummy3	-5735	-1146	75	C3-	1508	-1135	148	COM38 / 27	5385	1106	221	SEG71 / 35	-1737	1135
3	Dummy4	-5663	-1146	76	C3-	1608	-1135	149	COM39 / 26	5315	1106	222	SEG72 / 34	-1833	1135
4	Dummy5	-5591	-1146	77	C3-	1708	-1135	150	COM40 / 25	5245	1106	223	SEG73 / 33	-1930	1135
5	Dummy6	-5519	-1146	78	C2+	1851	-1135	151	SEG1 / 105	5017	1135	224	SEG74 / 32	-2026	1135
6	Dummy7	-5447	-1146	79	C2+	1951	-1135	152	SEG2 / 104	4920	1135	225	SEG75 / 31	-2123	1135
7	Dummy8	-5375	-1146	80	C2+	2051	-1135	153	SEG3 / 103	4824	1135	226	SEG76 / 30	-2219	1135
8	Dummy9	-5303	-1146	81	C2-	2195	-1135	154	SEG4 / 102	4728	1135	227	SEG77 / 29	-2316	1135
9	Dummy10	-5231	-1146	82	C2-	2294	-1135	155	SEG5 / 101	4631	1135	228	SEG78 / 28	-2412	1135
10	GNDDUM1	-5084	-1146	83	C2-	2394	-1135	156	SEG6 / 100	4535	1135	229	SEG79 / 27	-2508	1135
11	IM2	-4984	-1146	84	C1+	2538	-1135	157	SEG7 / 99	4438	1135	230	SEG80 / 26	-2605	1135
12	IM1	-4800	-1146	85	C1+	2638	-1135	158	SEG8 / 98	4342	1135	231	SEG81 / 25	-2701	1135
13	GNDDUM2	-4712	-1146	86	C1+	2737	-1135	159	SEG9 / 97	4245	1135	232	SEG82 / 24	-2798	1135
14	IM0	-4624	-1146	87	C1+	2837	-1135	160	SEG10 / 96	4149	1135	233	SEG83 / 23	-2894	1135
15	VccDUM1	-4524	-1146	88	C1-	2981	-1135	161	SEG11 / 95	4052	1135	234	SEG84 / 22	-2991	1135
16	OPOFF	-4424	-1146	89	C1-	3081	-1135	162	SEG12 / 94	3956	1135	235	SEG85 / 21	-3087	1135
17	TEST	-4323	-1146	90	C1-	3180	-1135	163	SEG13 / 93	3859	1135	236	SEG86 / 20	-3184	1135
18	GNDDUM3	-4234	-1146	91	C1-	3280	-1135	164	SEG14 / 92	3763	1135	237	SEG87 / 19	-3280	1135
19	DB7	-4145	-1146	92	VLOUT	3424	-1135	165	SEG15 / 91	3666	1135	238	SEG88 / 18	-3377	1135
20	DB7	-4064	-1146	93	VLOUT	3524	-1135	166	SEG16 / 90	3570	1135	239	SEG89 / 17	-3473	1135
21	DB6	-3961	-1146	94	VLOUT	3623	-1135	167	SEG17 / 89	3473	1135	240	SEG90 / 16	-3570	1135
22	DB6	-3880	-1146	95	VLCD	3767	-1135	168	SEG18 / 88	3377	1135	241	SEG91 / 15	-3666	1135
23	DB5	-3777	-1146	96	VLCD	3867	-1135	169	SEG19 / 87	3280	1135	242	SEG92 / 14	-3763	1135
24	DB5	-3696	-1146	97	VLCD	3967	-1135	170	SEG20 / 86	3184	1135	243	SEG93 / 13	-3859	1135
25	DB4	-3593	-1146	98	V1OUT	4141	-1136	171	SEG21 / 85	3087	1135	244	SEG94 / 12	-3956	1135
26	DB4	-3512	-1146	99	V2OUT	4272	-1136	172	SEG22 / 84	2991	1135	245	SEG95 / 11	-4052	1135
27	DB3	-3409	-1146	100	V3OUT	4402	-1136	173	SEG23 / 83	2894	1135	246	SEG96 / 10	-4149	1135
28	DB3	-3328	-1146	101	V4OUT	4532	-1136	174	SEG24 / 82	2798	1135	247	SEG97 / 9	-4245	1135
29	DB2	-3225	-1146	102	V5OUT	4662	-1136	175	SEG25 / 81	2701	1135	248	SEG98 / 8	-4342	1135
30	DB2	-3144	-1146	103	VTEST1	4792	-1136	176	SEG26 / 80	2605	1135	249	SEG99 / 7	-4438	1135
31	DB1	-3041	-1146	104	VTEST2	4922	-1136	177	SEG27 / 79	2508	1135	250	SEG100 / 6	-4535	1135
32	DB1	-2960	-1146	105	VTEST3	5052	-1136	178	SEG28 / 78	2412	1135	251	SEG101 / 5	-4631	1135
33	DB0	-2857	-1146	106	Dummy14	5270	-1146	179	SEG29 / 77	2316	1135	252	SEG102 / 4	-4728	1135
34	DB0	-2776	-1146	107	Dummy15	5342	-1146	180	SEG30 / 76	2219	1135	253	SEG103 / 3	-4824	1135
35	GNDDUM4	-2673	-1146	108	Dummy16	5414	-1146	181	SEG31 / 75	2123	1135	254	SEG104 / 2	-4920	1135
36	RESET*	-2592	-1146	109	Dummy17	5486	-1146	182	SEG32 / 74	2026	1135	255	SEG105 / 1	-5017	1135
37	RESET*	-2511	-1146	110	Dummy18	5558	-1146	183	SEG33 / 73	1930	1135	256	COM68 / 65	-5245	1106
38	CS*	-2424	-1146	111	VccDUM2	5630	-1146	184	SEG34 / 72	1833	1135	257	COM67 / 66	-5315	1106
39	CS*	-2343	-1146	112	GNDDUM5	5702	-1146	185	SEG35 / 71	1737	1135	258	COM66 / 67	-5385	1106
40	RS	-2240	-1146	113	Dummy19	5915	-1146	186	SEG36 / 70	1640	1135	259	COM65 / 68	-5455	1106
41	RS	-2159	-1146	114	Dummy20	5915	-966	187	SEG37 / 69	1544	1135	260	COM64 / 1	-5525	1106
42	E/WR*/SCL	-2056	-1146	115	Dummy21	5915	-894	188	SEG38 / 68	1447	1135	261	COM63 / 2	-5595	1106
43	E/WR*/SCL	-1975	-1146	116	Dummy22	5915	-822	189	SEG39 / 67	1351	1135	262	COM62 / 3	-5665	1106
44	RW/RD*/SDA	-1866	-1146	117	Dummy23	5915	-750	190	SEG40 / 66	1254	1135	263	COM61 / 4	-5735	1106
45	RW/RD*/SDA	-1785	-1146	118	COM9 / 56	5915	-665	191	SEG41 / 65	1158	1135	264	Dummy1	-5915	1135
46	OSC2	-1688	-1146	119	COM10 / 55	5915	-595	192	SEG42 / 64	1061	1135	265	COM60 / 5	-5915	945
47	OSC2	-1607	-1146	120	COM11 / 54	5915	-525	193	SEG43 / 63	965	1135	266	COM59 / 6	-5915	875
48	OSC1	-1504	-1146	121	COM12 / 53	5915	-455	194	SEG44 / 62	868	1135	267	COM58 / 7	-5915	805
49	OSC1	-1423	-1146	122	COM13 / 52	5915	-385	195	SEG45 / 61	772	1135	268	COM57 / 8	-5915	735
50	GND	-1327	-1146	123	COM14 / 51	5915	-315	196	SEG46 / 60	675	1135	269	COM56 / 9	-5915	665
51	GND	-1224	-1146	124	COM15 / 50	5915	-245	197	SEG47 / 59	579	1135	270	COM55 / 10	-5915	595
52	GND	-1120	-1146	125	COM16 / 49	5915	-175	198	SEG48 / 58	482	1135	271	COM54 / 11	-5915	525
53	GND	-1017	-1146	126	COM17 / 48	5915	-105	199	SEG49 / 57	386	1135	272	COM53 / 12	-5915	455
54	GND	-913	-1146	127	COM18 / 47	5915	-35	200	SEG50 / 56	289	1135	273	COM52 / 13	-5915	385
55	Vcc	-789	-1089	128	COM19 / 46	5915	35	201	SEG51 / 55	193	1135	274	COM51 / 14	-5915	315
56	Vcc	-659	-1089	129	COM20 / 45	5915	105	202	SEG52 / 54	96	1135	275	COM50 / 15	-5915	245
57	Vcc	-528	-1089	130	COM21 / 44	5915	175	203	SEG53 / 53	0	1135	276	COM49 / 16	-5915	175
58	Vcc	-398	-1089	131	COM22 / 43	5915	245	204	SEG54 / 52	-96	1135	277	COM48 / 17	-5915	105
59	Dummy11	-246	-1146	132	COM23 / 42	5915	315	205	SEG55 / 51	-193	1135	278	COM47 / 18	-5915	35
60	Dummy12	-174	-1146	133	COM24 / 41	5915	385	206	SEG56 / 50	-289	1135	279	COM46 / 19	-5915	-35
61	Dummy13	-102	-1146	134	COM25 / 40	5915	455	207	SEG57 / 49	-386	1135	280	COM45 / 20	-5915	-105
62	Vci	35	-1135	135	COM26 / 39	5915	525	208	SEG58 / 48	-482	1135	281	COM44 / 21	-5915	-175
63	Vci	135	-1135	136	COM27 / 38	5915	595	209	SEG59 / 47	-579	1135	282	COM43 / 22	-5915	-245
64	Vci	235	-1135	137	COM28 / 37	5915	665	210	SEG60 / 46	-675	1135	283	COM42 / 23	-5915	-315
65	Vci	335	-1135	138	COM29 / 36	5915	735	211	SEG61 / 45	-772	1135	284	COM41 / 24	-5915	-385
66	C4+	478	-1135	139	COM30 / 35	5915	805	212	SEG62 / 44	-868	1135	285	COM8 / 57	-5915	-455
67	C4+	578	-1135	140	COM31 / 34	5915	875	213	SEG63 / 43	-965	1135	286	COM7 / 58	-5915	-525
68	C4+	678	-1135	141	COM32 / 33	5915	945	214	SEG64 / 42	-1061	1135	287	COM6 / 59	-5915	-595
69	C4-	822	-1135	142	Dummy24	5915	1135	215	SEG65 / 41	-1158	1135	288	COM5 / 60	-5915	-665
70	C4-	921	-1135	143	COM33 / 32	5735	1106	216	SEG66 / 40	-1254	1135	289	COM4 / 61	-5915	-735
71	C4-	1021	-1135	144	COM34 / 31	5665	1106	217	SEG67 / 39	-1351	1135	290	COM3 / 62	-5915	-805
72	C3+	1165	-1135	145	COM35 / 30	5595	1106	218	SEG68 / 38	-1447	1135	291	COM2 / 63	-5915	-875
73	C3+	1265	-1135	146	COM36 / 29	5525	1106	219	SEG69 / 37	-1544	1135	292	COM1 / 64	-5915	-945

TCP Dimensions (HD66729TB0)



Pin Functions

Table 2 Pin Functional Description

<table>
<tr><th>Signals</th><th>Number of Pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>IM2, IM1</td><td>2</td><td>I</td><td>GND or V_{CC}</td><td>Selects the MPU interface mode:
<table>
<tr><th>IM2</th><th>IM1</th><th>MPU interface mode</th></tr>
<tr><td>"GND"</td><td>"GND"</td><td>Clock-synchronized serial interface</td></tr>
<tr><td>"GND"</td><td>"Vcc"</td><td>68-system parallel bus interface</td></tr>
<tr><td>"Vcc"</td><td>"GND"</td><td>Setting inhibited</td></tr>
<tr><td>"Vcc"</td><td>"Vcc"</td><td>80-system parallel bus interface</td></tr>
</table></td></tr>
<tr><td>IM0/ID</td><td>1</td><td>I</td><td>GND or V_{CC}</td><td>Selects the transfer bus length for a parallel bus interface.
GND: 8-bit bus, Vcc: 4-bit bus
Inputs the ID of the device ID code for a serial bus interface.</td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>Selects the HD66729:
Low: HD66729 is selected and can be accessed
High: HD66729 is not selected and cannot be accessed
Must be fixed at GND level when not in use.</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Selects the register for a parallel bus interface.
Low: Instruction High: RAM access
Fix this pin to the Vcc or GND level for a serial interface.</td></tr>
<tr><td>E/WR*/SCL</td><td>1</td><td>I</td><td>MPU</td><td>For an 80-system parallel bus interface, serves as a write strobe signal and writes data at the low level.
For a 68-system parallel bus interface, serves as an enable signal to activate data read/write operation.
Inputs the serial transfer clock for a serial interface.
Fetches data at the rising edge of a clock.</td></tr>
<tr><td>RW/RD*/
SDA</td><td>1</td><td>I or
I/O</td><td>MPU</td><td>For an 80-system parallel bus interface, serves as a write strobe signal and reads data at the low level.
For a 68-system parallel bus interface, serves as a signal to select data read/write operation.
Low: Write High: Read
Serves as the bidirectional serial transfer data for a serial interface. Sends/Receives data.</td></tr>
<tr><td>DB0–DB7</td><td>8</td><td>I/O</td><td>MPU</td><td>Serves as a bidirectional data bus for a parallel bus interface.
For a 4-bit bus, data transfer uses DB7-DB4; fix unused DB3-DB0 to the Vcc or GND level. Fix all pins to the Vcc or GND level for a serial interface.</td></tr>
</table>

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
COM1/64–COM64/1, COM65/68, COM66/67, COM67/66, COM68/65	68	O	LCD	Output signals for common drive: COM1 to COM8 for the first line, COM9 to COM16 for the second line, COM17 to COM24 for the third line, COM25 to COM32 for the fourth line, and COM57 to COM64 for the 8th line. All the unused pins output unselected waveforms. In the display-off period (D = 0), sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, COM1/64 is COM1. If CMS = 1, COM1/64 is COM64. Note that the start position of the common output (the first line) is shifted by CN1–CN0 bits.
SEG1/105–SEG105/1	105	O	LCD	Output signals for segment drive. In the display-off period (D = 0), sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, SEG1/105 is SEG1. If SGS = 1, SEG1/105 is SEG105.
V1OUT–V5OUT	5	I or O	Open or external bleeder-resistor	Used for output from the internal operational amplifiers when they are used (OPOFF = GND); attach a capacitor to stabilize the output. When the amplifiers are not used (OPOFF = V_{CC}), V1 to V5 voltages can be supplied to these pins externally.
V_{LCD}	3	—	Power supply	Power supply for LCD drive. V_{LCD} − GND = 13 V max.
V_{CC}, GND	8	—	Power supply	V_{CC}: +1.8 V to +5.5 V; GND (logic): 0 V
OSC1, OSC2	2	I or O	Oscillation-resistor or clock	For R-C oscillation using an external resistor, connect an external resistor. For external clock supply, insert the dumping resistance (about 600 Ω to 2 kΩ) and input clock pulses to OSC1.
Vci	4	I	Power supply	Inputs a reference voltage and supplies power to the booster; generates the liquid crystal display drive voltage from the operating voltage. The boosting output voltage must not be larger than the absolute maximum ratings. Must be left disconnected when the booster is not used.
VLOUT	3	O	V_{LCD} pin/booster capacitance	Potential difference between Vci and GND is double- to quintuple-boosted and then output. Magnitude of boost is selected by instruction.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
C1+, C1–	8	—	Booster capacitance	External capacitance should be connected here when using the double or more booster.
C2+, C2–	6	—	Booster capacitance	External capacitance should be connected here when using the triple or more booster.
C3+, C3–	6	—	Booster capacitance	External capacitance should be connected here when using the quadruple and quintuple booster.
C4+, C4–	6	—	Booster capacitance	External capacitance should be connected here when using the quintuple booster.
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low.
OPOFF	1	I	V_{cc} or GND	Turns the internal operational amplifier off when OPOFF = V_{CC}, and turns it on when OPOFF = GND. If the amplifier is turned off (OPOFF = V_{CC}), V1 to V5 must be supplied to the V1OUT to V5OUT pins.
VccDUM	2	O	Input pins	Outputs the internal V_{cc} level; shorting this pin sets the adjacent input pin to the V_{cc} level.
GNDDUM	5	O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy	16	—	—	Dummy pad. Must be left disconnected.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
VTEST1	1	I	GND or V_{cc}	Adjusts the driving capability of the internal operational amplifier for the LCD. This signal enters the normal drive mode in the GND side, and it enters the high-power drive mode in the V_{cc} side. When the display quality is not sufficient, use the high-power drive mode even though the power-consumption current is large.
VTEST2	1	—	—	Test pin. Must be left disconnected.
VTEST3	1	I	V_{cc} or GND	Adjusts the driving capability of the internal operational amplifier for the LCD. This signal enters the normal drive mode or high-power mode in the GND side according to the VTEST1 pin setting, and it enters the low-power drive mode in the V_{cc} side. Use this signal in the low-power mode so that the display quality is not lowered.

Block Function Description

System Interface

The HD66729 has five types of system interfaces, and a clock-synchronized serial, a 68-system 4-bit/8-bit bus, and a 80-system 4-bit/8-bit bus. The interface mode is selected by the IM2-0 pins.

The HD66729 has two 8-bit registers: an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display control, and address information for the graphic RAM (CGRAM).

The DR temporarily stores data to be written into or read from the CGRAM. Data written into the DR from the MPU is automatically written into the CGRAM by internal operation. When address information is written into the IR, data is read and then stored in the DR from the CGRAM by internal operation. Data is read through the DR when reading from the RAM, and the first read data is invalid and the second and the following data are normal. After reading, data in the CGRAM at the next address is sent to the DR for the next reading from the MPU.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

Table 3 Register Selection by RS and R/W Bits

R/W Bits	RS Bits	Operations
0	0	Write instructions to IR
1	0	Disabled
0	1	DR write as an internal operation (DR to CGRAM)
1	1	DR read as an internal operation (CGRAM to DR)

Address Counter (AC)

The address counter (AC) assigns addresses to the CGRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the CGRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the RDM bit automatically updates or does not update the AC.

Graphic RAM (CGRAM)

The graphic RAM (CGRAM) stores bit-pattern data of 112 x 80 dots. A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the CGRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another.

Oscillation Circuit (OSC)

The HD66729 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 68 common signal drivers (COM1 to COM68) and 105 segment signal drivers (SEG1 to SEG105). When the number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output unselected waveforms.

Display pattern data is sent to a 105-bit shift register and latched when all needed data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs. The shift direction of 105-bit data can be changed by the SGS bit. The shift direction for the common driver can also be changed by the CMS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

Booster (DC-DC Converter)

The booster generates double, triple, quadruple, or quintuple voltage input to the Vci pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. Boost output level from double to quintuple boost can be selected by software. For details, see the Power Supply for Liquid Crystal Display Drive section.

V-Pin Voltage Follower

A voltage follower for each voltage level (V1 to V5) reduces current consumption by the LCD drive power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD drive voltage. This internal bleeder-resistor can be software-specified from 1/4 bias to 1/9 bias, according to the liquid crystal display drive duty value. The voltage followers can be turned off while multiplexing drive is not being used. For details, see the Power Supply for Liquid Crystal Display Drive section.

Contrast Adjuster

The contrast adjuster can be used to adjust LCD contrast in 64 steps by varying the LCD drive voltage by software. This can be used to select an appropriate LCD brightness or to compensate for temperature.

CGRAM Address Map

Table 4 Relationship between Display Position and CGRAM Address (1)

Segment Driver		SEG1/105	SEG2/104	SEG3/103	SEG4/102	SEG5/101	SEG6/100	SEG7/99	SEG8/98	SEG9/97	SEG10/96	SEG11/95	SEG12/94	SEG13/93	SEG14/92	SEG15/91	SEG16/90	SEG17/89	...	SEG101/5	SEG102/4	SEG103/3	SEG104/2	SEG105/1	Segment / Common
Address	SGS="0"	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	...	064	065	066	067	068	**(HEX)**
	SGS="1"	068	067	066	065	064	063	062	061	060	05F	05E	05D	05C	05B	05A	059	058	...	004	003	002	001	000	
	DB0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	...	0	0	1	0	0	COM1
	DB1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	...	0	1	1	0	0	COM2
	DB2	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	...	0	0	1	0	0	COM3
	DB3	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	0	0	1	0	0	COM4
	DB4	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	0	1	0	0	COM5
	DB5	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	0	1	0	0	COM6
	DB6	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	0	1	1	1	0	COM7
	DB7	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	0	0	0	0	COM8
Address	SGS="0"	080	081	082	083	084	085	086	087	088	089	08A	08B	08C	08D	08E	08F	090	...	0E4	0E5	0E6	0E7	0E8	**(HEX)**
	SGS="1"	0E8	0E7	0E6	0E5	0E4	0E3	0E2	0E1	0E0	0DF	0DE	0DD	0DC	0DB	0DA	0D9	0D8	...	084	083	082	081	080	
	DB0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	..	0	1	1	1	0	COM9
	DB1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	..	1	0	0	0	1	COM10
	DB2	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	..	0	0	0	0	1	COM11
	DB3	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	..	0	0	0	1	0	COM12
	DB4	0	0	0	0	1		0	0	1	0	0	0	1	0	0	0	0	..	0	0	1	0	0	COM13
	DB5	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	..	0	1	0	0	0	COM14
	DB6	0	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	..	1	1	1	1	1	COM15
	DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	..	0	0	0	0	0	COM16
Address	SGS="0"	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	...	164	165	166	167	168	**(HEX)**
	SGS="1"	168	167	166	165	164	163	162	161	160	15F	15E	15D	15C	15B	15A	159	158	...	104	103	102	101	100	
	DB0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	...	1	1	1	1	1	COM17
	DB1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	0	0	0	1	0	COM18
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	0	0	0	0	0	COM24
Address	SGS="0"	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	180	...	1E4	1E5	1E6	1E7	1E8	**(HEX)**
	SGS="1"	1E8	1E7	1E6	1E5	1E4	1E3	1E2	1E1	1E0	1DF	1DE	1DD	1DC	1DB	1DA	1D9	1D8	...	184	183	182	181	180	
	DB0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	...	0	0	0	1	0	COM25
	DB1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	...	0	0	1	1	0	COM26
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	...	0	0	0	0	0	COM32
Address	SGS="0"	200	201	202	203	204	205	206	207	208	209	20A	20B	20C	20D	20E	20F	210	...	264	265	266	267	268	**(HEX)**
	SGS="1"	268	267	266	265	264	263	262	261	260	25F	25E	25D	25C	25B	25A	259	258	...	204	203	202	201	200	
	DB0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	...	0	0	0	1	0	COM33
	DB1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	...	0	0	1	1	0	COM34
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	...	0	0	0	0	0	COM40

Notes: 1. A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).
2. Addresses x69H–x6FH and xE9H–xEF exist but have no meanings for display.

Table 5 Relationship between Display Position and CGRAM Address (2)

Segment Driver	SEG1/105	SEG2/104	SEG3/103	SEG4/102	SEG5/101	SEG6/100	SEG7/99	SEG8/98	SEG9/97	SEG10/96	SEG11/95	SEG12/94	SEG13/93	SEG14/92	SEG15/91	SEG16/90	SEG17/89	…	SEG101/5	SEG102/4	SEG103/3	SEG104/2	SEG105/1	Segment / Common
Address SGS="0"	280	281	282	283	284	285	286	287	288	289	28A	28B	28C	28D	28E	28F	290	…	2E4	2E5	2E6	2E7	2E8	(HEX)
Address SGS="1"	2E8	2E7	2E6	2E5	2E4	2E3	2E2	2E1	2E0	2DF	2DE	2DD	2DC	2DB	2DA	2D9	2D8	…	284	283	282	281	280	
DB0	0	1	1	0	0	0	1	1	0	0	0	1	1	1	1	1		…	1	1	1	1	1	COM41
DB1	1	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1	…	0	0	0	1	0	COM42
DB2	1	1	1	1	1	1	1	1	1	0	0	0	1	0	1	0	0	…	0	1	1	0	0	COM43
DB3	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	0	…	0	0	0	1	0	COM44
DB4	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	…	0	0	0	0	1	COM45
DB5	0	1	1	1	1	1	1	1	0	0	1	1	0	0	0	1	1	…	1	0	0	0	1	COM46
DB6	0	0	1	1	1	1	1	0	0	0	1	1	1	0	1	1	1	…	0	1	1	1	0	COM47
DB7	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	0	…	0	0	0	0	0	COM48
Address SGS="0"	300	301	302	303	304	305	306	307	308	309	30A	30B	30C	30D	30E	30F	310	…	364	365	366	367	368	(HEX)
Address SGS="1"	368	367	366	365	364	363	362	361	360	35F	35E	35D	35C	35B	35A	359	358	…	304	303	302	301	300	
DB0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1		…	1	1	1	1	1	COM49
DB1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	…	1	0	0	0	0	COM50
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
DB7	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	…	0	0	0	0	0	COM56
Address SGS="0"	380	381	382	383	384	385	386	387	388	389	38A	38B	38C	38D	38E	38F	390	…	3E4	3E5	3E6	3E7	3E8	(HEX)
Address SGS="1"	3E8	3E7	3E6	3E5	3E4	3E3	3E2	3E1	3E0	3DF	3DE	3DD	3DC	3DB	3DA	3D9	3D8	…	384	383	382	381	380	
DB0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1		…	0	0	1	0	0	COM57
DB1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	…	0	1	1	0	0	COM58
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
DB7	0	0	0	0	1	1	1	0	0	0	0	1	1	1	1	1	0	…	0	0	0	0	0	COM64
Address SGS="0"	400	401	402	403	404	405	406	407	408	409	40A	40B	40C	40D	40E	40F	410	…	464	465	466	467	468	(HEX)
Address SGS="1"	468	467	466	465	464	463	462	461	460	45F	45E	45D	45C	45B	45A	459	458	…	404	403	402	401	400	
DB0	0	1	1	0	0	0	1	1	0	0	0	1	1	1	1	1		…	0	1	1	1	0	COM65
DB1	1	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1	…	1	0	0	0	1	COM66
DB2	1	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1	…	1	0	0	0	1	COM67
DB3	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	0	…	0	0	0	0	0	COM68
DB4 – DB7	Displayed by horizontal scrolling.*3																							
Address SGS="0"	480	481	482	483	484	485	486	487	488	489	48A	48B	48C	48D	48E	48F	490	…	4E4	4E5	4E6	4E7	4E8	(HEX)
Address SGS="1"	4E8	4E7	4E6	4E5	4E4	4E3	4E2	4E1	4E0	4DF	4DE	4DD	4DC	4DB	4DA	4D9	4D8	…	484	483	482	481	480	
DB0 – DB7	Displayed by horizontal scrolling.*3																							

Notes: 1. A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).
2. Addresses x69H–x6FH and xE9H–xEF exist but have no meanings for display.
3. Lower 12-raster-row display areas are displayed by horizontal scrolling.

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66729 can be controlled by the MPU. Before starting internal operation of the HD66729, control information is temporarily stored in these registers to allow interfacing with various peripheral control devices or MPUs which operate at different speeds. The internal operation of the HD66729 is determined by signals sent from the MPU. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signal (DB0 to DB7), make up the HD66729 instructions. There are four categories of instructions that:

- Control the display
- Control power management
- Set internal CGRAM addresses
- Transfer data with the internal CGRAM

Normally, instructions that perform data transfer with the internal CGRAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66729 CGRAM addresses after each data write can lighten the MPU program load.

Because instructions are executed in 0 cycle, instructions can be written in succession.

Instruction Descriptions

Start Oscillation

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**

Figure 2 Start Oscillation Instruction

Driver Output Control

CMS: Selects the output shift direction of a common driver. When CMS = 0, COM1/64 shifts to COM1, and COM64/1 to COM64. When CMS = 1, COM1/64 shifts to COM64, and COM64/1 to COM1. Output position of a common driver shifts depending on the CN1–0 bit setting. For details, see the Display Line Control section.

SGS: Selects the output shift direction of a segment driver. When SGS = 0, SEG1/105 shifts to SEG1, and SEG105/1 to SEG105. When SGS = 1, SEG1/105 shifts SEG105, and SEG105/1 to SEG1.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**1**	**CMS**	**SGS**

Figure 3 Driver Output Control Instruction

Power Control

AMP: When AMP = 1, each voltage follower for V1 to V5 pins and the booster are turned on. When AMP = 0, current consumption can be reduced while the display is not being used.

SLP: When SLP = 1, the HD66729 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. For details, see the Sleep Mode section. Only the power control instructions (AMP, SLP, and STB bits) can be executed during the sleep mode.

During the sleep mode, the other CGRAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66729 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)
b. Voltage follower circuit on/off (AMP = 1/0)
c. Start oscillation

During the standby mode, the CGRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**1**	**AMP**	**SLP**	**STB**

Figure 4 Power Control Instruction

Contrast Control 1/2

SW: Switches the bit configuration for the contrast control instruction.

CT4–CT0: When SW = 0, they control the LCD drive voltage (potential difference between V1 and GND) to adjust contrast. A 64-step adjustment is also possible by using the CT5 bit which are set in the entry mode register. For details, see the Contrast Adjuster section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	1	0	SW	CT4	CT3	(SW = 0)
								BT1	BT0	(SW = 1)
0	0	0	0	0	1	1	CT2	CT1	CT0	(SW = 0)
							BS2	BS1	BS0	(SW = 1)

Figure 5 Contrast-Control 1/2 Instruction

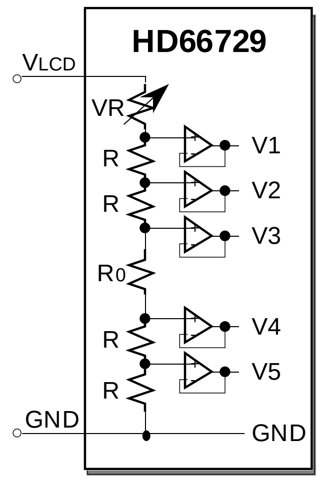


Figure 6 Contrast Adjuster

Table 6 CT Bits and Variable Resistor Value of Contrast Adjuster

CT Set Value						
CT5	CT4	CT3	CT2	CT1	CT0	Variable Resistor (VR)
0	0	0	0	0	0	3.20 x R
0	0	0	0	0	1	3.15 x R
0	0	0	0	1	0	3.10 x R
0	0	0	0	1	1	3.05 x R
0	0	0	1	0	0	3.00 x R
			•			•
			•			•
0	1	1	1	1	1	1.65 x R
1	0	0	0	0	0	1.60 x R
1	0	0	0	0	1	1.55 x R
1	0	0	0	1	0	1.50 x R
			•			•
			•			•
1	1	1	1	0	1	0.15 x R
1	1	1	1	1	0	0.10 x R
1	1	1	1	1	1	0.05 x R

BT1-0: When SW = 1, they switch the output of V5OUT between double, triple, quadruple, and quintuple boost. The liquid crystal display drive voltage level can be selected according to its drive duty ratio and bias. A lower amplification of the booster consumes less current.

BS2-0: When SW = 1, they set the crystal display drive bias value within the range of 1/4 to 1/9 bias. The liquid crystal display drive bias value can be selected according to its drive duty ratio and voltage. For details, see the Liquid Crystal Display Drive Bias Selector section.

Table 7 BT Bits and Output Level

BT1	BT0	V5OUT Output Level
0	0	Triple boost
0	1	Quadruple boost
1	0	Quintuple boost
1	1	Double boost

Table 8 BS Bits and LCD Drive Bias Value

BS2	BS1	BS0	Liquid Crystal Display Drive Bias Value
0	0	0	Setting inhibited
0	0	1	Setting inhibited
0	1	0	1/9 bias drive
0	1	1	1/8 bias drive
1	0	0	1/7 bias drive
1	0	1	1/6 bias drive
1	1	0	1/5 bias drive
1	1	1	1/4 bias drive

Entry Mode

After power-on reset, ensure the setting. Since the DB0 bit is the test bit, set DB0 when SW = 0, and clear DB0 when SW = 1.

REV: Displays all character and graphics display sections with black-and-white reversal when SW = 0 and REV = 1. For details, see the Reversed Display Function section.

I/D: When SW = 0, increments (I/D = 1) or decrements (I/D = 0) the CGRAM address by 1 when data is written into or read from the CGRAM.

CT5: Sets the most significant bit (CT5) for contrast adjustment when SW = 1. A 64-step adjustment is also possible by using the CT4–CT0 bits which are set in the contrast-control 1/2 instruction.

RDM: When SW = 1 and RDM = 0, the RDM increments or decrements the address counter value according to the I/D bit setting after reading the data from the CGRAM. When RDM = 1, the address counter value is not updated after the data has been read from the CGRAM. The address counter value is used when the RAM data is read, modified, and written. Since the first read data is invalid, the read must be continuously done twice. After writing to the CGRAM, the address counter value must be updated.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	0	0	REV	I/D	1	(SW = 0)
							CT5	RDM	0	(SW = 1)

Figure 7 Entry Mode Set Instruction

Display On/Off Control

D: Display is on when SW = 0 and D = 1 and off when D = 0. When off, the display data remains in the CGRAM, and can be displayed instantly by setting D = 1. When D is 0, the display is off with the SEG1 to SEG105 outputs and COM1 to COM68 outputs set to the GND level. Because of this, the HD66729 can control charging current for the LCD with AC driving.

DL10: When SW = 0, DL10 can be set. When DL10 = 1, the 10th line is displayed at double height.

DL9–DL7: When SW = 1, DL9–DL7 can be set. Double-height display is specified for any display line. When DL7 = 1, the seventh line is displayed at double height. Double-height display is used for the eighth line when DL8 = 1 and for the ninth line when DL9 = 1. For double-height display for the first to the sixth lines, control them by using DL1–DL6 bits in the display-line control instruction.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**0**	**1**	**1**	**0**	**D**	**DL10**	**0**	(SW = 0)
							DL9	**DL8**	**DL7**	(SW = 1)

Figure 8 Display On/Off Control Instruction

Display Line Control

NL3-0: Set NL2–NL0 bits when SW = 0, and the NL3 bit when SW = 1 to specify the display lines. A line consists of 8 dots. Display lines change the liquid crystal display drive duty ratio. CGRAM address mapping does not depend on the number of display lines.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**0**	**1**	**1**	**1**	**NL2**	**NL1**	**NL0**	(SW = 0)
							0	**CN**	**NL3**	(SW = 1)

Figure 9 Display-line Control Instruction

Table 9 NL Bits and Display Lines

NL3	NL2	NL1	NL0	Display Size	LCD Drive Duty	Common Driver Used
0	0	0	0	105 x 8 dots	1/8 Duty	COM1–COM8
0	0	0	1	105 x 16 dots	1/16 Duty	COM1–COM16
0	0	1	0	105 x 24 dots	1/24 Duty	COM1–COM24
0	0	1	1	105 x 32 dots	1/32 Duty	COM1–COM32
0	1	0	0	105 x 40 dots	1/40 Duty	COM1–COM40
0	1	0	1	105 x 48 dots	1/48 Duty	COM1–COM48
0	1	1	0	105 x 56 dots	1/56 Duty	COM1–COM56
0	1	1	1	105 x 64 dots	1/64 Duty	COM1–COM64
1	0	0	0	105 x 68 dots	1/68 Duty	COM1–COM68

CN: Set CN bit when SW = 1. If CN = 1, the display position is shifted down by 16 dots (two lines) and display starts from COM17. If the liquid crystal is driven at a low-duty ratio in the system wait state, there is a partial display at the center of the screen (centering display). If CN = 1, the LCD-drive duty ratio must be 1/48 or less (NL3–0 = 0000–0101). For details, see the Partial-display-on Function section.

Table 10 Common Driver Pin Function

Common Driver Pin	Common Driver Pin Function			
	CN = 0 (Normal Output)		CN = 1 (Center Output)	
	CMS = 0	CMS = 1	CMS = 0	CMS = 1
COM1/64	**COM1**	COM64	Non-selected	COM48
COM2/63	COM2	COM63	Non-selected	COM47
:	:	:	:	:
COM7/58	COM7	COM58	Non-selected	COM42
COM8/57	COM8	COM57	Non-selected	COM41
COM9/56	COM9	COM56	Non-selected	COM40
COM10/55	COM10	COM55	Non-selected	COM39
:	:	:	:	:
COM15/50	COM15	COM50	Non-selected	COM34
COM16/49	COM16	COM49	Non-selected	COM33
COM17/48	COM17	COM48	**COM1**	COM32
COM18/47	COM18	COM47	COM2	COM31
:	:	:	:	:
COM24/41	COM24	COM41	COM8	COM25
COM25/40	COM25	COM40	COM9	COM24
:	:	:	:	:
COM32/33	COM32	COM33	COM16	COM17
COM33/32	COM33	COM32	COM17	COM16
:	:	:	:	:
COM40/25	COM40	COM25	COM24	COM9
COM41/24	COM41	COM24	COM25	COM8
:	:	:	:	:
COM48/17	COM48	COM17	COM32	**COM1**
COM49/16	COM49	COM16	COM33	Non-selected
:	:	:	:	:
COM56/9	COM56	COM9	COM40	Non-selected
COM57/8	COM57	COM8	COM41	Non-selected
:	:	:	:	:
COM64/1	COM64	COM1	COM48	Non-selected
COM65/68	COM65	COM68	Non-selected	Non-selected
COM66/67	COM66	COM67	Non-selected	Non-selected
COM67/66	COM67	COM66	Non-selected	Non-selected
COM68/65	COM68	COM65	Non-selected	Non-selected

Note: When the display is centered (CN = 1), the LCD-drive duty ratio must be set to 1/48 or less.

Double-height Display Control

DL3-1: Can be specified when SW = 0. Specify the double-height display for any line. When DL1 = 1, the first line (8 dots) is displayed as 16 dots at double height. When DL2 = 1, the second line is displayed at double height. When DL3 = 1, the third line is displayed at double height. Double-height display of multiple lines is possible. For details, see the Double-height Display section.

DL6-4: Can be specified when SW = 1. Specify the double-height display for any line. When DL4 = 1, the fourth line (8 dots) is displayed at double height. When DL5 = 1, the fifth line is displayed at double height. When DL6 = 1, the sixth line is displayed at double height. For the seventh to 10th lines, control double-height display by using the DL7–DL10 bits in the display-line control instruction.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**1**	**0**	**0**	**0**	**DL3**	**DL2**	**DL1**	(SW = 0)
							DL6	**DL5**	**DL4**	(SW = 1)

Figure 10 Double-height Display Control Instruction

Vertical Scroll Control 1/2

SN3-0: Set SN2 to SN0 bits when SW = 0. Set the SN3 bit when SW = 1. Specify the display start line output from COM1. Because the CGRAM is assigned a 10-line display area in which a line consists of 8 dots, the data is displayed sequentially from the first line to the 10th line then repeated from the first line again. In partial smooth scrolling, these bits specify the display start line for the next line of the fixed-display line. For details, see the Partial Smooth Scroll Display Function section.

SL2–0: Select the top raster-row to be displayed (display-start raster-row) in the display-start line specified by SN2 to SN0. Any raster-row from the first to eighth can be selected (table 12). This function is used to achieve vertical smooth scrolling together with SN2 to SN0. For details, see the Vertical Smooth Scroll section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**1**	**0**	**0**	**1**	**SN2**	**SN1**	**SN0**	(SW = 0)
							<0>	**<0>**	**SN3**	(SW = 1)
0	0	**0**	**1**	**0**	**1**	**0**	**SL2**	**SL1**	**SL0**	(SW = 0)
							<0>	**PS1**	**PS0**	(SW = 1)

Figure 11 Vertical Scroll Control 1/2 Instruction

Table 11 SN Bits and Display-start Lines

SN3	SN2	SN1	SN0	Display-start Line
0	0	0	0	1st line
0	0	0	1	2nd line
0	0	1	0	3rd line
0	0	1	1	4th line
0	1	0	0	5th line
0	1	0	1	6th line
0	1	1	0	7th line
0	1	1	1	8th line
1	0	0	0	9th line
1	0	0	1	10th line

Table 12 SL Bits and Display-start Raster-row

SL2	SL1	SL0	Display-start Raster-row
0	0	0	1st raster-row
0	0	1	2nd raster-row
0	1	0	3rd raster-row
0	1	1	4th raster-row
1	0	0	5th raster-row
1	0	1	6th raster-row
1	1	0	7th raster-row
1	1	1	8th raster-row

PS1–0: Specify PS1 to PS0 bits when SW = 1. When PS1–0 = 01, only the first line is fixed-displayed in vertical smooth scrolling, and the other display lines are smooth-scrolled. When PS1–0 = 10, the first and second lines are fixed-displayed. When PS1–0 = 11, the first to third lines are fixed-displayed. For details, see the Partial Smooth Scroll Display Function section.

Booster Control

B/C: When SW = 1 and B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD driving. When B/C = 1, a C-pattern waveform is generated and alternates (n-raster-row reversed AC drive) in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

DCC: When SW = 1 and DCC = 0, a booster operates with the 64-divided clock of the operating frequency. When DCC = 1, the booster operates with the 32-divided clock. When the booster operates with the 64-divided clock, current consumption in the booster is low, but boosting ability is weak.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	1	1	0	0	0	0	(SW = 0)
							<0>	DCC	B/C	(SW = 1)

Figure 12 Booster Control Instruction

LCD-Driving-Waveform Control

EOR: When the C-pattern waveform is set (B/C = 1) and SW = 1 and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW4–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW4–NW0 alternate in every set value + 1 raster-row, and the first to the 32nd raster-rows can be selected. When SW = 0, bits NW2, NW1, and NW0 can be set. When SW = 1, bits NW4 and NW3 can be set.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	1	1	1	NW2	NW1	NW0	(SW = 0)
							EOR	NW4	NW3	(SW = 1)

Figure 13 LCD-Driving-Waveform Control Instruction

RAM Address Set

AD10-0: Initially set CGRAM addresses to the address counter (AC). Once the CGRAM data is written, the AC is automatically updated according to the I/D bit. This allows consecutive accesses without resetting addresses. Once the CGRAM data is read, the AC is automatically updated according to the I/D bit when RDM = 0, and not updated when RDM = 1. Set RDM to 1 when read, modify, and write are done in every one-byte data.

Addresses “*69”H–“*6F”H and “*E9”H–“*EF”H in the CGRAM area exist but do not appear in the display.

CGRAM address setting is not allowed in the sleep mode or standby mode.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**1**	**0**	**1**	**AD10**	**AD9**	**AD8**	**AD7**	**AD6**
0	0	**1**	**1**	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**

Figure 14 RAM Address Set Instruction

Table 13 AD Bits and CGRAM Settings

RM	AD10–AD0	CGRAM Setting
1	"000"H–"06F"H	Display data for COM1 to COM8
1	"080"H–"0EF"H	Display data for COM9 to COM16
1	"100"H–"16F"H	Display data for COM17 to COM24
1	"180"H–"1EF"H	Display data for COM25 to COM32
1	"200"H–"26F"H	Display data for COM33 to COM40
1	"280"H–"2EF"H	Display data for COM41 to COM48
1	"300"H–"36F"H	Display data for COM49 to COM56
1	"380"H–"3EF"H	Display data for COM57 to COM64
1	"400"H–"46F"H	Display data for COM65 to COM68
1	"480"H–"4EF"H	Displayed by upward scrolling

Write Data to CGRAM

WD7-0 : Write 8-bit data to the CGRAM. After a write, the address is automatically incremented or decremented by 1 according to the I/D bit setting. During the sleep and standby modes, the CGRAM cannot be accessed.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	**WD7**	**WD6**	**WD5**	**WD4**	**WD3**	**WD2**	**WD1**	**WD0**

Figure 15 Write Data to CGRAM Instruction

Read Data from CGRAM

RD7-0 : Read 8-bit data from the CGRAM. In the parallel bus interface mode, the first-byte data read will be invalid immediately after the CGRAM address set, and the consecutive second-byte data will be read normally. In the serial interface mode, two bytes will be invalid immediately after the start byte, and the consecutive third-byte data will be read normally. For details, see the Serial Data Transfer section.

After a CGRAM read, when RDM = 0, the address is automatically incremented or decremented by 1 according to the I/D bit. When RDM = 1, the address is not updated.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	**RD7**	**RD6**	**RD5**	**RD4**	**RD3**	**RD2**	**RD1**	**RD0**

Figure 16 Read Data from CGRAM Instruction

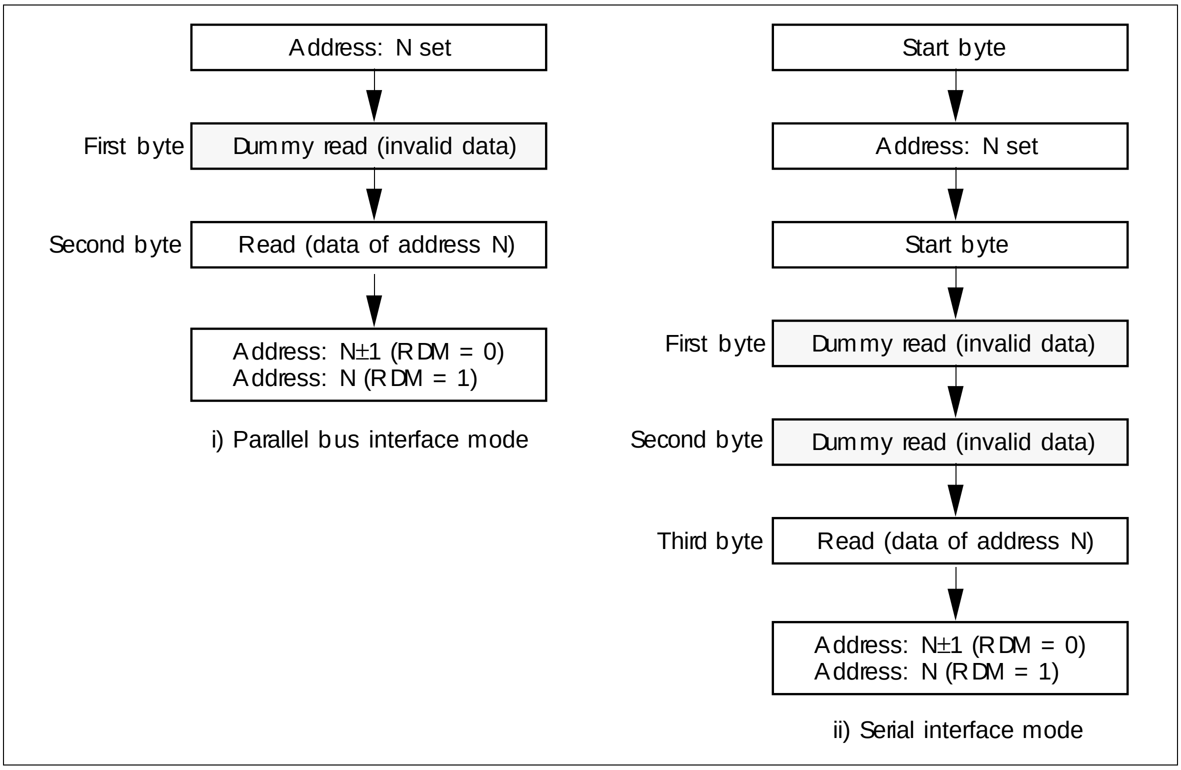


Figure 17 CGRAM Read Sequence

Table 14 Instruction List

Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
Start oscillation	0	0	0	0	0	0	0	0	1	1	Starts the oscillation standby mode.	—
Driver output control	0	0	0	0	0	0	0	1	CMS	SGS	Selects the common driver shift direction (CMS) and segment driver shift direction (SGS).	0
Power control	0	0	0	0	0	0	1	AMP	SLP	STB	Turns on LCD power supply (AMP), and sets the sleep mode (SLP) and standby mode (STB).	0
Contrast control 1	0	0	0	0	0	1	0	SW	CT4	CT3	Sets the register selection (SW) or upper contrast adjustment bits (CT4-3).	0
									BT1	BT0	Sets the register selection (SW) or boost level (BT1/0).	0
Contrast control 2	0	0	0	0	0	1	1	CT2	CT1	CT0	Sets the lower contrast adjustment bits (CT2-0).	0
								BS2	BS1	BS0	Sets the LCD bias value (BS2-0).	0
Entry mode set	0	0	0	0	1	0	0	REV	I/D	1	Sets the black-and-white reversal (REV) or address update direction after RAM access (I/D).	0
								CT5	RDM	0	Sets the higher contrast adjustment bit (CT5) or read, modify, write (RDM).	0
Display on/off control	0	0	0	0	1	1	0	D	DL10	0	Sets display on (D) or double-height display line (DL10).	0
								DL9	DL8	DL7	Specifies double-height display lines (DL9–DL7).	0
Display line control	0	0	0	0	1	1	1	NL2	NL1	NL0	Sets the number of display lines (NL2-0).	0
								0	CN	NL3	Specifies centering (CN) or the number of display lines (NL3).	0
Double-height display control	0	0	0	1	0	0	0	DL3	DL2	DL1	Specifies double-height display lines (DL3-1).	0
								DL6	DL5	DL4	Specifies double-height display lines (DL6–4).	0

Table 14 Instruction List (cont)

Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
Vertical scroll control 1	0	0	0	1	0	0	1	SN2	SN1	SN0	Sets the display-start line (SN2-0).	0
								<0>	<0>	SN3	Sets the display-start line (SN3).	0
Vertical scroll control 2	0	0	0	1	0	1	0	SL2	SL1	SL0	Sets the display-start raster-row (SL2-0).	0
								<0>	PS1	PS0	Sets the partial scroll (PS1–0).	0
Booster control	0	0	0	1	1	1	0	0	0	0	NOP.	0
								<0>	DCC	B/C	Selects the boosting cycle (DCC) or LCD drive AC waveform (B/C).	0
LCD-driving-waveform control	0	0	0	1	1	1	1	NW2	NW1	NW0	Sets the number of n-raster-rows (NW2–0) in C-pattern AC drive.	0
								EOR	NW4	NW3	Sets the EOR output (EOR) or the number of n-raster-rows (NW4–3) in C-pattern AC drive.	0
RAM address set (upper bits)	0	0	1	0	1	AD10–6 (upper bits)					Initially sets the upper addresses of the CGRAM to the address counter (AC).	0
RAM address set (lower bits)	0	0	1	1	AD5-0 (lower bits)						Initially sets the lower addresses of the CGRAM to the AC.	0
Write data to RAM	0	1	Write data								Writes data to CGRAM.	0
Read data from RAM	1	1	Read data								Reads data from CGRAM.	0

Note: The upper column of each register can be set when SW = 0. The lower column can be set when SW = 1.

Bit definition:

CMS = 0: COM1/64 => COM1

SGS = 0: SEG1/105 => SEG1

AMP = 1: Operational amplifier and booster circuit on

SLP = 1: Sleep mode

STB = 1: Standby mode

SW = 0: Upper register setting

SW = 1: Lower register setting

CT5-0: Contrast adjustment

BT1/0: Boost level selection (00: Triple, 01: Quadruple, 10: Quintuple, 11: Double)

BS2-0: LCD drive bias selection

REV = 0: Normal display

REV = 1: Black-and-white reversed display of the graphics display

ID = 1: Address increment

ID = 0: Address decrement

RDM = 1: Read, modify, and write mode (Not automatically update the address counter after reading)

D = 1: Display on

NL3-0: Display line setting (0000: 1/8 duty ratio, 0001: 1/16 duty ratio, 0010: 1/24 duty ratio, 0011: 1/32 duty ratio, 0100: 1/40 duty ratio, 0101: 1/48 duty ratio, 0110: 1/56 duty ratio, 0111: 1/64 duty ratio, 1000: 1/68 duty ratio)

DL1-10: Double-height line specifications (DL1: 1st line, DL2: 2nd line, ..., DL10: 10th line)

SN3-0: Display-start line (0000: 1st line, 0001: 2nd line, 0010: 3rd line, 0011: 4th line, 0100: 5th line, 0101: 6th line, 0110: 7th line, 0111: 8th line, 1000: 9th line, 1001: 10th line)

SL2-0: Display-start raster-row specifications (000: 1st raster-row...111: 8th raster-row)

CN = 1: Centering specifications (LCD driving started at COM17)

B/C = 0: B-pattern waveform drive

B/C = 1: C-pattern waveform drive

EOR = 1: EOR alternating drive at C-pattern waveform

NW4–0: Reversed number of n raster-rows at C-pattern waveform drive (alternating with the set value + one raster-row)

DCC = 0: Boosted at 1/64-divided clock

DCC = 1: Boosted at 1/32-divided clock

ADD10-0: CGRAM address set (000H–4EFH)

Reset Function

The HD66729 is internally initialized by RESET input. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period and the 1000-clock cycle period following reset cancellation, no instruction or CGRAM data access from the MPU is accepted. Any initializing instruction must wait for 1,000 clock cycles after the reset is canceled so that internal busy status can be completed. The reset input must be held for at least 1 ms.

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (SGS = 0, CMS = 0)
3. Power control (AMP = 0: LCD power off, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
4. Triple boost (BT1/0 = 00), 1/10 bias drive (BS2/1/0 = 000), Weak contrast (CT5-0 = 00000)
5. Entry mode set (REV = 0: Normal display, I/D = 1: Increment by 1, RDM = 0: Automatically update after reading)
6. Display on/off control (D = 0: Display off, CEN = 0: Normal position)
7. Display line control (NL3/2/1/0 = 1001: 1/80 duty ratio)
8. Double-height display off (DL10–1 = 0000000000)
9. Vertical scroll control (SN3/2/1/0 = 0000: First line displayed at the top, SL2/1/0: First raster-row displayed at the top of the first line, PS1/0 = 00: Partial scroll off)
10. 1/64-divided clock boost (DCC = 0)
11. B-pattern waveform AC drive (B/C = 0, EOR = 0, NW4/3/2/1/0 = 00000)

CGRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D = 0).

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Outputs GND level
2. Booster output pins (VLOUT): Outputs Vcc level
3. Oscillator output pin (OSC2): Outputs oscillation signal

Serial Data Transfer

Setting the IM1 and IM2 pins (interface mode pins) to the GND level allows standard clock-synchronized serial data transfer, using the chip select line (CS*), serial data line (SDA), and serial transfer clock line (SCL). For a serial interface, the IM0/ID pin function uses an ID pin.

The HD66729 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66729 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66729. The HD66729, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66729 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, an instruction can be issued, and when RS = 1, data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit) as shown in table 26.

After receiving the start byte, the HD66729 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. To transfer data consecutively, note that only the display-clear instruction requires a longer execution time than the others (see table 24, Instruction List).

Two bytes of CGRAM read data after the start byte are invalid. The HD66729 starts to read correct CGRAM data from the third byte.

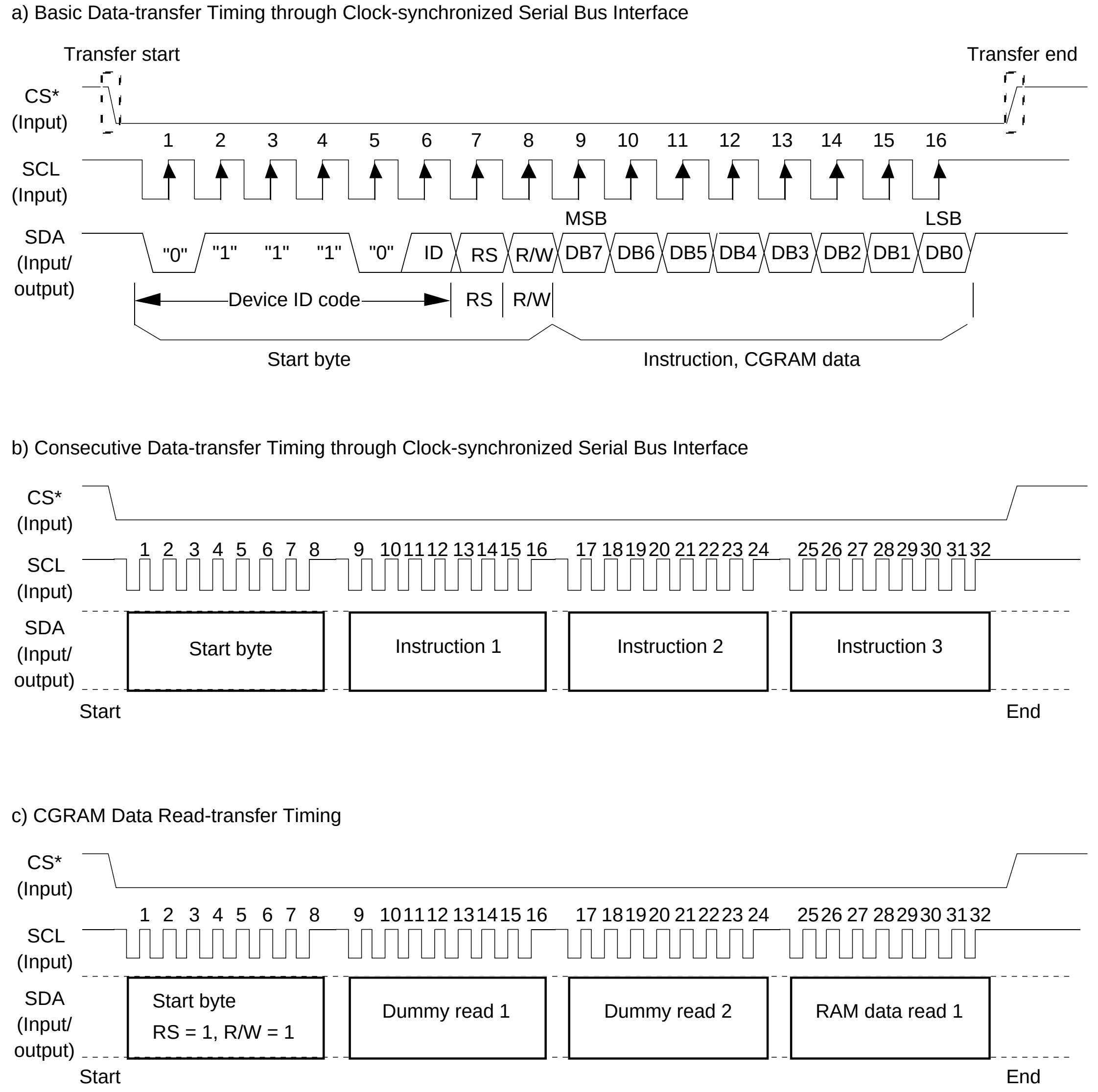
Table 15 Start Byte Format

Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

Table 16 RS and R/W Bit Function

RS	R/W	Function
0	0	Writes instruction
0	1	Invalid
1	0	Writes RAM data
1	1	Reads RAM data



Note: Two bytes of the RAM read data after the start byte are invalid. The HD66729 starts to read the correct RAM data from the third byte.

Figure 18 Clock-synchronized Serial Interface Timing Sequence

Parallel Data Transfer

8-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/Vcc/GND level allows E-clock-synchronized 68-system 8-bit parallel data transfer. Setting the IM2/1/0 (interface mode) to the Vcc/Vcc/GND level allows 80-system 8-bit parallel data transfer. When the number of buses or the mounting area is limited, use a 4-bit bus interface or serial data transfer.

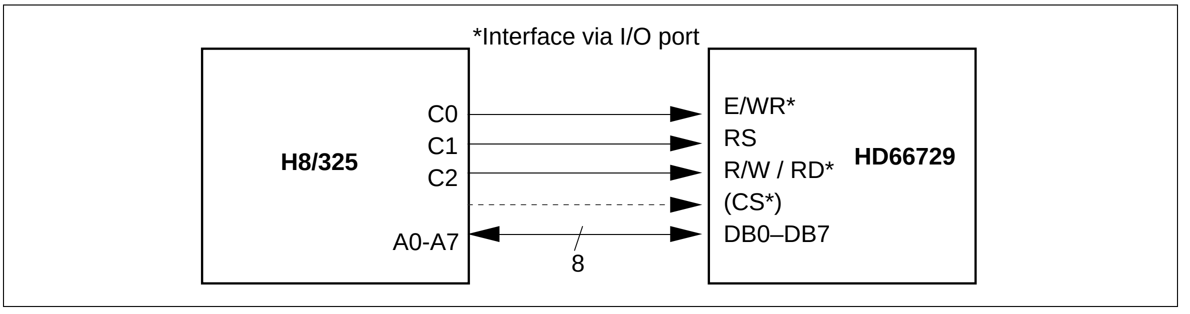


Figure 19 Interface to 8-bit Microcomputer

4-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/Vcc/Vcc level allows E-clock-synchronized 68-system 4-bit parallel data transfer using pins DB7-DB4. Setting the IM2/1/0 (interface mode) to the Vcc/Vcc/Vcc level allows 80-system 4-bit parallel data transfer. The 8-bit instructions and RAM data are divided into four upper/lower bits and the transfer starts from the upper four bits.

Note: Transfer synchronization function for a 4-bit bus interface
The HD66729 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 4-bit data transfer in the 4-bit bus interface. Noise causing transfer mismatch between the four upper and lower bits can be corrected by a reset triggered by consecutively writing a 0000 instruction four times. The next transfer starts from the upper four bits. Executing synchronization function periodically can recover any runaway in the display system.
When the 4-bit synchronization function is executed, the blink synchronization is executed simultaneously.

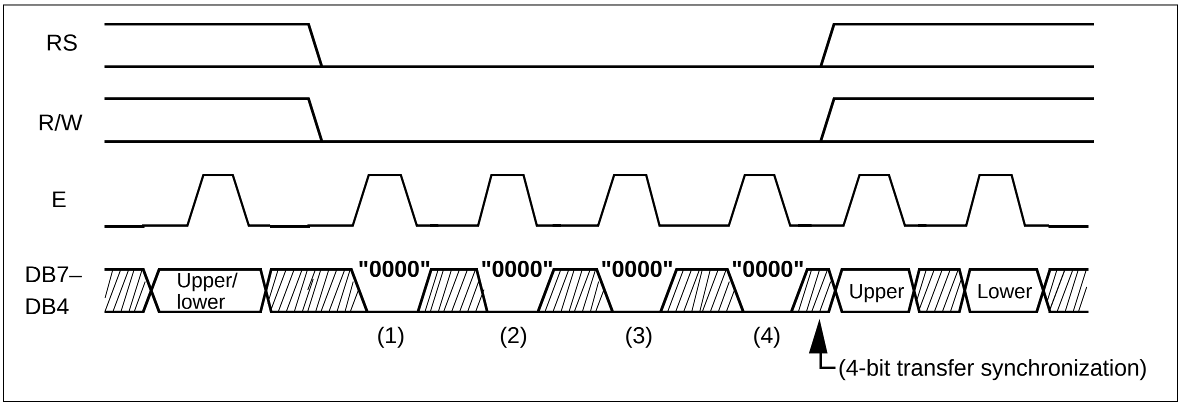


Figure 20 4-bit Transfer Synchronization

Oscillation Circuit

The HD66729 can either be supplied with operating pulses externally (external clock mode) or oscillate using an internal R-C oscillator with an external oscillator-resistor (external resistor oscillation mode). Note that in R-C oscillation, the oscillation frequency is changed according to the internal capacitance value, the external resistance value, or operating power-supply voltage. Insert the dumping resistance of about 2 kΩ to prevent malfunctions caused by over-shoot or under-shoot noise in the external clock mode.

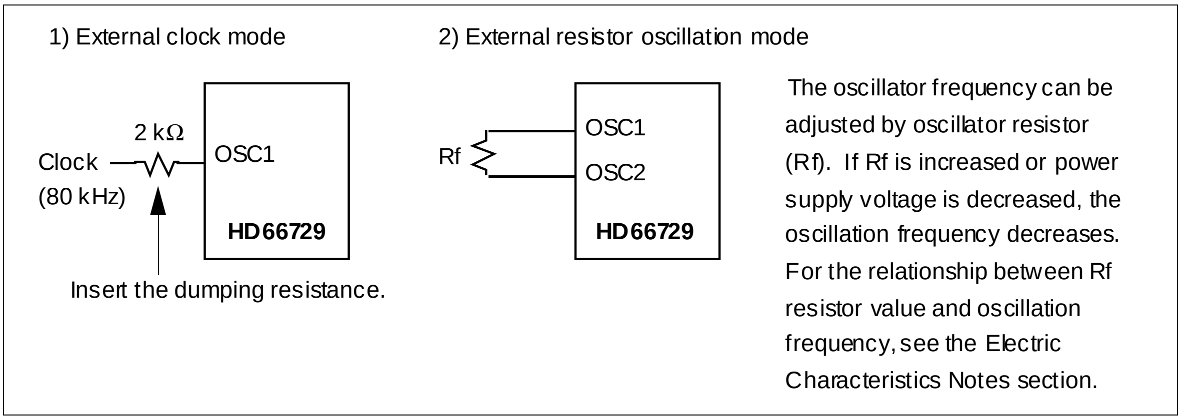


Figure 21 Oscillation Circuits

Table 17 Relationship between Drive Duty Ratio and Frame Frequency (fosc = 75 kHz)

	Display mode								
	1-line Display	**2-line Display**	**3-line Display**	**4-line Display**	**5-line Display**	**6-line Display**	**7-line Display**	**8-line Display**	**8.5-line Display**
	Set value for NL3–0								
LCD Drive	**0000**	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**	**0111**	**1000**
Multiplexing duty ratio	1/8	1/16	1/24	1/32	1/40	1/48	1/56	1/64	1/68
Drive bias (recommended value)	1/4	1/5	1/6	1/6	1/7	1/8	1/8	1/9	1/9
Frame frequency	73 Hz	73 Hz	73 Hz	73 Hz	72 Hz	74 Hz	74 Hz	73 Hz	69 Hz
One-frame frequency	1,024	1,024	1,032	1,024	1,040	1,008	1,008	1,024	1,088

Note: If the frame frequency is low and the display flickers, increase the oscillation frequency (fosc).

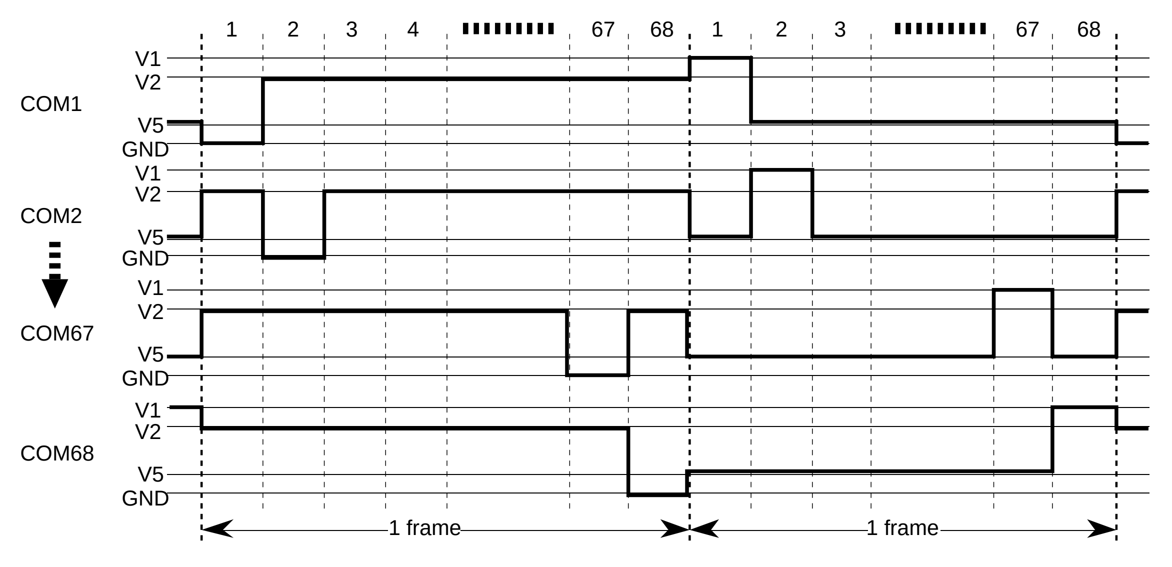
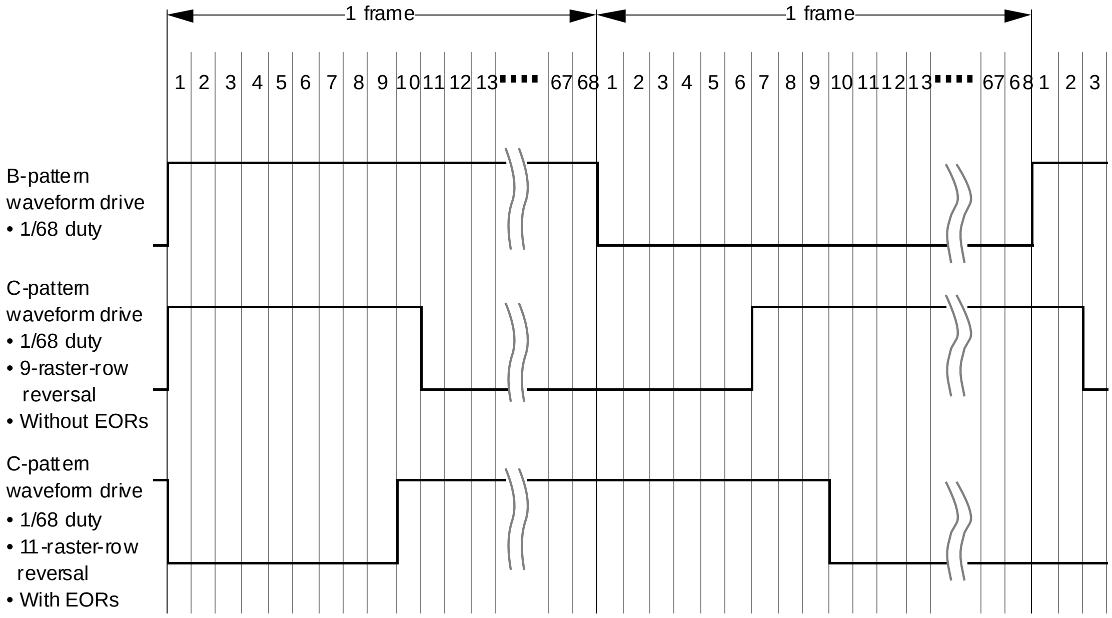


Figure 22 LCD Drive Output Waveform (B-pattern AC Drive with 1/68 Multiplexing Duty Ratio)

n-raster-row Reversed AC Drive

The HD66729 supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 32 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as crosstalk at high-duty driving of more than six lines (1/48 duty), the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality. Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.



Note: Specify the number of AC drive raster-rows and the necessity of EOR so that the DC bias is not generated for the liquid crystal.

Figure 23 Example of an AC Signal under n-raster-row Reversed AC Drive

Liquid Crystal Display Voltage Generator

When External Power Supply and Internal Operational Amplifiers are Used

To supply LCD drive voltage directly from the external power supply without using the internal booster, circuits should be connected as shown in figure 24. Here, contrast can be adjusted by software through the CT bits of the contrast adjustment register.

The HD66729 incorporates a voltage-follower operational amplifier for each V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, potential difference between V_{LCD} and V1 must be 0.1 V or higher, and that between V4 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.1 µF to 0.47 µF between each internal operational amplifier V1OUT to V5OUT output and GND and stabilize the output level of the operational amplifier.

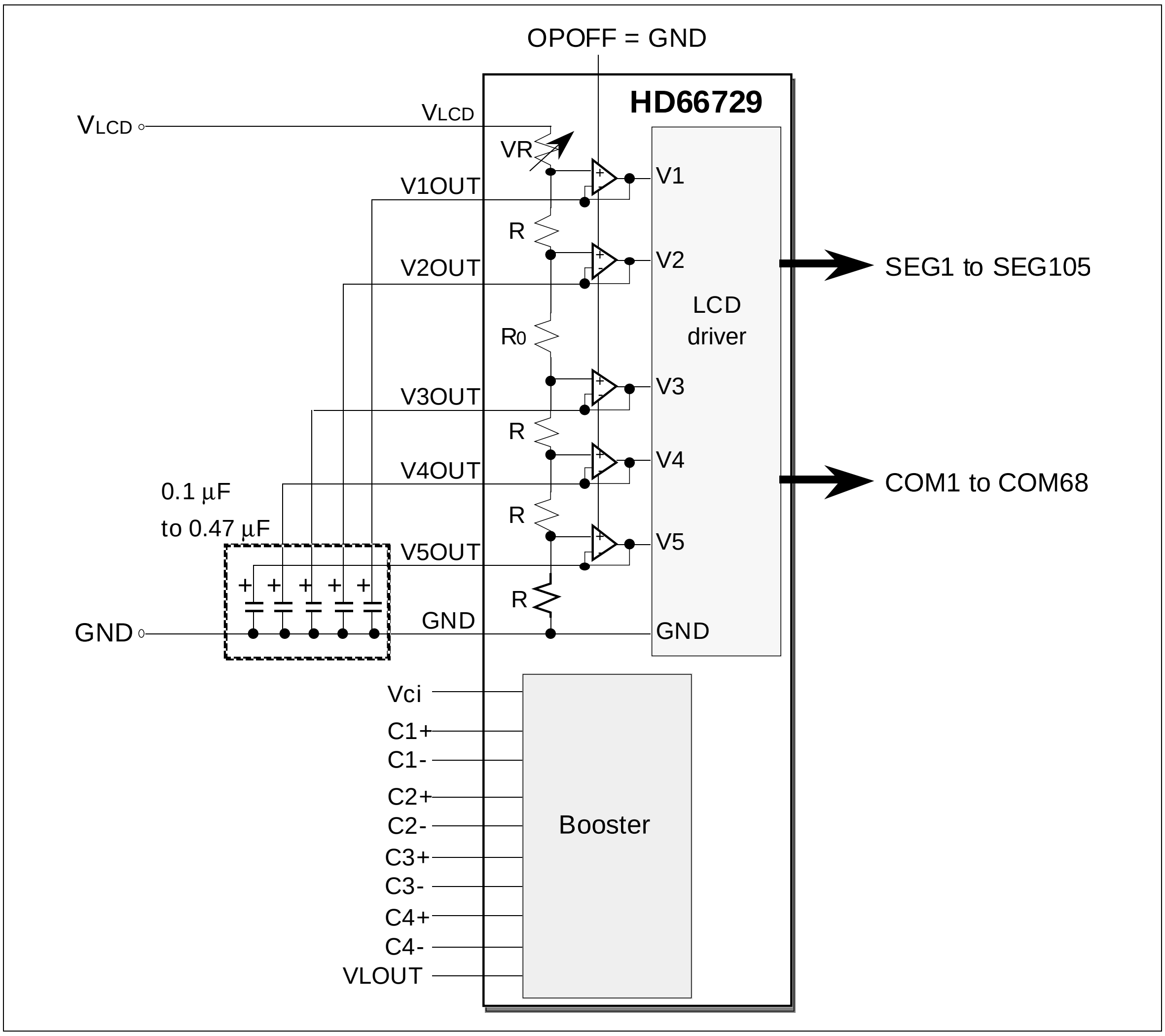


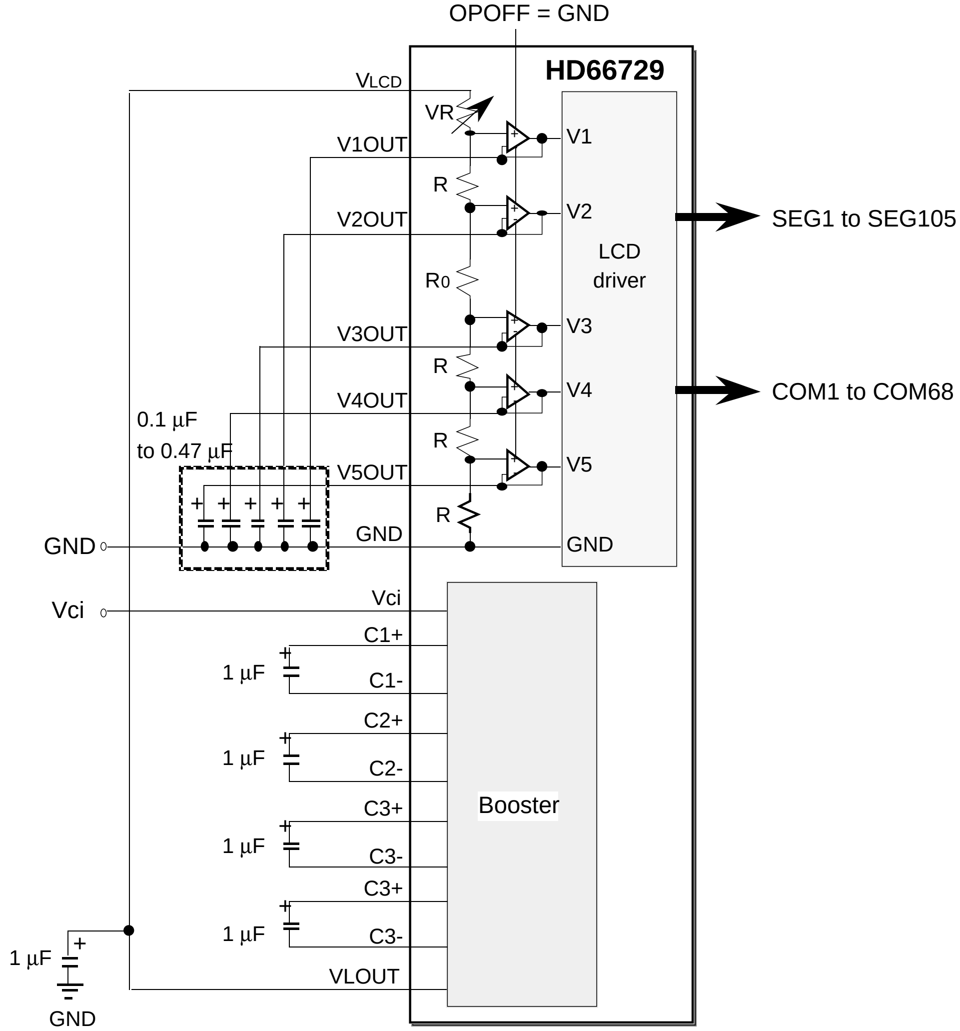
Figure 24 External Power Supply Circuit for LCD Drive Voltage Generation

When an Internal Booster and Internal Operational Amplifiers are Used

To supply LCD drive voltage using the internal booster, circuits should be connected as shown in figure 25. Here, contrast can be adjusted through the CT bits of the contrast control instruction. Temperature can be compensated either through the CT bits or by controlling the reference voltage for the booster (Vci pin) using a thermistor.

Note that Vci is both a reference voltage and power supply for the booster. The reference voltage must therefore be adjusted using an emitter-follower or a similar element so that sufficient current can be supplied. In this case, Vci must be equal to or smaller than the V_{CC} level.

The HD66729 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different liquid-crystal drive voltages. Thus, potential difference between V_{LCD} and V1 must be 0.1 V or higher, and that between V4 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.1 µF to 0.47 µF between each internal operational amplifier V1OUT to V5OUT output and GND and stabilize the output level of the operational amplifier.



Notes: 1. The reference voltage input (Vci) must be adjusted so that the output voltage after boosting will not exceed the absolute maximum rating for the liquid-crystal power supply voltage (15 V). Particularly, Vci must be 3.0 V or less for quintuple boosting.
2. Vci is both a reference voltage and power supply for the booster; connect it to Vcc directly or combine it with a transistor so that sufficient current can be obtained.
3. Polarized capacitors must be connected correctly.
4. Circuits for temperature compensation should be based on the sample circuit in figure 26.

Figure 25 Internal Booster for LCD Drive Voltage Generation

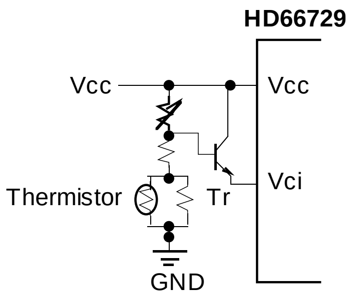


Figure 26 Temperature Compensation Circuit

Switching the Boosting Multiplying Factor

Instruction bits (BT1/0 bits) can optionally select the boosting multiplying factor of the internal booster. According to the display status, power consumption can be reduced by changing the LCD drive duty and the LCD drive bias, and by controlling the boosting multiplying factor for the minimum requirements. For details, see the Partial-display-on Function section.

Due to the maximum boosting multiplying factor, the following external capacitor needs to be connected. For example, when the maximum boosting is quadrupled, the capacitors between C4+ and C4– for quintuple boosting are not needed, so these pins must be open.

Table 18 VLOUT Output Status

BT1	BT0	VLOUT Output Status
0	0	Triple boosting output
0	1	Quadruple boosting output
1	0	Quintuple boosting output
1	1	Double boosting output

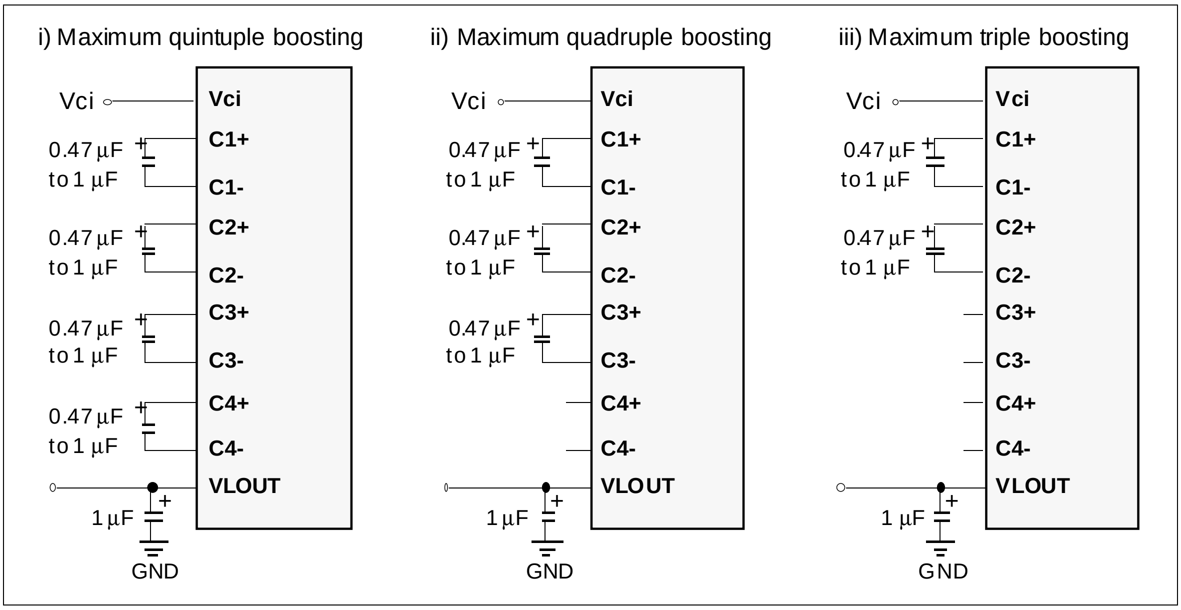


Figure 27 Booster Output Multiplying Factor Switching

Example of Power-supply Voltage Generator for More Than Quintuple Boosting Output

The HD66729 incorporates the booster for up to quintuple boosting. However, the LCD drive voltage (VLCD) will not be enough for quintuple boosting from Vcc when the power-supply voltage of Vcc is low or when the LCD drive voltage is high for the high-contrast LCD display. In this case, the reference voltage (Vci) for boosting can be set higher than the power-supply voltage of Vcc.

Set the Vci input voltage for the booster to 5.5 V or less within the range of Vcc + 1.0 V. Control the Vci voltage so that the boosting output voltage (VLOUT) should be less than the absolute maximum ratings (15 V).

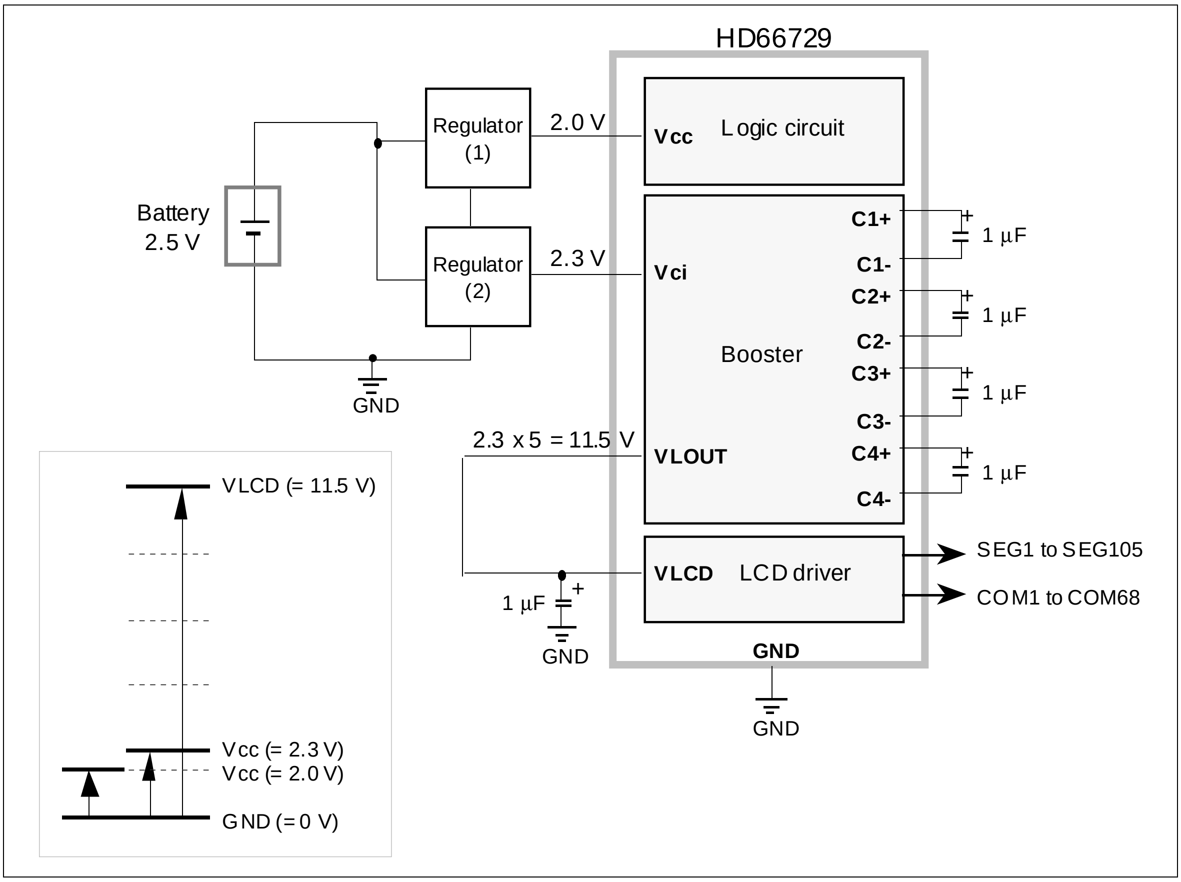


Figure 28 Usage Example of Booster at Vci > Vcc

Contrast Adjuster

Software can adjust 64-step contrast for an LCD by varying the liquid-crystal drive voltage (potential difference between V_{LCD} and V1) through the CT bits of the contrast adjustment register (electron volume function). The value of a variable resistor between V_{LCD} and V1 (VR) can be precisely adjusted in a 0.05 x R unit within a range from 0.05 x R through 3.20 x R, where R is a reference resistance obtained by dividing the total resistance.

The HD66729 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder resistors, which generate different liquid-crystal drive voltages. Thus, CT5-0 bits must be adjusted so that potential difference between V_{LCD} and V1 is 0.1 V or higher and that between V4 and GND is 1.4 V or higher when liquid-crystal drives, particularly when the VR is small.

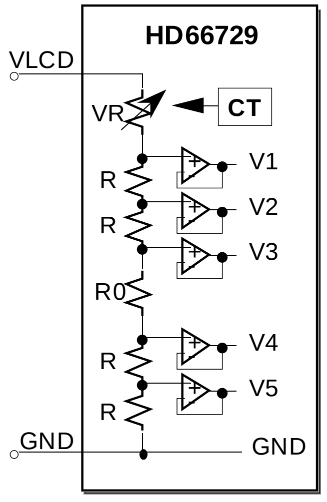


Figure 29 Contrast Adjuster

Table 19 Contrast Adjustment Bits (CT) and Variable Resistor Values

CT Set Value						Variable Resistor Value (VR)	Potential Difference between V1 and GND	Display Color
CT5	CT4	CT3	CT2	CT1	CT0			
0	0	0	0	0	0	3.20 x R	(Small)	(Light)
0	0	0	0	0	1	3.15 x R	↑	↑
0	0	0	0	1	0	3.10 x R		
0	0	0	0	1	1	3.05 x R		
0	0	0	1	0	0	3.00 x R		
0	0	0	1	0	1	2.95 x R		
0	0	0	1	1	0	2.90 x R		
0	0	0	1	1	1	2.85 x R		
0	0	1	0	0	0	2.80 x R		
0	0	1	0	0	1	2.75 x R		
0	0	1	0	1	0	2.70 x R		
0	0	1	0	1	1	2.65 x R		
0	0	1	1	0	0	2.60 x R		
⋮						⋮		
0	1	1	1	1	1	1.65 x R		
1	0	0	0	0	0	1.60 x R		
1	0	0	0	0	1	1.55 x R		
1	0	0	0	1	0	1.50 x R		
1	0	0	0	1	1	1.45 x R		
1	0	0	1	0	0	1.40 x R		
1	0	0	1	0	1	1.35 x R		
1	0	0	1	1	0	1.30 x R		
1	0	0	1	1	1	1.25 x R		
1	0	1	0	0	0	1.20 x R		
1	1	1	0	0	1	1.15x R		
⋮						⋮		
1	1	1	1	0	0	0.20 x R		
1	1	1	1	0	1	0.15 x R	↓	↓
1	1	1	1	1	0	0.10 x R		
1	1	1	1	1	1	0.05 x R	(Large)	(Deep)

Table 20 Contrast Adjustment per Bias Drive Voltage

Bias	LCD drive voltage: V_{DR}	Contrast adjustment range	
1/9 bias drive	$\frac{9 \times R}{9 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range	: $0.737 \times (V_{LCD}\text{-}GND) \leq V_{DR} \leq 0.994 \times (V_{LCD}\text{-}GND)$
		- Limit of potential difference between V4 and GND	: $\frac{2 \times R}{9 \times R + VR} \times (V_{LCD}\text{-}GND) \geq 1.4$ [V]
		- Limit if potential difference between VLCD and V1	: $\frac{VR}{9 \times R + VR} \times (V_{LCD}\text{-}GND) \geq 0.1$ [V]
1/8 bias drive	$\frac{8 \times R}{8 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range	: $0.714 \times (V_{LCD}\text{-}GND) \leq V_{DR} \leq 0.993 \times (V_{LCD}\text{-}GND)$
		- Limit of potential difference between V4 and GND	: $\frac{2 \times R}{8 \times R + VR} \times (V_{LCD}\text{-}GND) \geq 1.4$ [V]
		- Limit if potential difference between VLCD and V1	: $\frac{VR}{8 \times R + VR} \times (V_{LCD}\text{-}GND) \geq 0.1$ [V]
1/7 bias drive	$\frac{7 \times R}{7 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range	: $0.686 \times (V_{LCD}\text{-}GND) \leq V_{DR} \leq 0.993 \times (V_{LCD}\text{-}GND)$
		- Limit of potential difference between V4 and GND	: $\frac{2 \times R}{7 \times R + VR} \times (V_{LCD}\text{-}GND) \geq 1.4$ [V]
		- Limit if potential difference between VLCD and V1	: $\frac{VR}{7 \times R + VR} \times (V_{LCD}\text{-}GND) \geq 0.1$ [V]
1/6 bias drive	$\frac{6 \times R}{6 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range	: $0.652 \times (V_{LCD}\text{-}GND) \leq V_{DR} \leq 0.992 \times (V_{LCD}\text{-}GND)$
		- Limit of potential difference between V4 and GND	: $\frac{2 \times R}{6 \times R + VR} \times (V_{LCD}\text{-}GND) \geq 1.4$ [V]
		- Limit if potential difference between VLCD and V1	: $\frac{VR}{6 \times R + VR} \times (V_{LCD}\text{-}GND) \geq 0.1$ [V]
1/5 bias drive	$\frac{5 \times R}{5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range	: $0.610 \times (V_{LCD}\text{-}GND) \leq V_{DR} \leq 0.990 \times (V_{LCD}\text{-}GND)$
		- Limit of potential difference between V4 and GND	: $\frac{2 \times R}{5 \times R + VR} \times (V_{LCD}\text{-}GND) \geq 1.4$ [V]
		- Limit if potential difference between VLCD and V1	: $\frac{VR}{5 \times R + VR} \times (V_{LCD}\text{-}GND) \geq 0.1$ [V]
1/4 bias drive	$\frac{4 \times R}{4 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range	: $0.556 \times (V_{LCD}\text{-}GND) \leq V_{DR} \leq 0.988 \times (V_{LCD}\text{-}GND)$
		- Limit of potential difference between V4 and GND	: $\frac{2 \times R}{4 \times R + VR} \times (V_{LCD}\text{-}GND) \geq 1.4$ [V]
		- Limit if potential difference between VLCD and V1	: $\frac{VR}{4 \times R + VR} \times (V_{LCD}\text{-}GND) \geq 0.1$ [V]

Liquid Crystal Display Drive Bias Selector

An optimum liquid crystal display bias value can be selected using BS2-0 bits, according to the liquid crystal drive duty ratio setting (NL3-0 bits). Liquid crystal display drive duty ratio and bias value can be displayed while switching software applications to match the LCD panel display status. The optimum bias value calculated using the following expression is an ideal value where the optimum contrast is obtained. Driving by using a lower value than the optimum bias value provides lower contrast and lower liquid crystal display voltage (potential difference between V1 and GND). When the liquid crystal display voltage is insufficient even if a quintuple booster is used or output voltage is lowered because the battery life has been reached, the display can be made easier to see by lowering the liquid crystal bias.

The liquid crystal display can be adjusted by using the contrast adjustment register (CT4-0 bits) and selecting the booster output level (BT1/0 bits).

$$\text{Optimum bias value for 1/N duty ratio drive voltage} = \frac{1}{\sqrt{N} + 1}$$

Table 21 Optimum Drive Bias Values

LCD drive duty ratio	1/68	1/64	1/56	1/48	1/40	1/32	1/24	1/16	1/8
(NL3-0 set value)	1000	0111	0110	0101	0100	0011	0010	0001	0000
Optimum drive bias value	1/9	1/9	1/8	1/8	1/7	1/6	1/6	1/5	1/4
(BS2-0 set value)	010	010	011	011	100	101	101	110	111

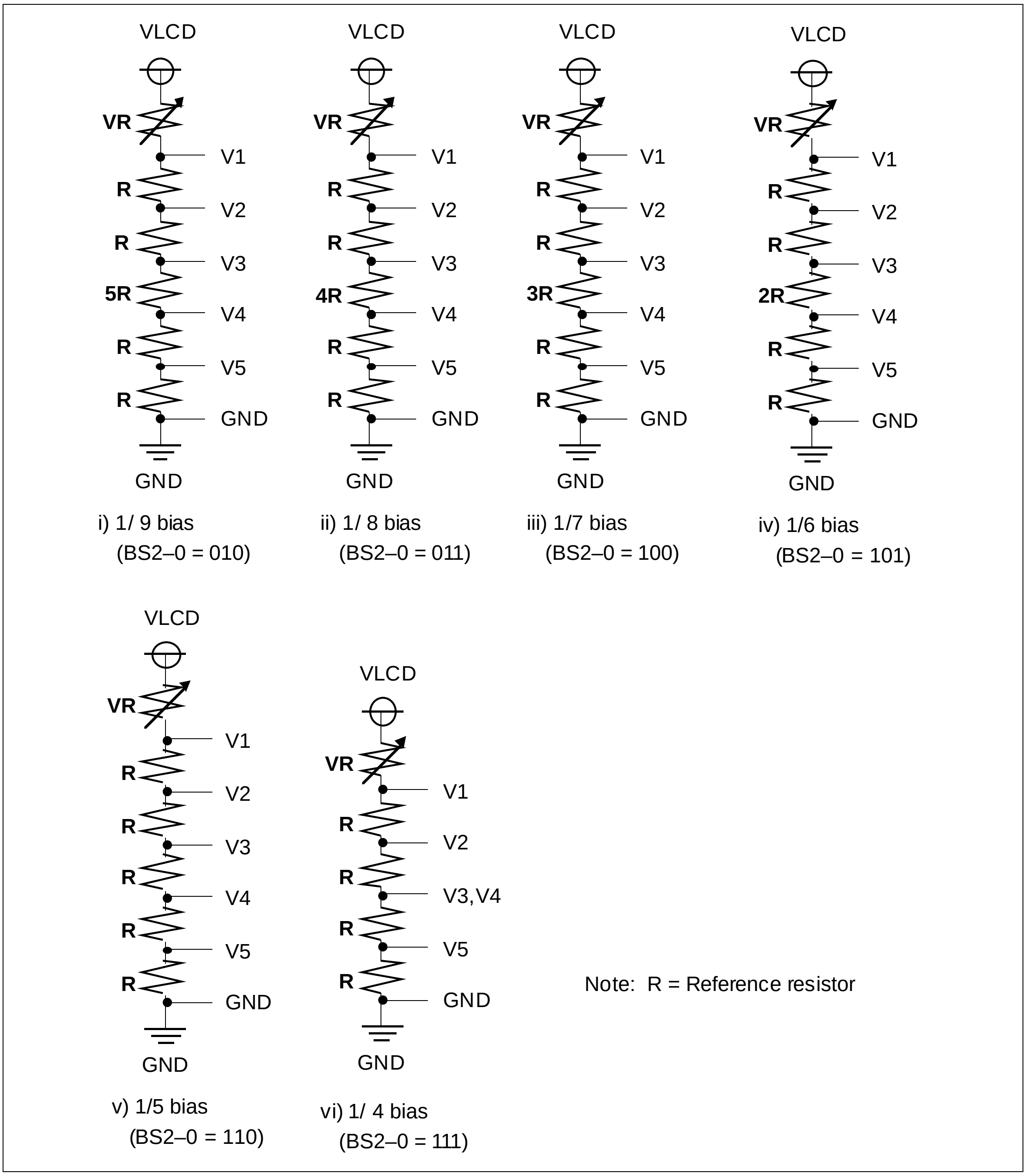


Figure 30 Liquid Crystal Display Drive Bias Circuit

LCD Panel Interface

The HD66729 has a function for changing the common driver/segment driver output shift direction using the CMS bit and SGS bit to meet the chip mounting positions of the HD66729. This is to facilitate the interface wiring to the LCD panel with COG or TCP installed.

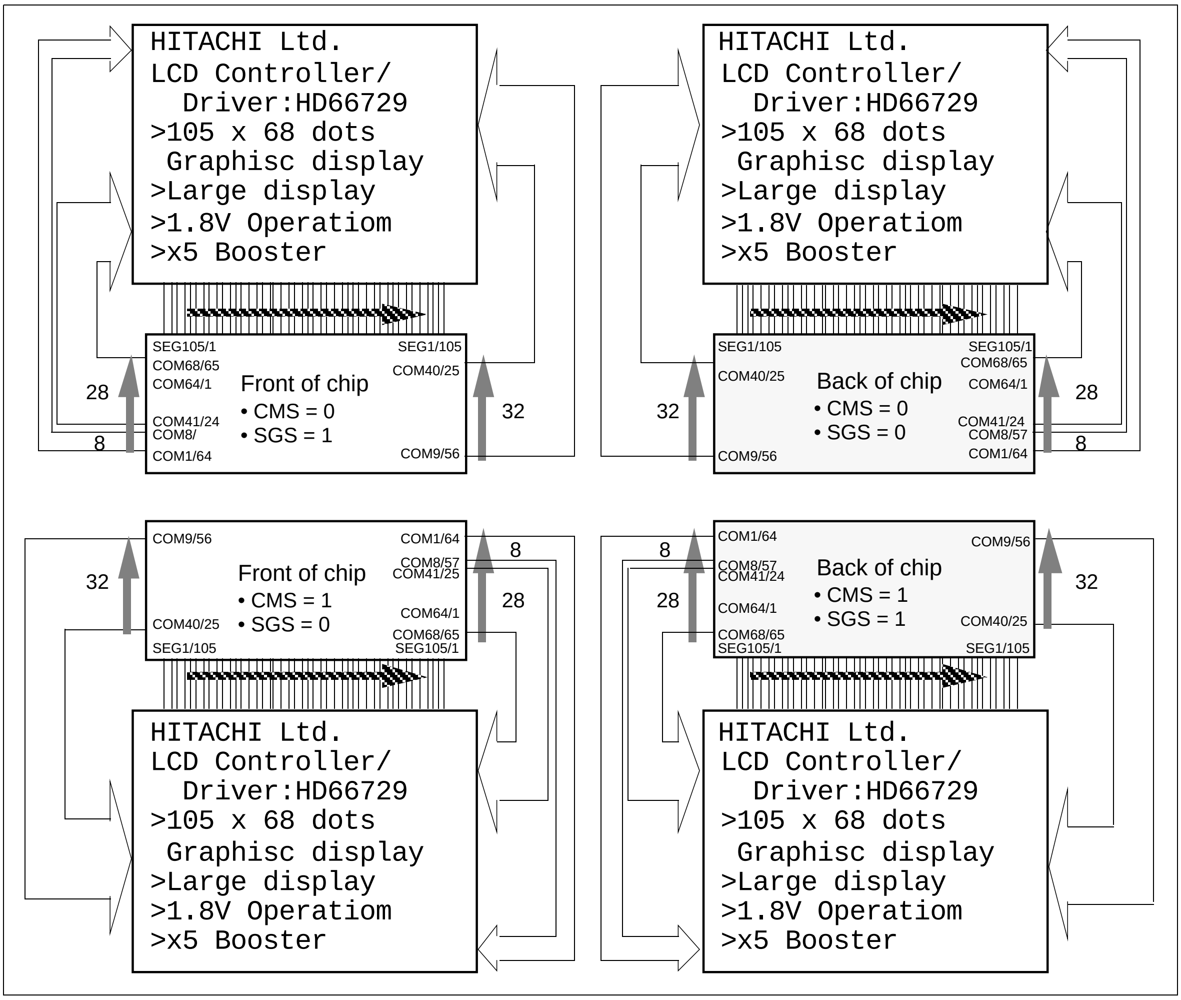


Figure 31 1/68-duty Drive Pattern Wiring

Vertical Smooth Scroll Display

The HD66729 can vertically scroll a graphics display in units of raster-rows. Because the HD66729 has an 80-raster-row vertical CGRAM area, it can write display data by using a 12-raster-row CGRAM area that is not displayed on the screen. In other words, the 80 raster-rows can be used to achieve continuous smooth vertical scrolling. After the 80th raster-row is displayed, the first raster-row is displayed again. Additionally, when display areas of a graphics icon such as a pictogram or a menu bar are partially fixed-displayed, the remaining areas can be displayed. For details, see the Partial Smooth Scroll Display Function section.

Specifically, this function is controlled by incrementing or decrementing the value in the display-start line bits (SL2 to SL0) and display-start raster-row bits (SN3 to SN0) by 1. For example, to smoothly scroll up, first set line bits SN3 to SN0 to 0000, and increment SL2 to SL0 by 1 from 000 to 111 to scroll seven raster-rows. Then increment line bits SN3 to SN0 to 0001, and again increment SL2 to SL0 by 1 from 000 to 111. If the vertical double-height display is at the top of the line, scrolling is done by each two raster-row.

When the response speed of the liquid crystal is low or when high-speed scrolling is needed, two- to four-raster-row scrolling is recommended.

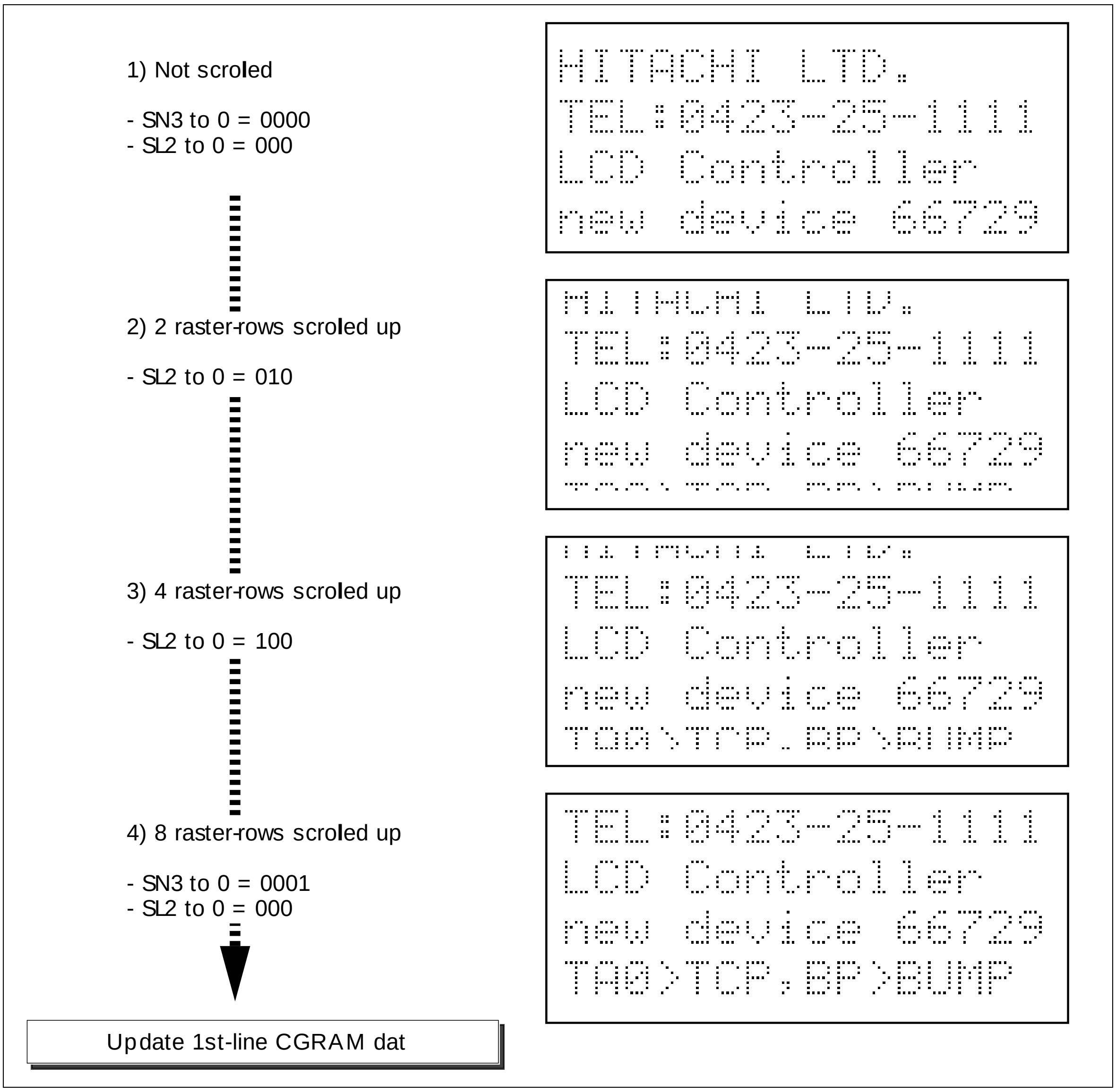


Figure 32 Vertical Smooth Scroll (4-line Display)

Setting Instructions (1/68-duty Drive: NL3-0 = 1000)

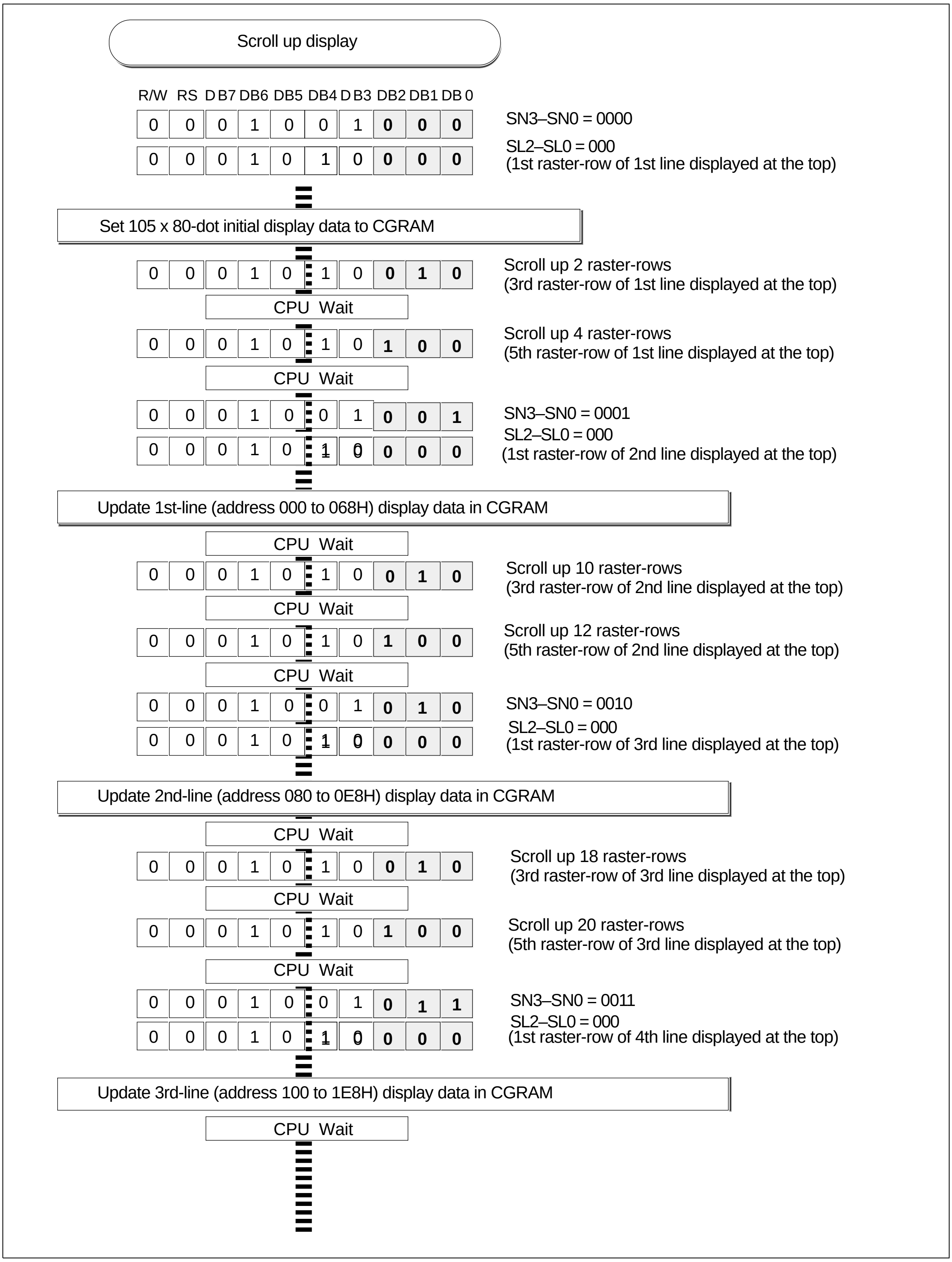


Figure 33 Setting Instructions for Vertical Smooth Scroll

Partial Smooth Scroll Display Function

The HD66729 can partially fixed-display the areas of a graphics icon at the top of the screen, such as a pictogram or a menu bar, and perform vertical smooth scrolling of the remaining bit-map areas. Since the PS1 to PS0 bits do not perform smooth scrolling of the upper first to third display lines but does fixed-display, pictograms can be placed. This function can largely control the bit-map rewrite frequencies and reduce software loads.

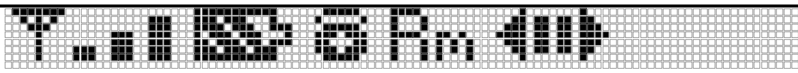
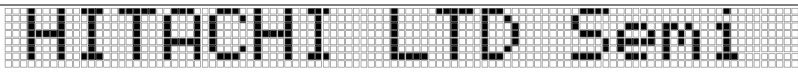
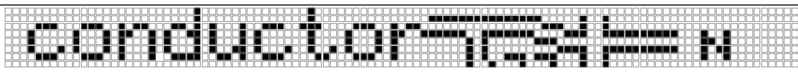
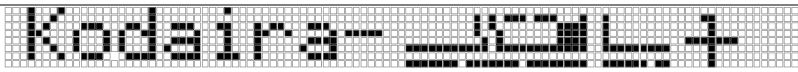
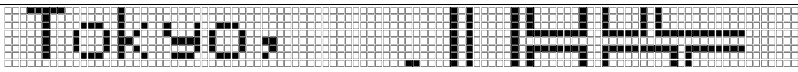
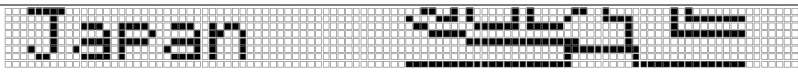
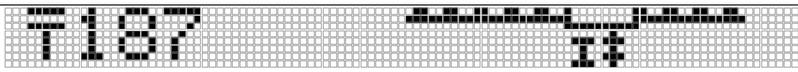
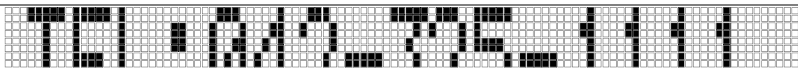
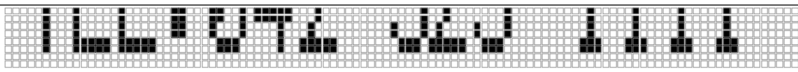
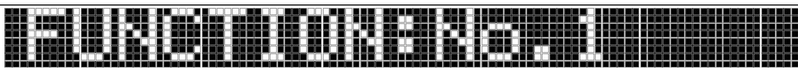
Table 22 Bit Setting and Display Lines

PS1–0 Bit Setting	COM Position	SN3–0 Bit Setting: 0000	0001	0010	0011	0101	0110–1001
PS1–0 = 00	COM1 ↓ COM68 (Not displayed)	1st line 2nd line 3rd line 4th line 5th line 6th line 7th line 8th line 9th line 10th line	2nd line 3rd line 4th line 5th line 6th line 7th line 8th line 9th line 10th line 1st line	3rd line 4th line 5th line 6th line 7th line 8th line 9th line 10th line 1st line 2nd line	4th line 5th line 6th line 7th line 8th line 9th line 10th line 1st line 2nd line 3rd line	5th line 6th line 7th line 8th line 9th line 10th line 1st line 2nd line 3rd line 4th line	→
PS1–0 = 01	COM1 ↓ COM68 (Not displayed)	1st line 1st line 2nd line 3rd line 4th line 5th line 6th line 7th line 8th line 9th line	1st line 2nd line 3rd line 4th line 5th line 6th line 7th line 8th line 9th line 10th line	1st line 3rd line 4th line 5th line 6th line 7th line 8th line 9th line 10th line 2nd line	1st line 4th line 5th line 6th line 7th line 8th line 9th line 10th line 2nd line 3rd line	1st line 5th line 6th line 7th line 8th line 9th line 10th line 2nd line 3rd line 4th line	→
PS1–0 = 10	COM1 ↓ COM68 (Not displayed)	1st line 2nd line 1st line 2nd line 3rd line 4th line 5th line 6th line 7th line 8th line	1st line 2nd line 2nd line 3rd line 4th line 5th line 6th line 7th line 8th line 9th line	1st line 2nd line 3rd line 4th line 5th line 6th line 7th line 8th line 9th line 10th line	1st line 2nd line 4th line 5th line 6th line 7th line 8th line 9th line 10th line 3rd line	1st line 2nd line 5th line 6th line 7th line 8th line 9th line 10th line 3rd line 4th line	→
PS1–0 = 11	COM1 ↓ COM68 (Not displayed)	1st line 2nd line 3rd line 1st line 2nd line 3rd line 4th line 5th line 6th line 7th line	1st line 2nd line 3rd line 2nd line 3rd line 4th line 5th line 6th line 7th line 8th line	1st line 2nd line 3rd line 3rd line 4th line 5th line 6th line 7th line 8th line 9th line	1st line 2nd line 3rd line 4th line 5th line 6th line 7th line 8th line 9th line 10th line	1st line 2nd line 3rd line 5th line 6th line 7th line 8th line 9th line 10th line 4th line	→

Notes: 1. The shadow lines above are fixed-displayed. They do not depend on the setting values of the SN3–0 or SL3–0 bits.
2. The SN3–0 and SL3–0 bits specify the next first scroll display line of the fixed-displayed lines.
3. The data in the 69th to 80th raster-rows are not displayed.

Partial Smooth Scroll Display Examples

Table 23 Data Setting to the CGRAM

CGRAM Address	CGRAM Data
000 to 068	
080 to 0E8	
100 to 168	
180 to 1E8	
200 to 268	
280 to 2E8	
300 to 368	
380 to 3E8	
400 to 468	
480 to 4E8	

i) Initial Screen Display

- PS1–0 = 01: Fixed-displays the first line
- SN3–0 = 0001: Starts display from the second line
- SL2–0 = 000

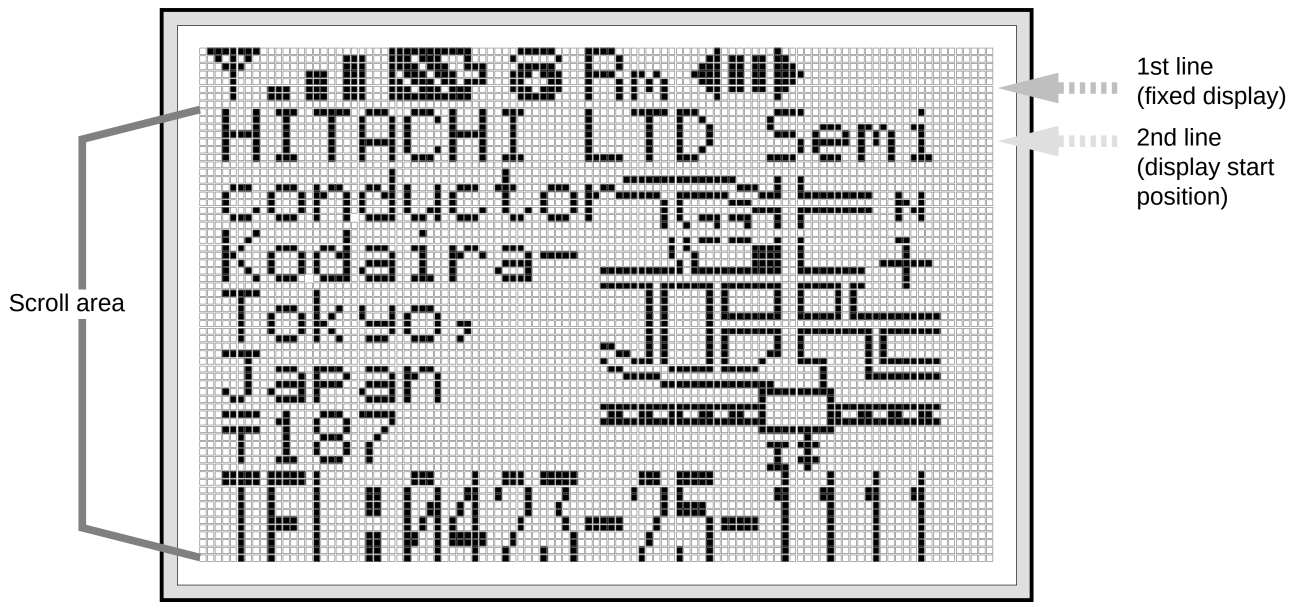


Figure 34 Example of Initial Screen in the Partial Smooth Scroll Mode

ii) 4-dot Partial Scroll Up

- PS1–0 = 01: Fixed-displays the first line
- SN3–0 = 0001: Starts display from the second line
- SL2–0 = 100: Shifts up by 4 dots

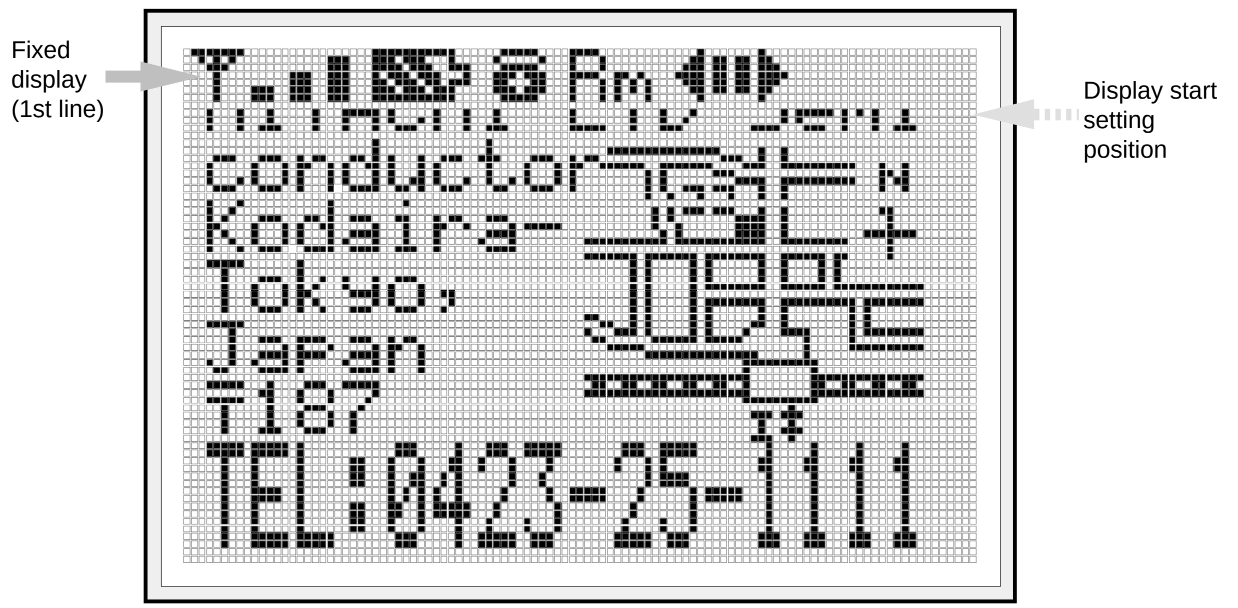


Figure 35 Example of Display Screen in the Partial Smooth Scroll Mode (1)

iii) 8-dot Partial Scroll Up

- PS1–0 = 01: Fixed-displays the first and second lines
- SN3–0 = 0010: Starts display from the third line
- SL2–0 = 000

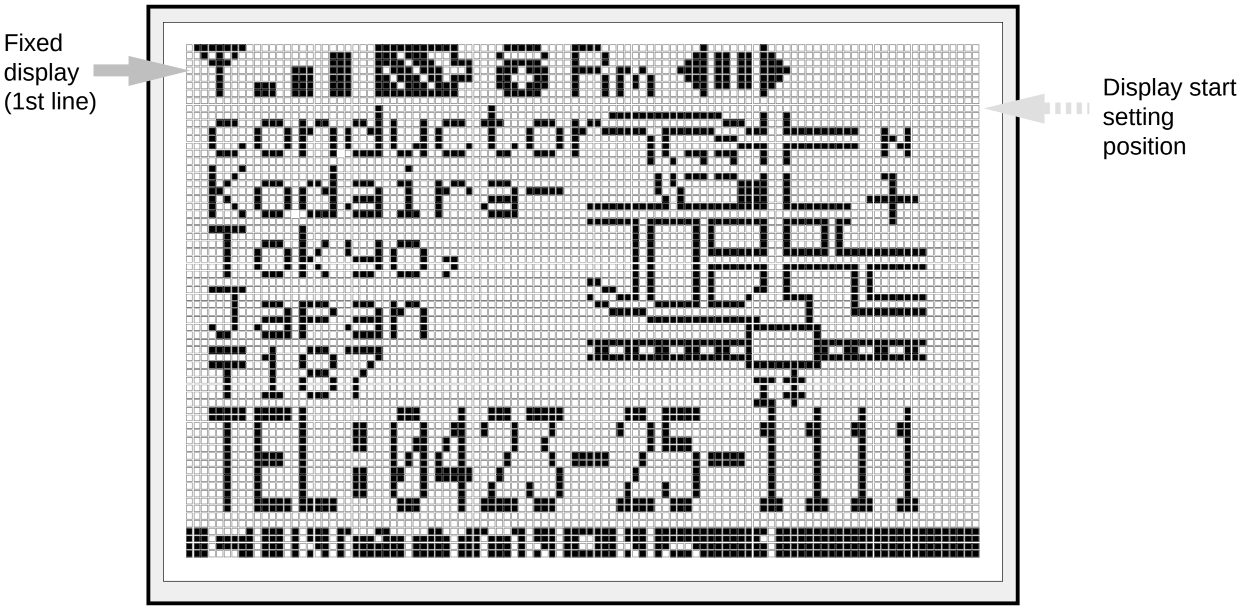


Figure 36 Example of Display Screen in the Partial Smooth Scroll Mode (2)

Double-height Display

The HD66729 can double the height of any desired area from the first to 10th lines. A line can be selected by the DL1 to DL10 bits as listed in table 24. All the font characters or graphics display patterns stored in the CGRAM can be doubled in height, allowing easy recognition. Note that there should be no space between the lines for double-height display (figure 37).

In vertical smooth scrolling, when the display-start setting line is displaying at double height, scrolling can be done by each two-line (dot).

Table 24 Double-height Display Specifications

Bit Setting	Display Position
DL1 = 1	1st line: double-height
DL2 = 1	2nd line: double-height
DL3 = 1	3rd line: double-height
DL4 = 1	4th line: double-height
DL5 = 1	5th line: double-height
DL6 = 1	6th line: double-height
DL7 = 1	7th line: double-height
DL8 = 1	8th line: double-height
DL9 = 1	9th line: double-height
DL10 = 1	10th line: double-height

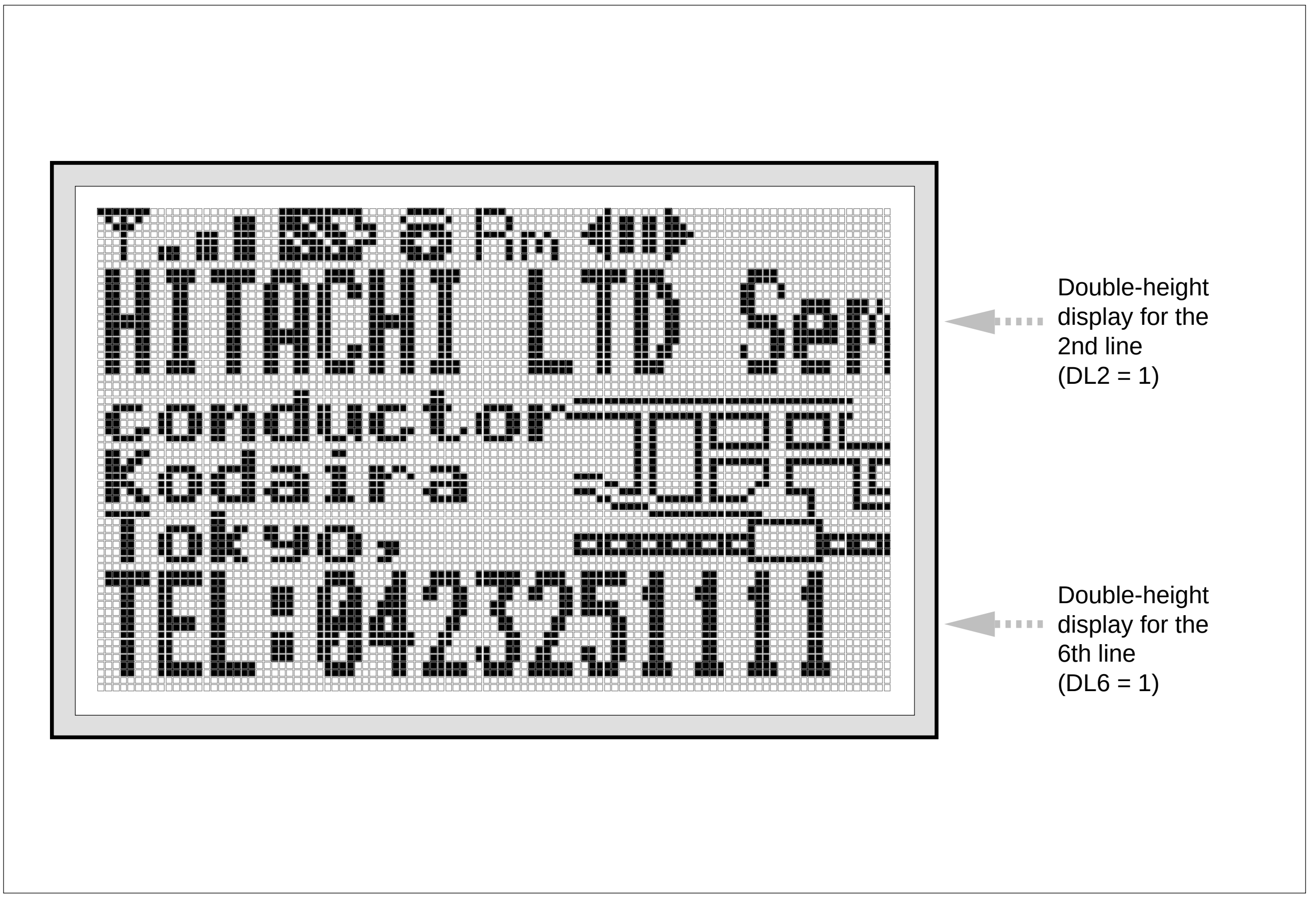


Figure 37 Double-height Display (2nd and 6th Lines)

Reversed Display Function

The HD66729 can display graphics display sections by black-and-white reversal. Black-and-white reversal can be easily displayed when REV is set to 1.

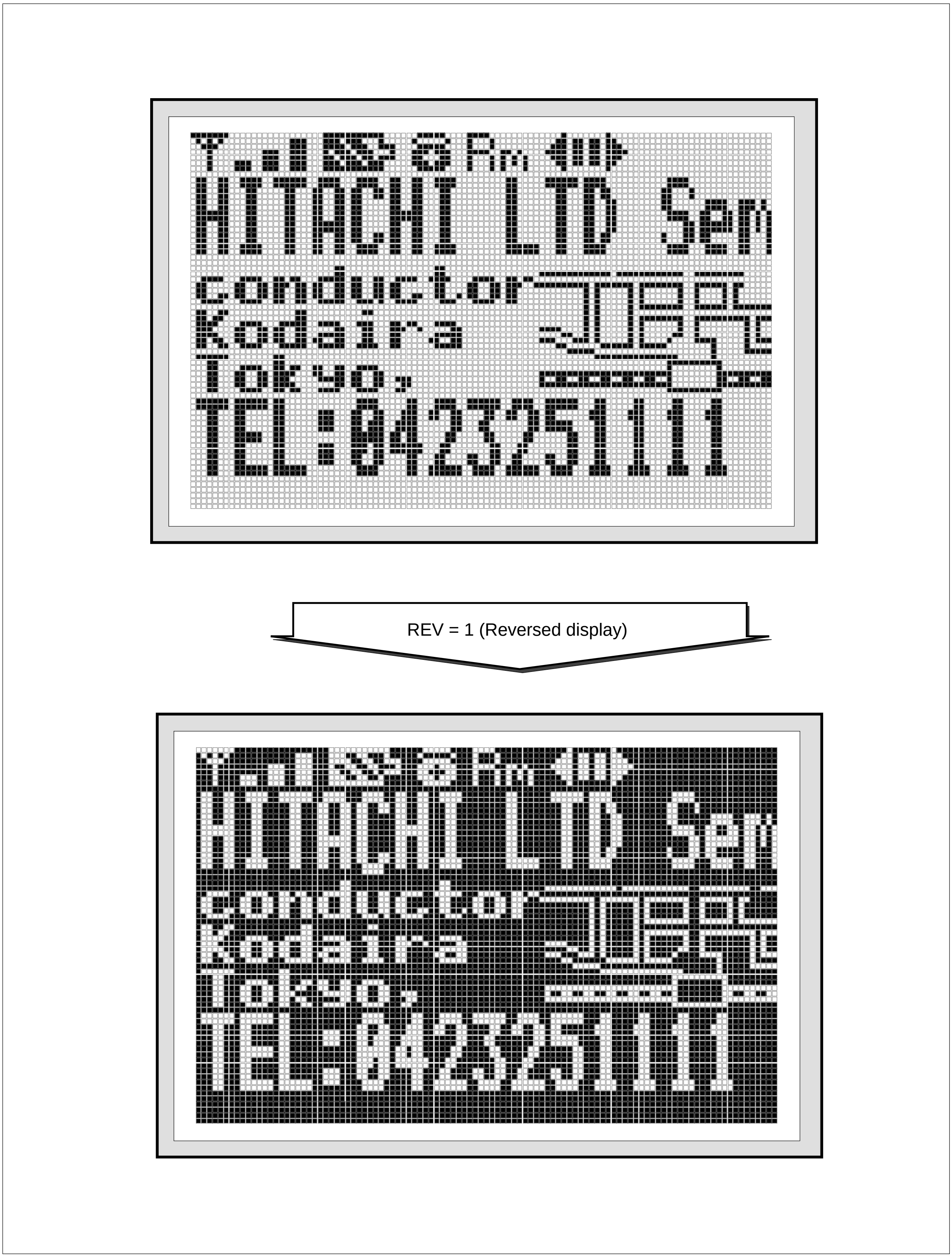


Figure 38   Reversed Display

Partial-display-on Function

The HD66729 can program the liquid crystal display drive duty ratio setting (NL3-0 bits), liquid crystal display drive bias value selection (BS2-0 bits), boost output level selection (BT1/0 bit) and contrast adjustment (CT5-0 bits). For example, in the 1/68 duty ratio, the HD66729 can selectively drive only the center of the screen or only the top or bottom of the screen by combining these register functions and the centering display (CN bit) function. This is called partial-display-on. Lowering the liquid crystal display drive duty ratio as required saves the liquid crystal display drive voltage, thus greatly reducing internal current consumption. This is suitable for eight to 16 raster-row display of a calendar or time, or the display of only graphics icons (pictograms) at the top or bottom of the screen, which needs to be continuous in the system standby state with minimal current consumption. Here, the non-displayed lines are constantly driven by the unselected level voltage, thus turning off the LCD for the lines.

In general, lowering the liquid crystal display drive duty ratio decreases the optimum liquid crystal display drive voltage and liquid crystal display drive bias value. This reduces output multiplying factors in the booster and greatly controls consumption current.

Table 25 Partial-display-on Function

Item	Normal 1/68-duty Drive	Partial-on Display Drive (Example: Limited 16-raster-row Display)	
LCD screen	Full-screen 68-raster-row display	Only 16 raster-rows displayed at center of screen (driven by 17 to 32 raster-rows)	Only 16 raster-rows displayed at top of screen (Driven by 1 to 16 raster-rows)
LCD drive position shift	Not necessary (CN = 0)	Necessary (CN = 1)	Not necessary (CN = 0)
LCD drive duty ratio	1/68 (NL3–0 = 1000)	1/16 (NL3–0 = 0001)	1/16 (NL3–0 = 0001)
LCD drive bias value	1/9 (BS2-0 = 010)	1/5 (BS2-0 = 110)	1/5 (BS2-0 = 110)
LCD drive voltage*	8 V to 11 V (adjustable using CT5–0)	4 V to 6 V (adjustable using CT5–0)	4 V to 6 V (adjustable using CT5–0)
Boosting output multiplying factor	Quadruple to quintuple (BT1–0 = 01/10)	Double (BT1–0 = 11)	Double (BT1–0 = 11)
Frame frequency (fosc = 75 kHz)	69 Hz	73 Hz	73 Hz

Note: The LCD drive voltage depends on the LCD materials which are actually used. Since the LCD drive voltage is high when the LCD drive duty ratio is high, a low duty ratio is suitable for low-power consumption.

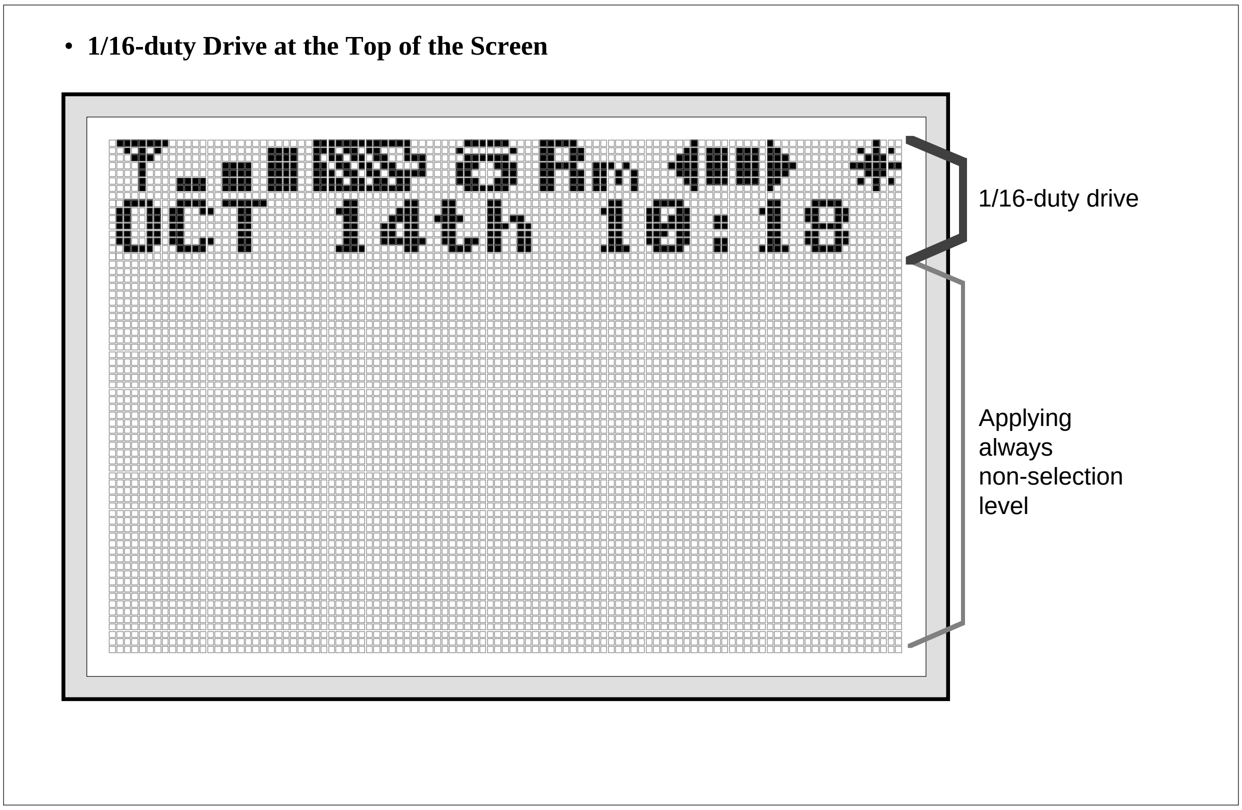


Figure 39 Partial-on Display (Date and Time Indicated) (1)

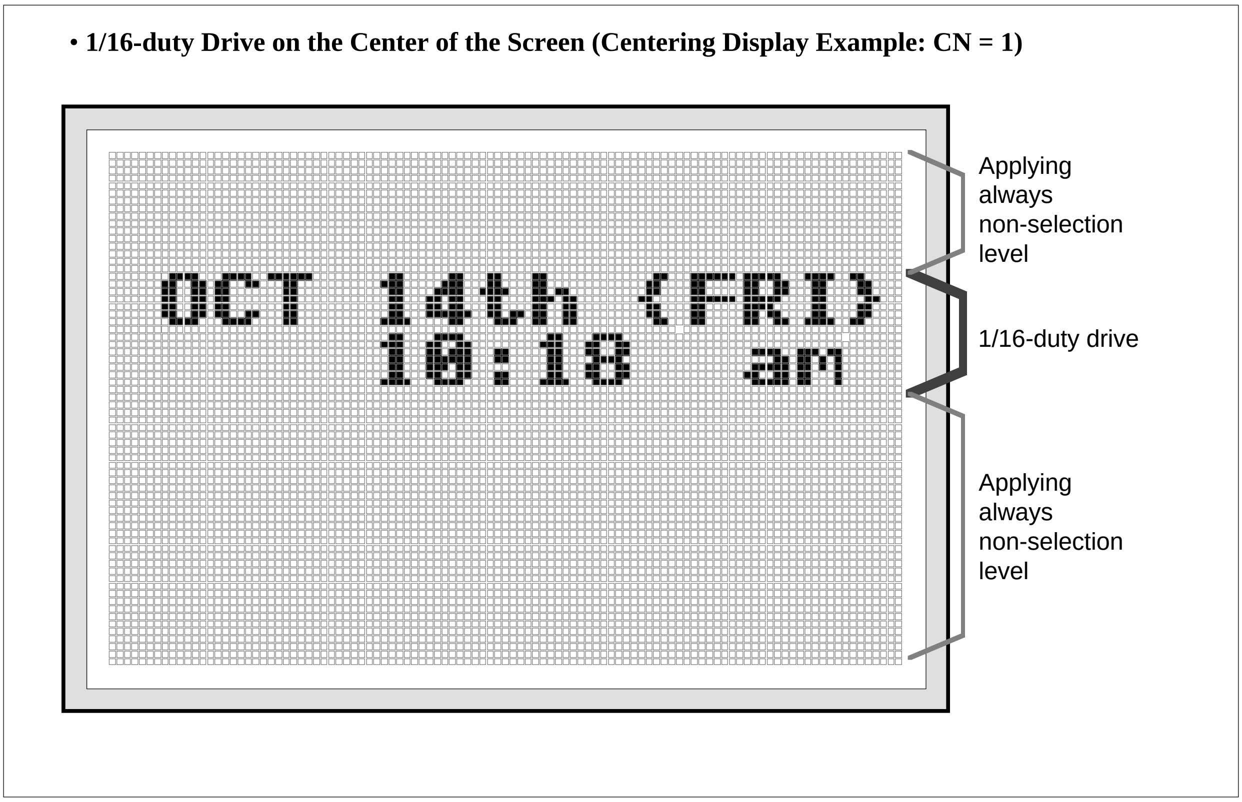


Figure 40 Partial-on Display (Date and Time Indicated) (2)

Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66729 in the sleep mode, where the device stops all internal display operations, thus reducing current consumption. Specifically, LCD drive is completely halted. Here, all the SEG (SEG1 to SEG105) and COM (COM1 to COM68) pins output the GND level, resulting in no display. If the AMP bit is set to 0 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

Table 26 Comparison of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)
LCD control	Turned off	Turned off
R-C oscillation circuit	Operates normally	Halted

Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66729 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, character and segment displays, which are controlled by the multiplexing drive method, are completely halted. Here, all the SEG (SEG1 to SEG105) and COM (COM1 to COM68) pins output the GND level, resulting in no display. If the AMP bit is set to 0 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than the start-oscillation instruction and the port control instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to 0.

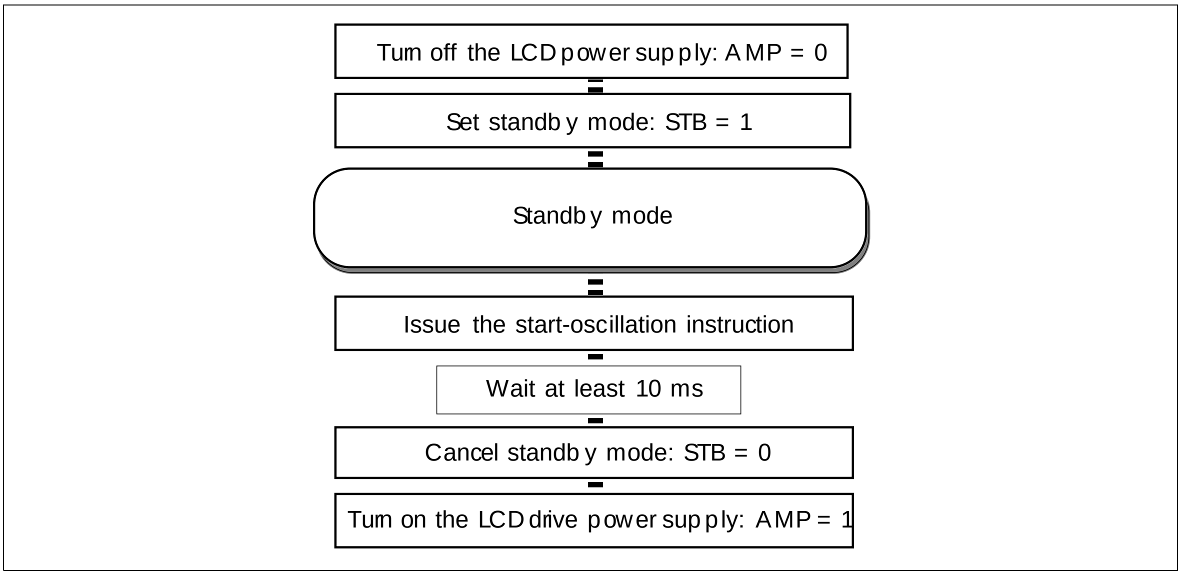


Figure 41 Procedure for Setting and Canceling Standby Mode

Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1, 2
Power supply voltage (2)	V_{LCD} – GND	V	–0.3 to +15.0	1, 3
Input voltage	Vt	V	–0.3 to V_{CC} + 0.3	1
Operating temperature	Topr	°C	–40 to +85	1, 4
Storage temperature	Tstg	°C	–55 to +110	1, 5

Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

2. VCC > GND must be maintained.
3. VLCD > GND must be maintained.
4. For bare die and wafer products, specified up to 85˚C.
5. This temperature specifications apply to the TCP package.

DC Characteristics (V_{CC} = 1.8 to 5.5 V, Ta = –40 to +85°C*[1])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V		2, 3
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 1.8 to 2.7 V	2, 3
		–0.3	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V	2, 3
Output high voltage (1) (SDA, DB0-7 pins)	V_{OH1}	0.75 V_{CC}	—	—	V	I_{OH} = –0.1 mA	2, 4
Output low voltage (1) (SDA, DB0-7 pins)	V_{OL1}	—	—	0.2 V_{CC}	V	V_{CC} = 1.8 to 2.7 V, I_{OL} = 0.1 mA	2
		—	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V, I_{OL} = 0.1 mA	2
Driver ON resistance (COM pins)	R_{COM}	—		10	kΩ	±Id = 0.05 mA, V_{LCD} = 8 V	5
Driver ON resistance (SEG pins)	R_{SEG}	—	4	10	kΩ	±Id = 0.05 mA, V_{LCD} = 8 V	5
I/O leakage current	I_{Li}	–1	—	1	µA	Vin = 0 to V_{CC}	6
Pull-up MOS current (SDA pin)	$-I_p$	1	6	25	µA	V_{CC} = 2.2 V, Vin = 0 V	2
Current consumption during normal operation (V_{CC}–GND)	I_{OP}	—	30 (T.B.D.)	50 (T.B.D.)	µA	R-C oscillation, V_{CC} = 2.2 V, Ta = 25 °C, f_{OSC} = 75 kHz (1/64 duty)	7, 8
Current consumption during sleep mode (V_{CC}–GND)	I_{SL}	—	8	—	µA	R-C oscillation, V_{CC} = 2.2 V, Ta = 25 °C, f_{OSC} = 75 kHz (1/64 duty)	7, 8
Current consumption during standby mode (V_{CC}–GND)	I_{ST}	—	0.1	5	µA	V_{CC} = 2.2 V, Ta = 25°C	7, 8
LCD drive power supply current (V_{LCD}–GND)	I_{LCD}	—	15	30	µA	V_{LCD} = 8 V, 1/9 bias, Ta = 25 °C, f_{OSC} = 75 kHz, VTEST3 = Vcc	8
LCD drive voltage (V_{LCD} – GND)	V_{LCD}	4.0	—	13.0	V		9

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Double-boost output voltage (VLOUT pin)	V_{UP2}	3.9	4.3	4.4	V	V_{CC} = Vci = 2.2 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 75 kHz, Ta = 25°C	12
Triple-boost output voltage (VLOUT pin)	V_{UP3}	6.1	6.5	6.6	V	V_{CC} = Vci = 2.2 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 75 kHz, Ta = 25°C	12
Quadruple-boost output voltage (VLOUT pin)	V_{UP4}	8.3	8.6	8.8	V	V_{CC} = Vci = 2.2 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 75 kHz, Ta = 25°C	12
Quintuple-boost output voltage (VLOUT pin)	V_{UP5}	10.5	10.8	11.0	V	V_{CC} = Vci = 2.2 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 75 kHz, Ta = 25°C	12
Use range of boost output voltages	V_{UP3}, V_{UP4}, V_{UP5}	Vcc	—	13.0	V	For triple to quintuple boost	12

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 1.8 to 5.5 V, Ta = –40 to +85°C*[1])

Clock Characteristics (V_{CC} = 1.8 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	fcp	50	75	150	kHz		10
External clock duty ratio	Duty	45	50	55	%		10
External clock rise time	trcp	—	—	0.2	µs		10
External clock fall time	tfcp	—	—	0.2	µs		10
R-C oscillation clock	f_{OSC}	59	74	89	kHz	Rf = 330 kΩ, V_{CC} = 2.2 V	11

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

68-system Bus Interface Timing Characteristics

(Vcc = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	600	—	—	ns	Figure 48
	Read	t_{CYCE}	800	—	—		
Enable high-level pulse width	Write	PW_{EH}	120	—	—	ns	Figure 48
	Read	PW_{EH}	350	—	—		
Enable low-level pulse width	Write	PW_{EL}	300	—	—	ns	Figure 48
	Read	PW_{EL}	300	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 48
Setup time (RS, R/W to E, CS*)		t_{ASE}	50	—	—	ns	Figure 48
Address hold time		t_{AHE}	20	—	—	ns	Figure 48
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 48
Write data hold time		t_{HE}	20	—	—	ns	Figure 48
Read data delay time		t_{DDRE}	—	—	300	ns	Figure 48
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 48

(Vcc = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	380	—	—	ns	Figure 48
	Read	t_{CYCE}	500	—	—		
Enable high-level pulse width	Write	PW_{EH}	70	—	—	ns	Figure 48
	Read	PW_{EH}	250	—	—		
Enable low-level pulse width	Write	PW_{EL}	150	—	—	ns	Figure 48
	Read	PW_{EL}	150	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 48
Setup time (RS, R/W to E, CS*)		t_{ASE}	50	—	—	ns	Figure 48
Address hold time		t_{AHE}	20	—	—	ns	Figure 48
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 48
Write data hold time		t_{HE}	20	—	—	ns	Figure 48
Read data delay time		t_{DDRE}	—	—	200	ns	Figure 48
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 48

80-system Bus Interface Timing Characteristics

(Vcc = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	600	—	—	ns	Figure 49
	Read	t_{CYCR}	800	—	—	ns	Figure 49
Write low-level pulse width		PW_{LW}	120	—	—	ns	Figure 49
Read low-level pulse width		PW_{LR}	350	—	—	ns	Figure 49
Write high-level pulse width		PW_{HW}	300	—	—	ns	Figure 49
Read high-level pulse width		PW_{HR}	300	—	—	ns	Figure 49
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns	Figure 49
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns	Figure 49
Address hold time		t_{AH}	20	—	—	ns	Figure 49
Write data setup time		t_{DSW}	60	—	—	ns	Figure 49
Write data hold time		t_{H}	20	—	—	ns	Figure 49
Read data delay time		t_{DDR}	—	—	300	ns	Figure 49
Read data hold time		t_{DHR}	5	—	—	ns	Figure 49

(Vcc = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	380	—	—	ns	Figure 49
	Read	t_{CYCR}	500	—	—	ns	Figure 49
Write low-level pulse width		PW_{LW}	70	—	—	ns	Figure 49
Read low-level pulse width		PW_{LR}	250	—	—	ns	Figure 49
Write high-level pulse width		PW_{HW}	150	—	—	ns	Figure 49
Read high-level pulse width		PW_{HR}	150	—	—	ns	Figure 49
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns	Figure 49
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns	Figure 49
Address hold time		t_{AH}	20	—	—	ns	Figure 49
Write data setup time		t_{DSW}	60	—	—	ns	Figure 49
Write data hold time		t_{H}	20	—	—	ns	Figure 49
Read data delay time		t_{DDR}	—	—	200	ns	Figure 49
Read data hold time		t_{DHR}	5	—	—	ns	Figure 49

Clock-synchronized Serial Interface Timing Characteristics (V_{CC} = 1.8 to 5.5 V)

(V_{CC} = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	At write (receive)	t_{SCYC}	0.5	—	20	µs	Figure 50
	At read (send)	t_{SCYC}	1	—	20	µs	Figure 50
Serial clock high-level width	At write (receive)	t_{SCH}	230	—	—	ns	Figure 50
	At read (send)	t_{SCH}	480	—	—	ns	Figure 50
Serial clock low-level width	At write (receive)	t_{SCL}	230	—	—	ns	Figure 50
	At read (send)	t_{SCL}	480	—	—	ns	Figure 50
Serial clock rise/fall time		t_{scf}, t_{scr}	—	—	20	ns	Figure 50
Chip select setup time		t_{CSU}	60	—	—	ns	Figure 50
Chip select hold time		t_{CH}	200	—	—	ns	Figure 50
Serial input data setup time		t_{SISU}	100	—	—	ns	Figure 50
Serial input data hold time		t_{SIH}	100	—	—	ns	Figure 50
Serial output data delay time		t_{SOD}	—	—	400	ns	Figure 50
Serial output data hold time		t_{SOH}	5	—	—	ns	Figure 50

(V_{CC} = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	At write (receive)	t_{SCYC}	0.2	—	20	µs	Figure 50
	At read (send)	t_{SCYC}	0.5	—	20	µs	Figure 50
Serial clock high-level width	At write (receive)	t_{SCH}	80	—	—	ns	Figure 50
	At read (send)	t_{SCH}	230	—	—	ns	Figure 50
Serial clock low-level width	At write (receive)	t_{SCL}	80	—	—	ns	Figure 50
	At read (send)	t_{SCL}	230	—	—	ns	Figure 50
Serial clock rise/fall time		t_{scf}, t_{scr}	—	—	20	ns	Figure 50
Chip select setup time		t_{CSU}	60	—	—	ns	Figure 50
Chip select hold time		t_{CH}	200	—	—	ns	Figure 50
Serial input data setup time		t_{SISU}	40	—	—	ns	Figure 50
Serial input data hold time		t_{SIH}	40	—	—	ns	Figure 50
Serial output data delay time		t_{SOD}	—	—	200	ns	Figure 50
Serial output data hold time		t_{SOH}	5	—	—	ns	Figure 50

Reset Timing Characteristics (V_{CC} = 1.8 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	1	—	—	ms	Figure 51

Electrical Characteristics Notes

1. For bare die products, specified up to 85˚C.
2. The following three circuits are I/O pin configurations (figure 42).

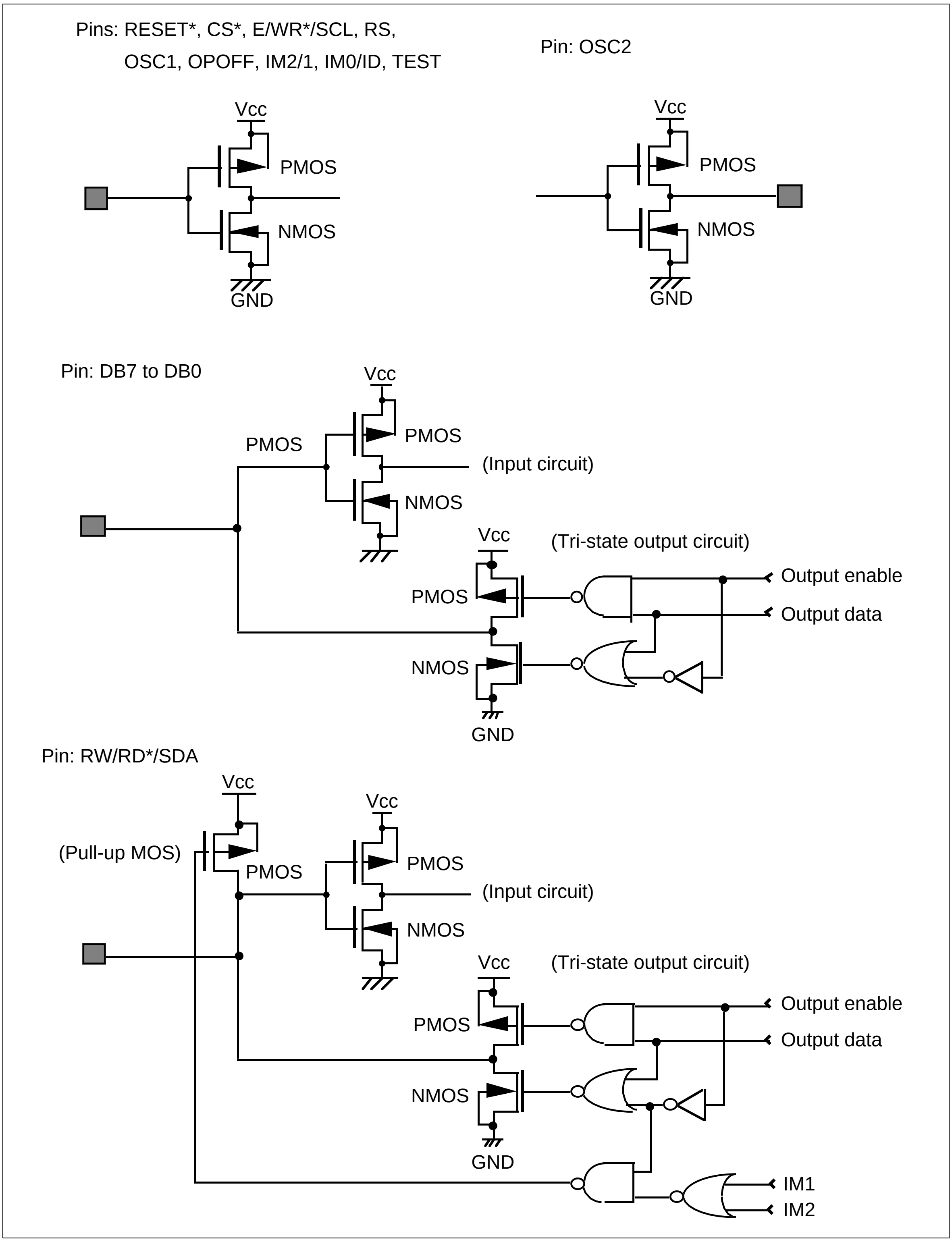


Figure 42 I/O Pin Configuration

3. The TEST pin must be grounded and the IM2/1, IM0/ID, and OPOFF pins must be grounded or connected to Vcc.
4. Corresponds to the high output for clock-synchronized serial interface.
5. Applies to the resistor value (RCOM) between power supply pins V1OUT, V2OUT, V5OUT, GND and common signal pins, and resistor value (RSEG) between power supply pins V1OUT, V3OUT, V4OUT, GND and segment signal pins.
6. This excludes the current flowing through pull-up MOSs and output drive MOSs.
7. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating.
8. The following shows the relationship between the operation frequency (fosc) and current consumption (Icc) (figure 43).

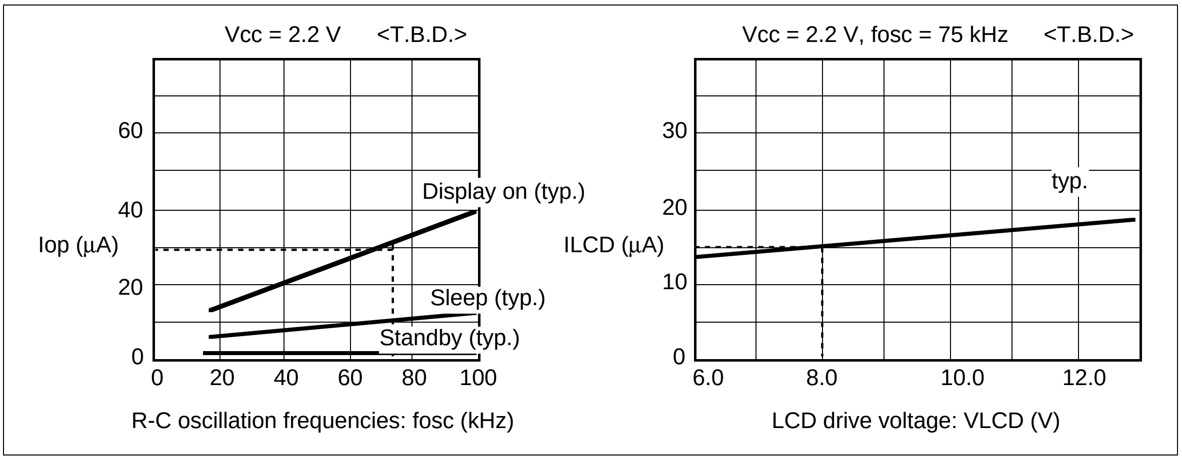


Figure 43 Relationship between the Operation Frequency and Current Consumption

9. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (Vcc, V1, V2, V3, V4, V5) when there is no load.
10. Applies to the external clock input (figure 44).

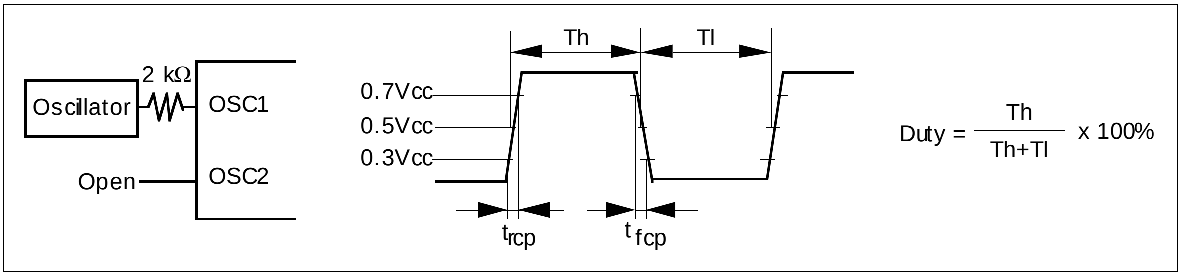
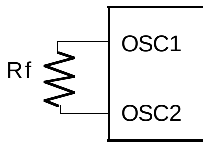


Figure 44 External Clock Supply

11. Applies to the internal oscillator operations using external oscillation resistor Rf (figure 45 and table 27).



Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

Figure 45 Internal Oscillation

Table 27 External Resistance Value and R-C Oscillation Frequency (Referential Data)

External Resistance (Rf)	R-C Oscillation Frequency: fosc				
	Vcc = 1.8 V	Vcc = 2.2 V	Vcc = 3.0 V	Vcc = 4.0 V	Vcc = 5.0 V
200 kΩ	86 kHz	111 kHz	130 kHz	140 kHz	148 kHz
270 kΩ	70 kHz	86 kHz	100 kHz	108 kHz	113 kHz
300 kΩ	64 kHz	79 kHz	92 kHz	98 kHz	102 kHz
330 kΩ	60 kHz	74 kHz	86 kHz	91 kHz	95 kHz
360 kΩ	57 kHz	69 kHz	79 kHz	84 kHz	87 kHz
390 kΩ	54 kHz	64 kHz	74 kHz	78 kHz	81 kHz
430 kΩ	49 kHz	59 kHz	67 kHz	71 kHz	74 kHz
470 kΩ	46 kHz	54 kHz	61 kHz	65 kHz	67 kHz

12. Booster characteristics test circuits are shown in figure 46.

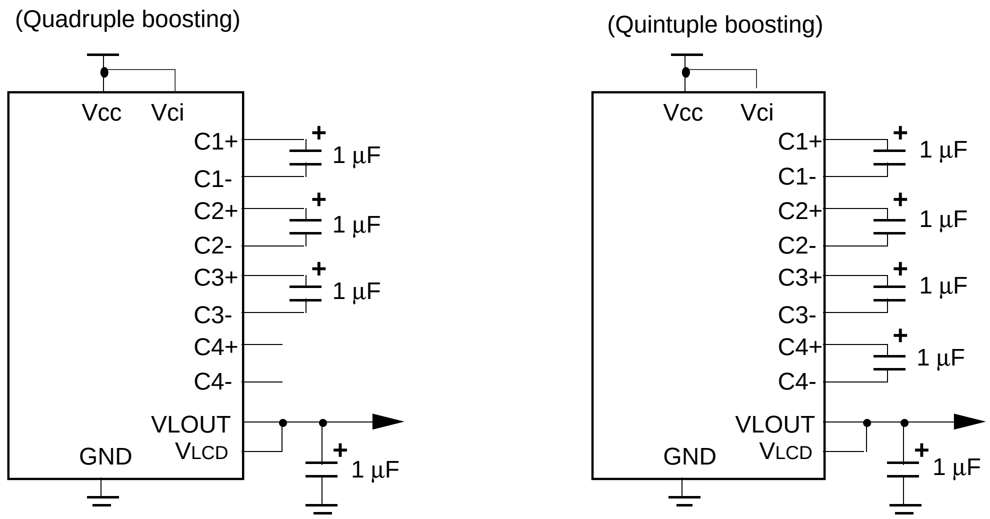


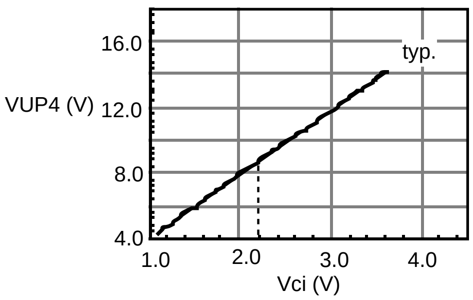
Figure 46 Booster

Referential data

VUP4 = VLCD – GND; VUP5 = VLCD – GND

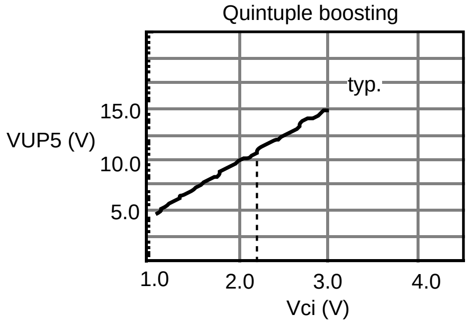
(i) Relation between the obtained voltage and input voltage

Quadruple boosting



Vci = Vcc, fosc = 75 kHz, Ta = 25°C, DCC = 0

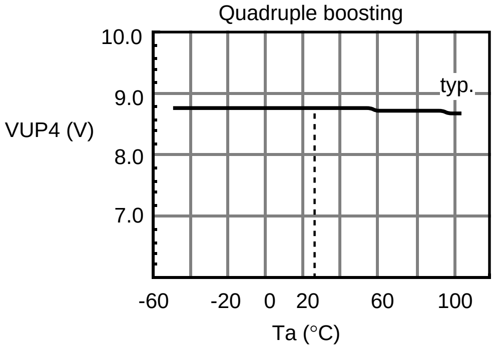
Quintuple boosting



Vci = Vcc, fosc = 75 kHz, Ta = 25°C, DCC = 0

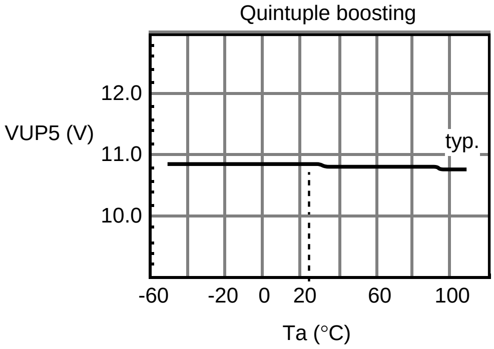
(ii) Relation between the obtained voltage and temperature

Quadruple boosting



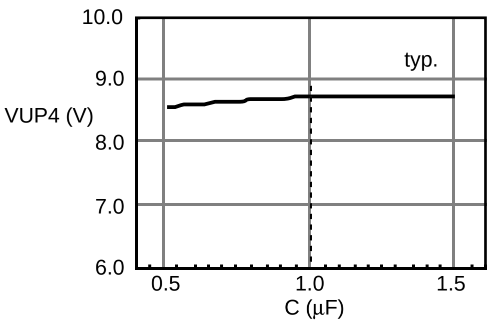
Vci = Vcc = 2.2 V, fosc = 75 kHz, Io = 30µA, DCC = 0

Quintuple boosting

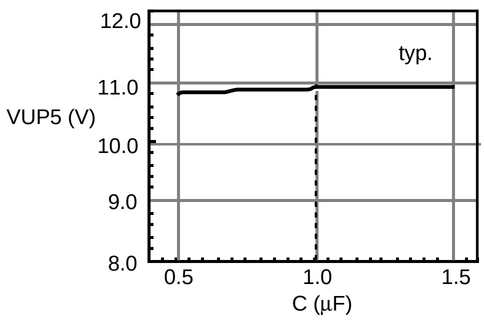


Vci = Vcc = 2.2 V, fosc = 75 kHz, Io = 30µA, DCC = 0

(iii) Relation between the obtained voltage and capacity



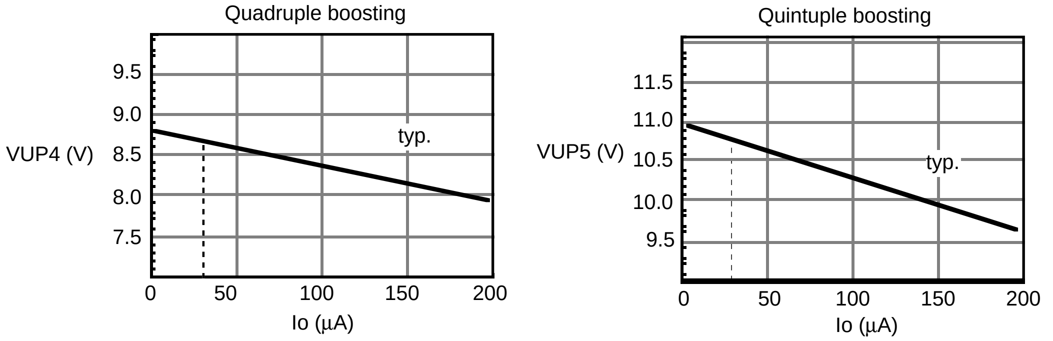
Vci = Vcc = 2.2 V, fosc = 75 kHz, Io = 30µA, DCC = 0



Vci = Vcc = 2.2 V, fosc = 75 kHz, Io = 30µA, DCC = 0

Figure 46 Booster (cont)

(iv) Relation between the obtained voltage and current



Vci = Vcc = 2.2 V, fosc = 75 kHz, Ta = 25 °C, DCC = 0

Vci = Vcc = 2.2 V, fosc = 75 kHz, Ta = 25 °C, DCC = 0

Figure 46 Booster (cont)

Load Circuits

AC Characteristics Test Load Circuits

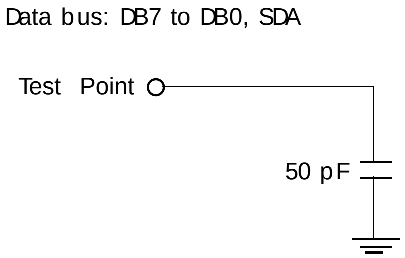


Figure 47 Load Circuit

Timing Characteristics

68-system Bus Operation

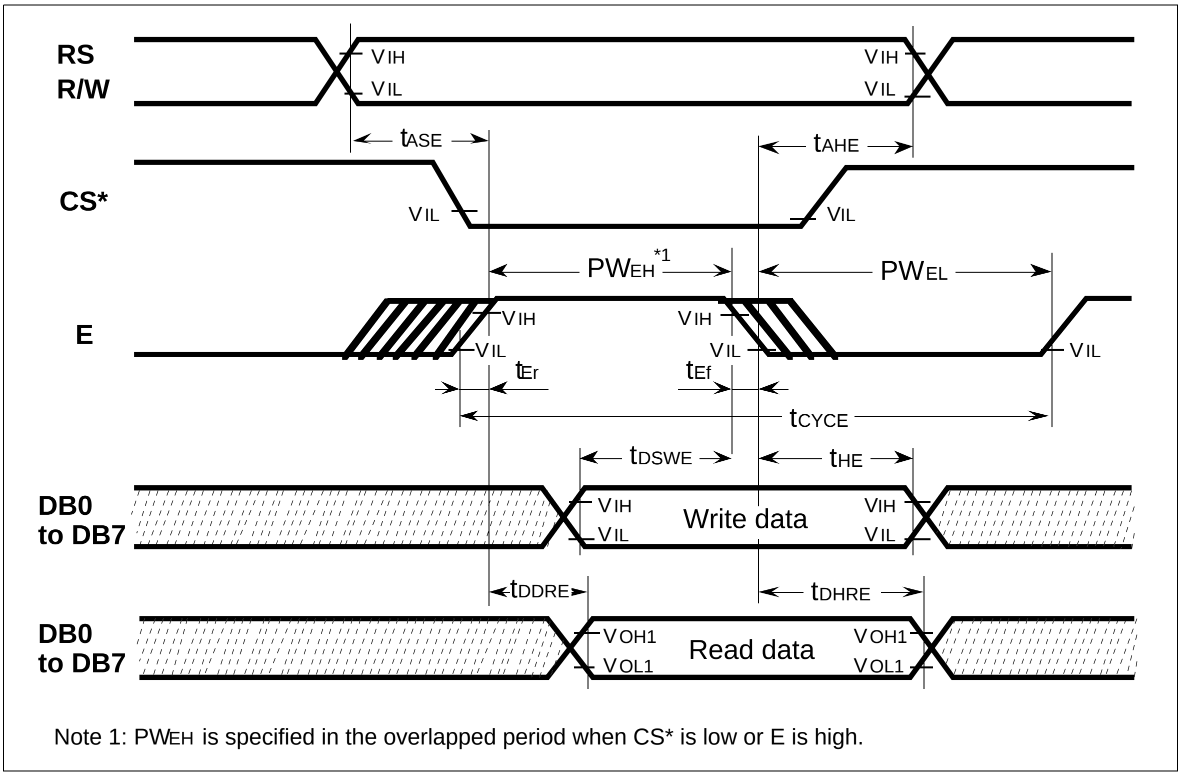
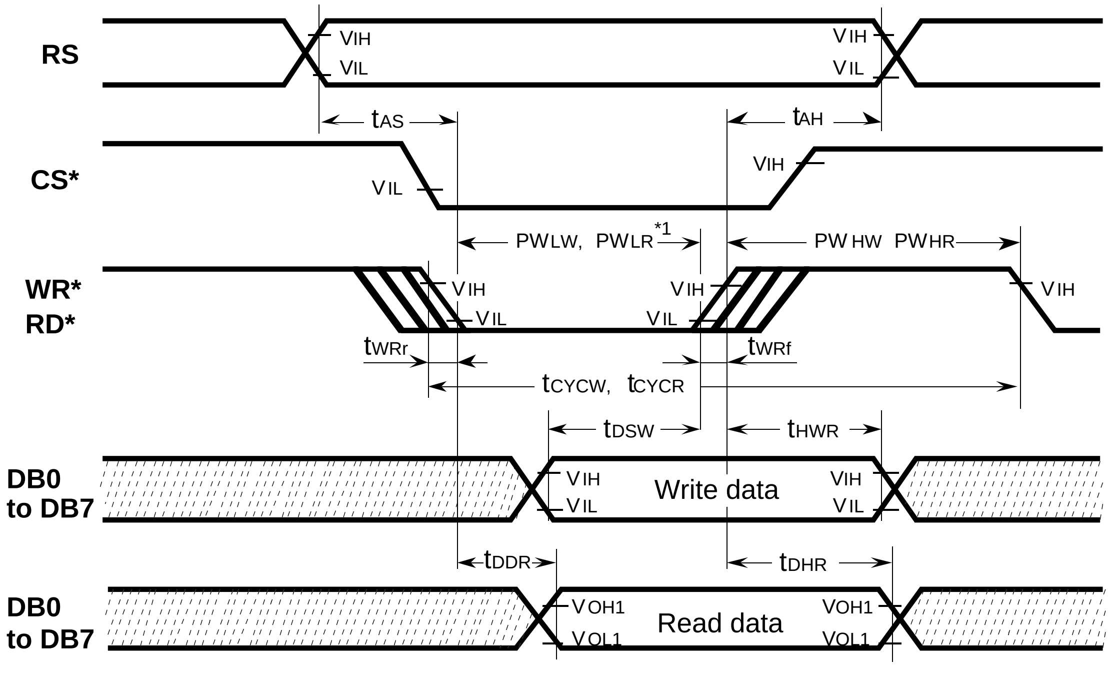


Figure 48 68-system Bus Timing

80-system Bus Operation



Note 1: PWLW and PWLR are specified in the overlapped period when CS* is low or WR* or RD* is low.

Figure 49 80-system Bus Timing

Clock-synchronized Serial Operation

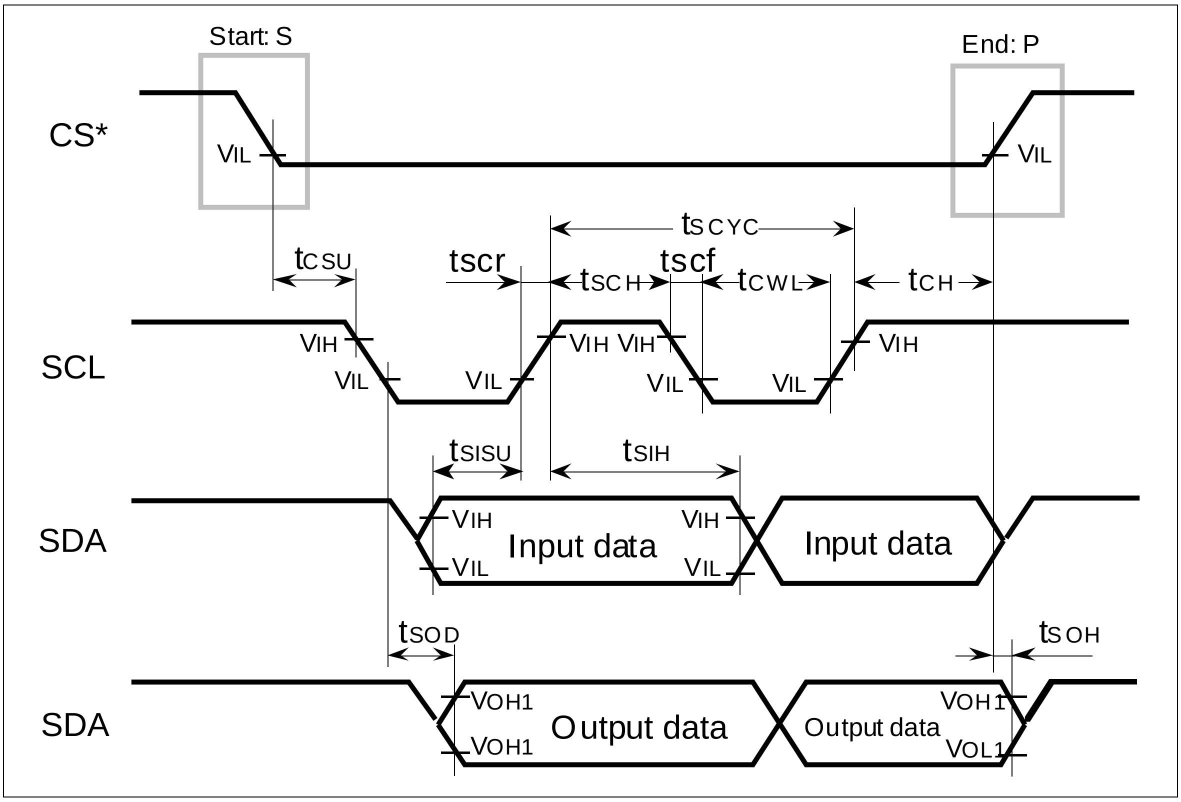


Figure 50 Clock-synchronized Serial Interface Timing

Reset Operation

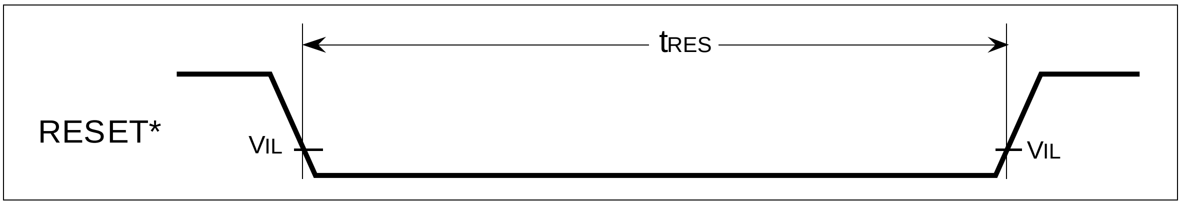
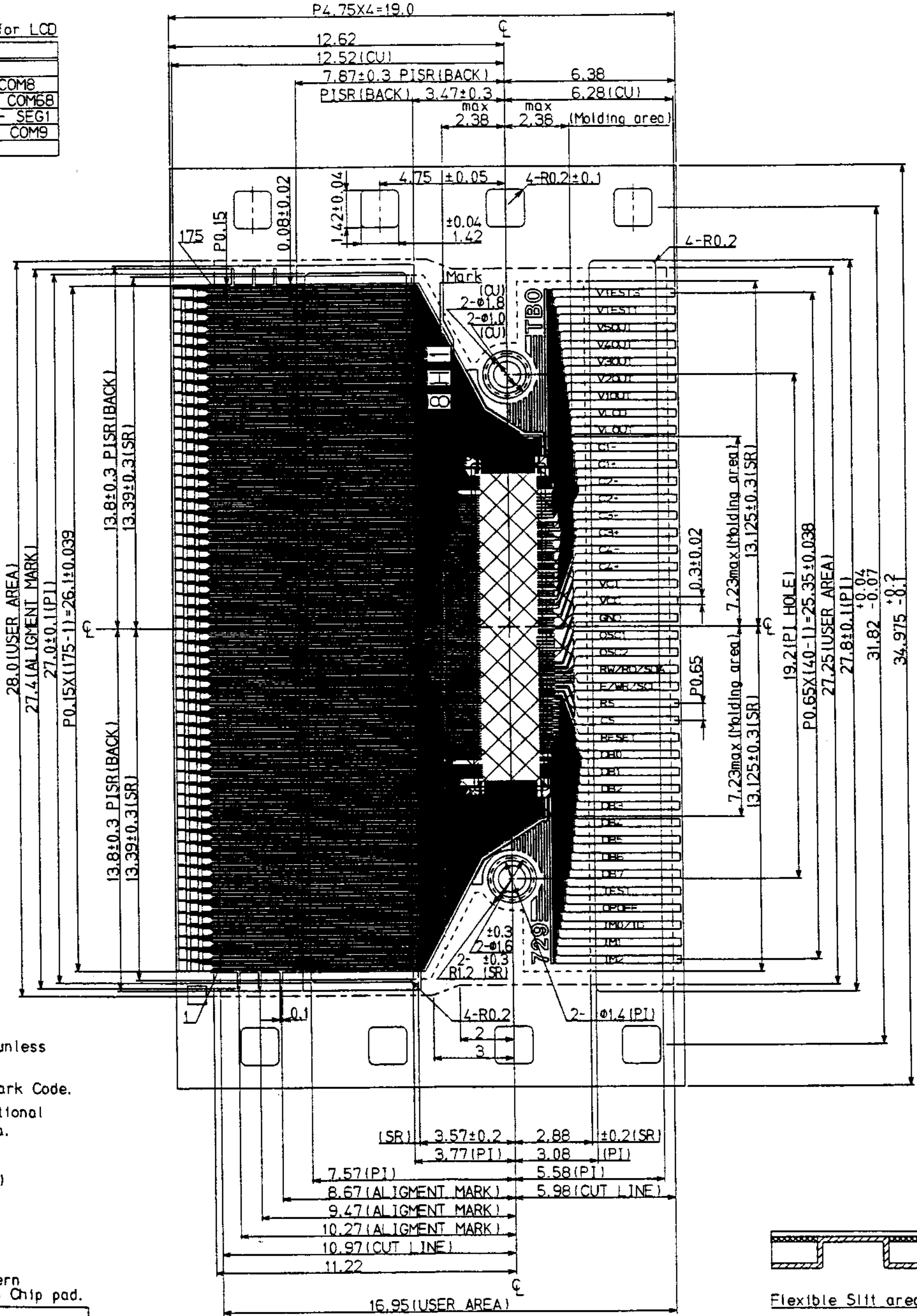
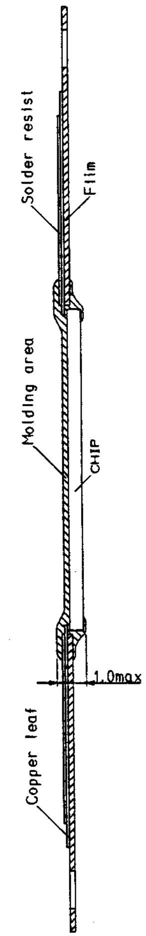


Figure 51 Reset Timing

Pin discription for LCD

No.	SYMBOL
1	DUMMY
2 - 9	COM1 - COM8
10 - 37	COM41 - COM68
38 - 142	SEG105 - SEG1
143 - 174	COM40 - COM9
175	DUMMY

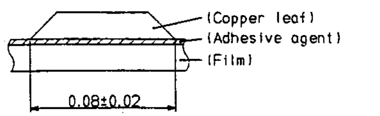




Notes: 1.Dimensional tolerances are ±0.1 mm unless otherwise noted.

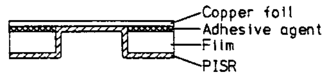
2.See "Mark Description" regarding Mark Code.

3.The figure below shows a cross sectional view of the outer lead bonding area.



4.The following table shows TCP pattern connection between TCP I/O pin and Chip pad.

TCP I/O Pin	Connection	
————	VTEST2	(Open)



Flexible Slit area Section (NTS)

MATERIAL

BASE FILM : UPILEX-S t=75μm
COPPER FOIL : VLP t=25μm
SOLDER RESIST
FRONT SIDE(SR) : CCR232GF
BACK SIDE(PISR): FS-100L
PLATING : Sn