HM538123 Series

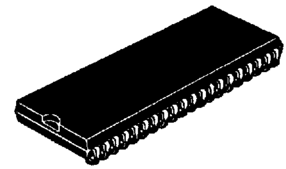
T-46-23-20

131,072-Word x 8-Bit Multiport CMOS Video RAM

■ DESCRIPTION

The HM538123 is a 1-Mbit multiport video RAM equipped with a 128k-word x 8-bit dynamic RAM and a 256-word x 8-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function. In addition, it has two new functions. Flash write clears the data of one row in one cycle in RAM. Special read transfer internally detects that the last address in SAM is read and transfers the next data of one row automatically from RAM if a transfer cycle has previously been executed. These functions make it easier to use the HM538123.

HM538123 Series



3DCP40D

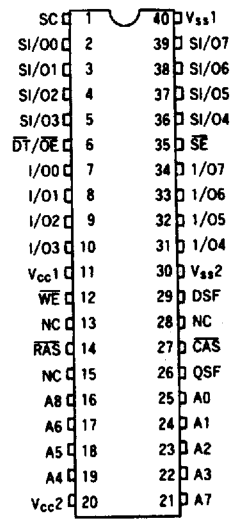
(CP-40D)

■ FEATURES

- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM .... 128k-word x 8-bit
  - SAM .... 256-word x 8-bit
- Access Time
  - RAM .... 100 ns/120 ns/150 ns (max)
  - SAM .... 30 ns/40 ns/50 ns (max)
- Cycle Time
  - RAM .... 190 ns/220 ns/260 ns (min)
  - SAM .... 30 ns/40 ns/60 ns (min)
- Low Power
  - Active
    - RAM .... 385 mW (max)
    - SAM .... 275 mW (max)
  - Standby .... 40 mW (max)
- High-Speed Page Mode Capability
- Mask Write Mode Capability
- Bidirectional Data Transfer Cycle between RAM and SAM Capability
- Special Read Transfer Cycle Capability
- Flash Write Cycle Capability
- 3 Variations of Refresh (8 ms/512 Cycles)
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

■ PIN OUT

HM538123JP Series



0111-1

(Top View)

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM538123JP-10	100 ns	400 mil
HM538123JP-12	120 ns	40-pin
HM538123JP-15	150 ns	Plastic SOJ (CP-40D)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Inputs
I/O_0–I/O_7	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_7	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{DT}/\overline{OE}$	Data Transfer Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
DSF	Special Function Input Flag
QSF	Data Register Empty Flag
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM

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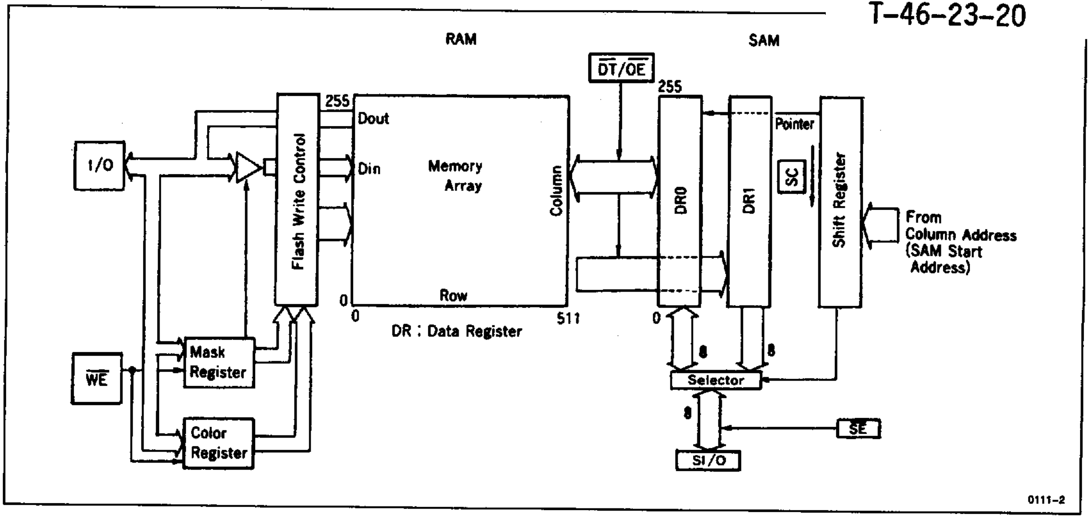

■ PIN FUNCTION

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in Table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM538123.

• Table 1. Operation Cycles of the HM538123

Input Level at the Falling Edge of $\overline{RAS}$					Operation Cycle
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	DSF	
H	H	H	X	L	RAM Read/Write
H	H	H	X	H	Color Register Set
H	H	L	X	L	Mask Write
H	H	L	X	H	Flash Write
H	L	H	X	L	Special Read Initialization
H	L	H	X	H	Special Read Transfer
H	L	L	H	X	Pseudo Transfer
H	L	L	L	X	Write Transfer
L	X	X	X	X	CBR Refresh

Note: X; Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column address is determined by A_0–A_7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538123 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write and flash write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a special read transfer cycle or special read initialization cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

DSF (input pin): DSF is a special data input flag pin. It is set to high when new functions such as color register set, special read transfer, and flash write, are used.

QSF (output pin): The HM538123 has a double buffer organization which includes two SAM data registers to relax the restriction on timings of $\overline{DT}/\overline{OE}$ and SC in real time transfer cycle. QSF flag turns high when output from one of SAM data registers finished (data register empty flag). If the condition is detected and special read transfer cycle is executed, data is transferred to the empty register. SC (serial clock) and data transfer cycle can be set asynchronously because detection of the last address in SAM and change of data register are executed automatically in the chip. It makes the system design flexible.

■ OPERATION OF HM538123

• Operation of RAM Port

RAM Read Cycle ($\overline{DT}/\overline{OE}$ High, $\overline{CAS}$ High, DSF Low at the Falling Edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle

(Early Write, Delayed Write, Read Modify Write) ($\overline{DT}/\overline{OE}$ High, $\overline{CAS}$ High, DSF Low at the Falling Edge of $\overline{RAS}$)

• Normal Mode Write Cycle

($\overline{WE}$ High at the Falling Edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 8 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read modify write cycle and enables read/write to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

• Mask Write Mode

($\overline{WE}$ Low at the Falling Edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ High, $\overline{CAS}$ High, DSF Low at the Falling Edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore, address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RAS} max (10 μs).

Flash Write Function (See Figure 1)

• Color Register Set Cycle ($\overline{CAS}$-$\overline{DT}/\overline{OE}$-$\overline{WE}$ High, DSF High at the Falling Edge of $\overline{RAS}$)

In color register set cycle, color data is set to the internal color register used in flash write cycle. 8 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it preserves the data until reset. The data set is just as same as in the usual write cycle except that DSF is set high at the falling edge of $\overline{RAS}$, and early write and delayed write cycle can be executed. In this cycle, memory array access is not executed, so it is unnecessary to give row and column addresses.

• Flash Write Cycle ($\overline{CAS}$-$\overline{DT}/\overline{OE}$ High, $\overline{WE}$ Low, DSF High at the Falling Edge of $\overline{RAS}$)

In a flash write cycle, a row of data (256 x 8 bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also possible to mask I/O in this cycle. When $\overline{CAS}$-$\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address and mask data is to I/O. Mask data is as same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is preserved. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time.

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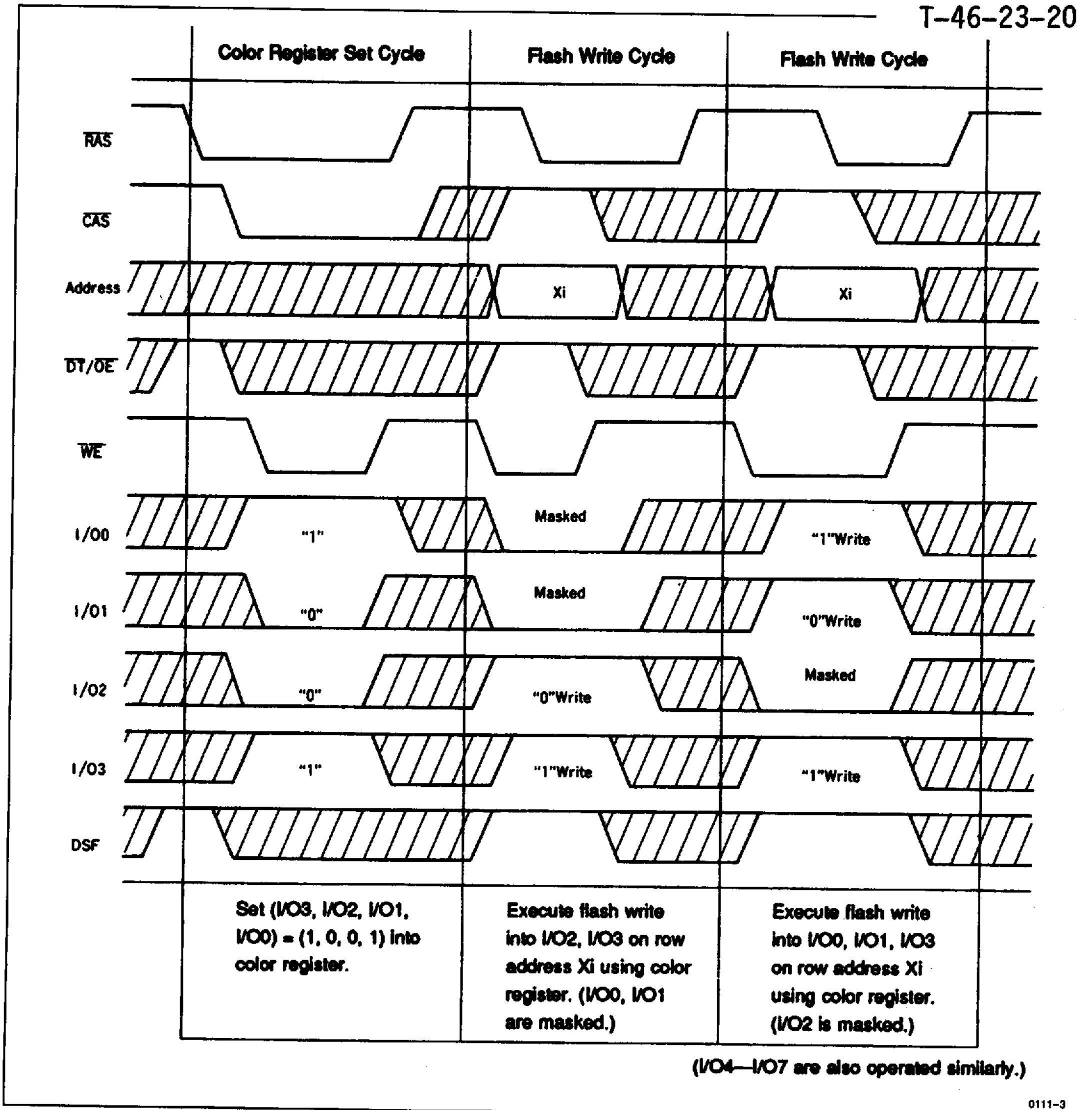

Figure 1. Use of Flash Write

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• **Transfer Operation**

The HM538123 provides the special read initialization cycle, special read transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer
 (a) Special read initialization cycle,
 Special read transfer cycle: RAM → SAM
 (b) write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)
 Special read initialization cycle: SI/O output
 Pseudo transfer cycle,
 write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address. When SAM start address is not changed, neither $\overline{CAS}$ nor address need to be set because SAM start address can be latched internally.

Special Read Initialization Cycle ($\overline{CAS}$ High, $\overline{DT}/\overline{OE}$ Low, $\overline{WE}$ High, DSF Low at the Falling Edge of $\overline{RAS}$)

If $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ is low, $\overline{WE}$ high, and DSF low at the falling edge of $\overline{RAS}$, this cycle becomes a special read initialization cycle. Special read initialization is used (1) to start special read transfer operation and (2) to switch SAM input/output pin (SI/O) set in input state by pseudo transfer cycle or write transfer cycle, to output state.

If the clock is set as mentioned before, address of SAM transfer word line is set to row address and first SAM address to access (SAM start address) to column address, it becomes possible to execute SAM read after t_{SRD} (min) after $\overline{RAS}$ is high. In this cycle, SI/O outputs uncertain data after the $\overline{RAS}$ falling edge. So when SAM is in input state before executing this cycle, it is necessary to stop input before the $\overline{RAS}$ falling edge.

SAM access is inhibited while $\overline{RAS}$ is low in this cycle. SC should not be raised during $\overline{RAS}$ low.

Special Read Transfer Cycle ($\overline{CAS}$ High, $\overline{DT}/\overline{OE}$ Low, $\overline{WE}$ High, DSF High at the Falling Edge of $\overline{RAS}$)

Ordinary multiport video RAM has some problems; (1) severe limitation on timings between processor clock $\overline{DT}/\overline{OE}$ and CRT clock SC, (2) complicated external control circuit to detect SAM last address externally and to insert transfer cycle synchronously. Special read transfer cycle makes it possible to relax the timing limitations and to set serial clock (SC) and transfer cycle perfectly synchronously.

Figure 2 shows the block diagram for a special read transfer. SAM double buffers are composed of two data registers (DR). When data is read out from DR0 serially, special read transfer cycle transfers a row of RAM data, which will be read from SAM next, to DR1.

The end of data read from DR0 is detected internally and data register switching circuit automatically switches to DR1 output. So data can be output continuously.

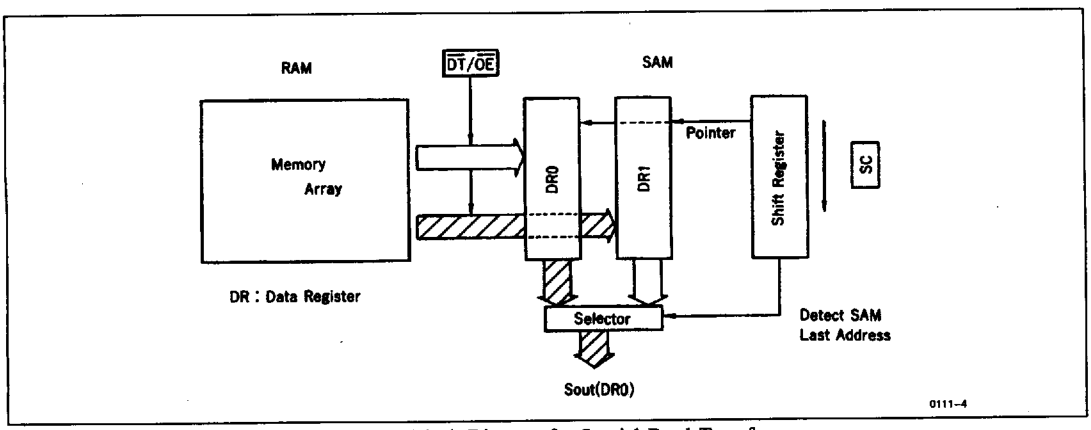

Figure 2. Block Diagram for Special Read Transfer

Figure 3 shows special read transfer operation sequence. QSF flag indicates that reading out from data register has finished (data register empty flag), and special read transfer can be executed while QSF is high. At first, special read operation starts by executing a special read initialization cycle. So QSF becomes high, the processor gives row address and SAM start address, which is needed next, to the memory, and inserts a special read transfer cycle. Data register becomes full after a special read transfer cycle, so QSF becomes low during the cycle. When the last SAM address is accessed, QSF becomes high and the data register, which outputs from the next SAM address, changes, and serial access can be executed.

By executing these handshakes, serial clock and transfer cycle can be executed perfectly asynchronously, and flexibility of the system design is improved.

Special read transfer cycle is set by making $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high, and DSF high at the falling edge of RAS (same as for special read initialization cycle except DSF). Like in other transfer cycles, the address of the word line to transfer into data register is specified by row address and SAM start is specified by column address. When the last SAM address data is output, the next data is output from the SAM start address specified by this RAS cycle. This transfer cycle can be executed asynchronously with SAM cycle. However, it is necessary to execute SAM access after $\overline{RAS}$ becomes high after SAM start address is specified by $\overline{RAS}$ cycle. (See Figure 4).

QSF should be high at the falling edge of $\overline{RAS}$ to execute a special read transfer cycle. A cycle whose QSF is low is neglected (refresh is executed). When the previous transfer cycle is a pseudo transfer or write transfer cycle and SI/O is in input state, special read transfer cycle cannot be used (neglected). Special read initialization cycle is required to switch SI/O to output state.

Pseudo Transfer Cycle ($\overline{CAS}$ High, $\overline{DT}/\overline{OE}$ Low, $\overline{WE}$ Low, and $\overline{SE}$ High at the Falling Edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of $\overline{RAS}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high, like in the special read initialization cycle. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

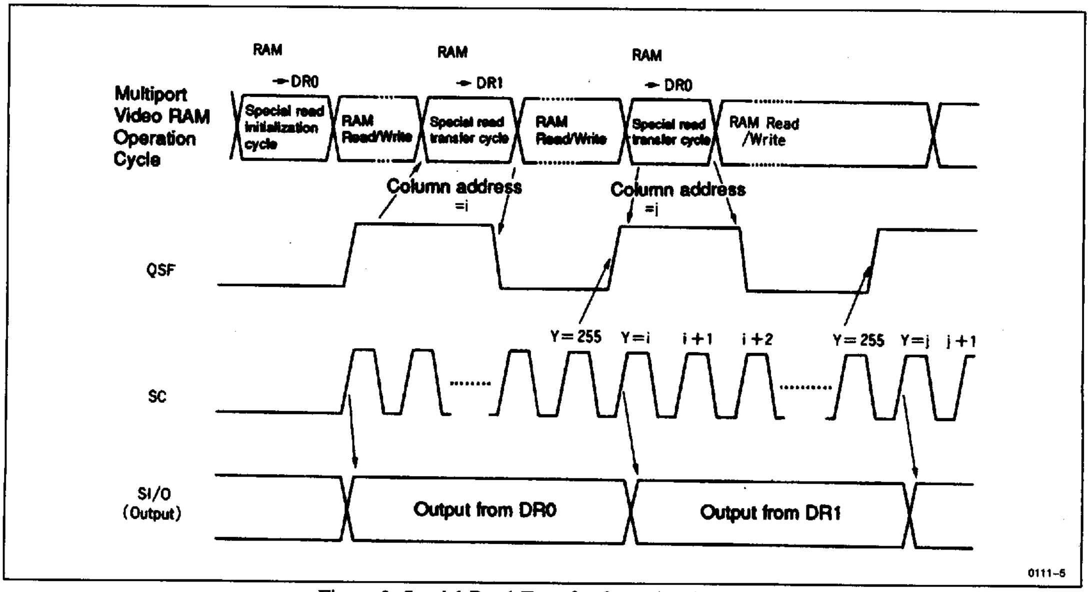

Figure 3. Special Read Transfer Operation Sequence

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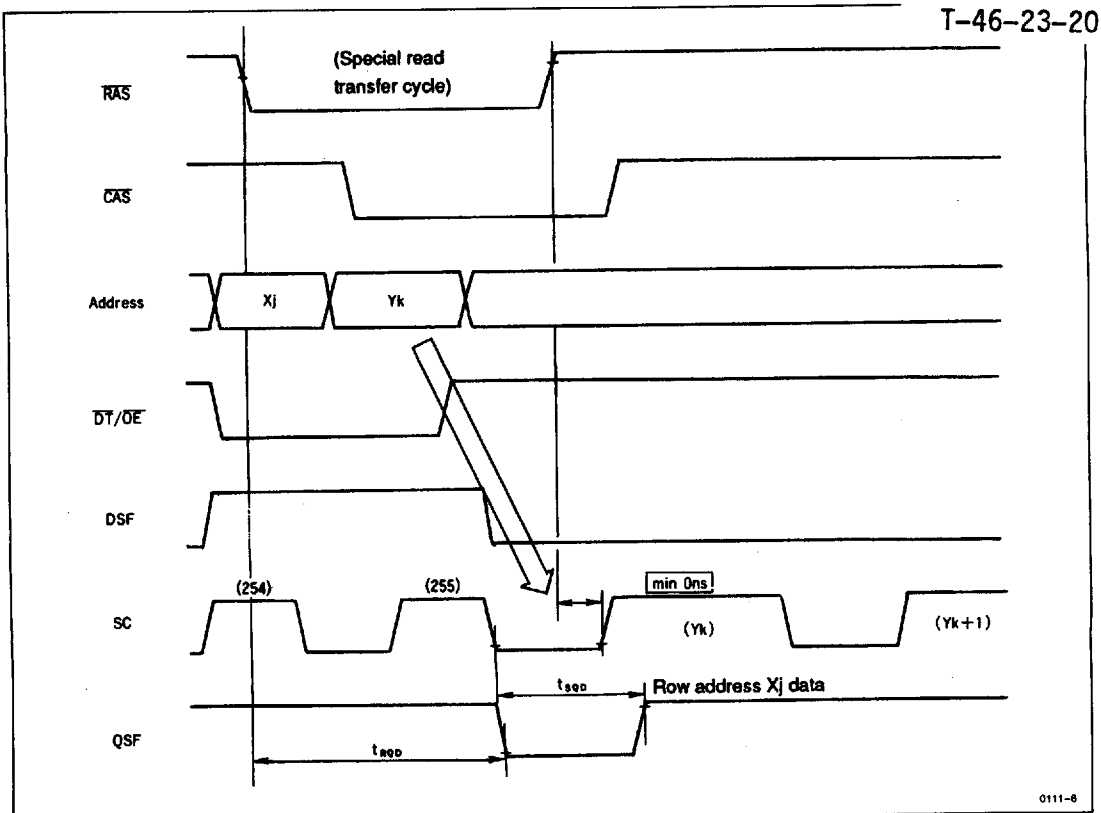

Figure 4. The Restriction of Special Read Transfer

Write Transfer Cycle ($\overline{CAS}$ High, $\overline{DT}/\overline{OE}$ Low, $\overline{WE}$ Low, and $\overline{SE}$ Low at the Falling Edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

• SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is special read initialization cycle or special read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When the last address is accessed at the state of QSF low (data register is full), it is signaled to external circuits that special read transfer is enabled by making QSF high. Next, after SAM access, output data register is switched, then the row address data given by previous special read transfer cycle is output from the SAM start address. If special read transfer isn't performed (QSF high), the column address 0 of the same row address is accessed after the last address is accessed.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data register. Internal pointer is incremented according to the SC rising edge, so SE high can be used to mask data for SAM.

• Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$ only refresh cycle, (2) $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$ Only Refresh Cycle: $\overline{RAS}$ only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. In this cycle, output is high-impedance and power dissipation is less than that of normal read/write cycles because $\overline{CAS}$ internal circuits don't operate. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered like in $\overline{RAS}$ only refresh cycles because $\overline{CAS}$ circuits don't operate.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Terminal Voltage	V_T	−1.0 to +7.0	V	1
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note: 1. Relative to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	1, 2

Notes: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Test Conditions		Note
		Min	Max	Min	Max	Min	Max		RAM Port	SAM Port	
Operating Current	I_{CC1}	—	70	—	60	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC7}	—	120	—	100	—	80	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Standby Current	I_{CC2}	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC8}	—	50	—	40	—	30	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	60	—	50	—	40	mA	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC9}	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Page Mode	I_{CC4}	—	65	—	55	—	45	mA	$\overline{CAS}$ Cycling $\overline{RAS}$ = V_{IL} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC10}	—	115	—	95	—	75	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC5}	—	60	—	50	—	40	mA	$\overline{RAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC11}	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Data Transfer Current	I_{CC6}	—	90	—	90	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC12}	—	125	—	125	—	125	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	

• **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

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Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	μA		
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA		
Output High Voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA	
Output Low Voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

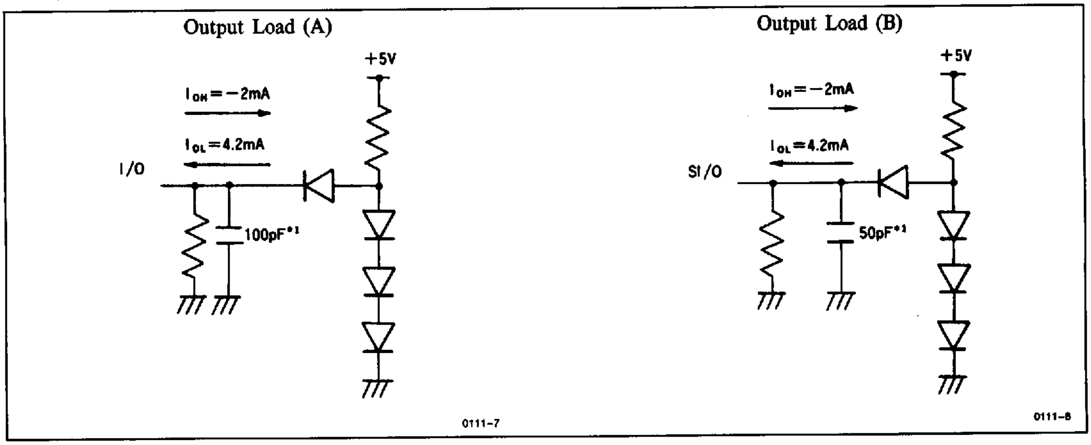
• **Capacitance** (T_A = 25°C, V_{CC} = 5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 11]

Test Conditions

Input Rise and Fall Time:	5 ns
Output Load:	See Figures
Input Timing Reference Levels:	0.8V, 2.4V
Output Timing Reference Levels:	0.4V, 2.4V



Note: 1. Including scope & jig.

Common Parameter

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
RAS Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
RAS Pulse Width	t_{RAS}	10000	100	120	10000	150	10000	ns	
CAS Pulse Width	t_{CAS}	30	10000	35	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
RAS to CAS Delay Time	t_{RCD}	25	70	25	85	30	110	ns	5, 6
RAS Hold Time	t_{RSH}	30	—	35	—	40	—	ns	
CAS Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	3	50	ns	
Refresh Period	t_{REF}	—	8	—	8	—	8	ns	
DT to RAS Setup Time	t_{DTS}	0	—	0	—	0	—	ns	
DT to RAS Hold Time	t_{DTH}	15	—	15	—	20	—	ns	
DSF to RAS Setup Time	t_{SFS}	0	—	0	—	0	—	ns	
DSF to RAS Hold Time	t_{SFH}	25	—	25	—	30	—	ns	
Data-in to OE Delay Time	t_{DZO}	0	—	0	—	0	—	ns	
Data-in to CAS Delay Time	t_{DZC}	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from RAS	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from CAS	t_{CAC}	—	30	—	35	—	40	ns	3, 5
Access Time from OE	t_{OAC}	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	55	—	70	ns	3, 6
Output Buffer Turn-off Delay Referenced to CAS	t_{OFF1}	0	25	0	30	0	40	ns	7
Output Buffer Turn-off Delay Referenced to OE	t_{OFF2}	0	25	0	30	0	40	ns	7
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	12
Read Command Hold Time Referenced to RAS	t_{RRH}	10	—	10	—	10	—	ns	12
RAS to Column Address Delay Time	t_{RAD}	20	55	20	65	25	80	ns	5, 6
Page Mode Cycle Time	t_{PC}	55	—	65	—	80	—	ns	
CAS Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Access Time from CAS Precharge	t_{ACP}	—	50	—	60	—	75	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	35	—	40	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	
Page Mode Cycle Time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	255	—	295	—	350	—	ns	
$\overline{RAS}$ Pulse Width	t_{RWS}	165	10000	195	10000	240	10000	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{CWD}	65	—	75	—	90	—	ns	9
Column Address to $\overline{WE}$ Delay	t_{AWD}	80	—	95	—	120	—	ns	9
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	—	30	—	40	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	55	—	70	ns	3, 6
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	65	25	80	ns	5, 6
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	

Refresh Cycle

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Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

Transfer Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
$\overline{\text{SE}}$ to $\overline{\text{RAS}}$ Setup Time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{\text{SE}}$ to $\overline{\text{RAS}}$ Hold Time	t_{EH}	15	—	15	—	20	—	ns	
$\overline{\text{RAS}}$ to SC Delay Time	t_{SRD}	25	—	30	—	35	—	ns	
SC to $\overline{\text{RAS}}$ Setup Time	t_{SRS}	30	—	40	—	45	—	ns	
$\overline{\text{RAS}}$ to QSF Delay Time	t_{RQD}	—	100	—	120	—	150	ns	4
$\overline{\text{RAS}}$ to QSF (High) Delay Time	t_{RQH}	—	TBD	—	TBD	—	TBD	ns	
Serial Data Input Delay Time from $\overline{\text{RAS}}$	t_{SID}	50	—	60	—	75	—	ns	
Serial Data Input to $\overline{\text{RAS}}$ Delay Time	t_{SZR}	—	10	—	10	—	10	ns	
Serial Output Buffer Turn-off Delay from $\overline{\text{RAS}}$	t_{SRZ}	10	50	10	60	10	75	ns	7
$\overline{\text{RAS}}$ to S_{out} (Low-Z) Delay Time	t_{RLZ}	5	—	10	—	10	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	40	—	50	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	

Serial Read Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	40	—	50	ns	4
Access Time from $\overline{\text{SE}}$	t_{SEA}	—	25	—	30	—	40	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{\text{SE}}$	t_{SEZ}	0	25	0	25	0	30	ns	7
Last SC to QSF Delay Time	t_{SQD}	—	TBD	—	TBD	—	TBD	ns	4

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Serial Write Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	60	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	35	—	50	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	30	—	35	—	50	—	ns	

Flash Write Cycle

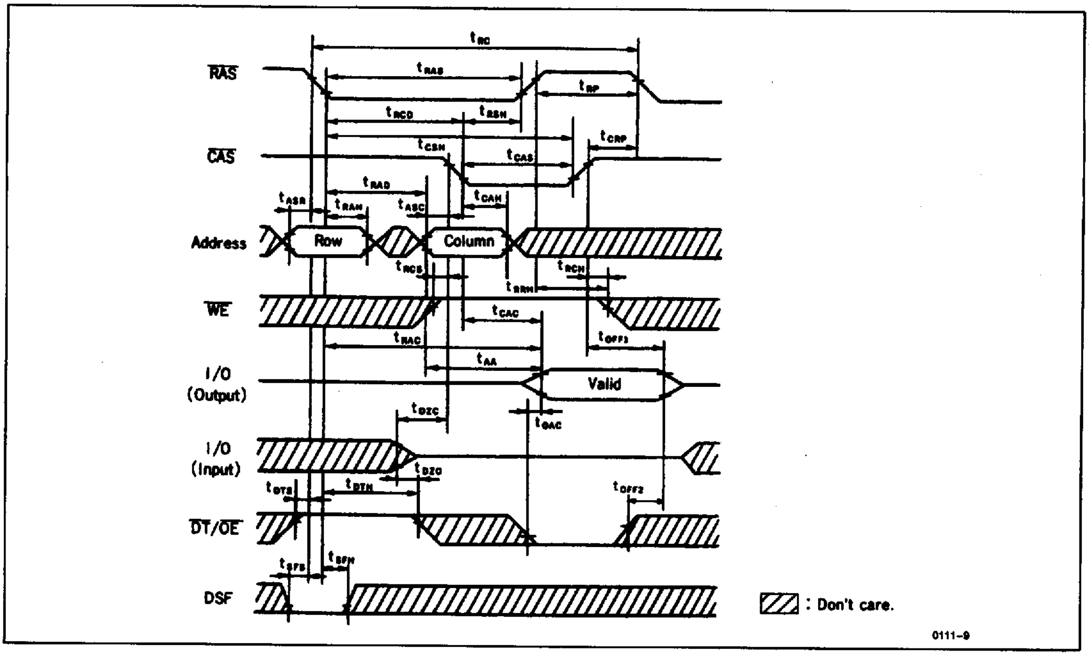
Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Flash Write Cycle Write	t_{RCFW}	230	—	265	—	310	—	ns	
$\overline{RAS}$ Pulse Width	t_{RCSFW}	140	—	165	—	200	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
$\overline{CAS}$ High Level Hold Time Reference to $\overline{RAS}$	t_{CHHR}	20	—	25	—	30	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	

Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assume that $t_{RCD} \le t_{RCD}$ (max) and $t_{RAD} \le t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL load and 100 pF.
4. Measured with a load circuit equivalent to 2 TTL load and 50 pF.
5. When $t_{RCD} \ge t_{RCD}$ (max) and $t_{RAD} \le t_{RAD}$ (max), access time is specified by t_{CAC}.
6. When $t_{RCD} \le t_{RCD}$ (max) and $t_{RAD} \ge t_{RAD}$ (max), access time is specified by t_{AA}.
7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} − 200 mV, V_{OL} + 200 mV).
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
9. When $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \ge t_{AWD}$ (min) and $t_{CWD} \ge t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data out pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
11. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.

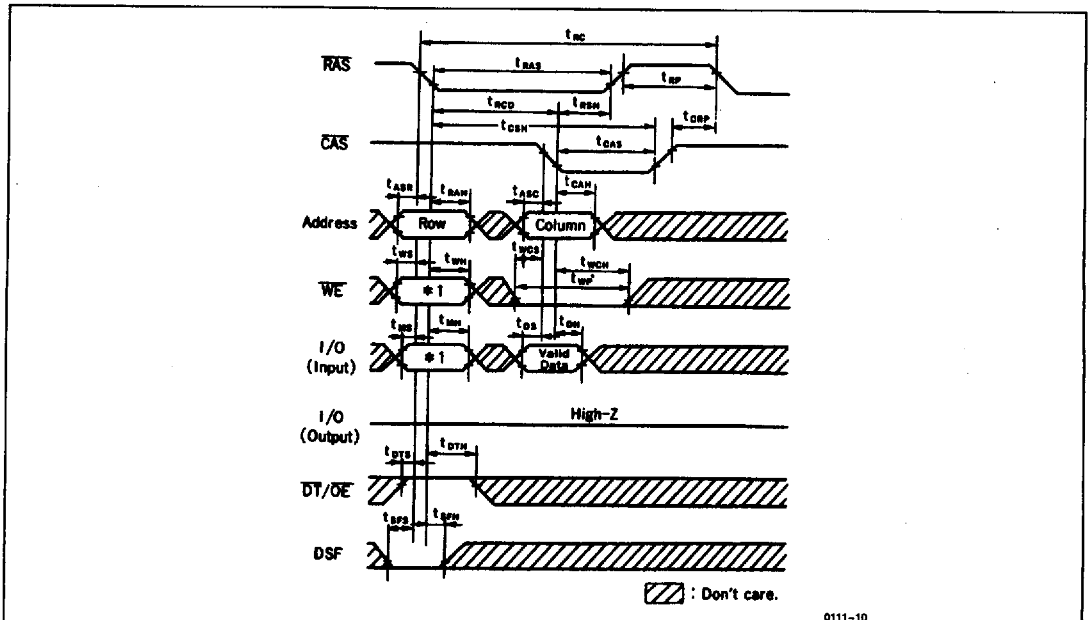
■ TIMING WAVEFORMS

T-46-23-20

• **Read Cycle**



• **Early Write Cycle**



Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Delayed Write Cycle**

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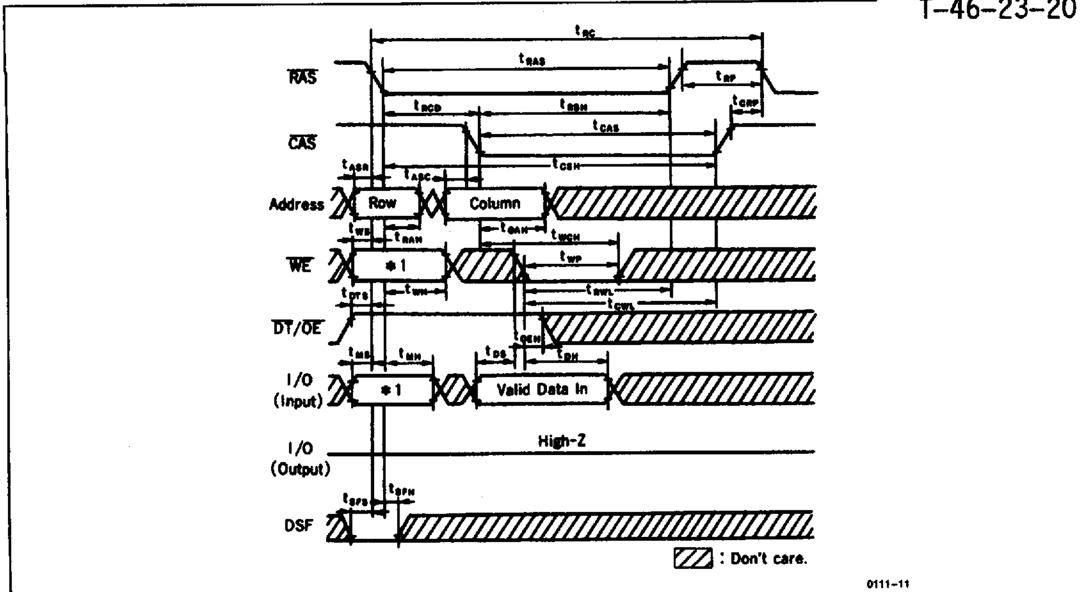
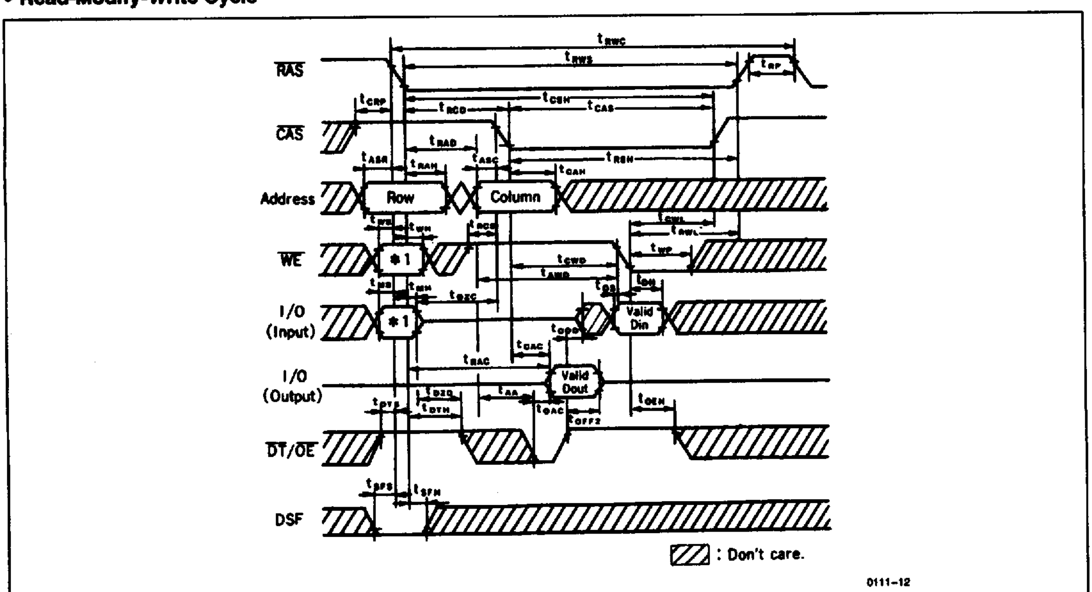


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Read-Modify-Write Cycle**



Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Page Mode Read Cycle**

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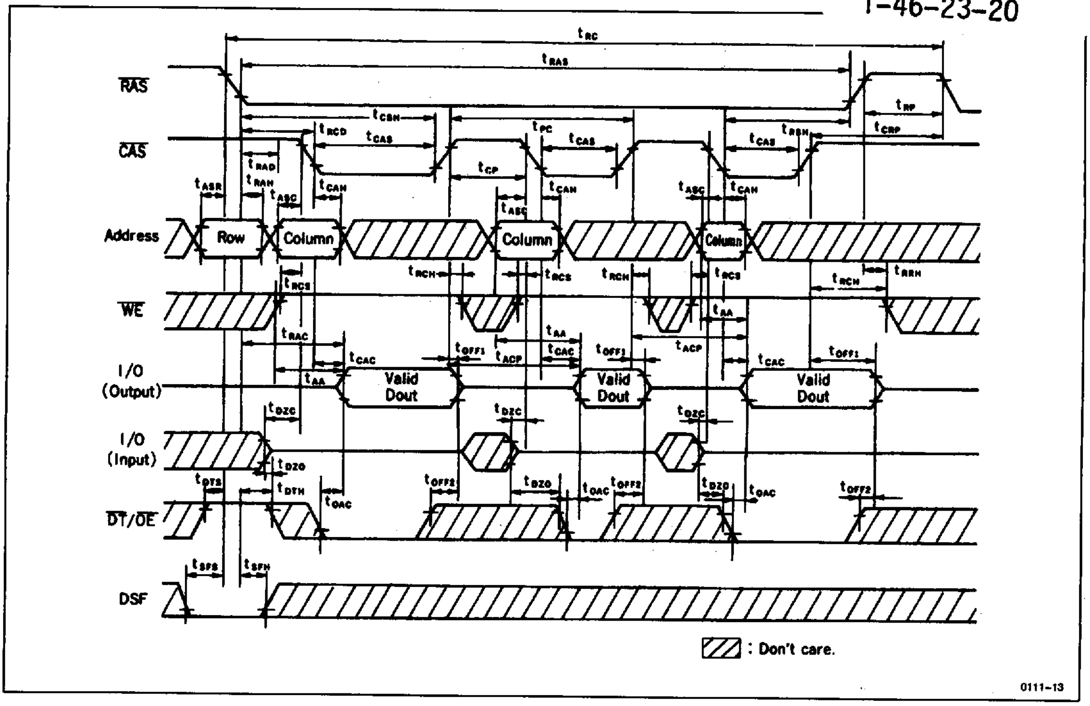
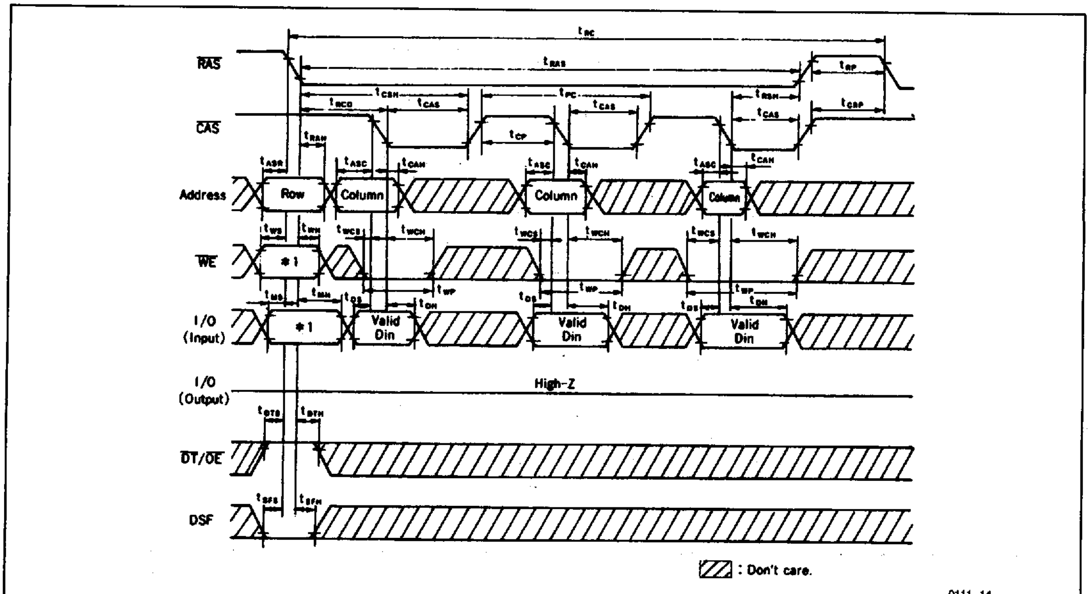


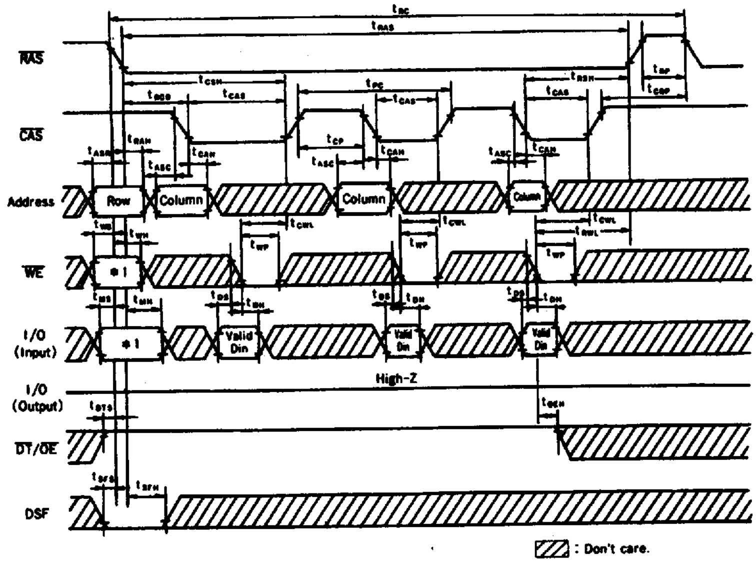
• **Page Mode Write Cycle (Early Write)**



Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

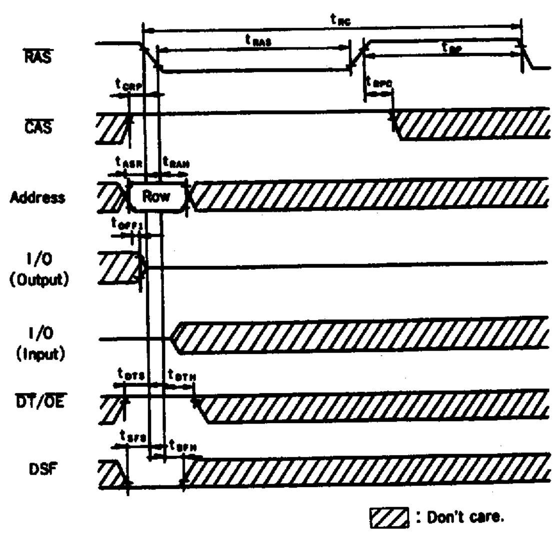
• **Page Mode Write Cycle (Delayed Write)**

T-46-23-20



Note: 1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **$\overline{RAS}$ Only Refresh Cycle**



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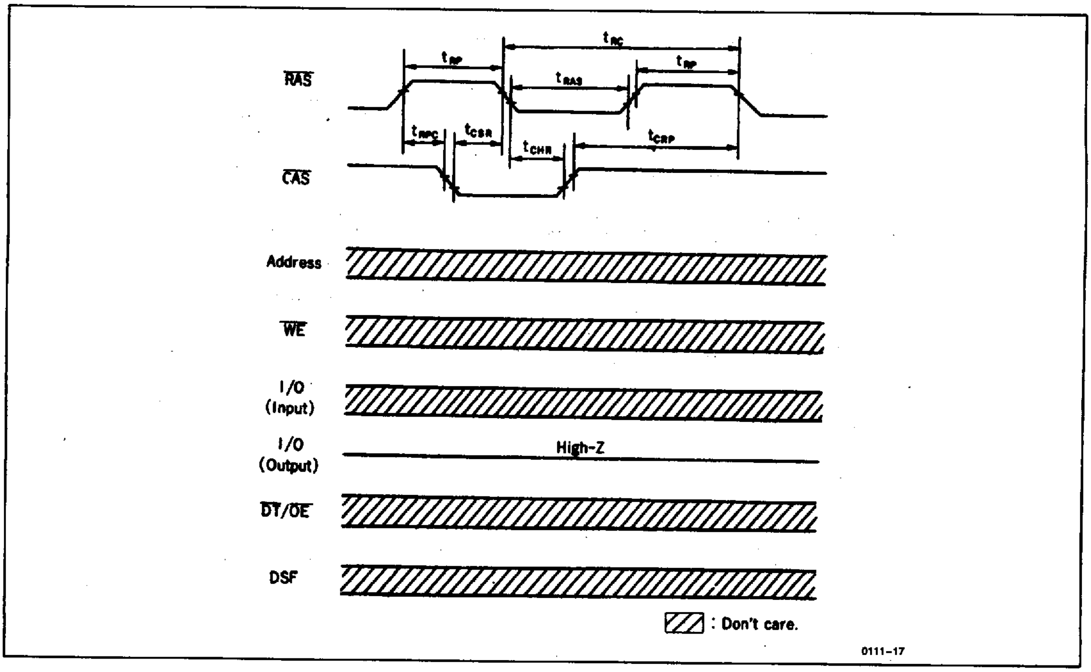
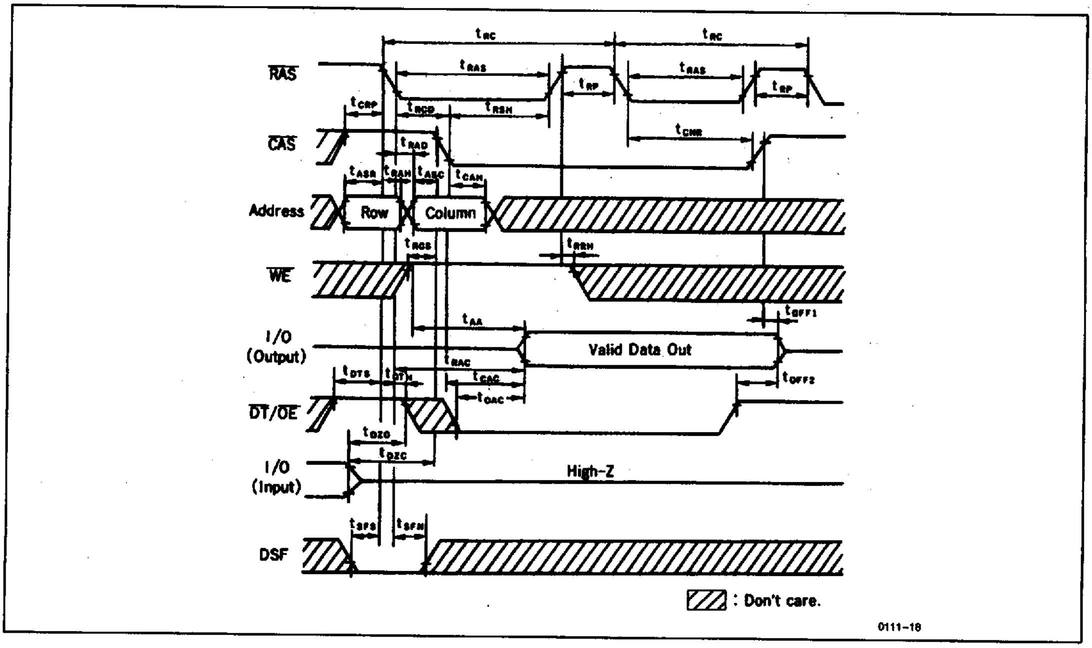
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• Hidden Refresh Cycle



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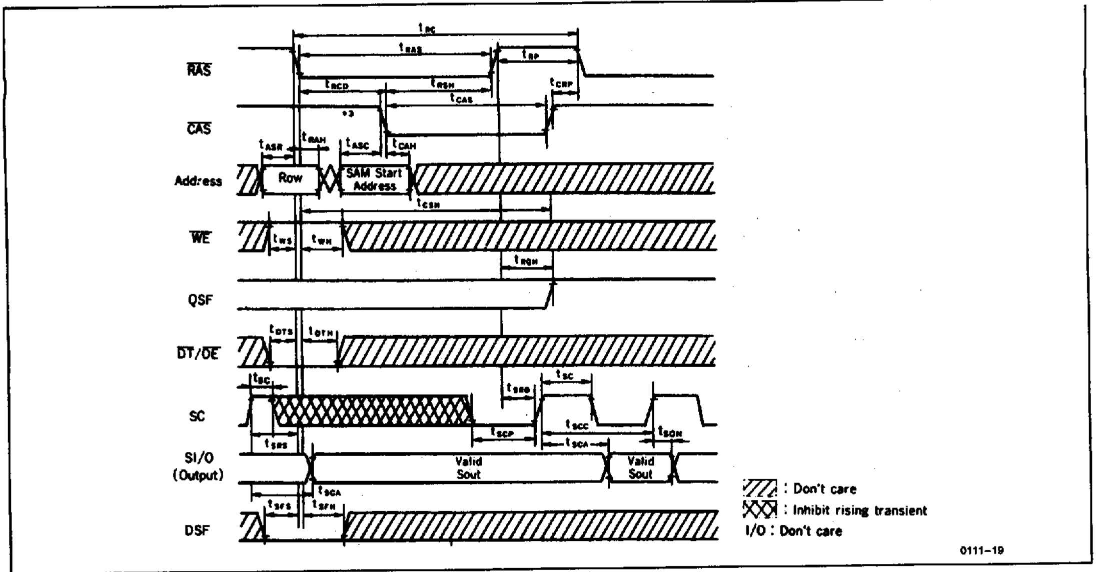
• **Special Read Initialization Cycle (1)*1, *2**

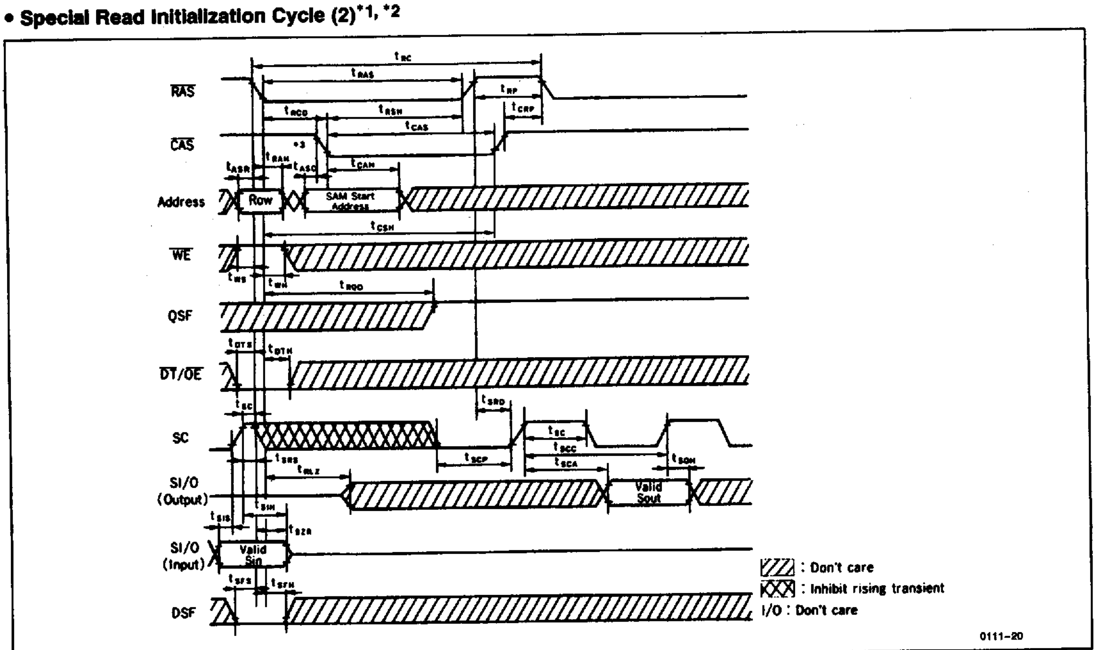


Notes: *1. When the previous data transfer cycle is a special read transfer cycle or special read initialization cycle, it is specified as special read initialization cycle (1).

*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)

*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Special Read Initialization Cycle (2)*1, *2**



Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is specified as special read initialization cycle (2).

*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)

*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Special Read Transfer Cycle** *1, *2

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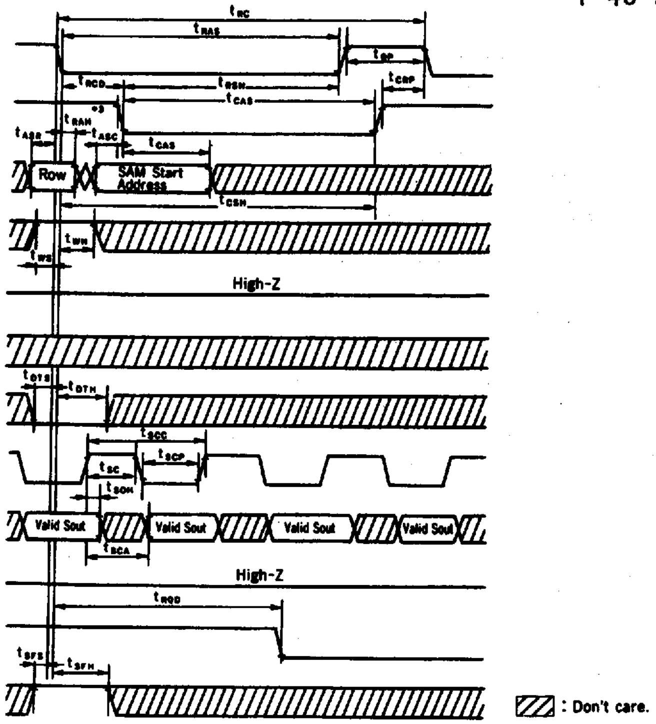
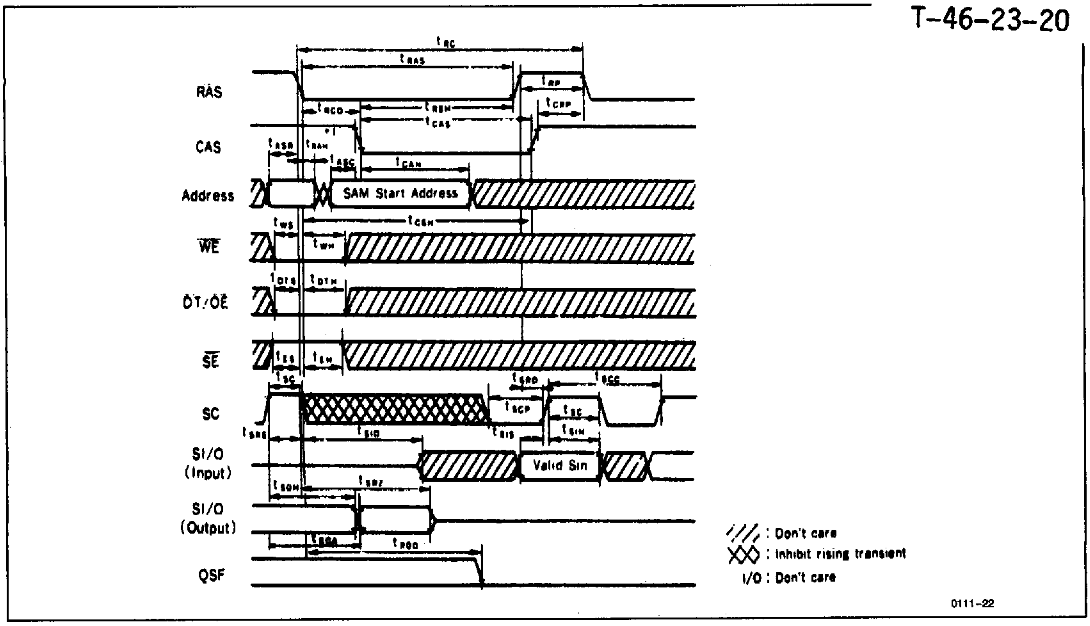


Notes: *1. When QSF is low level at the falling edge of $\overline{RAS}$, the special read transfer cycle is not performed.
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

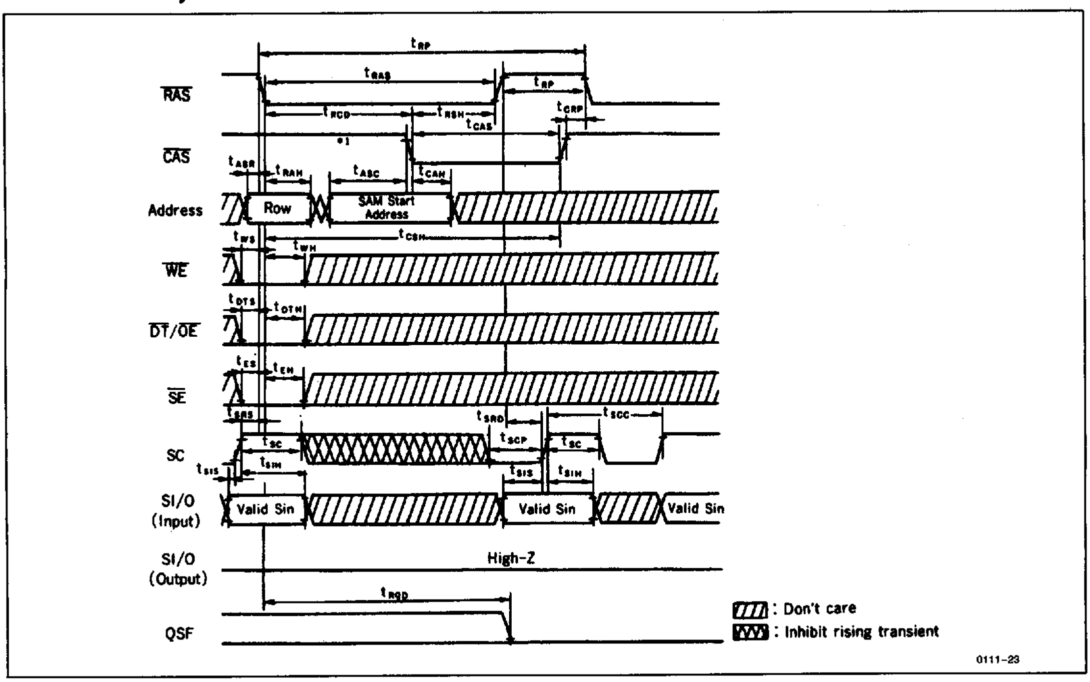
• **Pseudo Transfer Cycle**

T-46-23-20



Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

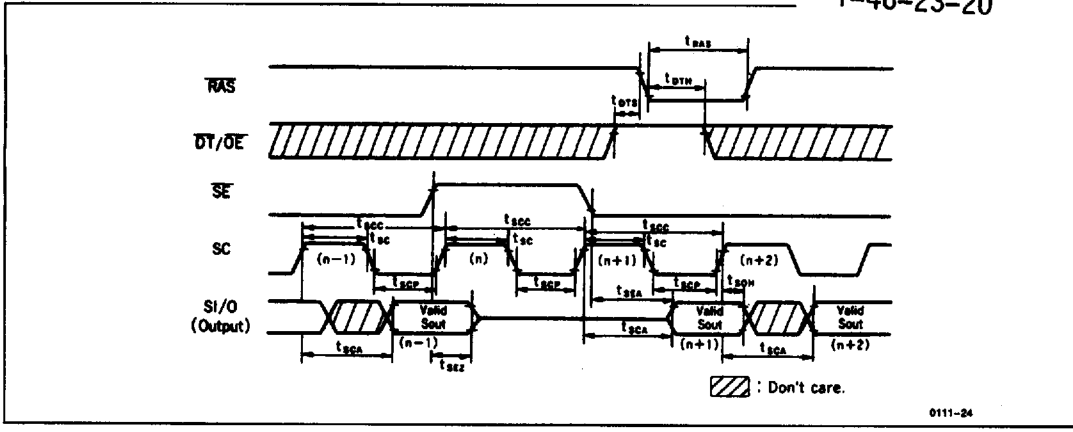
• **Write Transfer Cycle**



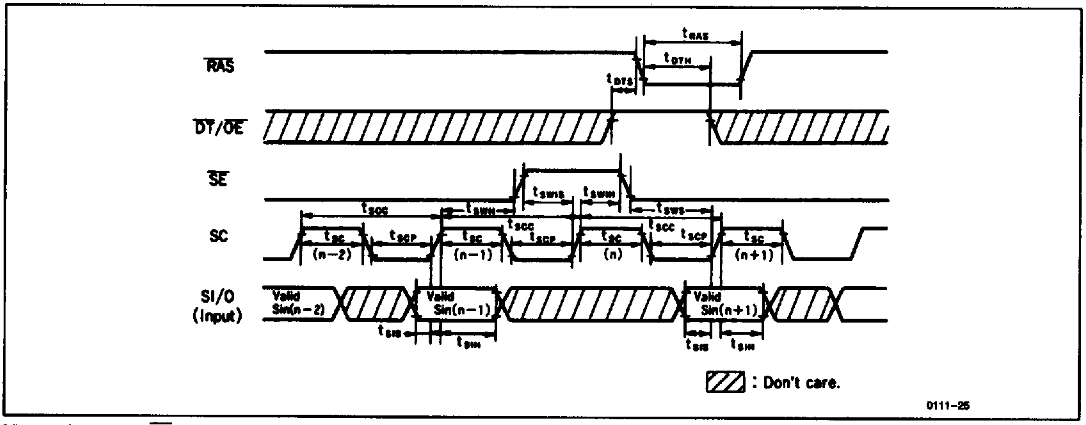
Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Serial Read Cycle**

T-46-23-20



• **Serial Write Cycle** *1, *2



Note: *1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
*2. Address 0 is accessed next to address 255.

• **Serial Read Cycle (Around Address 255 in SAM)**

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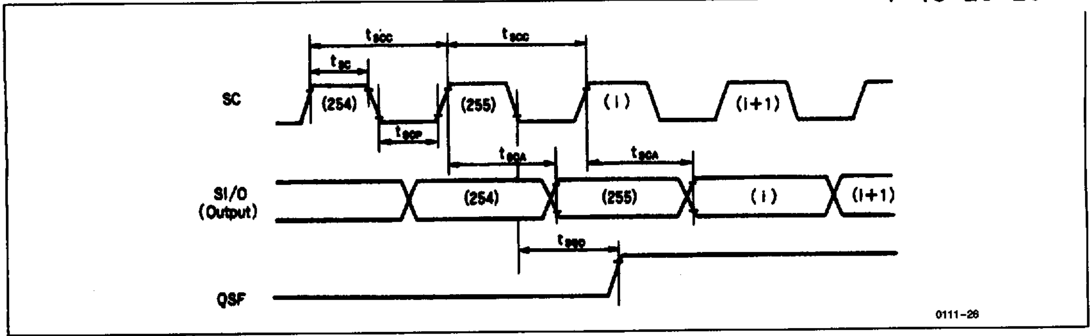
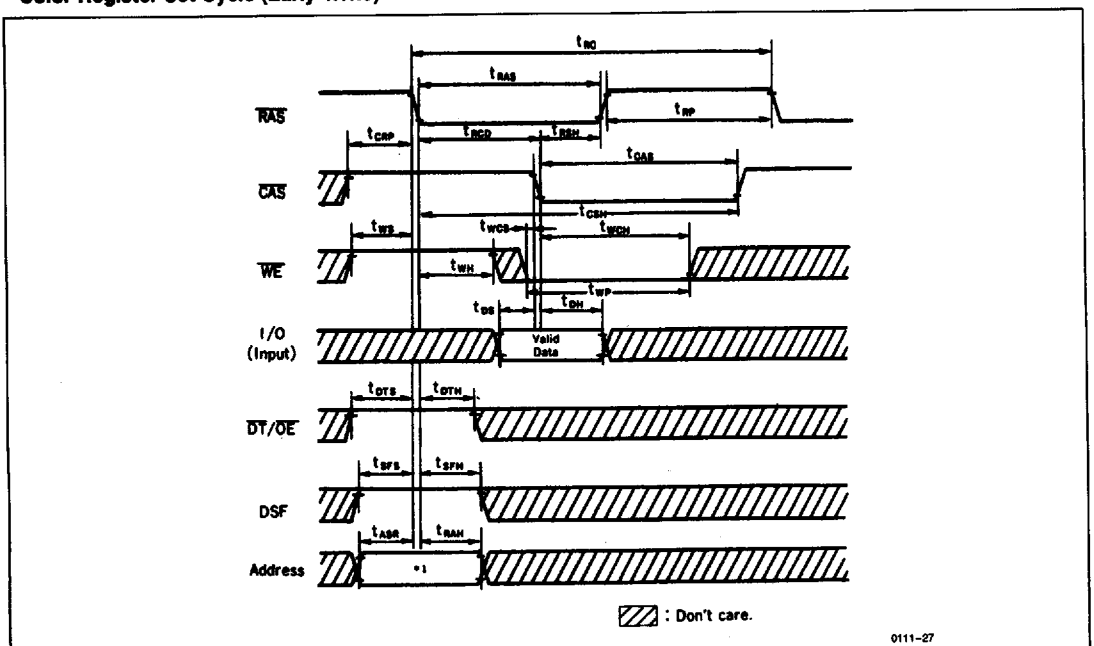


Note: *1. Address (i) is the SAM start address provided in the previous special read transfer cycle. When special read transfer cycle isn't executed (QSF remains in high level), address 0 is accessed next to address 255.

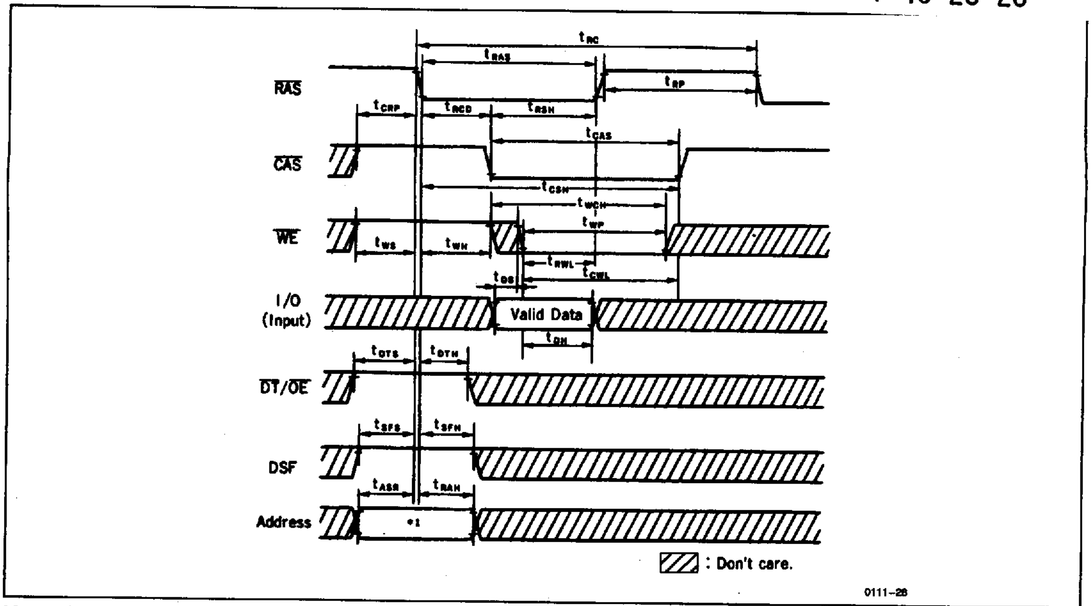
• **Color Register Set Cycle (Early Write)**



Note: *1. The level of address pin is don't care, but cannot be changed in this period.

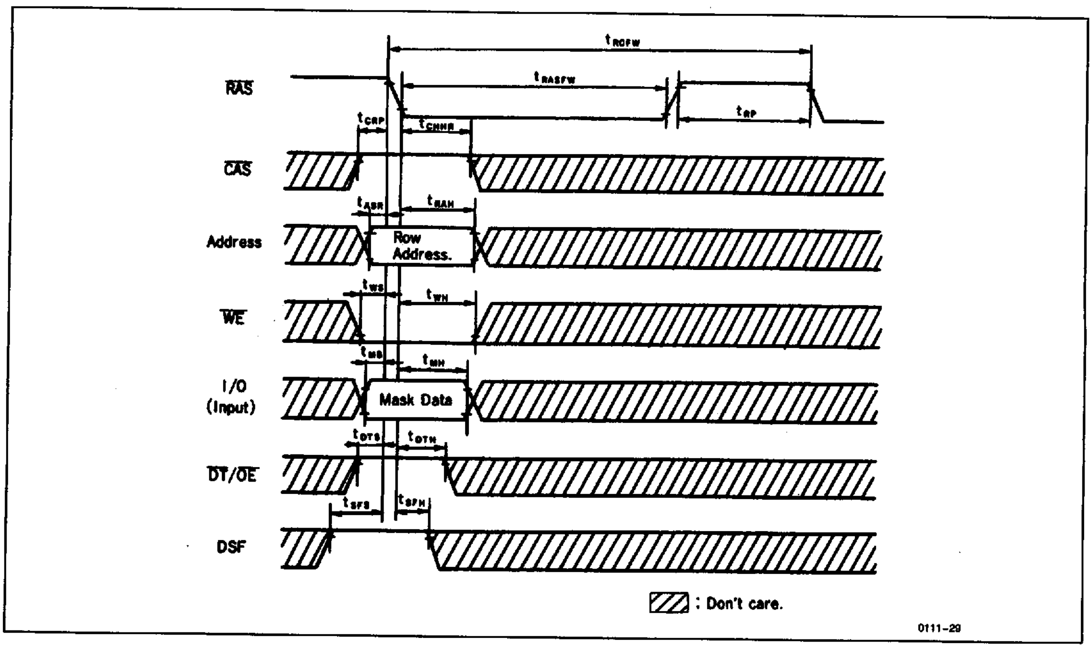
Color Register Set Cycle (Delayed Write)

T-46-23-20



Note: *1. The level of address pin is don't care, but cannot be changed in this period.

• Flash Write Cycle



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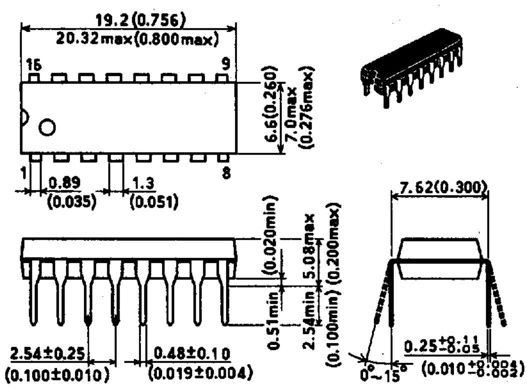
■ PACKAGE INFORMATION

T-90-20

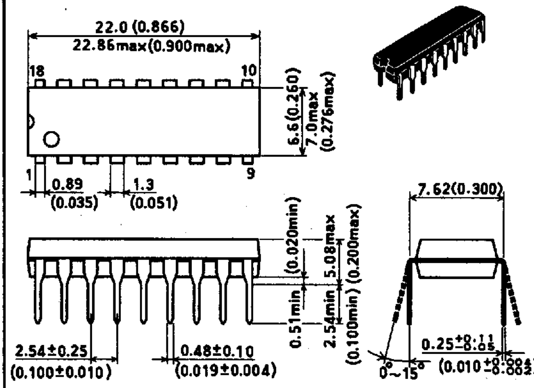
• **Dual-in-line Plastic**

Unit: mm (inch) Scale 3/2

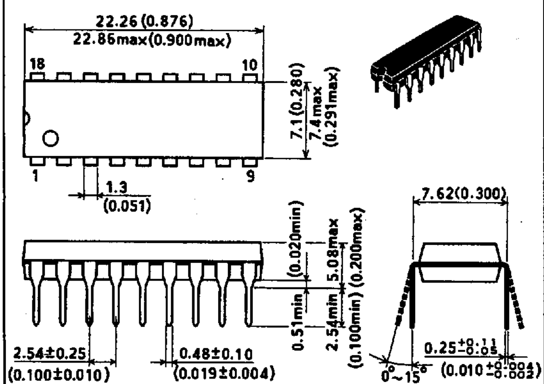
• **DP-16B**



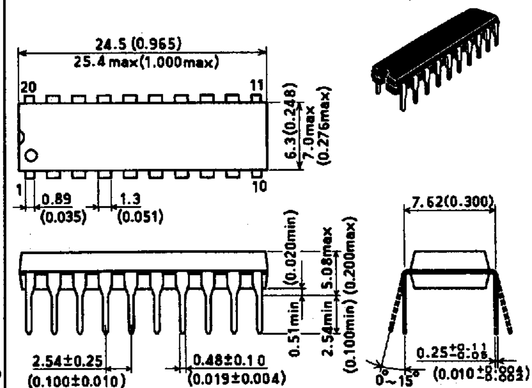
• **DP-18B**



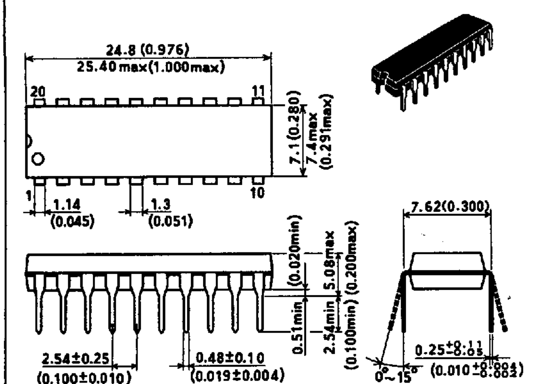
• **DP-18C**



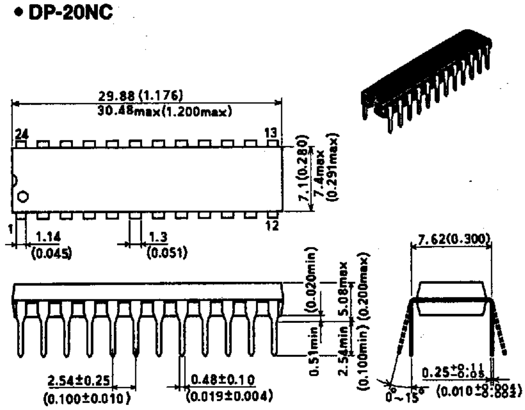
• **DP-20N**



• **DP-20NA**



• **DP-20NC**

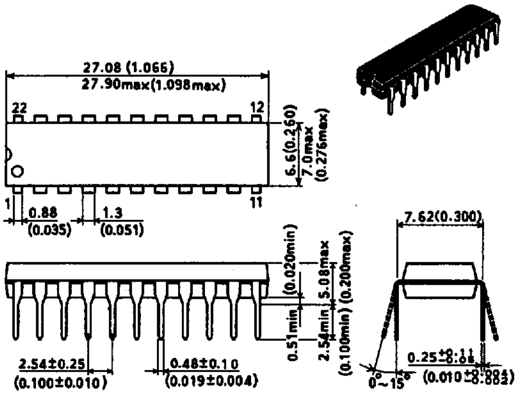


• Dual-in-line Plastic

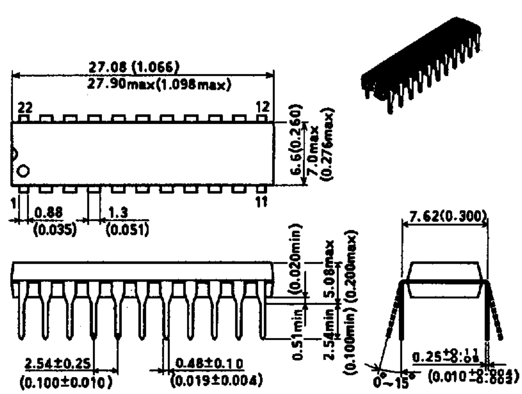
Unit: mm (inch) Scale 3/2

T-90-20

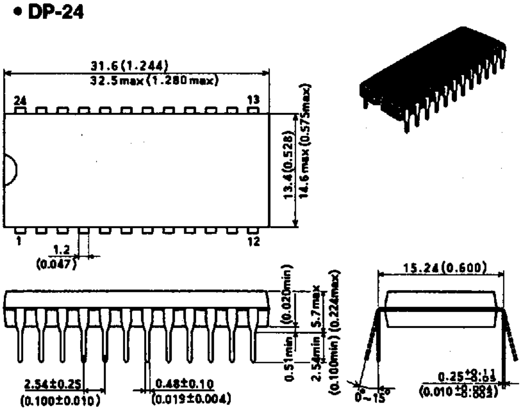
• DP-22N



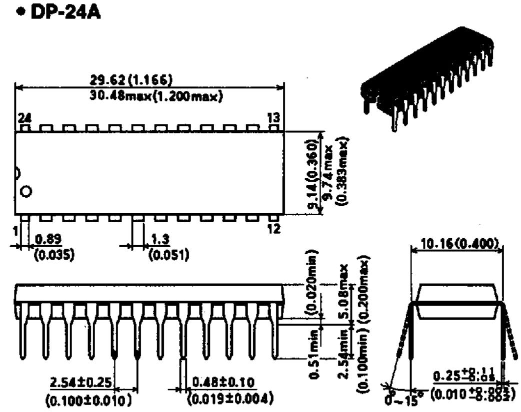
• DP-22NB



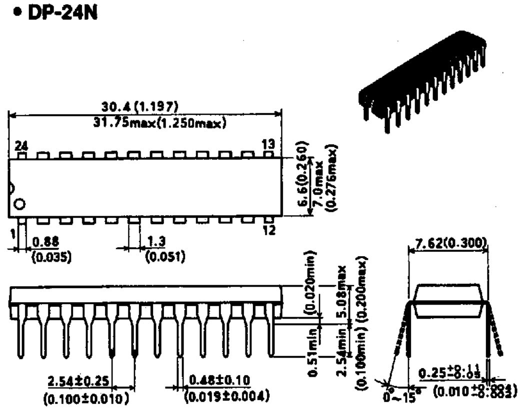
• DP-24



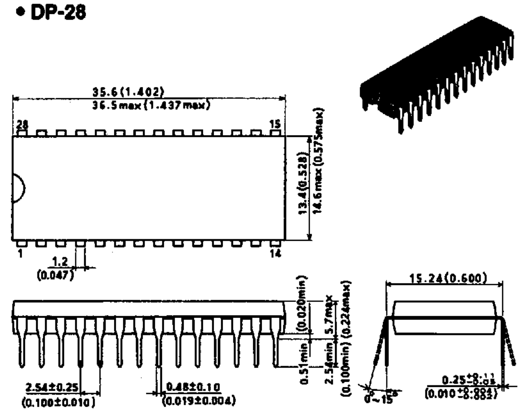
• DP-24A



• DP-24N



• DP-28



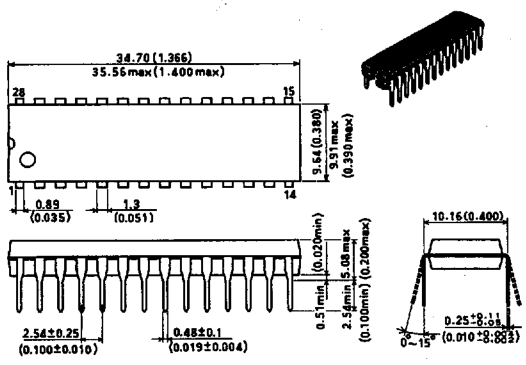
HITACHI/ LOGIC/ARRAYS/MEM

T-90-20

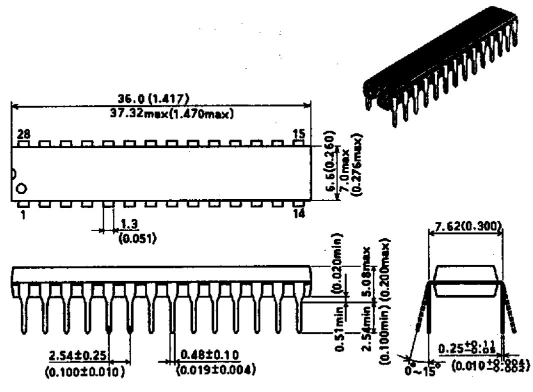
• Dual-in-line Plastic

Unit: mm (inch) Scale 3/2

• DP-28C



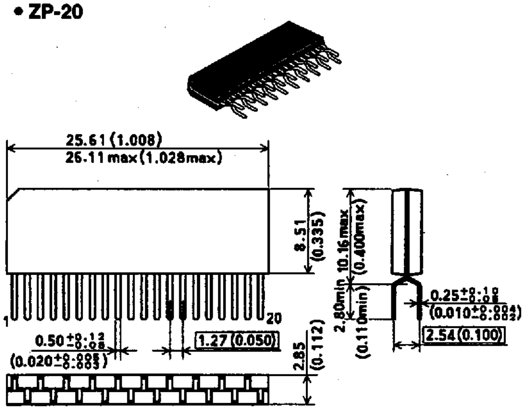
• DP-28N



• **Zigzag-in-line Plastic** HITACHI/ LOGIC/ARRAYS/MEM

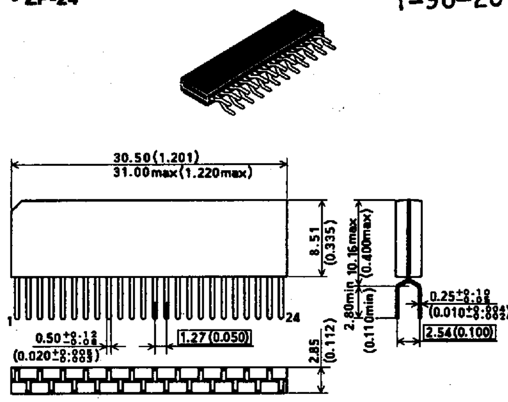
Unit: mm (inch) Scale 3/2

• **ZP-20**

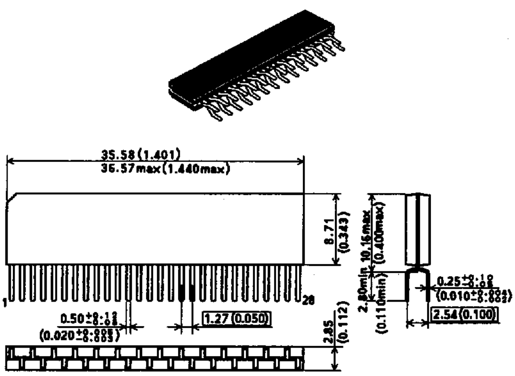


• **ZP-24**

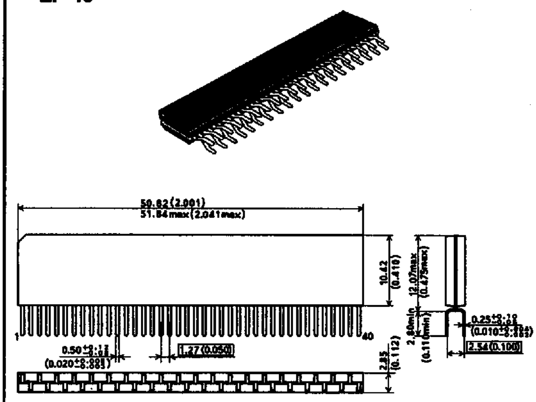
T-90-20



• **ZP-28**



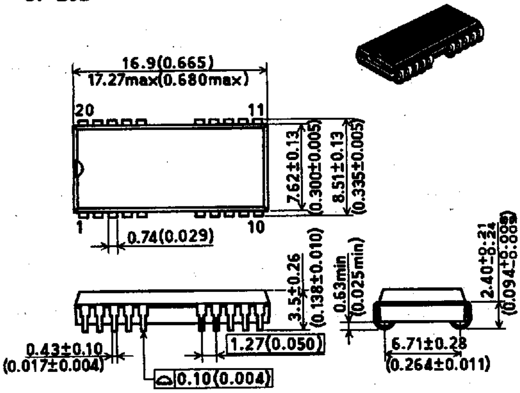
• **ZP-40**



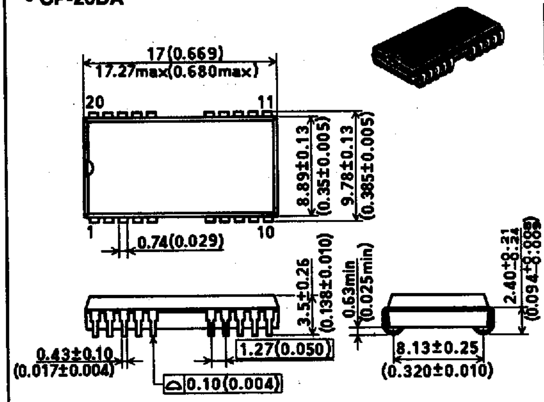
• **Flat Package (J-bend Leads)** HITACHI/ LOGIC/ARRAYS/MEM Unit: mm (inch) Scale 3/2

T-90-20

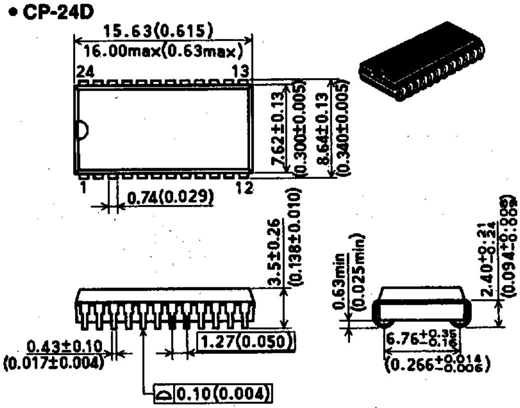
• **CP-20D**



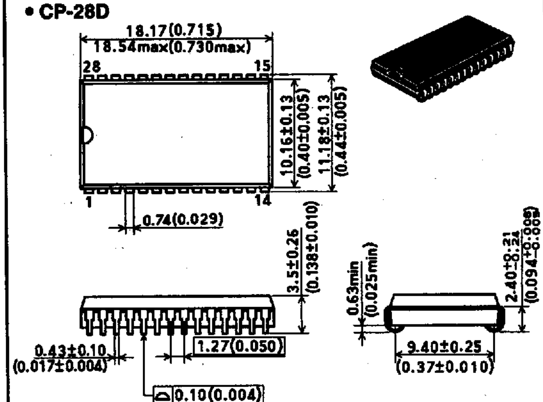
• **CP-20DA**



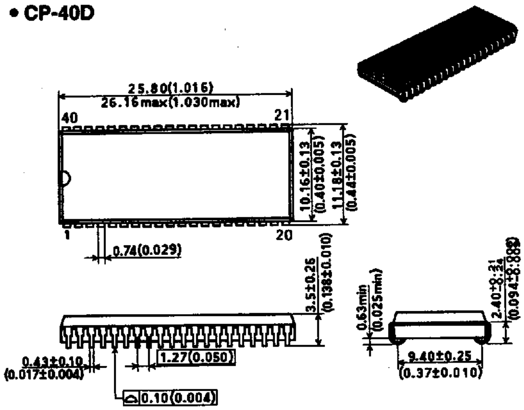
• **CP-24D**



• **CP-28D**



• **CP-40D**

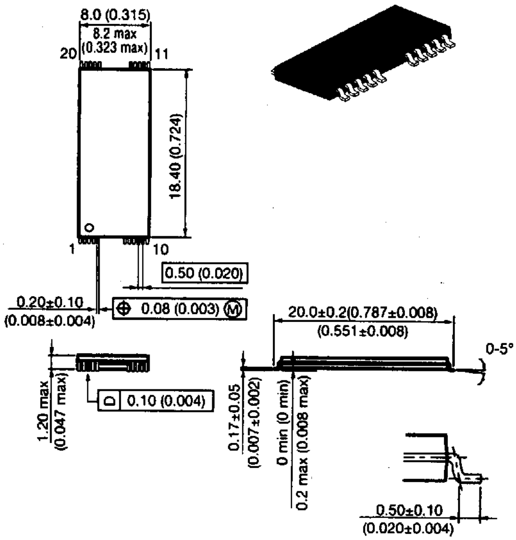


• TSOP (Thin Small Outline Package)

HITACHI/ LOGIC/ARRAYS/MEM

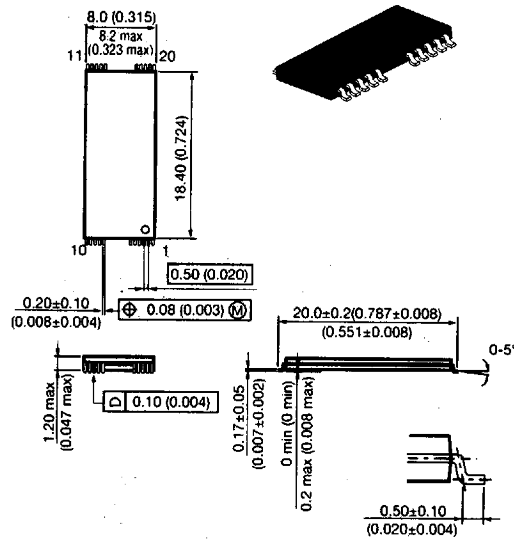
Unit: mm (inch) Scale 3/2

• TFP-20DA

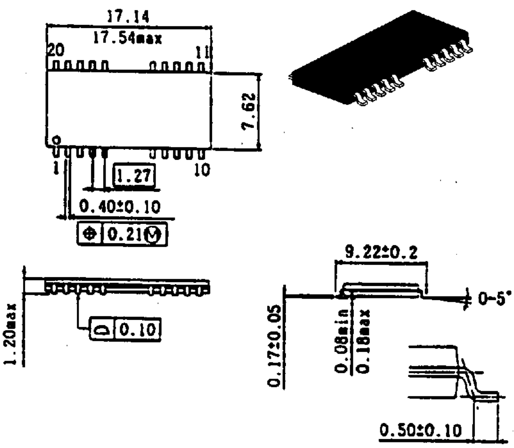


• TFP-20DAR

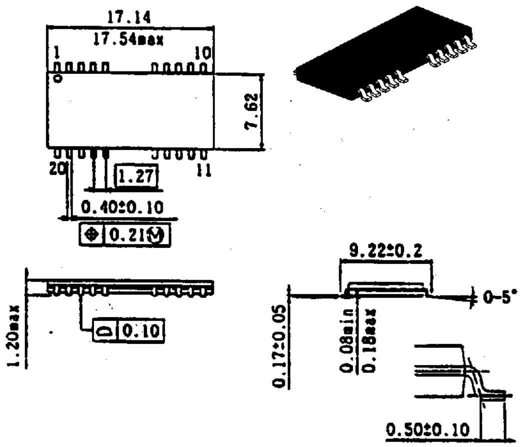
T-90-20



• TTP-20D



• TTP-20DR



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Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300