IS27LV512

65,536 x 8 LOW VOLTAGE CMOS EPROM

NOVEMBER 1997

FEATURES

- Single 2.7V to 3.6V power supply
- Fast access time: 90 ns
- JEDEC-approved pinout
- Low power consumption
  - — 20 µA (max) standby current
  - — 8 mA (max) active current at 5 MHz
- High-speed write programming
  - — Typically less than eight seconds
- Industrial and commercial temperature ranges available
- Standard 28-pin DIP and TSOP, and 32-pin PLCC packages

DESCRIPTION

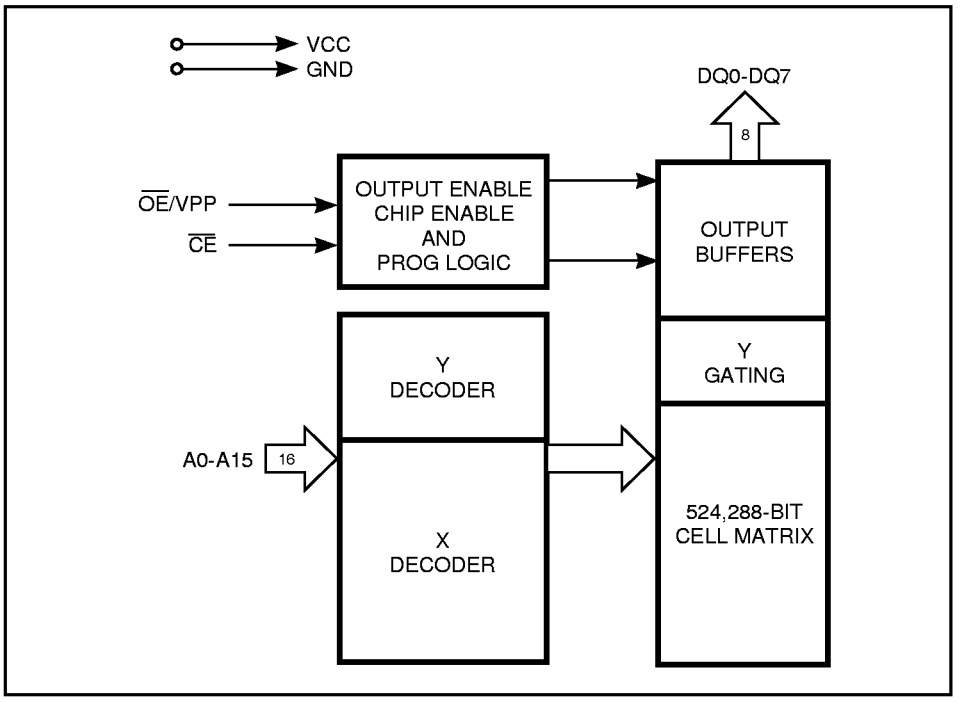
The *ISSI* IS27LV512 is a low voltage, low power, high-speed 512K-bit CMOS (64K-word by 8-bit) CMOS Programmable Read-Only Memory. It utilizes the standard JEDEC pinout making it functionally compatible with the IS27C512 EPROM.

The superior access time combined with low power consumption is the result of innovative design and process technology. If the device is constantly accessed at 5 MHz, the maximum power consumption is increased to 36 mW. These power ratings are significantly lower than the standard IS27C512 EPROM.

The IS27LV512 uses *ISSI*'s write programming algorithm which allows the entire chip to be programmed in typically less than thirty seconds.

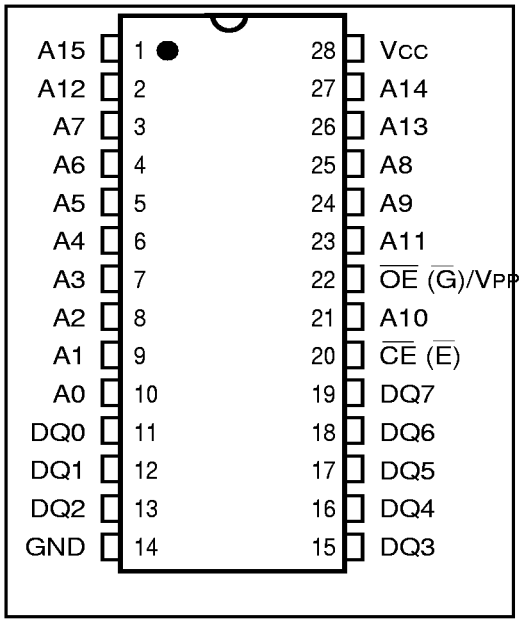
This product is available in One-Time Programmable (OTP) PDIP, PLCC, and TSOP packages over commercial and industrial temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

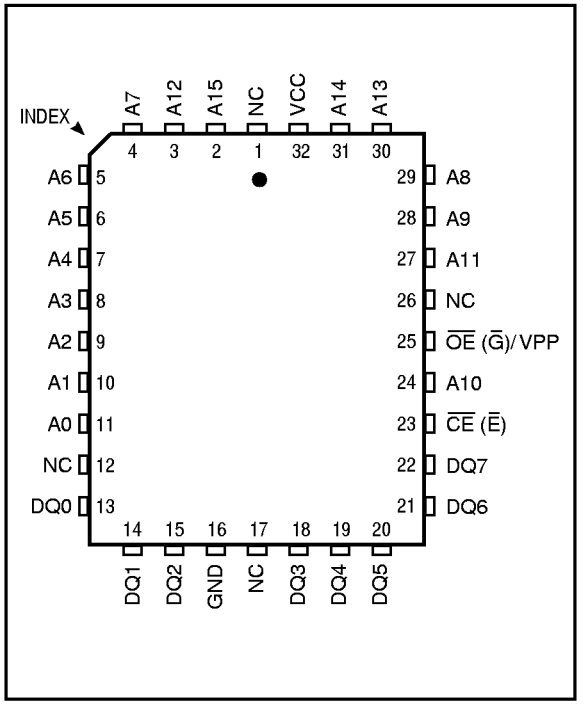
28-Pin DIP



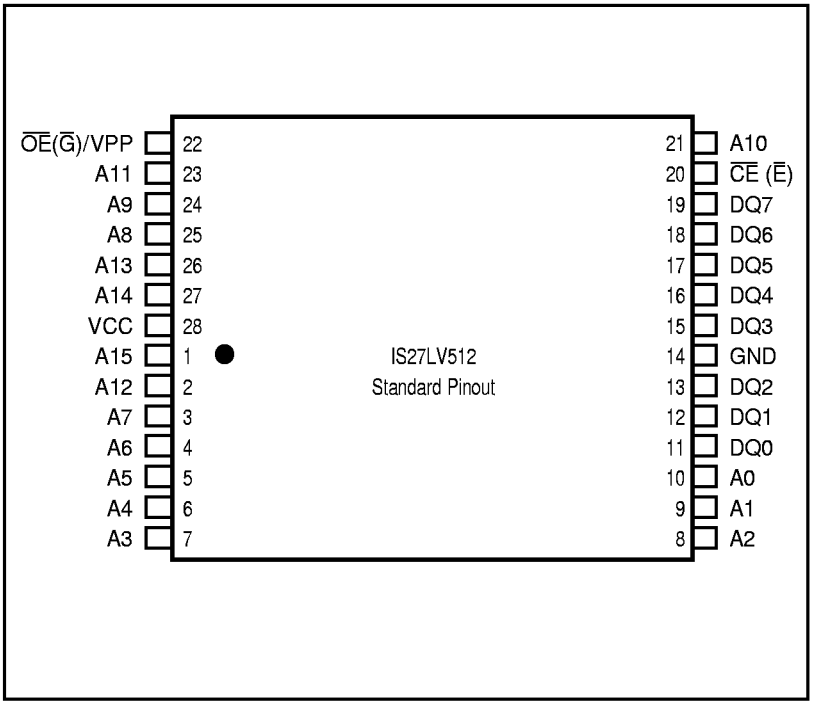
PIN DESCRIPTIONS

A0-A15	Address Inputs
$\overline{CE}$ ($\overline{E}$)	Chip Enable Input
DQ0-DQ7	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)/ VPP	Output Enable Input/ Program Voltage Input
Vcc	Power Supply Voltage
GND	Ground
NC	No Internal Connection

32-Pin PLCC



28-Pin TSOP



FUNCTIONAL DESCRIPTION

Programming the IS27LV512

Upon delivery, the IS27LV512 has 524,288 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the IS27LV512 through the procedure of programming.

The programming mode is entered when 12.5 ± 0.25V is applied to the $\overline{OE}$/V_{PP} pin, V_{CC} = 6V and $\overline{CE}$ is at V_{IL}. For programming, the data to be programmed is applied eight bits in parallel to the data output pins.

The write programming algorithm reduces programming time by using 100 µs programming pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The write programming algorithm programs and verifies at V_{CC} = 6V and $\overline{OE}$/V_{PP} = 12.5V. After the final address is completed, all byte are compared to the original data with V_{CC} = 5.25V.

Program Inhibit

Programming of multiple IS27LV512s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel IS27LV512 may be common. A TTL low-level program pulse applied to an IS27LV512 $\overline{CE}$ input with $\overline{OE}$/V_{PP} = 12.5 ± 0.25V will program that IS27LV512. A high-level $\overline{CE}$ input inhibits the other IS27LV512 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{CE}$ at V_{IL} and $\overline{OE}$/V_{PP} at V_{IL}.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the IS27LV512.

To activate this mode, the programming equipment must force 12.0 ± 0.5V on address line A9 of the IS27LV512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and byte 1 (A0 = V_{IH}), the device identifier code. For the IS27LV512, these two identifier bytes are given in the Mode Select table. All identifiers manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The IS27LV512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Output Enable ($\overline{OE}$) is the output control and should be used to get data to the output pins, independent of device selection. Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$ assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The IS27LV512 has a standby mode which reduces the maximum V_{CC} active current. It is placed in standby mode when $\overline{CE}$ is at V_{IH}. The amount of current drawn in standby mode depends on the frequency and the number of address pins switching. The IS27LV512 is specified with 50% of the address lines toggling at 5 MHz. A reduction of the frequency or quantity of address lines toggling will significantly reduce the actual standby current.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$/ V_{PP} be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

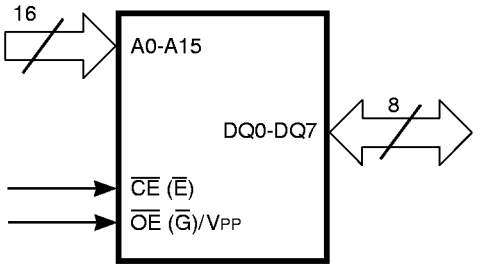
During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device at a minimum, a 0.1 µF ceramic capacitor (high-frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

TRUTH TABLE[1,2,4]

Mode		$\overline{CE}$	$\overline{OE}$/ V_{PP}	A0	A9	Outputs
Read		V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable		X	V_{IH}	X	X	Hi-Z
Standby		V_{IH}	X	X	X	Hi-Z
Program		V_{IL}	V_{PP}	X	X	D_{IN}
Program Verify		V_{IL}	V_{IL}	X	X	D_{OUT}
Program Inhibit		V_{IH}	V_{PP}	X	X	Hi-Z
Auto Select[3,5]	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	D5H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	91H

Notes:
1. V_H = 12.0V ± 0.5V.
2. X = Either V_{IH} or V_{IL}.
3. A1-A8 = A10-A15 = V_{IL}.
4. See DC Programming Characteristics for V_{PP} voltage during programming.
5. The IS27LV512 can use the same write algorithm during program as other IS27C512 or IS27512 devices.

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND		
	All pins except A9 and V_{PP}	–0.6 to V_{CC} + 0.5[2]	V
	V_{PP}	V_{CC} – 0.3 to 13.5[2,3]	V
	A9	–0.6 to 13.5[2,3]	V
	V_{CC}	–0.6 to 7.0[2]	V
T_A	Ambient Temperature with Power Applied	–65 to +125	°C
T_{STG}	Storage Temperature (OTP)	–65 to +125	°C
T_{STG}	Storage Temperature (All others)	–65 to +150	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods less than 10 ns. Maximum DC voltage on output pins is Vcc + 0.5V which may overshoot to Vcc + 2.0V for periods less than 10 ns.
3. Maximum DC voltage on A9 or V_{PP} may overshoot to +13.5V for periods less than 10 ns.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.7 to 3.6V
Industrial[1]	–40°C to +85°C	2.7 to 3.6V

Note:
1. Operating ranges define those limits between which the functionally of the device is guaranteed.

DC ELECTRICAL CHARACTERISTICS[1,2,3] (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –400 µA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA	—	0.45	V
V_{IH}	Input HIGH Voltage[4]		2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[4]		–0.3	0.8	V
I_{LI}	Input Load Current	V_{IN} = 0V to +V_{CC}	—	5.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to +V_{CC}	—	10	µA

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. Never try to force V_{PP} LOW to 1V below V_{CC}. Manufacturer suggests to tie V_{PP} and V_{CC} together during the READ operation.
2. **Caution:** the IS27LV512 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
3. Minimum DC input voltage is –0.5V. During transitions, the inputs may undershoot to –2.0V for periods less than 10 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2.0V for periods less than 10 ns.
4. Tested under static DC conditions.

POWER SUPPLY CHARACTERISTICS[1,2,4] (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
I_{CC1}	Vcc Operating Supply Current[3]	V_{CC} = Max., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = 5 MHz (Open outputs)	Commercial Industrial	— —	8 10	mA
I_{CCSB0}	Vcc CMOS Standby Current	$\overline{CE} \geq V_{CC} - 0.3V$ All pins $\geq V_{CC} - 0.3V$ or $\leq 0.3V$ toggling f $\leq$ 5 MHz		—	20	µA
I_{CCSB1}	Vcc TTL Standby Current	$\overline{CE} \geq V_{IH}$ All pins = V_{IH} or V_{IL} (TTL level) toggling f $\leq$ 5 MHz		—	1	mA

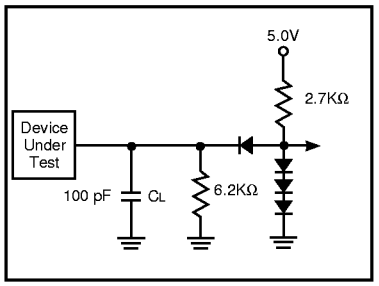
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. Never try to force V_{PP} LOW to 1V below Vcc. Manufacturer suggests to tie V_{PP} and V_{CC} together during the READ operation.
2. **Caution:** the IS27LV512 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
3. I_{CC1} is tested with $\overline{OE}/V_{PP}$ = V_{IH} to simulate open outputs.
4. Minimum DC input voltage is –0.5V. During transitions, the inputs may undershoot to –2.0V for periods less than 10 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2.0V for periods less than 10 ns.

CAPACITANCE[1,2,3]

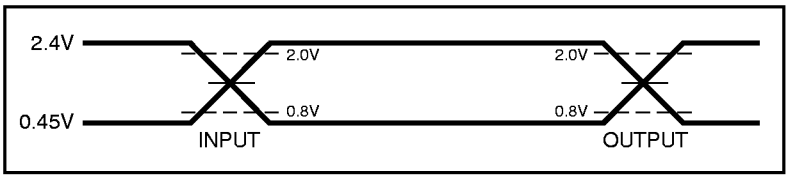
			DIP		PLCC/TSOP		
Symbol	Parameter	Conditions	Typ.	Max.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	6	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	6	9	pF
C_{IN} $\overline{OE}/V_{PP}$	$\overline{OE}/V_{PP}$ Capacitance	$\overline{OE}/V_{PP}$ = 0V	12	15	12	15	pF

Notes:
1. Typical values are for nominal supply voltage.
2. This parameter is only sampled, but not 100% tested.
3. Test conditions: T_A = 25°C, f = 1 MHz.

SWITCHING TEST CIRCUIT



SWITCHING TEST WAVEFORM



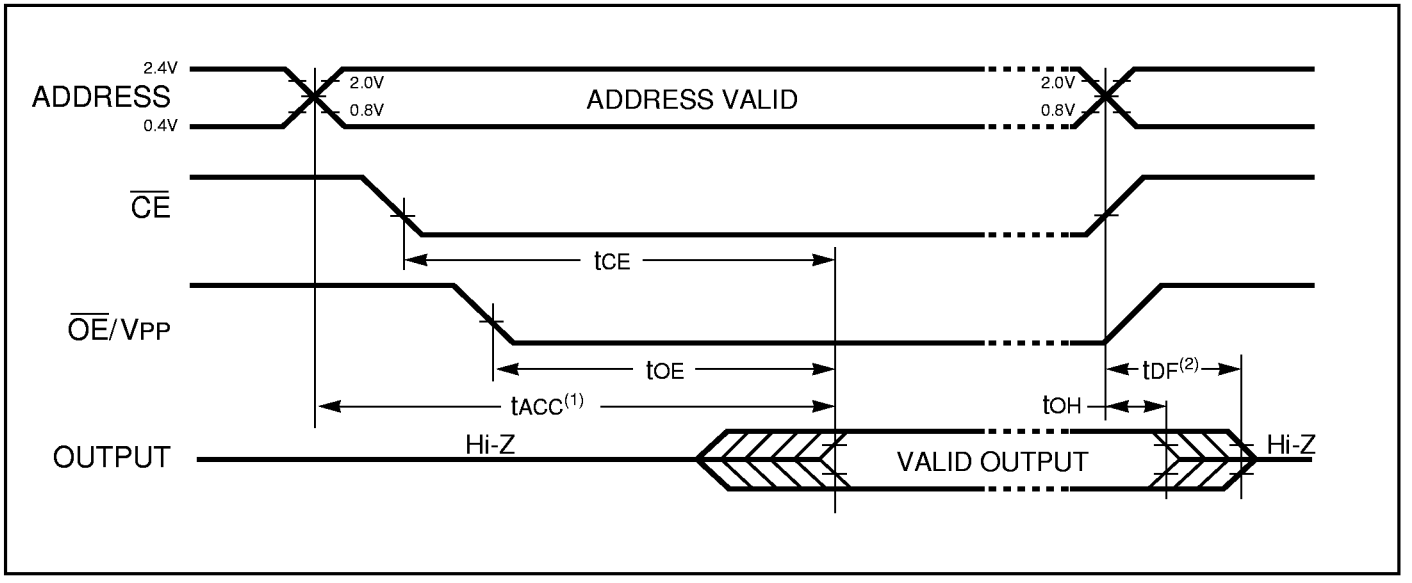
Notes:
AC Testing:
1. Inputs are driven at 2.4V for a logic "1" and .45V for a logic "0".
2. Input pulse rise and fall times are < 20ns.

SWITCHING CHARACTERISTICS[1,2,3,4] (Over Operating Range)

JEDEC Symbol	Std. Symbol	Parameter	Test Conditions	-90 Min.	-90 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	Unit
t_{AVQA}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$, $C_L = C_{L1}$	—	90	—	120	—	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$, $C_L = C_{L1}$	—	90	—	120	—	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$, $C_L = C_{L1}$	—	45	—	50	—	65	ns
t_{EHQZ}, t_{GHQZ}	t_{DF}[2]	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float	$C_L = C_{L2}$	0	30	0	35	0	35	ns
t_{AVOX}	t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ whichever occured first		0	—	0	—	0	—	ns

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled, not 100% tested.
3. **Caution:** The IS27LV512 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall times: 20 ns.
   Input Pulse Levels: 0.45 to 2.4V.
   Timing Measurement Reference Level: 0.8V to 2.0V for inputs and outputs.

SWITCHING WAVEFORMS



Notes:
1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

DC PROGRAMMING CHARACTERISTICS[1,2,3] (T_A = +25°C ± 5°C)

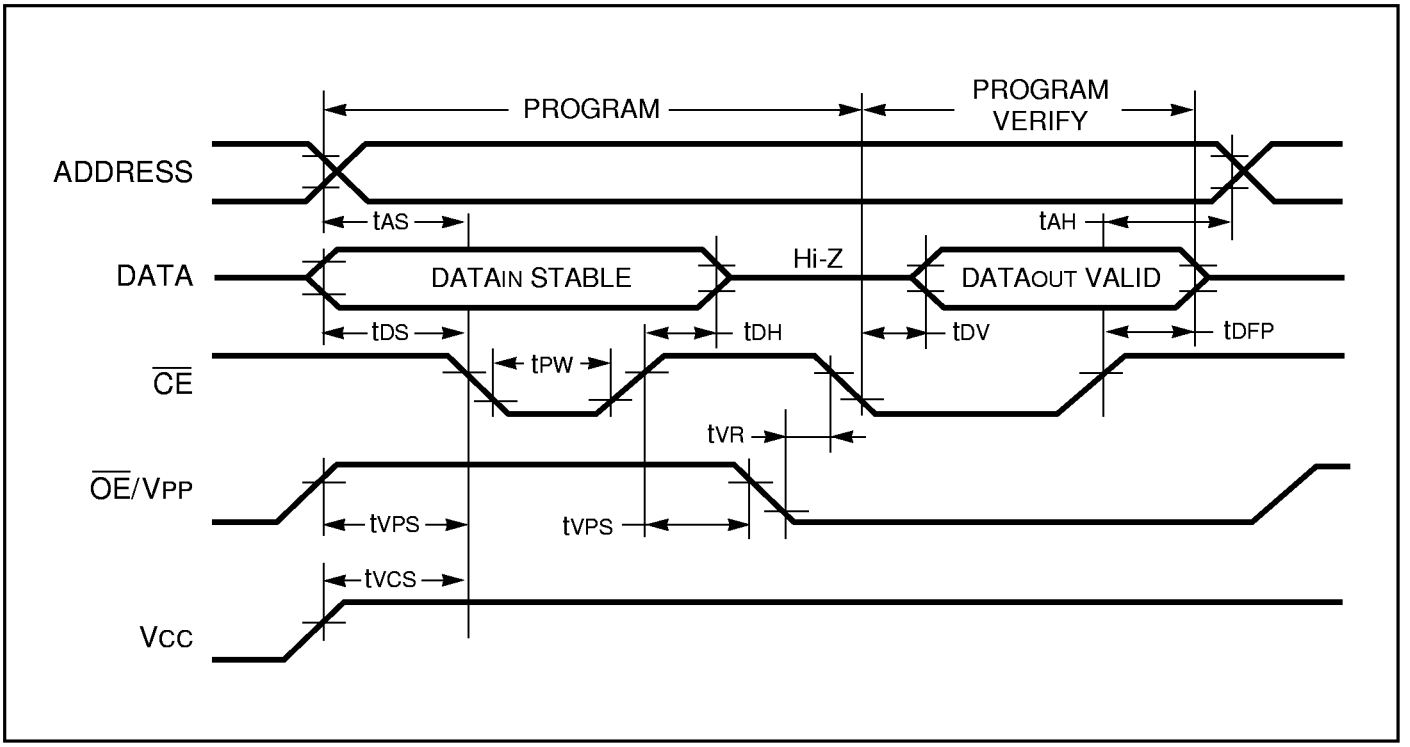
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4	—	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA	—	0.45	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage (All Inputs)		–0.3	0.8	V
V_H	A9 Auto Select Voltage		11.5	12.5	V
I_{LI}	Input Current (All Inputs)	V_{IN} = V_{IL} or V_{IH}	—	10.0	µA
I_{CC}	Vcc Supply Current (Program & Verify)		—	50	mA
I_{PP}	V_{PP} Supply Current	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	—	30	mA
V_{CC}	Supply Voltage		5.75	6.25	V
V_{PP}	Programming Voltage		12.25	12.75	V

SWITCH PROGRAMMING CHARACTERISTICS[1,2,3] (T_A = +25°C ± 5°C)

JEDEC Symbol	Std. Symbol	Parameter	Min.	Max.	Unit
t_{AVEL}	t_{AS}	Address Setup Time	2	—	µs
t_{EHGL}	t_{OEH}	$\overline{OE}$/V_{PP} Hold Time	2	—	µs
t_{DVEL}	t_{DS}	Data Setup Time	2	—	µs
t_{GHAX}	t_{AH}	Address Hold Time	0	—	µs
t_{EHDX}	t_{DH}	Data Hold Time	2	—	µs
t_{EHQZ}	t_{DFP}	$\overline{CE}$ HIGH to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2	—	µs
t_{ELEH1}	t_{PW}	$\overline{CE}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2	—	µs
t_{GLEL}	t_{VR}	$\overline{OE}$/V_{PP} Recovery Time	2	—	µs
t_{ELQV}	t_{DV}	Data Valid from $\overline{CE}$	—	150	ns

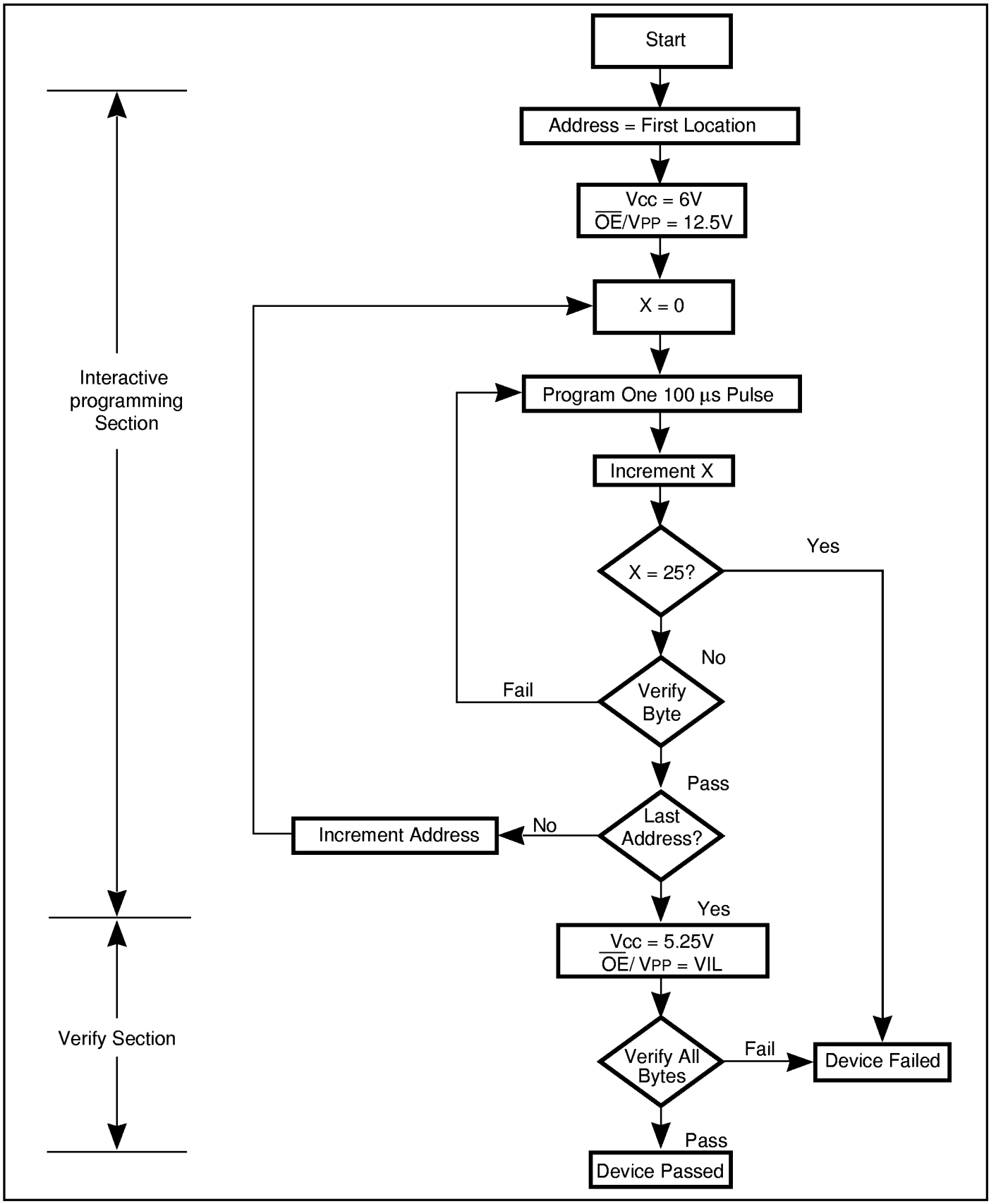
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. When programming IS27LV512, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

PROGRAMMING ALGORITHM WAVEFORM[1,2]



Notes:
1. The timing reference level is 0.8V to 2V for inputs and outputs.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

PROGRAMMING FLOW CHART



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part Number	Package
90	IS27LV512-90W	600-mil Plastic DIP
	IS27LV512-90PL	PLCC – Plastic Leaded Chip Carrier
	IS27LV512-90T	TSOP
120	IS27LV512-12W	600-mil Plastic DIP
	IS27LV512-12PL	PLCC – Plastic Leaded Chip Carrier
	IS27LV512-12T	TSOP
150	IS27LV512-15W	600-mil Plastic DIP
	IS27LV512-15PL	PLCC – Plastic Leaded Chip Carrier
	IS27LV512-15T	TSOP

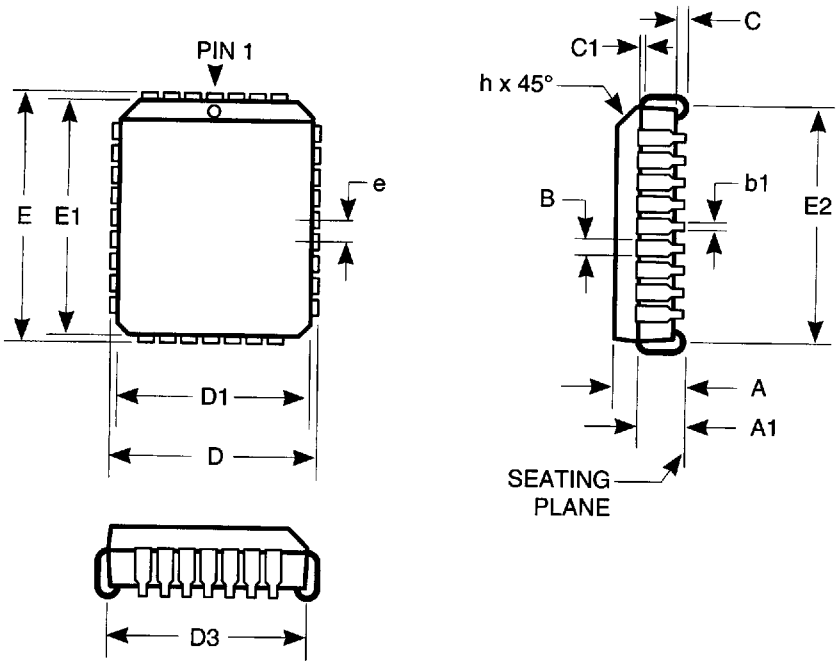
ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part Number	Package
90	IS27LV512-90WI	600-mil Plastic DIP
	IS27LV512-90PLI	PLCC – Plastic Leaded Chip Carrier
	IS27LV512-90TI	TSOP
120	IS27LV512-12WI	600-mil Plastic DIP
	IS27LV512-12PLI	PLCC – Plastic Leaded Chip Carrier
	IS27LV512-12TI	TSOP
150	IS27LV512-15WI	600-mil Plastic DIP
	IS27LV512-15PLI	PLCC – Plastic Leaded Chip Carrier
	IS27LV512-15TI	TSOP

Integrated Silicon Solution, Inc.
2231 Lawson Lane
Santa Clara, CA 95054
Fax: (408) 588-0806
Toll Free: 1-800-379-4774
http://www.issiusa.com

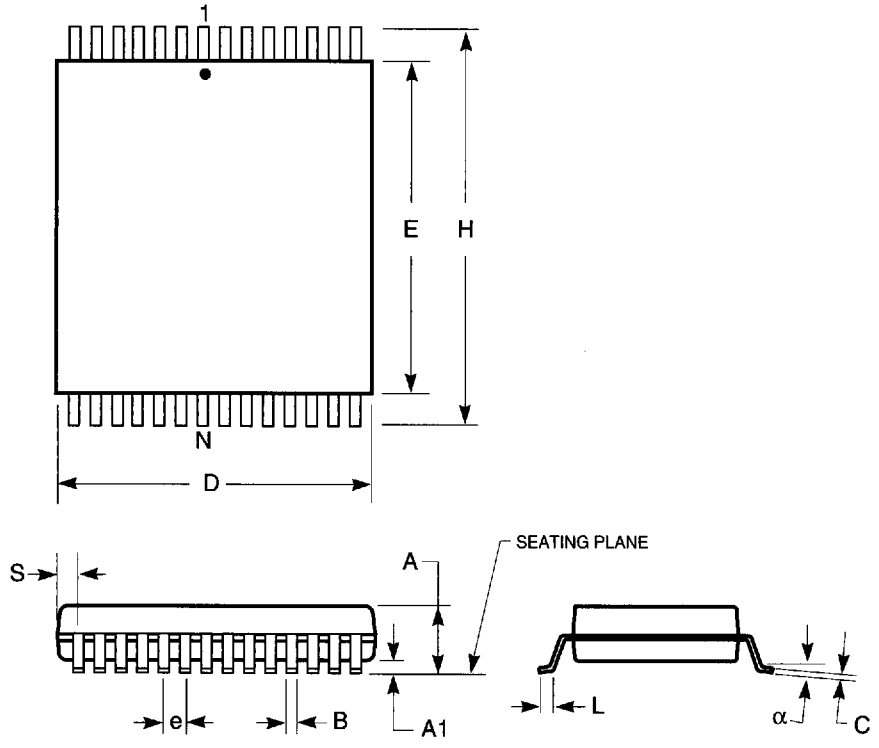
PLCC (Plastic Leaded Chip Carrier)
Package Code: PL



Plasstic Leaded Chip Carrier (PL)				
	Inches			
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads	32		44	
A	0.131	0.140	0.165	0.180
A1	0.075	0.095	0.090	0.120
B	0.026	0.032	0.026	0.032
b1	0.013	0.021	0.013	0.021
C	0.020	0.040	0.020	0.040
C1	0.008	0.014	0.008	0.014
D	0.485	0.495	0.685	0.695
D1	0.447	0.453	0.650	0.656
D2	0.390	0.430	—	—
E	0.585	0.595	0.685	0.695
E1	0.547	0.553	0.650	0.656
E2	0.490	0.530	0.659	0.680
e	0.050 BSC		0.050 BSC	
ND/NE	7/9		11/11	

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.
5. ND and NE represent the number of leads in D and E directions, respectively.
6. D1 and E1 should be measured from the bottom of the package.

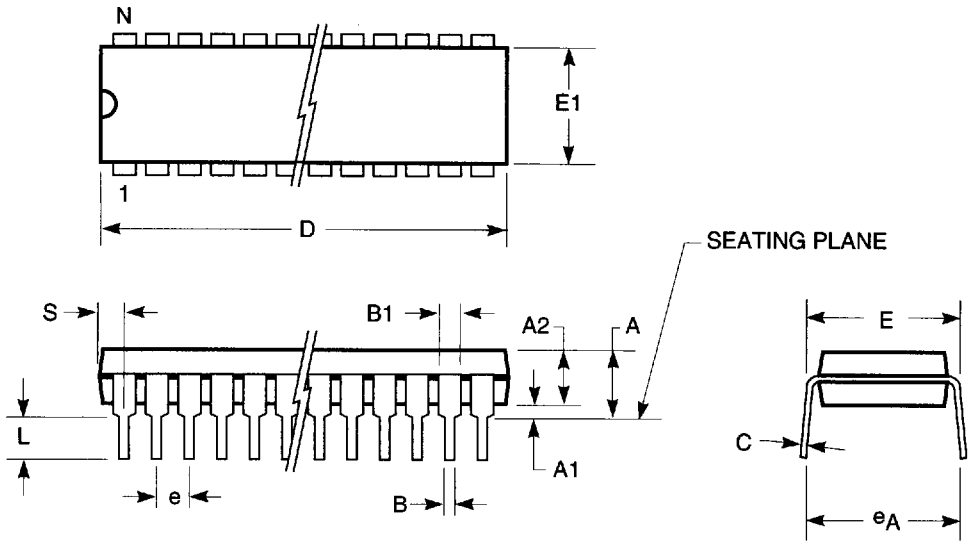
Plastic TSOP - 28-pins
Package Code: T



Plastic TSOP (T)		
	Inches	
Symbol	Min	Max
Ref. Std.		
N	28	
A	0.037	0.047
A1	0.002	0.008
B	0.006	0.011
C	0.004	0.008
D	0.311	0.319
E	0.460	0.468
H	0.520	0.536
e	0.020 BSC	
L	0.011	0.027
α	0°	5°

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

600-mil Plastic DIP
Package Code: W



600-mil Plastic DIP (W)						
	Inches					
Symbol	Min	Max	Min	Max	Min	Max
Ref. Std.						
N	28		32		40	
A	0.160	0.185	0.165	0.180	0.165	0.200
A1	0.015	0.035	0.010	—	0.020	0.045
B	0.015	0.020	0.018		0.015	0.022
B1	0.050	0.065	0.050		0.045	0.067
C	0.008	0.012	0.010		0.008	0.015
D	1.420	1.460	1.645	1.655	1.415	1.460
E	0.600	0.620	0.590	0.610	0.600	0.620
E1	0.530	0.550	0.540	0.555	0.530	0.560
e_A	0.610	0.670	0.620	0.680	0.600	0.680
e	0.100 BSC		0.100 BSC		0.100 BSC	
L	0.120	0.150	0.120	0.140	0.120	0.138
S	0.055	0.080	0.065	0.085	0.055	0.085
α	0°	15°	2°	8°	—	—

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

11