

2-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

FEATURES

- Drives 2-1/2 Digit LED Displays
- Internal Voltage Reference 150 ppm/°C Max
- Low Supply Current 2 mA Max
- Ratiometric Measurements
- Auto-Zero Cycle Eliminates External Trimmers
- Dynamic Range ± 200 Counts
- Multiple Package Options
 - Low-Cost 40-Pin Package
 - 44-Pin Plastic Flat Package
 - 44-Pin PLCC Package

GENERAL DESCRIPTION

The TC807 is a 2-1/2 digit analog-to-digital converter (ADC) designed to drive standard 7-segment LED displays without external drive electronics.

This 0.5% resolution converter is ideal for low-cost pressure, temperature, pH or flow-rate indicators.

The TC807 features differential inputs and references for ratiometric readings. An auto-zero cycle eliminates external offset adjustment potentiometers.

This dual-slope converter automatically rejects 50-, 60- and 400-Hz line frequency interference signals. Polarity information is displayed, giving the device a ± 200 count dynamic range.

Overall system cost is reduced by incorporating a low-temperature coefficient voltage reference on-chip.

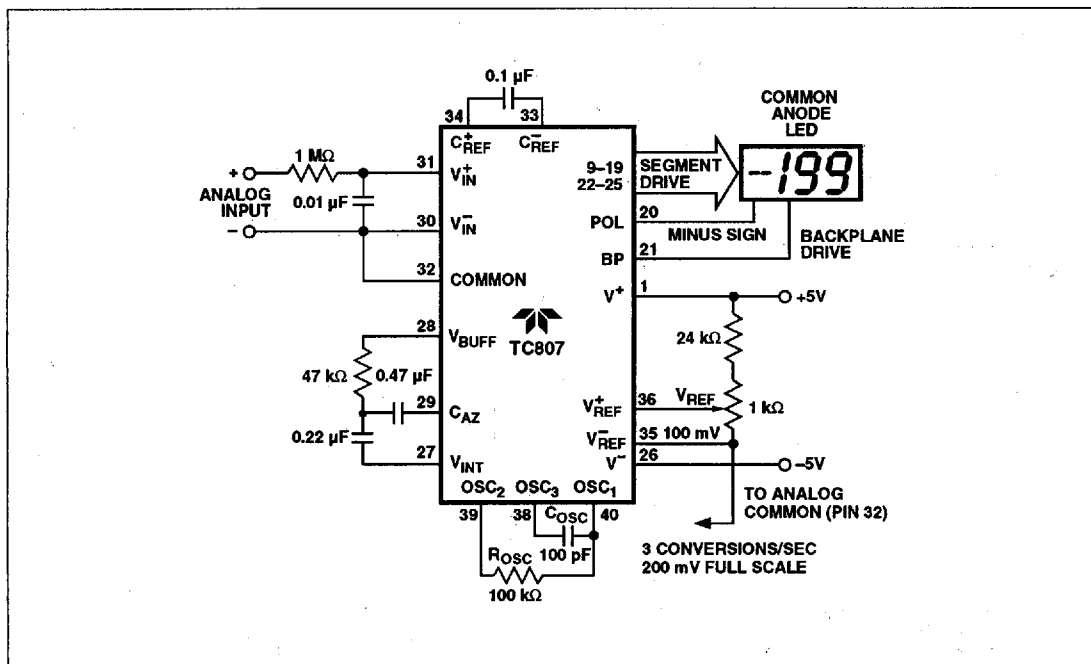
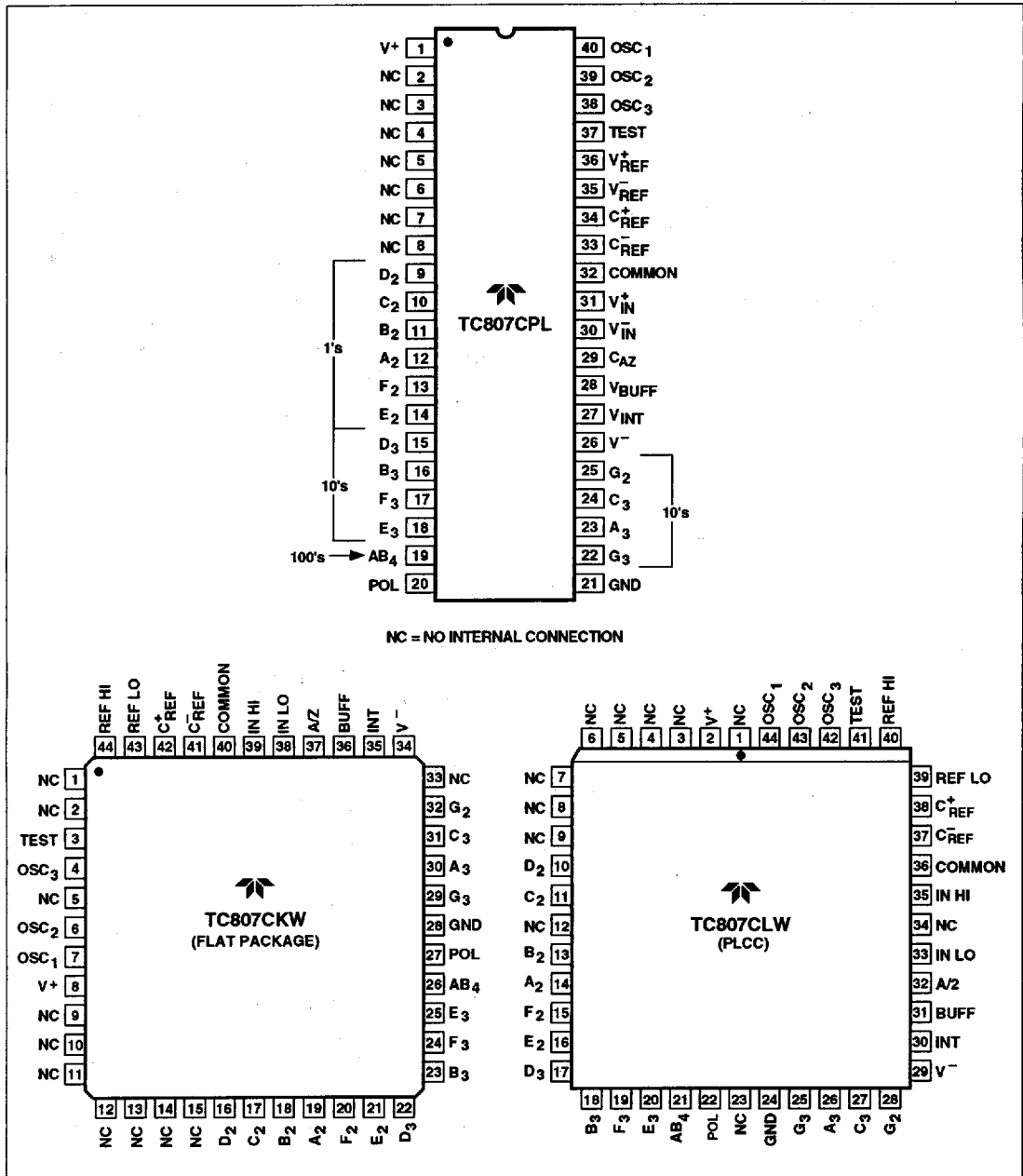


Figure 1. Typical Operating Circuit

2-1/2 DIGIT
ANALOG-TO-DIGITAL CONVERTER

TC807

PIN CONFIGURATIONS



T-52-13-07

2-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

1

TC807

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC807CPL	40-Pin Plastic DIP	0°C to +70°C
TC807CKW	44-Pin Plastic Flat	0°C to +70°C
TC807CLW	44-Pin PLCC	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage

V⁺ +6V

V⁻ -9V

Analog Input Voltage (Either Input) (Note 1) V⁺ to V⁻

Reference Input Voltage (Either Input) V⁺ to V⁻

Clock Input GND to V⁺

Power Dissipation (Note 2) 800 mW

Operating Temperature Range 0°C to +70°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (Soldering, 60 Sec) +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C, f_{CLK} = 48 kHz, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V _{IN} = 0V Full Scale = 200 mV	-0	±0	+0	Digital Reading
Ratiometric Reading	V _{IN} = V _{REF} V _{REF} = 100 mV	99	99/100	100	Digital Reading
Roll-Over Error (Difference in Reading for Equal Positive and Negative Reading Near Full Scale)	-V _{IN} = +V _{IN} = 200 mV	-1	±0.2	+1	Counts
Linearity (Max Deviation from Best Straight Line Fit)	Full Scale = 200 mV or Full Scale = 2V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 3)	V _{CM} = ±1V, V _{IN} = 0V Full Scale = 200 mV	—	50	—	μV/V
Noise (Peak-Peak Value Not Exceeded 95% of Time)	V _{IN} = 0V, Full Scale = 200 mV	—	15	—	μV
Leakage Current at Input	V _{IN} = 0V	—	1	25	pA
Zero Reading Drift	V _{IN} = 0V	—	0.2	5	μV/°C
Supply Current (Does Not Include LED Current)	V _{IN} = 0V	—	0.8	2	mA
Internal Voltage Reference (Analog Common Potential with Respect to Positive Supply)	25 kW Between Common and Positive Supply	2.7	3.05	3.35	V
Temperature Coefficient of Analog Common (With Respect to Positive Supply)	25 kW Between Common and Positive Supply 0°C ≤ T _A ≤ 70°C	—	20	150	ppm/°C
Segment Sinking Current (Except Pin 19)	V ⁺ = 5V, Segment Voltage = 3V	4	8	—	mA
Segment Sinking Current, Pin 19	V ⁺ = 5V, Segment Voltage = 3V	8	16	—	mA

- NOTES:**
1. Input voltages may exceed supply voltages, provided input current is limited to ±100 μA.
 2. Dissipation rating assumes device is mounted with all leads soldered to PC board.
 3. Refer to "Differential Input" discussion.

T-52-13-07

2-1/2 DIGIT
ANALOG-TO-DIGITAL CONVERTER

TC807

PIN DESCRIPTION

40-Pin DIP Pin Number	Name	Description
1	V ⁺	Positive supply voltage.
2	NC	No connection.
3	NC	No connection.
4	NC	No connection.
5	NC	No connection.
6	NC	No connection.
7	NC	No connection.
8	NC	No connection.
9	D ₁	Activates the D section of the units display.
10	C ₁	Activates the C section of the units display.
11	B ₁	Activates the B section of the units display.
12	A ₁	Activates the A section of the units display.
13	F ₁	Activates the F section of the units display.
14	E ₁	Activates the E section of the units display.
15	D ₂	Activates the D section of the tens display.
16	B ₂	Activates the B section of the tens display.
17	F ₂	Activates the F section of the tens display.
18	E ₂	Activates the E section of the tens display.
19	AB ₃	Activates both halves of the "1" in the hundreds display.
20	POL	Activates the negative polarity display.
21	GND	Digital ground.
22	G ₂	Activates the G section of the tens display.
23	A ₂	Activates the A section of the tens display.
24	C ₂	Activates the C section of the tens display.
25	G ₁	Activates the G section of the ones display.
26	V ⁻	Negative power supply voltage.
27	V _{INT}	Integrator output. Connection point for integration capacitor. See "Integrating Capacitor" for additional details.
28	V _{BUFF}	Integration resistor connection. Use a 47 kΩ resistor for 200 mV full-scale range and a 470 kΩ resistor for 2V full-scale range.
29	CAZ	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for 200 mV full scale, and a 0.47 μF capacitor for 2V full scale. See "Auto-Zero Capacitor" for more details.
30	V _{IN} ⁻	The analog low input is connected to this pin.
31	V _{IN} ⁺	The analog high input is connected to this pin.
32	COMMON	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See "Analog Common" for more details. It also acts as a reference voltage source.
33	C _{REF} ⁻	See pin 34.
34	C _{REF} ⁺	A 0.1 μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V _{IN} ⁻ pin is not at analog common), and a 200 mV scale is used, a 1 μF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	V _{REF} ⁻	See pin 36.
36	V _{REF} ⁺	The analog input required to generate a full-scale output (199 counts). Place 100 mV between pins 35 and 36 for 200 mV full scale. Place 1V between pins 35 and 36 for 2V full scale. See "Reference Voltage."

T-52-13-07

1

2-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

TC807

PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number	Name	Description
37	TEST	Lamp test. When pulled high (to V^+), all segments will be turned on and the display should read "-188". It may also be used as a negative supply for externally-generated decimal points. See "Test" for additional information.
38	OSC ₃	See pin 40.
39	OSC ₂	See pin 40.
40	OSC ₁	Pins 40, 39, and 38 make up the oscillator section. For a 48 kHz clock (three readings per second), connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is held to pin 39 and the 100 pF capacitor is tied to pin 38.

ANALOG SECTION

Figure 2 is a block diagram of the TC807. Each measurement cycle is divided into three phases: (1) auto-zero (A-Z), (2) signal integration (SI), and (3) reference integration (RI). The conversion rate is set by the clock oscillator frequency and is independent of the analog input amplitude.

Auto-Zero Cycle

During the auto-zero cycle, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero-input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on CAZ compensates for device offset voltages. The offset error referred to the input is less than 10 μ V.

The auto-zero cycle length is 4000 to 12,000 clock cycles.

Signal-Integrate Cycle

The auto-zero loop is opened, the internal short removed, and the internal differential inputs connect to V_{IN}^+ and V_{IN}^- . The differential input signal is integrated for a fixed time period. The signal integration period is 4000 cycles. The integration time period is:

$$t_{SI} = \frac{4}{f_{OSC}} \times 1000,$$

where f_{OSC} = external clock frequency.

The differential input voltage must be within the device's common-mode range (1V of either supply) when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of the signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference-Integrate Cycle

The final phase is reference integrate or deintegrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously charged reference capacitor. Circuitry within the chip ensures the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal, and is between 0 and 8000 clock cycles. The digital reading displayed is:

$$100 \times \frac{V_{IN}}{V_{REF}}$$

DIGITAL SECTION

The TC807 contains all the segment drivers necessary to directly drive a 2-1/2 digit LED display. The segment is typically 8 mA. The 100's output (pin 19) sinks current from two LED segments, and has a 16-mA drive capability. The TC807 is designed to drive common anode LED displays. (See Figure 2.)

The polarity indication is "ON" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

The display font is shown in Figure 3.

System Timing

The oscillator frequency is $\div 4$ prior to clocking the internal decade counters. The three-phase measurement cycle takes a total of 16,000 clock pulses.

T-52-13-07

2-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

TC807

1

Each phase of the measurement cycle has the following length:

- (1) Auto-Zero Phase: 4000 to 12,000 clock pulses — For signals less than full-scale, the auto-zero phase is assigned the unused reference integrate time period.
- (2) Signal Integrate: 4000 clock pulses — This time period is fixed. The integration period is:

$$t_{SI} = 4000 \left[\frac{1}{f_{OSC}} \right],$$

where f_{OSC} is the externally set clock frequency.

- (3) Reference Integrate: 0 to 8000 clock pulses.

Component Value Selection

Auto-Zero Capacitor (C_{AZ})

The C_{AZ} size has some influence on system noise. A 0.47 μF capacitor is recommended for 200 mV full scale. A 0.047 μF capacitor is adequate for 2V full-scale applications. A Mylar-type dielectric capacitor is adequate.

Reference Voltage Capacitor (C_{REF})

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF} . A 0.1 μF capacitor is acceptable when V_{IN^-} is tied to analog common. If a large common-mode voltage exists ($V_{REF^-} \neq$ analog common) and the application requires a 200-mV full scale, increase C_{REF} to 1 μF . Roll-over error will be held to less than 0.5 count. A Mylar-type dielectric capacitor is adequate.

Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case, a $\pm 2\text{V}$ full-scale integrator output swing is satisfactory. For 3 readings/second ($f_{OSC} = 48 \text{ kHz}$), a 0.22 μF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal $\pm 2\text{V}$ integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000) \left(\frac{1}{f_{OSC}} \right) \left(\frac{V_{FS}}{R_{INT}} \right)}{V_{INT}}$$

where: f_{OSC} = Clock frequency at pin 38
 V_{FS} = Full-scale input voltage
 R_{INT} = Integrating resistor
 V_{INT} = Desired full-scale integrator output swing.

C_{INT} must have low dielectric absorption to minimize roll-over error. An inexpensive polypropylene capacitor is recommended.

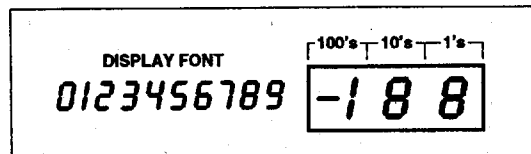


Figure 3. Display Font and Segment Assignment

Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with Class A output stages. The output stage idling current is 100 μA . The integrator and buffer can supply 20 μA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200 mV full scale, R_{INT} is 47 k Ω . A 2V full scale requires 470 k Ω .

Component Value	Nominal Full-Scale Voltage	
	200 mV	2V
C_{AZ}	0.47 μF	0.047 μF
R_{INT}	47 k Ω	470 k Ω
C_{INT}	0.22 μF	0.22 μF

NOTE: $f_{OSC} = 48 \text{ kHz}$ (3 readings/second)

Oscillator Components

R_{OSC} (pin 40 to pin 38) should be 100 k Ω . C_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

For f_{OSC} of 48 kHz, C_{OSC} is 100 pF, nominally.

Note that f_{OSC} is +4 to generate the TC807 internal control clock.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33-1/3 kHz, etc., should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc., would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Reference Voltage Selection

A full-scale reading (280 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	V_{REF}
200 mV	100 mV
2V	1V

* $V_{FS} = 2 V_{REF}$

T-52-13-07

2-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

TC807

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. For example, assume a pressure transducer output for 200 lb/in.² is 400 mV. Rather than dividing the input voltage by two, the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^- . The transducer output is connected between V_{IN}^+ and analog common.

The internal voltage reference potential available at analog common is normally used to supply the converter's reference. This potential is stable whenever the supply potential is greater than approximately 7V. In applications where an externally-generated reference voltage is desired, refer to Figure 4.

DEVICE PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs

V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30)

The TC807 is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is $V^+ - 1V$ to $V^- + 1V$. Common-mode voltages are removed from the system when the TC807 operates from a floating power source (isolated from measured system) and V_{IN}^- is connected to analog common.

In systems where common-mode voltages exist, the 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worst-case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 5). For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of V^+ or V^- without increasing linearity errors.

Differential Reference

V_{REF}^+ (Pin 36), V_{REF}^- (Pin 39)

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent roll-over errors being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance.

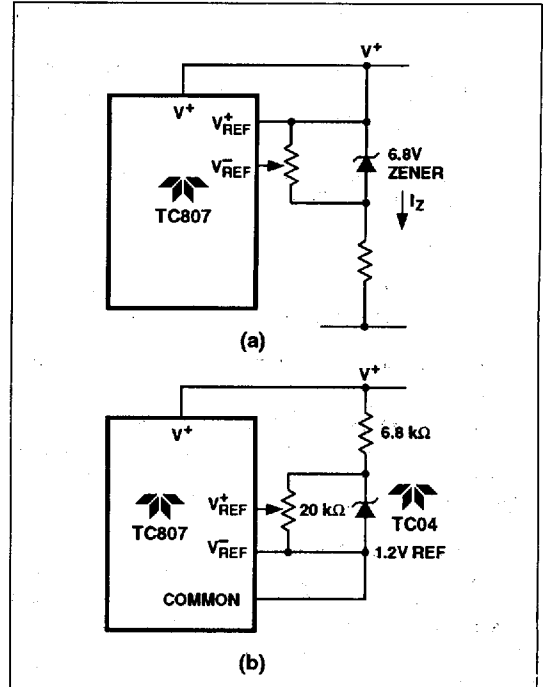


Figure 4. External Reference

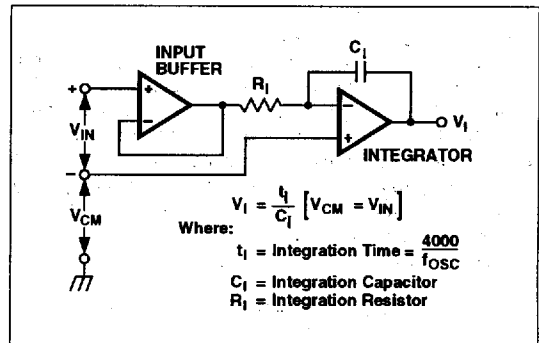


Figure 5. Common-Mode Voltage Reduces Available Integrator Swing ($V_{CM} \neq V_{IN}$)

2-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

TC807

Analog Common

Analog COMMON (pin 32) is set at a voltage potential approximately 3V below V^+ . The potential is guaranteed to be between 2.7V and 3.35V below V^+ . Analog common is tied internally to an N-channel FET capable of sinking 30 mA. This FET will hold the common line at 3V should an external load attempt to pull the common line toward V^+ . Analog common source current is limited to 10 μ A. Therefore, analog common is easily pulled to a more negative voltage (i.e., below $V^+ - 3V$).

The TC807 connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero cycle. During the reference-integrate phase, V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converter's 86-dB common-mode rejection ratio. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^- .

Analog common serves to set the analog section reference or common point. The common potential has a 0.001%/ % voltage coefficient and 15 Ω output impedance.

With sufficiently high total supply voltage ($V^+ - V^- > 7V$), analog common is a very stable potential with excellent temperature stability (typically 20 ppm/ $^{\circ}$ C). This potential can be used to generate reference voltage.

If analog common is connected to power ground, the internal reference is disabled. An external reference is required when analog common is connected to power ground.

Test

TEST (pin 37) potential is 5V less than V^+ . If test is pulled high (to V^+), all segments plus the minus sign will be activated.

The test pin will sink about 10 mA when pulled to V^+ .

POWER SUPPLIES

The TC807 is designed to work from $\pm 5V$ supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors, and an inexpensive IC. (See Figure 6.)

In selected applications, a negative supply is not required. The conditions to use a single +5V supply are:

- (1) The input signal can be referenced to the center of the common-mode range of the converter.

- (2) The signal is less than $\pm 1.5V$.

- (3) An external reference is used.

- (4) The TC7660 DC-to-DC converter may also be used to generate $-5V$ from +5V (Figure 7).

Ratiometric Resistance Measurements

True differential input and differential reference make ratiometric readings possible. Typically, in a ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 100. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{\text{UNKNOWN}}}{R_{\text{STANDARD}}} \times 100.$$

The display will overrange for $R_{\text{UNKNOWN}} \geq 2 \times R_{\text{STANDARD}}$.

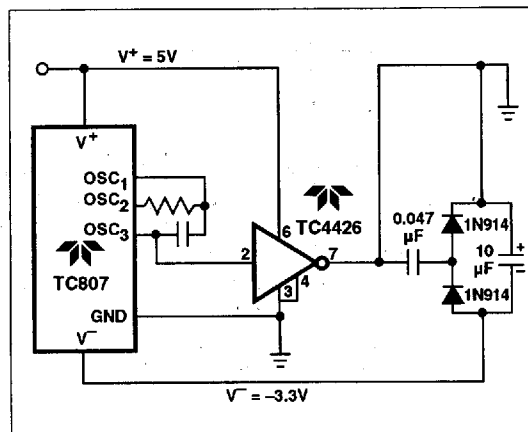


Figure 6. Generating Negative Supply From +5V

T-52-13-07

2-1/2 DIGIT

ANALOG-TO-DIGITAL CONVERTER

TC807

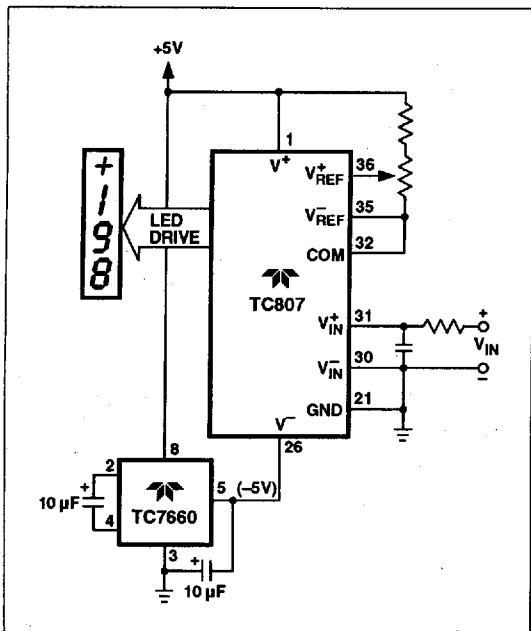


Figure 7. Negative Power Supply Generation With TC7660

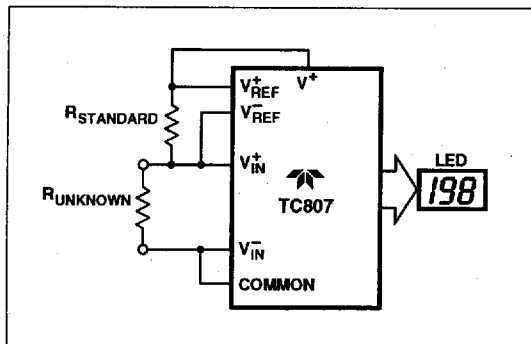


Figure 8. Low Parts Count Ratiometric Resistance Measurement

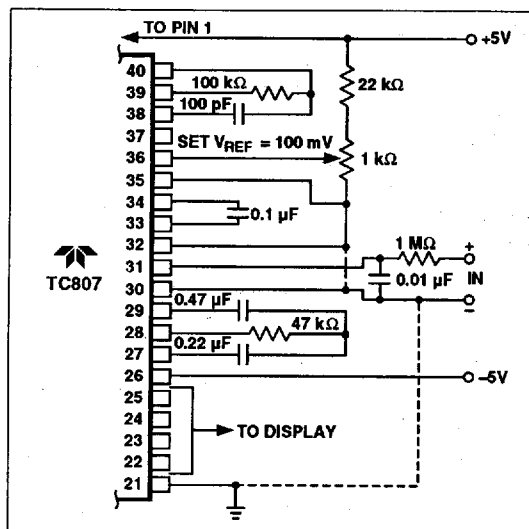


Figure 9. Internal Reference (200 mV Full Scale, 3 RPS, V-IN Tied to Ground for Single-Ended Inputs)

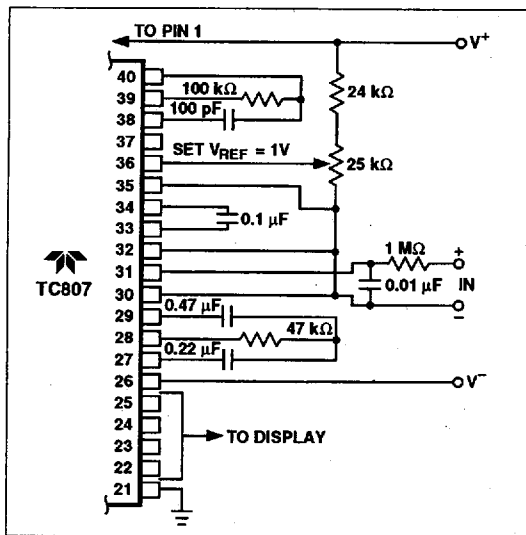


Figure 10. Recommended Component Values for 2V Full Scale

T-52-13-07

2-1/2 DIGIT
ANALOG-TO-DIGITAL CONVERTER

1

TC807

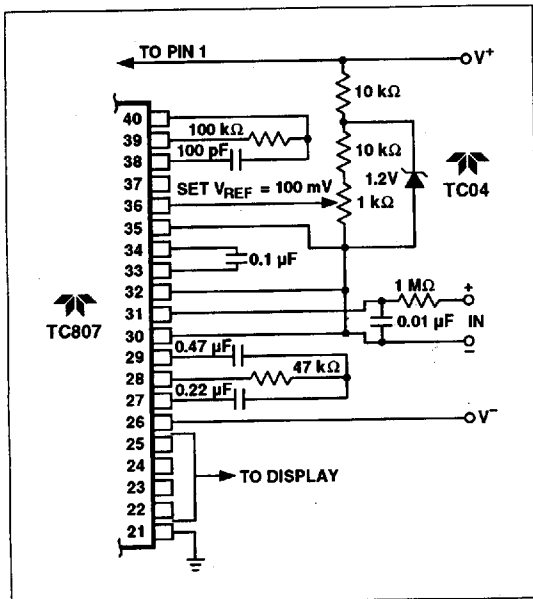


Figure 11. TC807 With a 1.25V External Band-Gap Reference (V_{IN-} Tied to Common)

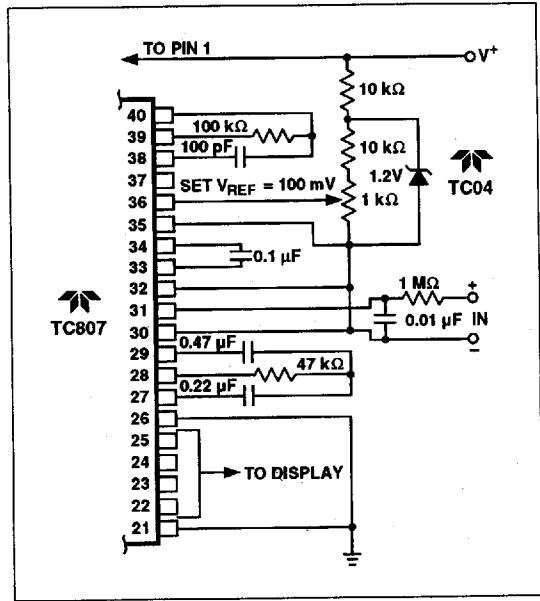


Figure 12. TC807 Operated From Single +5V Supply (An External Reference Must Be Used in This Application)