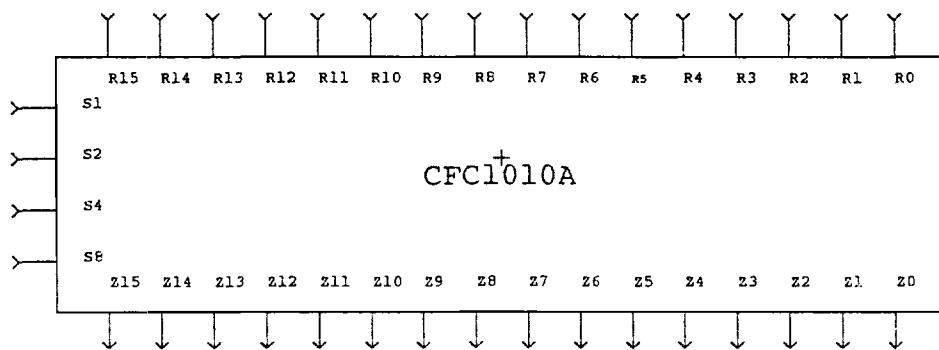


CFC1010A

16-bit Barrel Shifter

DESCRIPTION: CFC1010A performs a 16-bit end-around shift, or what is commonly known as a barrel shift. There are four control lines (S_1 , S_2 , S_4 , and S_8) to determine how many places to the left the 16-bit inputs (R_{15} through R_0) will be shifted at the outputs (Z_{15} through Z_0). All outputs are in-phase with the inputs.

LOGIC SYMBOL:



INPUTS (LOADING IN TRANSISTOR PAIRS):

$R_{15}(8)$, $R_{14}(8)$, $R_{13}(8)$, $R_{12}(8)$, $R_{11}(8)$, $R_{10}(8)$, $R_9(8)$, $R_8(8)$,
 $R_7(8)$, $R_6(8)$, $R_5(8)$, $R_4(8)$, $R_3(8)$, $R_2(8)$, $R_1(8)$, $R_0(8)$,
 $S_1(4.5)$, $S_2(4.5)$, $S_4(4.5)$, $S_8(4.5)$

OUTPUTS (DRIVE IN (#P,#N)):

$Z_{15}(0.5,0.5)$, $Z_{14}(0.5,0.5)$, $Z_{13}(0.5,0.5)$, $Z_{12}(0.5,0.5)$,
 $Z_{11}(0.5,0.5)$, $Z_{10}(0.5,0.5)$, $Z_9(0.5,0.5)$, $Z_8(0.5,0.5)$,
 $Z_7(0.5,0.5)$, $Z_6(0.5,0.5)$, $Z_5(0.5,0.5)$, $Z_4(0.5,0.5)$,
 $Z_3(0.5,0.5)$, $Z_2(0.5,0.5)$, $Z_1(0.5,0.5)$, $Z_0(0.5,0.5)$

GATE COUNT:

GATES USED = 145

AREA USED = 146

CFC1010A

TRUTH TABLE:

S8	S4	S2	S1	Z15	Z14	Z13	Z12	Z11	Z10	Z9	Z8	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0
0	0	0	0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
0	0	0	1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	R15
0	0	1	0	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	R15	R14
0	0	1	1	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	R15	R14	R13
0	1	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	R15	R14	R13	R12
0	1	0	1	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	R15	R14	R13	R12	R11
0	1	1	0	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	R15	R14	R13	R12	R11	R10
0	1	1	1	R8	R7	R6	R5	R4	R3	R2	R1	R0	R15	R14	R13	R12	R11	R10	R9
1	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0	R15	R14	R13	R12	R11	R10	R9	R8
1	0	0	1	R6	R5	R4	R3	R2	R1	R0	R15	R14	R13	R12	R11	R10	R9	R8	R7
1	0	1	0	R5	R4	R3	R2	R1	R0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6
1	0	1	1	R4	R3	R2	R1	R0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5
1	1	0	0	R3	R2	R1	R0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4
1	1	0	1	R2	R1	R0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3
1	1	1	0	R1	R0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2
1	1	1	1	R0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1

AC CHARACTERISTICS:

PATH	10K TYP. DELAY(NS)
R(I) TO OUTPUT Z(I)	5.6
S(I) TO OUTPUT Z(I)	7.8

* ASSUMING OUTPUT LOADING OF 3