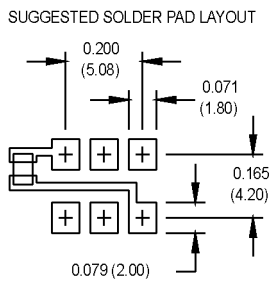
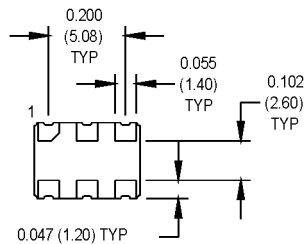
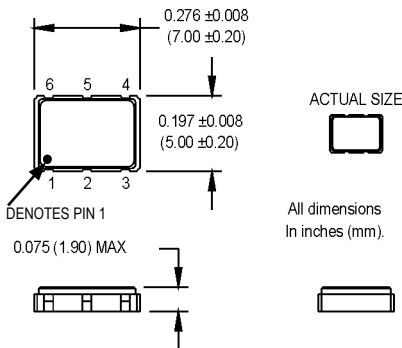
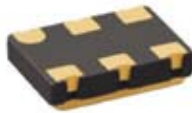


UVC Series

5x7 mm, 3.3 Volt, LVPECL/LVDS, Clock Oscillators



Pad Connections

Pad	Function
1	Enable/Disable for "R" Output Type or N/C for "Z" Output Type
2	N/C
3	Ground
4	Output Q
5	Complementary Output $\bar{Q}$
6	+ Vdd

Ordering Information

Product Series	UVC	1	8	R	L	N	00.0000 MHz
Temperature Range	1: 0°C to +70°C	2: -40°C to +85°C	6: -20°C to +70°C	7: -0°C to +85°C	8: 0°C to +50°C		
Stability	3: ±100 ppm	4: ±50 ppm	6: ±25 ppm	8: ±20 ppm			
Output Type	R: Complementary Enable	Z: Complementary w/o Enable					
Symmetry/Output Logic Type	L: 45/55% LVDS	P: 45/55% PECL	H: 40/60% LVDS	Q: 40/60% PECL			
Package/Lead Configurations	N: Leadless Ceramic (6 pads)						
Frequency (customer specified)							

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	0.75		800	MHz	
Operating Temperature	T _A	(See Ordering Information)				
Storage Temperature	T _S	-55		+125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				
Aging						See Note 1
1st Year		-3		+3	ppm	
Thereafter (per year)		-1		+1	ppm	
Input Voltage	V _{CC}	3.135	3.3	3.465	V	
PECL Input Current	I _{CC}			70	mA	0.75 to 24 MHz
				100	mA	24 to 96 MHz
				110	mA	96 to 800 MHz
LVDS Input Current	I _{CC}			30	mA	0.75 to 24 MHz
				60	mA	24 to 96 MHz
				60	mA	96 to 800 MHz
Output Type						PECL/LVDS
Load		50 Ohms to V _{CC} -2 VDC 100 Ohm differential load				See Note 2 PECL Waveform LVDS Waveform
Symmetry (Duty Cycle)		(See Ordering Information)				
Output Skew				200	ps	PECL
Differential Voltage		250	340	450	mV	LVDS
Logic "1" Level	V _{OH}	V _{CC} -1.02			V	PECL
Logic "0" Level	V _{OL}			V _{CC} -1.63	V	PECL
Rise/Fall Time	T _r /T _f		0.35 .50	0.55 1.0	ns	@ 20/80% LVPECL @ 20/80% LVDS
Enable Function		80% V _{CC} min or N/C: output active 20% V _{CC} max: output disables to high-Z				Output Option R
Start up Time			5		ms	
Phase Jitter	φ _J		3	5	ps RMS	Integrated 12 kHz - 20 Mhz

1. Inclusive of initial tolerance, deviation over temperature, shock, vibration, voltage, and aging.
2. PECL load - see load circuit diagram #5. LVDS load - see load circuit diagram #9.

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