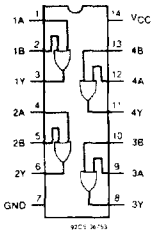


CD54/74HC32 CD54/74HCT32

High-Speed CMOS Logic



**FUNCTIONAL DIAGRAM AND
TERMINAL ASSIGNMENT**

Quad 2-Input OR Gate

Type Features:

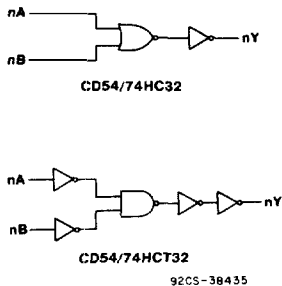
- Typical propagation delay = 7 ns
@ $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{ C}$ (HC32)

The RCA-CD54/74HC32 and CD54/74HCT32 contain four 2-input OR gates in one package.

The CD54HC/HCT32 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT32 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to $+85^\circ\text{ C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}
@ $V_{CC} = 5\text{ V}$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8\text{ V Max.}$, $V_{IH} = 2\text{ V Min.}$
CMOS Input Compatibility
 $I_I \leq 1\text{ }\mu\text{A}$ @ V_{OL} , V_{OH}



TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level.
L = LOW voltage level.

Fig. 1 - Logic diagrams.

CD54/74HC32

CD54/74HCT32

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):
 (Voltages referenced to ground) -0.5 to + 7 V

DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V) ± 20 mA

DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V) ± 20 mA

DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V) ± 25 mA

DC V_{CC} OR GROUND CURRENT (I_{CC}) ± 50 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE E) 500 mW

For $T_A = +60$ to $+85^\circ$ C (PACKAGE TYPE E) Derate Linearly at 8 mW/ $^\circ$ C to 300 mW

For $T_A = -55$ to $+100^\circ$ C (PACKAGE TYPE F, H) 500 mW

For $T_A = +100$ to $+125^\circ$ C (PACKAGE TYPE F, H) Derate Linearly at 8 mW/ $^\circ$ C to 300 mW

For $T_A = -40$ to $+70^\circ$ C (PACKAGE TYPE M) 400 mW

For $T_A = +70$ to $+125^\circ$ C (PACKAGE TYPE M) Derate Linearly at 6 mW/ $^\circ$ C to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE F, H -55 to $+125^\circ$ C

PACKAGE TYPE E M -40 to $+85^\circ$ C

STORAGE TEMPERATURE (T_{STG}) -65 to $+150^\circ$ C

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ$ C

Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only $+300^\circ$ C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For $T_A =$ Full Package Temperature Range) V_{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_i, V_o	0	V_{CC}	V
Operating Temperature T_A :			
CD74 Types	-40	+85	$^\circ$ C
CD54 Types	-55	+125	$^\circ$ C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC32 CD54/74HCT32

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC32/CD54HC32										CD74HCT32/CD54HCT32								UNITS			
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE			TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE			54HCT TYPE		
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C			V _I V	V _{CC} V	+25°C			-40/ +85°C			-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max	Min			Max	Min	Max	Min	Max		Min	Max	
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5	to	2	—	—	2	—	2	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	5.5										
			6	4.2	—	—	4.2	—	4.2	—	—											
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5	to	—	—	0.8	—	0.8	—	0.8	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	5.5										
			6	—	—	1.8	—	1.8	—	1.8	—											
High-Level Output Voltage V _{OH}	V _{IL}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL}	4.5	4.4	—	—	4.4	—	4.4	—	4.4	V	
	or		4.5	4.4	—	—	4.4	—	4.4	—	4.4											—
	V _{IH}		6	5.9	—	—	5.9	—	5.9	—	V _{IH}											
TTL Loads	V _{IL}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V _{IL}	4.5	3.98	—	—	3.84	—	3.7	—	V		
	or		4.5	3.98	—	—	3.84	—	3.7	—												
	V _{IH}		5.2	6	5.48	—	—	5.34	—	5.2	—										V _{IH}	
Low-Level Output Voltage V _{OL}	V _{IL}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL}	4.5	—	—	0.1	—	0.1	—	0.1	V		
	or		4.5	—	—	0.1	—	0.1	—	0.1	—											
	V _{IH}		6	—	—	0.1	—	0.1	—	0.1	—										V _{IH}	
TTL Loads	V _{IL}	4	4.5	—	—	0.26	—	0.33	—	0.4	V _{IL}	4.5	—	—	0.26	—	0.33	—	0.4	V		
	or		4.5	—	—	0.26	—	0.33	—	0.4	—											
	V _{IH}		5.2	6	—	—	0.26	—	0.33	—	0.4										V _{IH}	
Input Leakage Current I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA		
Quiescent Device Current I _{CC}	V _{CC} or Gnd	0	6	—	—	2	—	20	—	40	V _{CC} or Gnd	5.5	—	—	2	—	20	—	40	μA		
Additional Quiescent Device Current per Input Pin, 1 Unit Load ΔI _{CC} *											V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA		

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
All Inputs	1.5

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC32 CD54/74HCT32

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{ C}$, Input t_r , $t_f = 6\text{ ns}$)

CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL VALUES		UNITS
			54/74HC	54/74HCT	
Propagation Delay A, B to Y	15	t_{PLH} t_{PHL}	7	9	ns
Power Dissipation Capacitance	—	C_{PD}^*	22	22	pF

* C_{PD} is used to determine the dynamic power consumption, per gate.

$P_D = f_i V_{CC}^2 (C_{PD} + C_L)$ where:

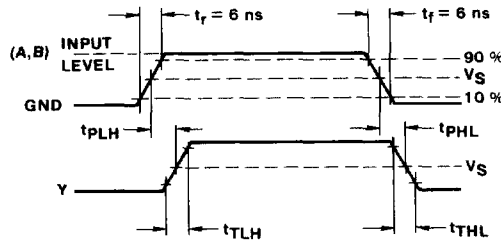
f_i = input frequency.

C_L = output load capacitance.

V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input t_r , $t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	V_{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay A, B to Y Figure 2	t_{PLH}	2	90	—	—	115	—	—	—	135	—	—	ns		
	t_{PHL}	4.5	18	24	23	30	27	36	—	—	—	—			
		6	15	—	20	—	23	—	—	—	—	—			
Transition Times Figure 2	t_{TLH}	2	75	—	95	—	—	110	—	—	—	ns			
	t_{THL}	4.5	15	15	19	19	22	22	—	—	—	—			
		6	13	—	16	—	19	—	—	—	—	—			
Input Capacitance	C_i	—	10	10	10	10	10	10	10	10	10	pF			



92CS-38436

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times and propagation delay times.