

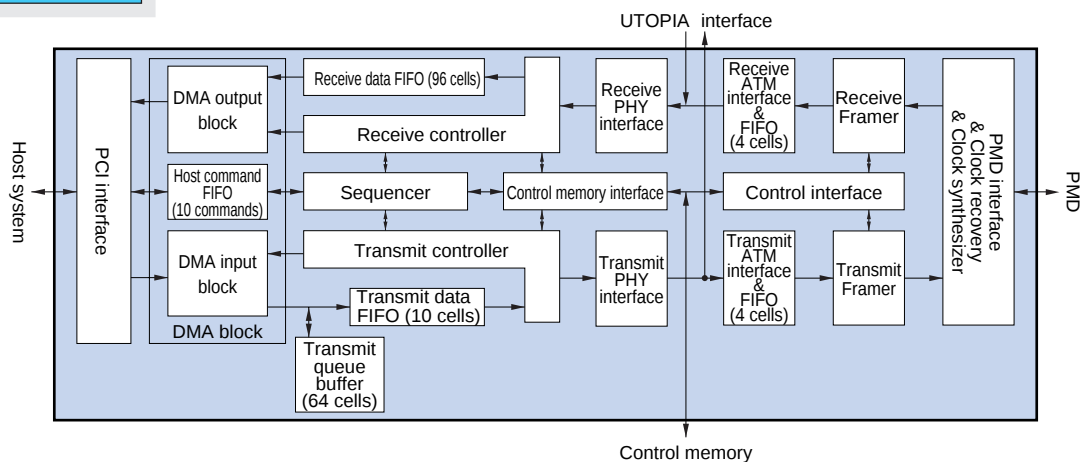
μ PD98405 PRELIMINARY

155M ATM INTEGRATED SAR CONTROLLER (NEASCOT-S20™)

Features

- Conforms to the ATM-Forum recommendations
- Supports PCI bus/Generic bus interface
 - Implements PCI bus interface (5/3.3 V, 32/64 bit, 33 MHz): PCI Specification Revision 2.1 compliant
 - Generic bus interface (5/3.3 V, 32 bit, 33 MHz)
- Implements AAL-5 SAR sublayer, ATM layer and TC sublayer
- AAL-5 type supported in hardware (non AAL-5 types can be supported in software)
- Implements SONET STS-3c/SDH STM-1 155 Mbps Framer
- Implements clock recovery/clock synthesizer
- Supports up to 32K virtual channels (VCs)
- 16 VBR traffic shapers for transmission scheduling
- ABR/UBR service supported in hardware
- Multiple-cell burst transaction for transmit and receive
- MIB counters for network management
- LAN emulation hooks
- Integrated 96 cell receive FIFO
- Supports external PHY device interface: UTOPIA Level-1 interface
- 0.35 μ m CMOS process, 5/3.3 V power supply, 304 pin plastic QFP (fine pitch)
 - Host bus interface 5 V mode: 5 V and 3.3 V power supply
 - Host bus interface 3.3 V mode: 3.3 V power supply

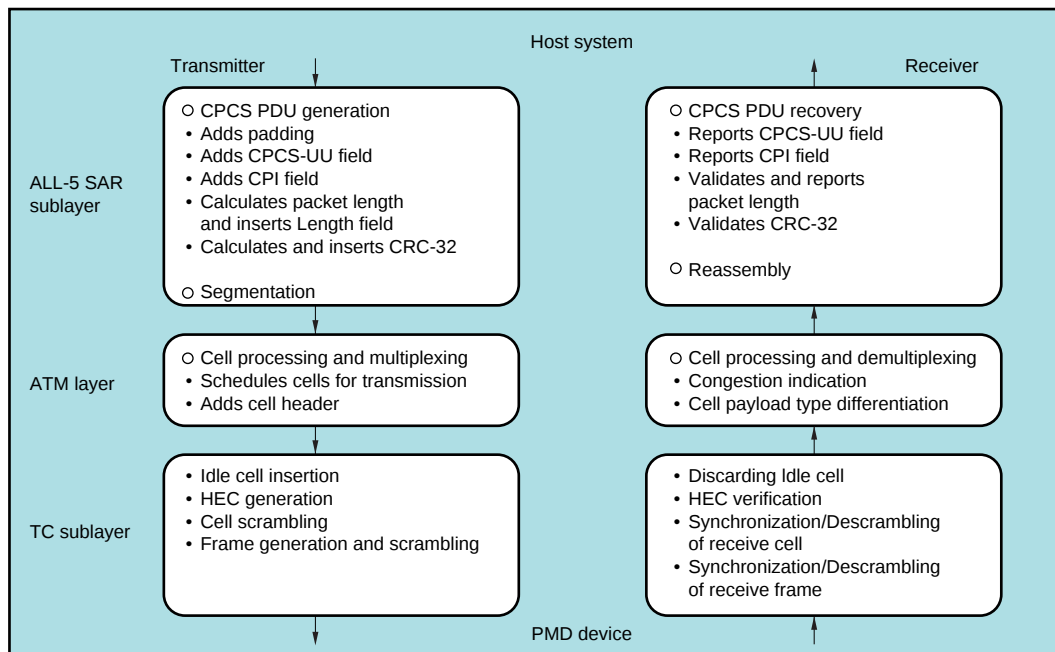
Block Diagram



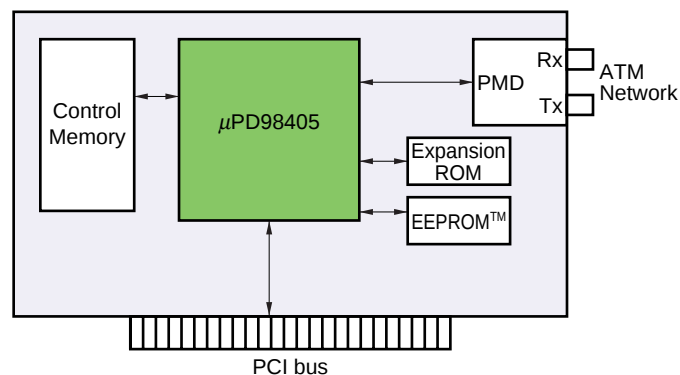
The information in this document is subject to change without notice.

Functions Overview

The μ PD98405 supports the ATM adaptation layer (AAL-5 SAR sublayer), ATM layer and TC sublayer function in hardware.



Sample configuration of ATM Adapter Card



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