Signetics

# 7476, LS76
# Flip-Flops

**Dual J-K Flip-Flop**
***Product Specification***

**Logic Products**

## DESCRIPTION

The '76 is a dual J-K flip-flop with individual J, K, Clock, Set and Reset inputs. The 7476 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

The 74LS76 is a negative edge-triggered flip-flop. The J and K inputs must be stable only one set-up time prior to the HIGH-to-LOW Clock transition.

The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active LOW inputs. When LOW, they override the Clock and Data inputs, forcing the outputs to the steady state levels as shown in the Function Table.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7476 | 20MHz | 10mA |
| 74LS76 | 45MHz | 4mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N7476N, N74LS76N |

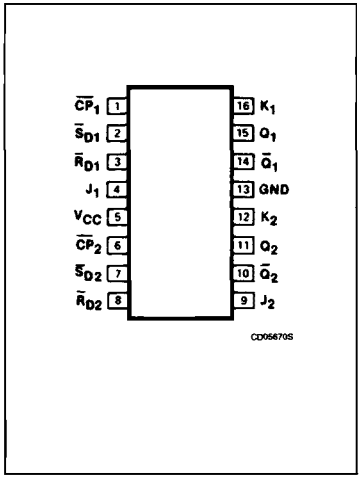
**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

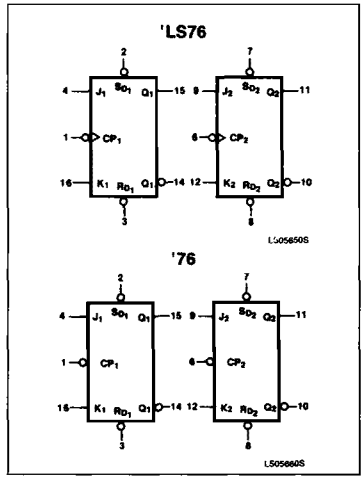
| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| $\overline{CP}$ | Clock input | 2ul | 2LSul |
| $\overline{R}_D$, $\overline{S}_D$ | Reset and Set inputs | 2ul | 2LSul |
| J, K | Data inputs | 1ul | 1LSul |
| Q, $\overline{Q}$ | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and −1.6mA $I_{IL}$, and a 74LS unit load (LSul) is 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

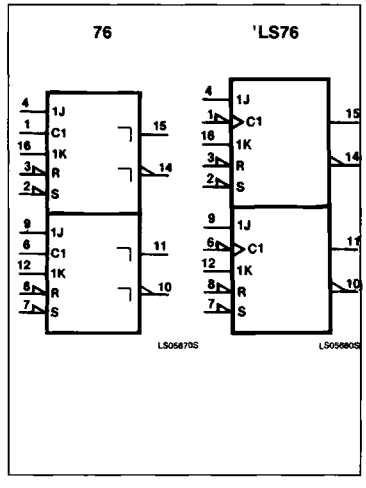
## PIN CONFIGURATION



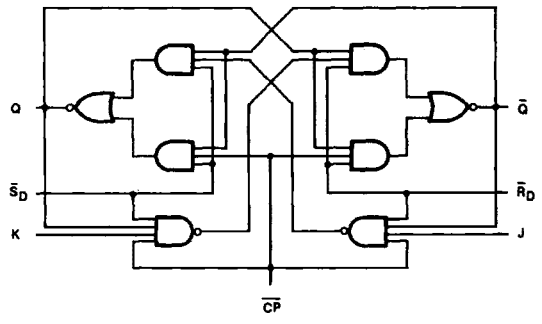

## LOGIC SYMBOL




## LOGIC SYMBOL (IEE/IEC)



## LOGIC DIAGRAM




## FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|
| | $\bar{S}_D$ | $\bar{R}_D$ | $\overline{CP}$[2] | J | K | Q | $\bar{Q}$ |
| Asynchronous set | L | H | X | X | X | H | L |
| Asynchronous reset (Clear) | H | L | X | X | X | L | H |
| Undetermined[1] | L | L | X | X | X | H | H |
| Toggle | H | H | ⎍ | h | h | $\bar{q}$ | q |
| Load "0" (Reset) | H | H | ⎍ | l | h | L | H |
| Load "1" (Set) | H | H | ⎍ | h | l | H | L |
| Hold "no change" | H | H | ⎍ | l | l | q | $\bar{q}$ |

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.[3]
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.[3]
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
X = Don't care.
⎍ = Positive Clock pulse.

**NOTES:**
1. Both outputs will be HIGH while both $\bar{S}_D$ and $\bar{R}_D$ are LOW, but the output states are unpredictable if $\bar{S}_D$ and $\bar{R}_D$ go HIGH simultaneously.
2. The 74LS76 is edge triggered. Data must be stable one set-up time prior to the negative edge of the Clock for predictable operation.
3. The J and K inputs of the 7476 must be stable while the Clock is HIGH for conventional operation.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to $+V_{CC}$ | −0.5 to $+V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74 | | | 74LS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −400 | | | −400 | μA |
| $I_{OL}$ | LOW-level output current | | | 16 | | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| PARAMETER | | TEST CONDITIONS[1] | | | 7476 | | | 74LS76 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ[2] | Max | Min | Typ[2] | Max | |
| $V_{OH}$ | HIGH-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = MIN, $V_{IL}$ = MAX, $I_{OH}$ = MAX | | | 2.4 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | LOW-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OL}$ = MAX | | | 0.2 | 0.4 | | 0.35 | 0.5 | V |
| | | | $I_{OL}$ = 4mA (74LS) | | | | | | 0.25 | 0.4 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = $I_{IK}$ | | | | | −1.5 | | | −1.5 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX | $V_I$ = 5.5V | | | | 1.0 | | | | mA |
| | | | $V_I$ = 7.0V | J, K Inputs | | | | | | 0.1 | mA |
| | | | | $\overline{S}_D$, $\overline{R}_D$ Inputs | | | | | | 0.3 | mA |
| | | | | $\overline{CP}$ Inputs | | | | | | 0.4 | mA |
| $I_{IH}$ | HIGH-level input current | $V_{CC}$ = MAX | $V_I$ = 2.4V | J, K Inputs | | | 40 | | | | μA |
| | | | | $\overline{S}_D$, $\overline{R}_D$ Inputs | | | 80 | | | | μA |
| | | | | $\overline{CP}$ Inputs | | | 80 | | | | μA |
| | | | $V_I$ = 2.7V | J, K Inputs | | | | | | 20 | μA |
| | | | | $\overline{S}_D$, $\overline{R}_D$ Inputs | | | | | | 60 | μA |
| | | | | $\overline{CP}$ Inputs | | | | | | 80 | μA |
| $I_{IL}$ | LOW-level input current[5] | $V_{CC}$ = MAX, $V_I$ = 0.4V | | J, K Inputs | | | −1.6 | | | −0.4 | mA |
| | | | | $\overline{S}_D$, $\overline{R}_D$ Inputs | | | −3.2 | | | −0.8 | mA |
| | | | | $\overline{CP}$ Inputs | | | −3.2 | | | −0.8 | mA |
| $I_{OS}$ | Short-circuit output current[3] | $V_{CC}$ = MAX | | | −18 | | −57 | −20 | | −100 | mA |
| $I_{CC}$ | Supply current[4] (total) | $V_{CC}$ = MAX | | | | 10 | 40 | | 4 | 8 | mA |

**NOTES:**
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.
3. $I_{OS}$ is tested with $V_{OUT}$ = +0.5V and $V_{CC}$ = $V_{CC}$ MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the Clock input grounded and all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs HIGH in turn.
5. $\overline{S}_D$ is tested with $\overline{R}_D$ HIGH, and $\overline{R}_D$ is tested with $\overline{S}_D$ HIGH.

## AC ELECTRICAL CHARACTERISTICS $T_A$ = 25°C, $V_{CC}$ = 5.0V

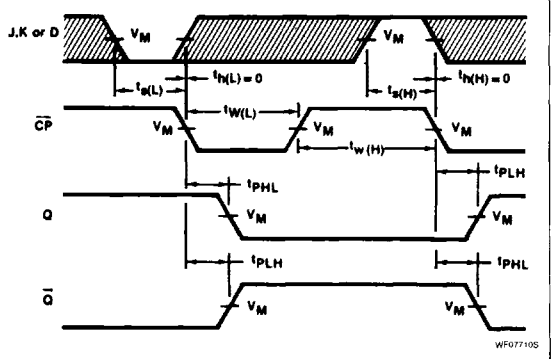
| PARAMETER | | TEST CONDITIONS | 74 | | 74LS | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $C_L$ = 15pF, $R_L$ = 400Ω | | $C_L$ = 15pF, $R_L$ = 2kΩ | | |
| | | | Min | Max | Min | Max | |
| $f_{MAX}$ | Maximum clock frequency | Waveform 3 | 15 | | 30 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>Clock to output | Waveform 1, 'LS76<br>Waveform 3, '76 | | 25<br>40 | | 20<br>30 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{S}_D$ or $\overline{R}_D$ to output | Waveform 2 | | 25<br>40 | | 20<br>30 | ns |

**NOTE:**
Per industry convention, $f_{MAX}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width of duty cycle.

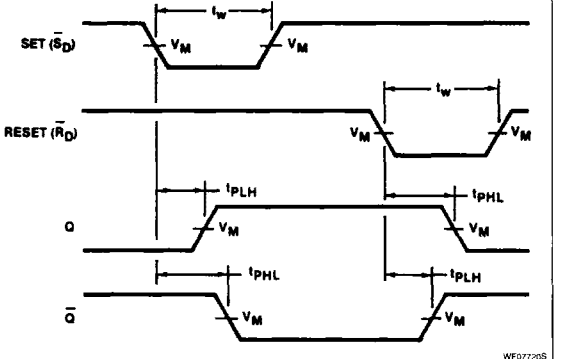
## AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

| PARAMETER | | TEST CONDITIONS | 74 | | 74LS | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_W(H)$ | Clock pulse width (HIGH) | Waveform 1 | 20 | | 20 | | ns |
| $t_W(L)$ | Clock pulse width (LOW) | Waveform 1 | 47 | | | | ns |
| $t_W(L)$ | Reset pulse width (LOW) | Waveform 2 | 25 | | 25 | | ns |
| $t_S$ | Set-up time J or K to Clock[C] | Waveform 1 | 0 | | 20 | | ns |
| $t_h$ | Hold time J or K to Clock | Waveform 1 | 0 | | 0 | | ns |

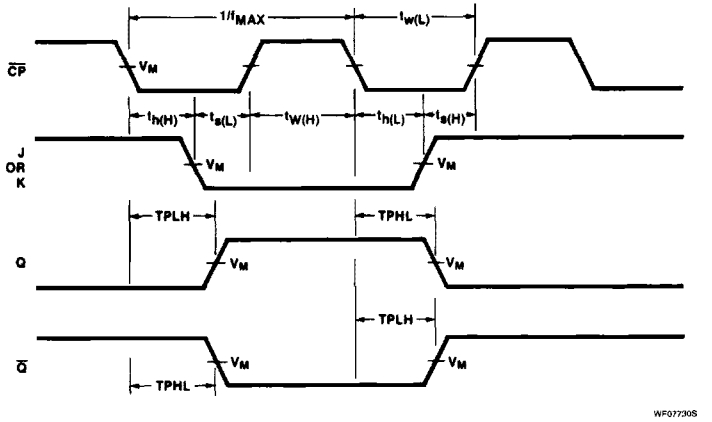
## AC WAVEFORMS




**Waveform 1. Clock To Output Delays, Data Set-up And Hold Times, Clock Pulse Width**



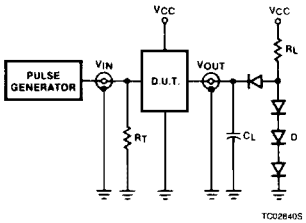

**Waveform 2. Set And Reset To Output Delays, Set And Reset Pulse Widths**



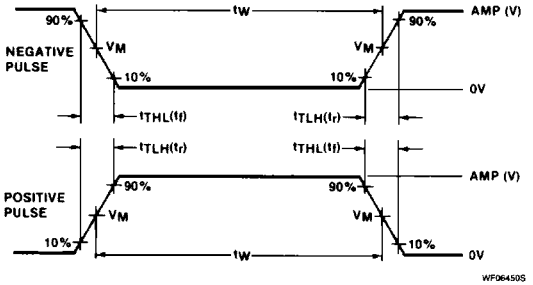

For all waveforms, $V_M = 1.3V$ for 74S; $V_M = 1.5V$ for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

**Waveform 3. Propagation Delay and $f_{MAX}$**

## TEST CIRCUITS AND WAVEFORMS




**Test Circuit For 74 Totem-Pole Outputs**




$V_M$ = 1.3V for 74LS; $V_M$ = 1.5V for all other TTL families.

**Input Pulse Definition**

DEFINITIONS

$R_L$ = Load resistor to $V_{CC}$; see AC CHARACTERISTICS for value.
$C_L$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
$t_{TLH}$, $t_{THL}$ Values should be less than or equal to the table entries.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|---|---|---|---|---|---|
| | Amplitude | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 74 | 3.0V | 1MHz | 500ns | 7ns | 7ns |
| 74LS | 3.0V | 1MHz | 500ns | 15ns | 6ns |
| 74S | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

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