6 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Ambient temperature under bias: PEB PEF	T_A T_A	0 – 40	70 85	°C °C
Storage temperature	T_{stg}	– 65	125	°C
Voltage on any pin with respect to ground	V_S	– 0.4	V_{DD} + 0.4	V
Maximum voltage on any pin	V_{max}		6	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter		Symbol	Limit Values		Unit	Test Condition
			min.	max.		
L-input voltage		V_{IL}	– 0.4	0.8	V	
H-input voltage		V_{IH}	2.2	V_{DD} + 0.4		
L-output voltage		V_{OL}		0.45	V	I_{OL} = 7 mA (pins DU3..0, DD3..0) I_{OL} = 2 mA (all other)
H-output voltage		V_{OH}	2.4		V	I_{OH} = – 400 µA
H-output voltage		V_{OH}	V_{DD} – 0.5		V	I_{OH} = – 100 µA
Power supply current	operational	I_{CC}		 9.5 6.5	mA mA	V_{DD} = 5 V, inputs at 0 V or V_{DD}, no output loads PDC > 4.096 MHz PDC ≤ 4.096 MHz
Input leakage current		I_{LI}		10	µA	0 V < V_{IN} < V_{DD} to 0 V
Output leakage current		I_{LO}		10	µA	0 V < V_{OUT} < V_{DD} to 0 V

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.

Capacitances

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}		10	pF
Output capacitance	C_{OUT}		15	pF
I/O	$C_{I/O}$		20	pF

AC Characteristics

Ambient temperature under bias range, V_{DD} = 5 V ± 5 %.

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0".
Timing measurements are made at 2.0 V for a logical "1" and at 0.8 V for a logical "0".
The AC-testing input/output wave forms are shown below.

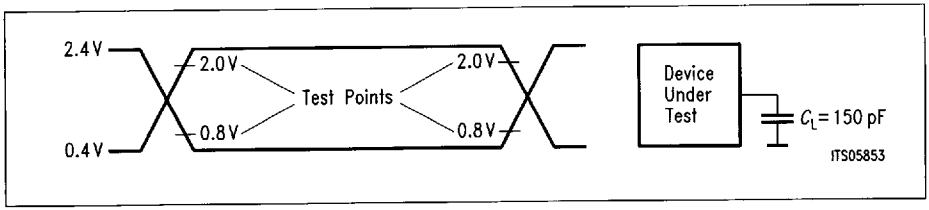


Figure 89
I/O-Wave Form for AC-Test

Bus Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
R or $\overline{W}$ set-up to $\overline{DS}$	t_{DSD}	0		ns
$\overline{RD}$-pulse width	t_{RR}	120		ns
$\overline{RD}$-control interval	t_{RI}	70		ns
Data output delay from $\overline{RD}$	t_{RD}		100	ns
Data float delay from $\overline{RD}$	t_{DF}		25	ns
$\overline{WR}$-pulse width	t_{WW}	60		ns
$\overline{WR}$-control interval	t_{WI}	70		ns
Data set-up time to $\overline{WR}$x$\overline{CS}$, $\overline{DS}$x$\overline{CS}$	t_{DW}	30		ns
Data hold time from $\overline{WR}$x$\overline{CS}$, $\overline{DS}$x$\overline{CS}$	t_{WD}	10		ns
ALE-pulse width	t_{AA}	30		ns
Address set-up time to ALE	t_{AL}	10		ns
Address hold time from ALE	t_{LA}	15		ns
ALE set-up time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address set-up time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10		ns
Address hold time from $\overline{WR}$	t_{AH}	40		ns

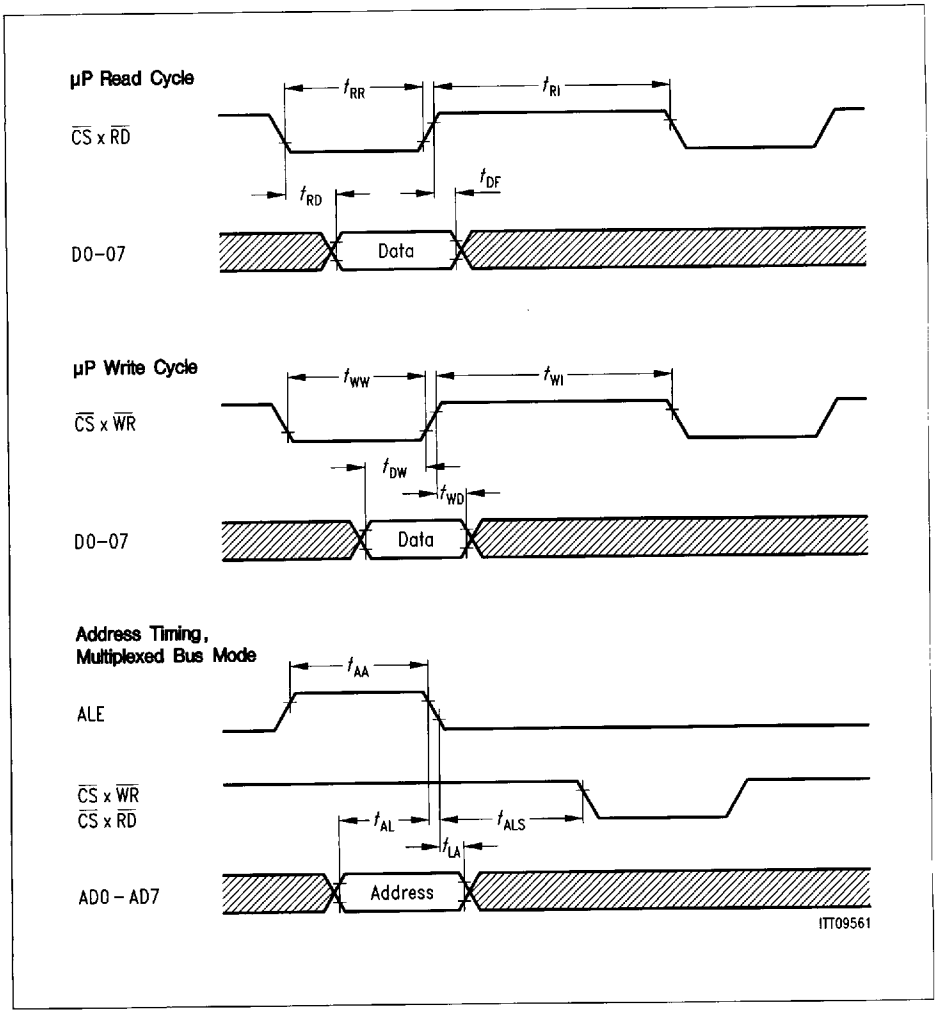


Figure 90
Siemens/Intel Bus Mode

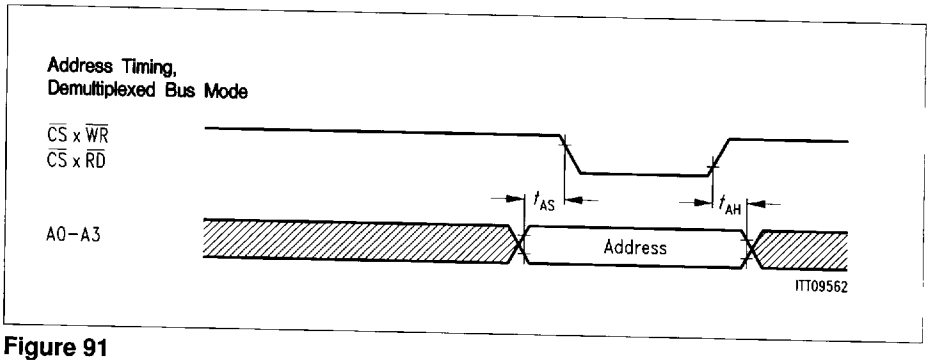


Figure 91
Siemens/Intel Bus Mode

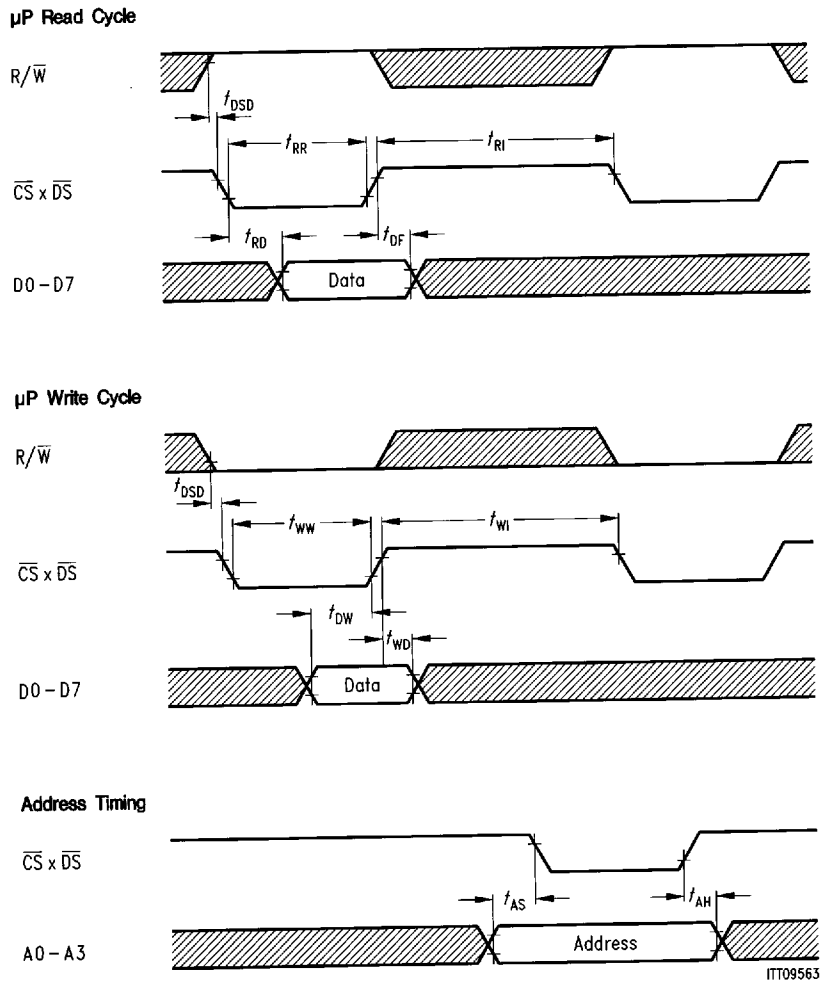


Figure 92
Motorola Bus Mode

PCM and Configurable Interface Timing

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Clock period	t_{CP}	240		ns	Clock frequency ≤ 4096 kHz
Clock period low	t_{CPL}	80		ns	
Clock period high	t_{CPH}	100		ns	
Clock period	t_{CP}	120		ns	Clock frequency > 4096 kHz
Clock period low	t_{CPL}	50		ns	
Clock period high	t_{CPH}	50		ns	
Frame set-up time to clock	t_{FS}	25		ns	
Frame hold time from clock	t_{FH}	50		ns	
Data clock delay	t_{DCD}		125	ns	2)
Serial data input set-up time (falling clock edge)	t_S	7		ns	PCM-input data frequency > 4096 kbit/s
Serial data input set-up time (rising clock edge)	t_S	15		ns	
Serial data hold time	t_H	35		ns	
Serial data input set-up time	t_S	15		ns	PCM-input data frequency ≤ 4096 kbit/s
Serial data hold time	t_H	55		ns	
Serial data input set-up time	t_S	20		ns	CFI-input data frequency > 4096 kbit/s
Serial data hold time	t_H	50		ns	
Serial data input set-up time	t_S	0		ns	CFI-input data frequency ≤ 4096 kbit/s
Serial data hold time	t_H	75		ns	
PCM-serial data output delay	t_D		55	ns	1)
Tristate control delay	t_T		60	ns	1)
CFI-serial data output delay	t_{CDF}		65	ns	Falling clock edge 2)
CFI-serial data output delay	t_{CDR}	–	90	ns	Rising clock edge 2)

1) Parameter can be estimated to: 20 ns + 0.25 ns x [C_L]

2) The max. difference between T_{DCD} and T_{CDF} / T_{CDR} is 60 ns / 35 ns

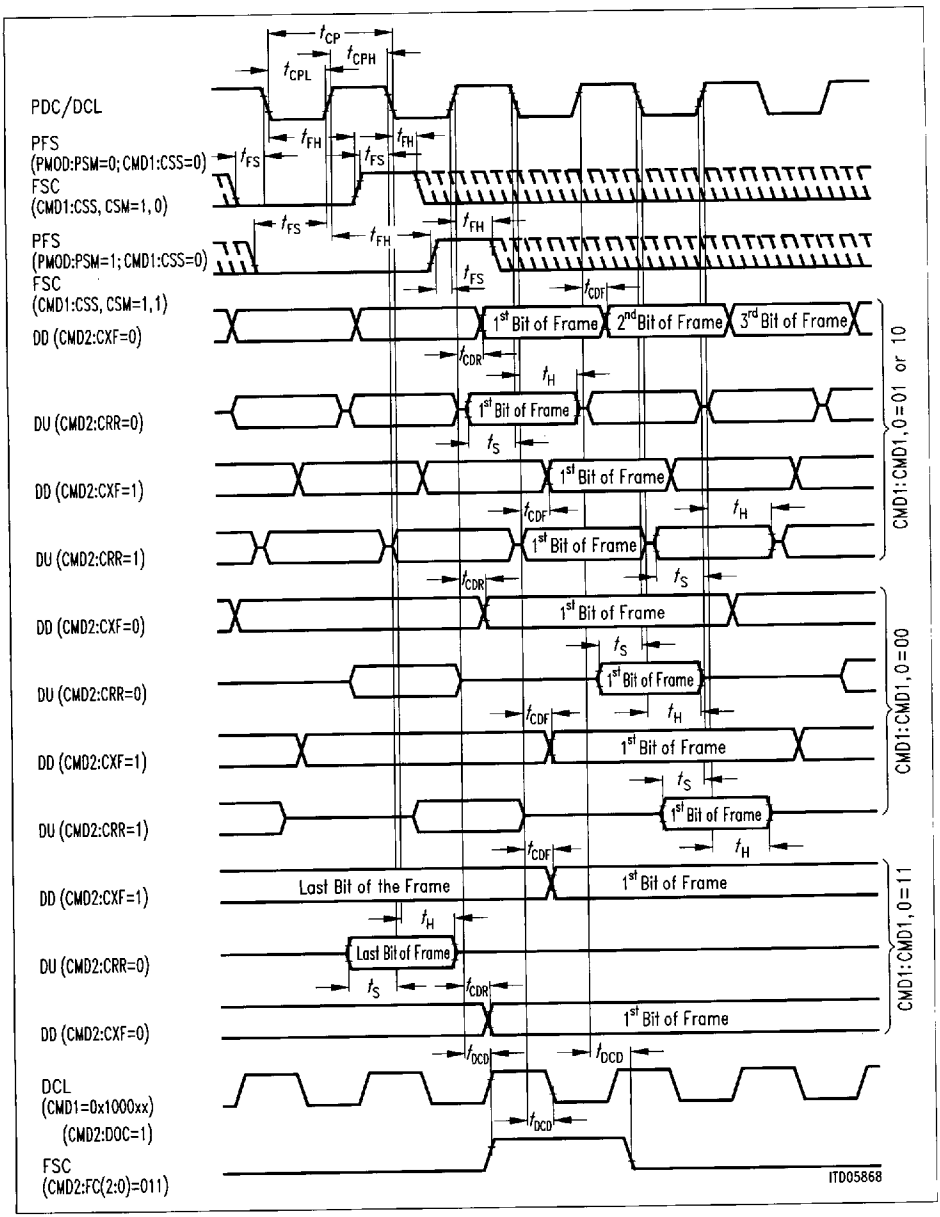


Figure 93
Configurable Interface Timing, CMD:CSP1,0 = 10 (prescaler divisor = 1)

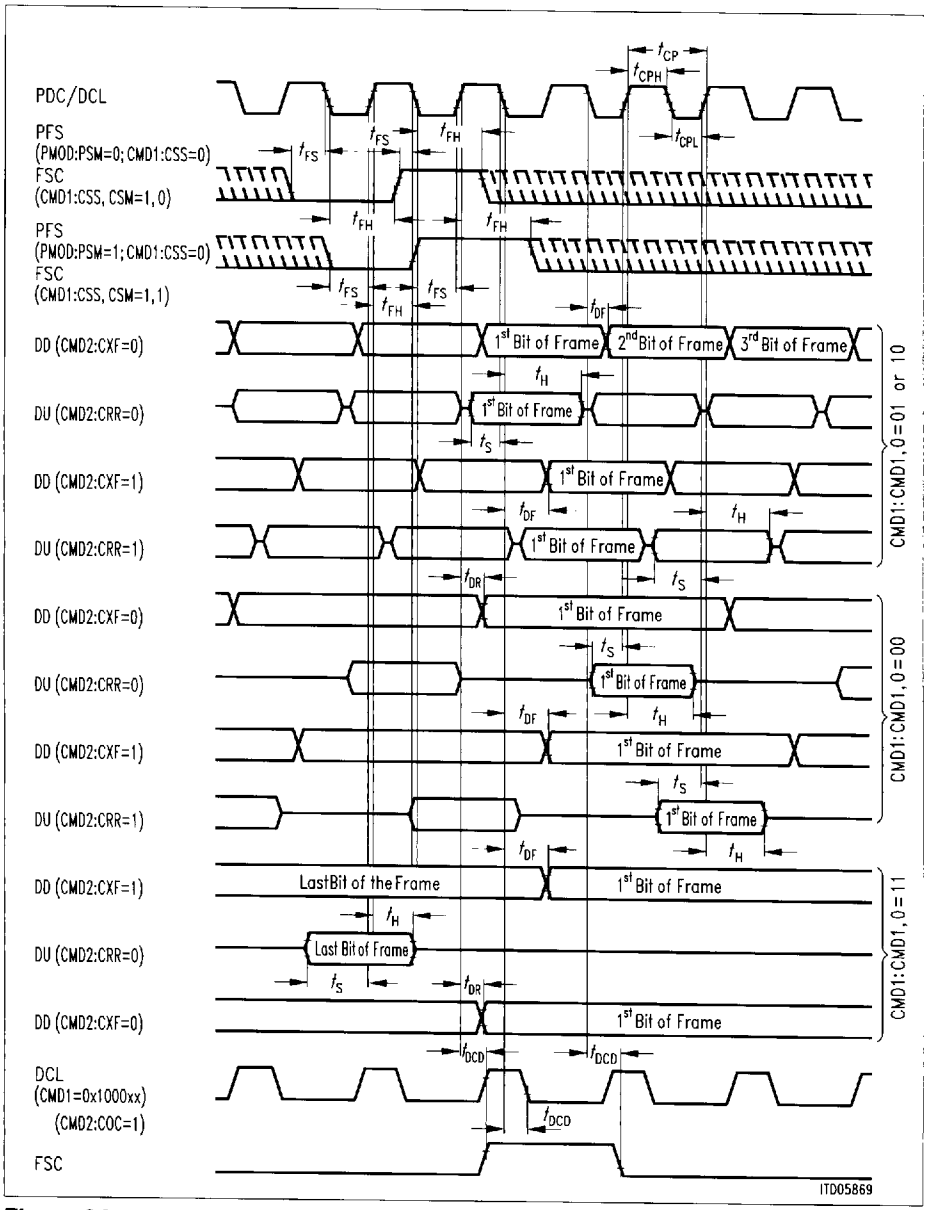


Figure 94
Configurable Interface Timing, CMD:CSP1,0 = 01 (prescaler divisor = 1,5)

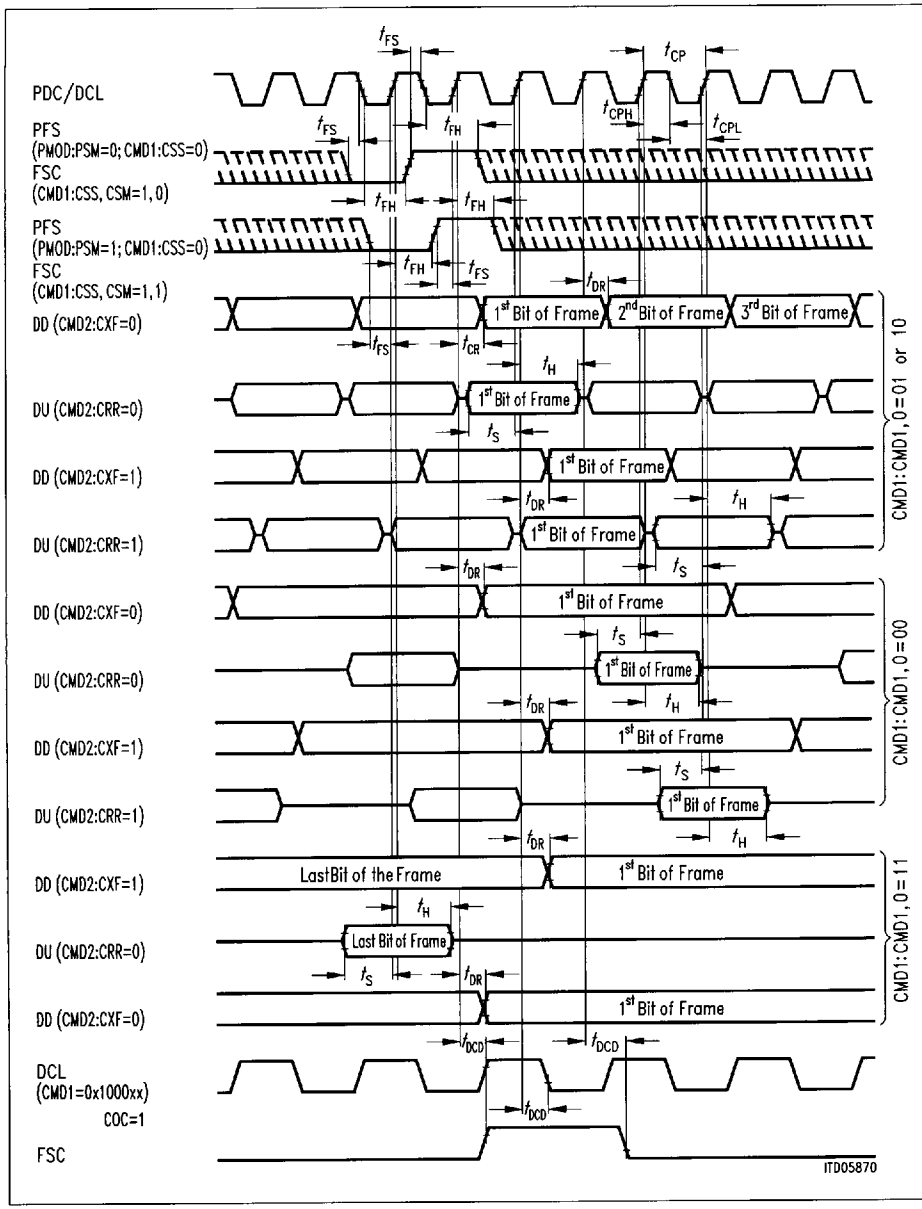


Figure 95
Configurable Interface Timing, CMD:CSP1,0 = 00 (prescaler divisor = 2)

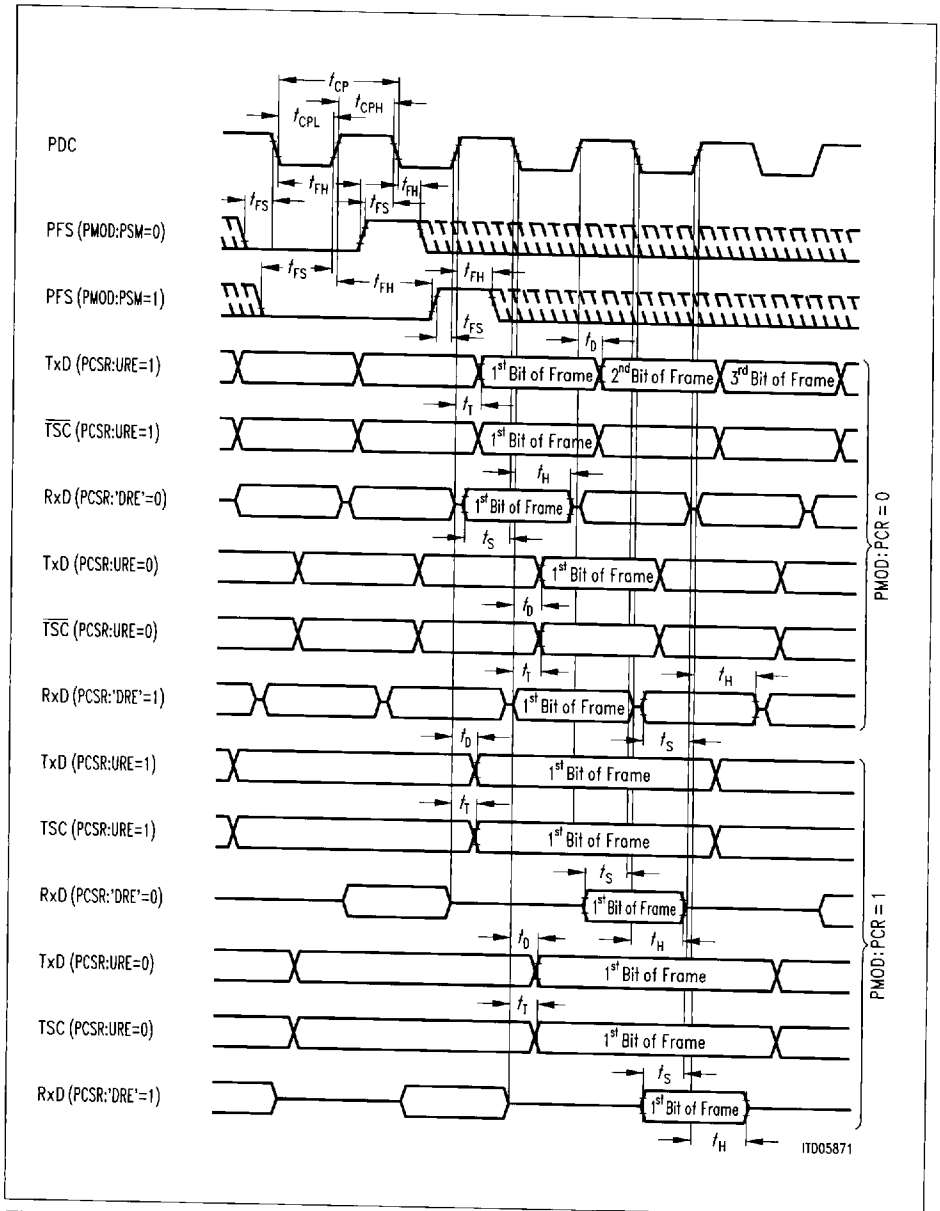
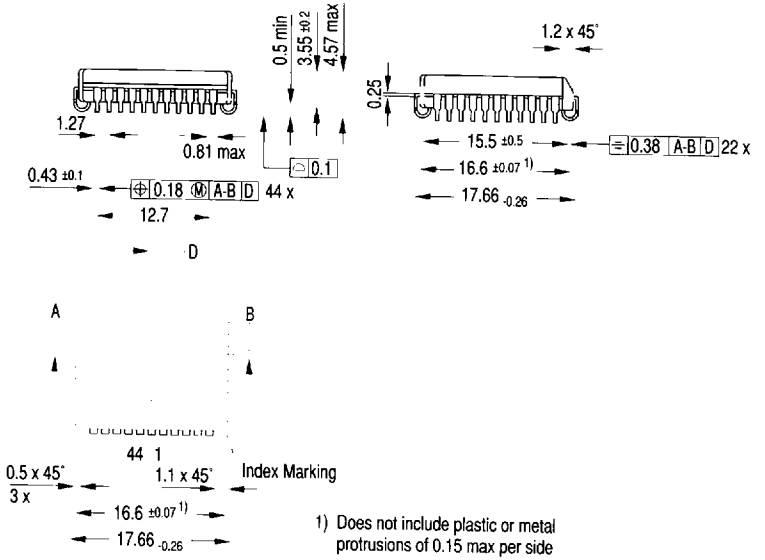


Figure 96
PCM-Interface Timing

7 Package Outlines

P-LCC-44-1
(Plastic Leaded Chip Carrier)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"
SMD = Surface Mounted Device

Dimensions in mm