

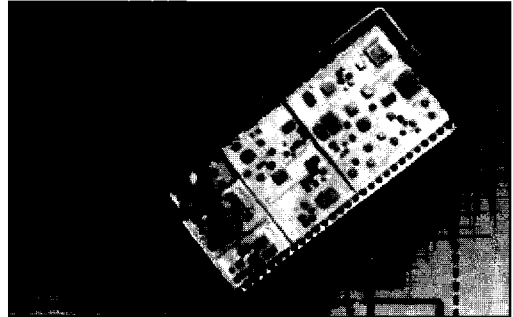
SP9490 16-Bit, 1MHz Sampling ADC

FEATURES

- 16-Bit Resolution
- 1MHz Sampling Rate
- $\pm 0.003\%$ FSR Integral Linearity
- 0V to +10V, $\pm 5V$ and $\pm 10V$ Input Ranges
- 3.5W Maximum Power Dissipation

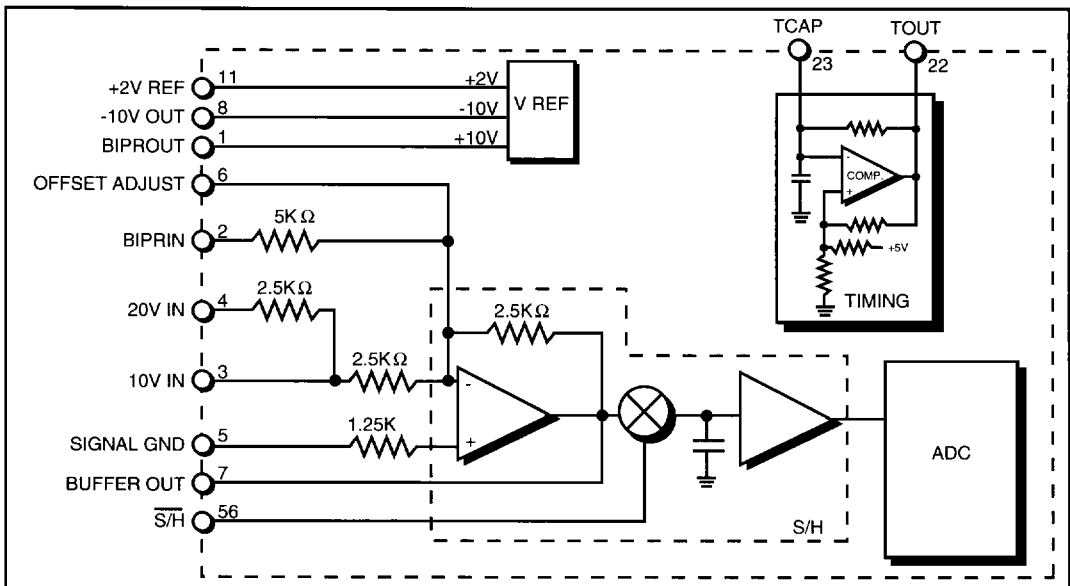
APPLICATIONS

- Medical Imaging —
CT Scanning and MRI
- Vibration Analysis
- Transient Recorders
- Waveform Analyzers
- High-speed Data Acquisition
- Analytical Instrumentation
- Communications
- Automated Test Equipment



DESCRIPTION

The **SP9490** is a complete high-performance 16-bit sampling ADC subsystem. It consists of a 16-bit accurate S/H amplifier and a 16-bit digital subranging ADC in a single package. All reference, timing and control circuitry is provided internally. The user simply provides an analog input signal, power supply volt-ages, and a single S/H MODE/CONVERT control signal.



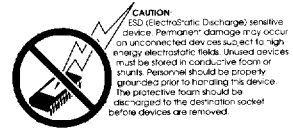
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Figure 1. Block Diagram

Absolute Maximum Ratings

+V ₂ to ANA GND	+17V
-V ₂ to ANA GND	-17V
+V _{2S} to ANA GND	+7.5V
-V _{2S} to ANA GND	-7.5V
V _{DD} to DIG GND	+7.5V
ANA GND to DIG GND	±300mV
Analog Input	±11V
Digital Inputs	-0.4V to V _{DD} +0.5V

Output Short Circuit Duration (without damage)	5 seconds
-10V Reference Output	5 seconds
Digital Outputs (to any other output)	5 seconds
Storage Temperature	-65°C to +150°C



SPECIFICATIONS

(Typical @ 25°C and nominal supply voltages unless otherwise specified)

	MIN	TYP	MAX	UNITS	CONDITIONS
ANALOG INPUT					
Input Range		0 to +10 ±5 ±10		Volts Volts Volts	
Input Impedance					
+10V Input Range		2.5		kohms	
+20V Input Range		5.0		kohms	
-10V (Hi Z) Input Range		10		Gohms	6pF input capacitance
DIGITAL INPUTS					
Logic Levels			0.8	Volts	
V _{IL}	2.0			Volts	
V _{IH}				Volts	
Input Current, I _{IN}		±0.5		μA	V _{IN} = 0.5V
Input Capacitance		20		pF	
DIGITAL OUTPUTS					
Logic Levels			0.4	Volts	
V _{OL}	2.4	0.2		Volts	I _{OL} = 3.2mA
V _{OH}		4.5		Volts	I _{OH} = -3.2mA
Output Capacitance		2.0		pF	
Leakage, Outputs Tri-stated	-30		+30	μA	
Data Valid		25	50	ns	after pos. edge of EOC
Ready/Busy	640	660	680	ns	
Resolution	16			ns	-55°C to +125°C
Data Output Coding		Binary Offset Binary		Bits	
TRANSFER CHARACTERISTICS					
Combined S/H and ADC			3	LSB	
Integral Linearity Error	-0.8		1.0	LSB	
Differential Linearity Error		Guaranteed			
No Missing Codes					
Gain Error					
+10V Range	-0.1		+0.1	%FSR	
+20V Range	-0.1		+0.1	%FSR	
Offset Error					
Unipolar	-0.1		+0.1	%FSR	
Bipolar	-0.1		+0.1	%FSR	
DC Noise					
10V Input		140		μV	-FS
		160		μV	+FS
Hi-Z (SIGGND) Input	100		100	μV	-FS
	130		130	μV	+FS
DYNAMIC PERFORMANCE					
Conversion Time	640		680	ns	at 1MHz sampling rate
Signal-to-Noise Ratio					
F _{IN} = 15kHz	82	84		dB	
F _{IN} = 100kHz		84		dB	
F _{IN} = 500kHz		82		dB	

SPECIFICATIONS (continued)

(Typical @ 25°C and nominal supply voltages unless otherwise specified)

	MIN	TYP	MAX	UNITS	CONDITIONS
DYNAMIC PERFORMANCE					
Total Harmonic Distortion					at 1MHz sampling rate
$F_{IN} = 15\text{kHz}$	87	92		dB	
$F_{IN} = 100\text{kHz}$		88		dB	
$F_{IN} = 500\text{kHz}$		60		dB	
SINAD					
$F_{IN} = 15\text{kHz}$	81	83		dB	at 1MHz sampling rate
$F_{IN} = 100\text{kHz}$		80		dB	
$F_{IN} = 500\text{kHz}$		60		dB	
Spurious-Free Dyn. Range					
$F_{IN} = 15\text{kHz}$	88	93		dB	at 1MHz sampling rate
$F_{IN} = 100\text{kHz}$		85		dB	
$F_{IN} = 500\text{kHz}$		60		dB	
SAMPLE-AND-HOLD					
Acquisition Time					
±20V Step		450		ns	to ±0.005%
±10V Step		350		ns	to ±0.005%
±5V Step		300		ns	to ±0.01%
Sample Distortion					
5V _{p,p} , 100kHz		86		dB	
20V _{p,p} , 15kHz		93		dB	
Frequency Response					
Small Signal		30		MHz	-3dB
Full Power					
20V _{p,p}		2		MHz	
10V _{p,p}		4		MHz	
Slew Rate		120		V/μs	
HOLD MODE DYNAMICS					
Pedestal Offset Error		±0.2		mV	
Pedestal Gain Error		±0.002		% FSR	
Pedestal Linearity Error		±0.0005		% FSR	
Dielectric Absorption		0.0055		% FSR	
Aperture Delay		30		ns	
Aperture Uncertainty		75		ps rms	
STABILITY					
Offset Tempco					
Unipolar		5		ppm/°C	
Bipolar		10		ppm/°C	
Gain Tempco					
+10V Range		20		ppm/°C	
+20V Range		20		ppm/°C	
Integral Linearity Tempco					
		3		ppm/°C	
Diff. Linearity Tempco					
		2		ppm/°C	
PSRR			1.0	%FSR/%Δ	
POWER REQUIREMENTS					
+15V Analog (+V _S)		60	75	mA	
-15V Analog (-V _S)	-55	-45		mA	
+5V Analog (+V _{SS})		270	330	mA	
-5V Analog (-V _{SS})	-90	-80		mA	
+5V Digital(+V _{DD})		0.3	5	mA	
Dissipation		3.25	3.5	W	
ENVIRONMENTAL					
Operating Temperature	0		+70	°C	

DESCRIPTION

(Continued from Page 1)

The full scale input range of the SP9490 is pin-selectable for 0V to -10V unipolar, or $\pm 5V$ and $\pm 10V$ bipolar ranges. Output data is presented in a 16-bit wide parallel TTL/CMOS-compatible format. The output latches are tri-stated for easy microprocessor interfacing. The single control signal determines the S/H acquisition time, and the overall throughput of the SP9490. Bipolar 5V and 15V power supplies at a combined maximum dissipation of 3.0 watts are required.

The **SP9490** is available for operation over the 0°C to +70°C commercial temperature range. The **SP9490** is packaged in a 58-pin metal package.

PIN ASSIGNMENTS

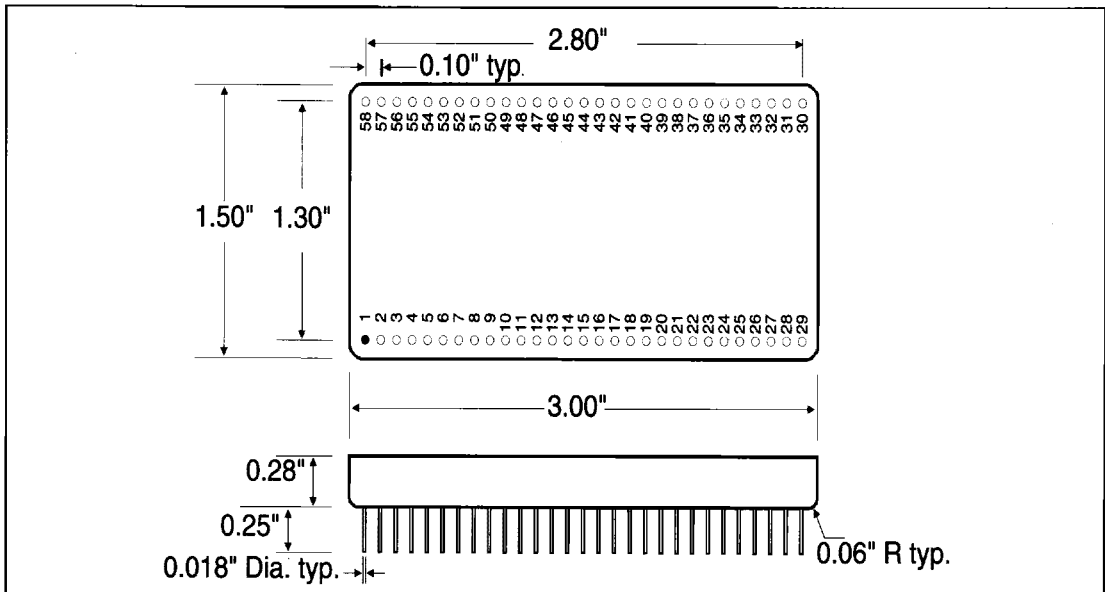
1. BIPROUT	58. DO NOT CONN.
2. BIPRIN	57. DO NOT CONN.
3. 10V IN	56. S/H
4. 20V IN	55. +15V
5. SIG GND	54. -15V
6. OFFSET ADJUST	53. DO NOT CONN.
7. BUFFER OUT	52. DO NOT CONN.
8. -10V REF	51. DO NOT CONN.
9. NC	50. DO NOT CONN.
10. DO NOT CONN.	49. DO NOT CONN.
11. +2V REF	48. OE
12. -5V ANA	47. BIT 1 (MSB)
13. +5V ANA	46. BIT 2
14. ANA GND.	45. BIT 3
15. NC	44. BIT 4
16. NC	43. BIT 5
17. READY/ <u>BUSY</u>	42. BIT 6
18. DO NOT CONN.	41. BIT 7
19. DO NOT CONN.	40. BIT 8
20. EOC	39. BIT 9
21. A/D CLK	38. BIT 10
22. TOUT	37. BIT 11
23. TCAP	36. BIT 12
24. -5V ANA	35. BIT 13
25. -15V ANA	34. BIT 14
26. +15V ANA	33. BIT 15
27. ANA GND	32. BIT 16 (LSB)
28. +5V ANA	31. +5V DIG
29. NC	30. DIG GND

ORDERING INFORMATION

16-Bit, 1MHz Sampling ADC

SP9490K 0°C to +70°C

MECHANICAL DIMENSIONS



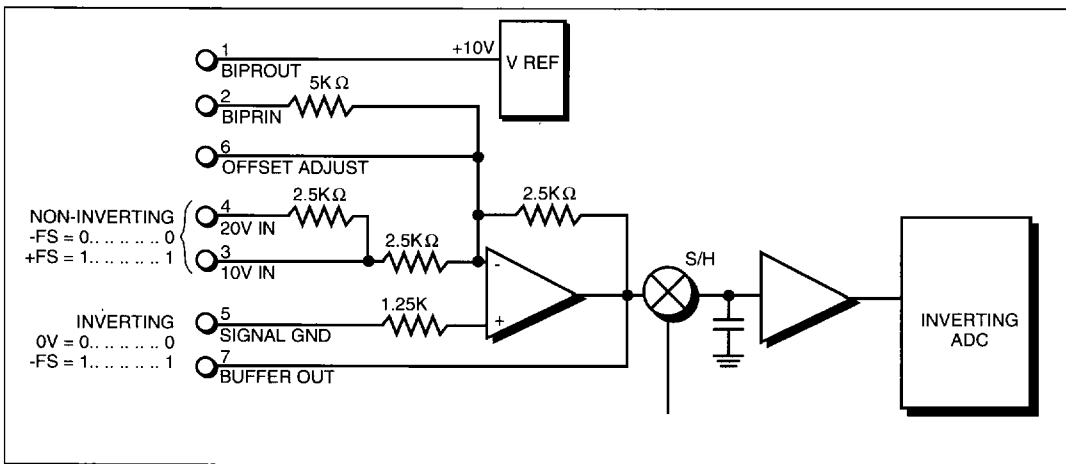


Figure 2. Input Circuitry

SELECTING THE FULL SCALE INPUT RANGE

The SP9490 supports 0V to +10V and 0V to +20V unipolar, and $\pm 5V$ and $\pm 10V$ bipolar full scale input ranges. Figure 2 shows the overall input circuitry of the SP9490. The figures that follow show the connections for each input range as described below.

It should be noted that input configurations that use the 10V and 20V inputs (pins 3 and 4 respectively) as the signal inputs are *non-inverting* inputs, despite the fact that they are connected to the inverting input of the input buffer amplifier. This overall non-inverting process is due to the inverting action of the ADC itself, plus the inversion of the buffer amplifier.

10V Unipolar Full Scale Range

Figure 3 shows the input connections required to achieve a 10V unipolar full scale

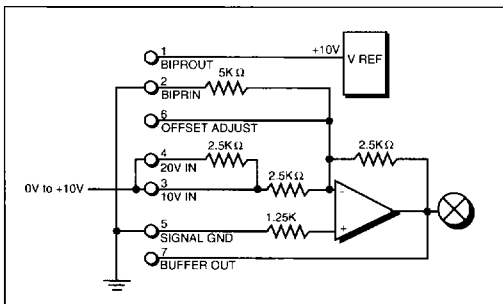


Figure 3. 10V Unipolar Input

input range. This configuration has a noise gain of 2.5. To reduce noise pickup, the bipolar reference input pin (BIPRIN, pin 2) should be tied to signal ground. The input impedance is nominally 2.5k Ω .

10V Bipolar Full Scale Range

Figure 4 shows the input connections required for $\pm 5V$ inputs. The bipolar reference out (BIPROUT, Pin 1) is connected to the reference input (pin 2) to provide the appropriate offset to the ADC. Again the noise gain in this configuration is 2.5, and the input impedance is nominally 2.5k Ω .

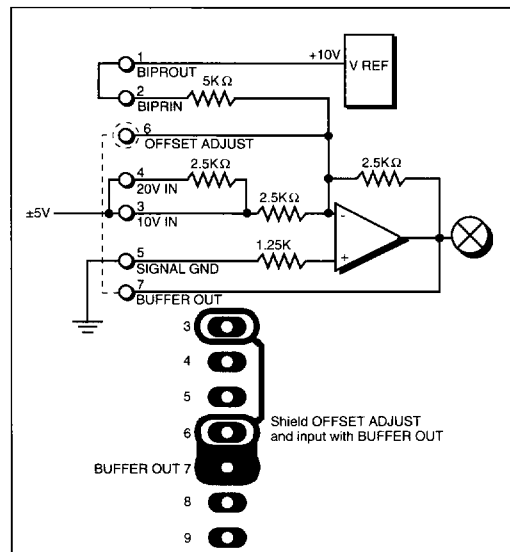


Figure 4. 10V Bipolar Input

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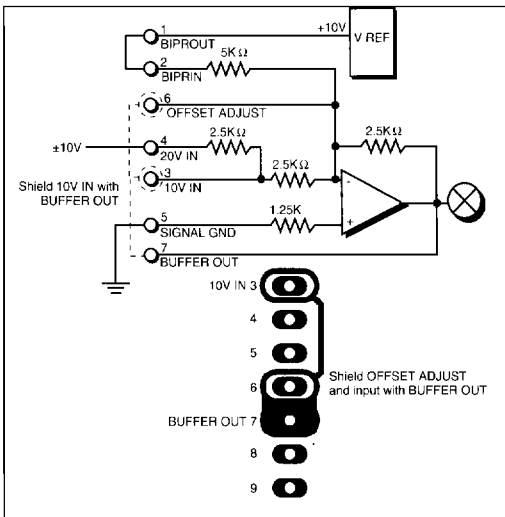


Figure 5. ±10V Bipolar Input

20V Bipolar (±10V) Full Scale Range

The ±10V bipolar input range connections are somewhat more critical than the previous two input configurations if noise pickup is to be tightly controlled. In this configuration, the 10V IN (pin 3) is not connected. If left unshielded, it will significantly contribute to the input noise, and therefore reduce converter performance. As shown in Figure 5, the output of the buffer amplifier is used to guard the 10V IN pin to reduce the amount of noise pickup. The input impedance of this configuration is 5kΩ.

Using the same input configuration, a unipolar 20V input range can be accommodated by 1) removing the connection between BIPROUT (pin 8) and BIPRIN (pin 2), and 2) connecting BIPRIN (pin 2) to signal

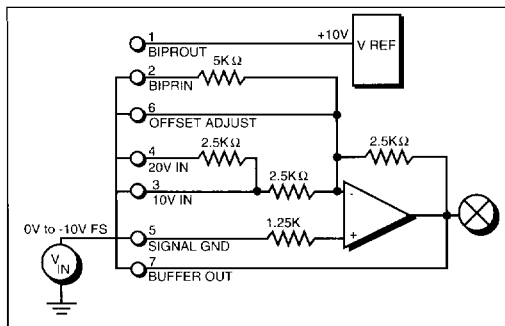


Figure 6. High Impedance Input

ground (pin 5).

High Impedance (Inverting) Input Applications requiring a high impedance input can drive the SIGGND pin directly with respect to the signal ground plane, as shown in Figure 6. All unused inputs must be connected to the BUFFER OUT (pin 7) signal to reduce noise pickup. The input impedance of this configuration is $10^{10}\Omega$ in parallel with 6pF. A graph showing the effect of temperature on input impedance is shown in Figure 7. Since this configuration uses the non-inverting input of the buffer amplifier, the overall ADC will invert the sense of the data with respect to the input signal:

$$\begin{aligned} 0V &= 0 \dots \dots 0 \\ -10V &= 1 \dots \dots 1 \end{aligned}$$

MULTIPLEXED INPUTS

The use of a multiplexer in front of the SP9490 requires that the SIGGND input (pin 5) be used as the signal input as shown in Figure 6, since it presents a very high input impedance. If multiple multiplexers are to be used in front of the SP9490, as shown in Figure 8, then a buffer amplifier should be used between the multiplexer outputs and the 10V (pin 3) or 20V (pin 4) signal inputs.

USING THE VOLTAGE REFERENCE

The -10V reference output (Pin 8) can be used by external circuitry provided no more than 500μA of current is required. Buffering of the reference output is strongly recommended in order to isolate it from any noise or other disturbances that could affect conversion accuracy. The largest tantalum or electrolytic capacitor that can physically be tolerated should be used at

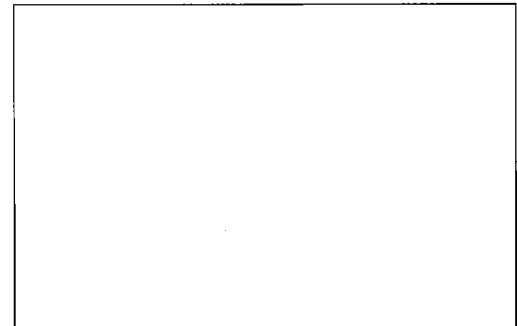


Figure 7. High Impedance Input vs Temperature

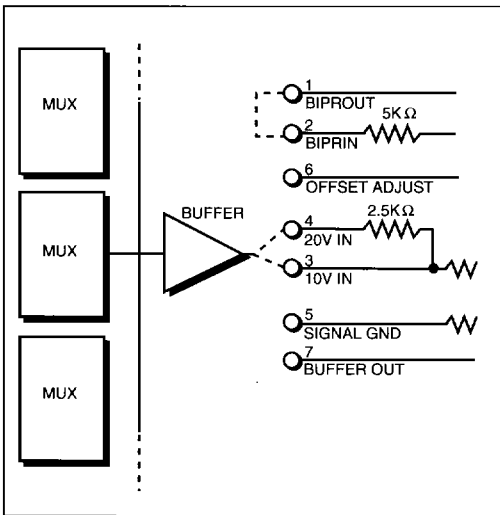


Figure 8. Multiple Multiplexer Inputs

the output of the buffer circuit, as shown in Figure 9. It is *not* recommended that the +10V reference output (BIPROUT, pin 1) be used by the system.

GROUNDING

Grounding practices are the single most important consideration for proper evaluation of and performance from the **SP9490**. The use of a single ground plane is *not* recommended. Figure 10 shows the preferred ground plane scheme, which was determined after much effort. It is the same as that used in our automated production test system.

From the figure, you can see that the ground plane is split into three separate



Figure 10. Ground Plane Topology

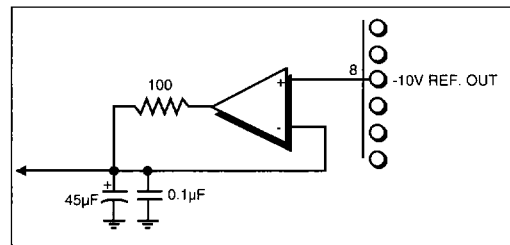


Figure 9. Voltage Reference Buffer Circuit

ground planes, connected at controlled 0V reference points. This separation can be achieved either as a single-layer on the wiring side of a double-sided printed circuit board, or, as three separate ground layers in a multi-layer pc board. In either case, the three ground planes are connected at the 0V reference points shown in Figure 10. The case of the **SP9490** is the analog ground and power return. It is critical that the case of the **SP9490** not come in contact with any of the ground planes. If possible, the ground planes should not be located on the component side of the pc board. See the following section on sockets for more information.

SOCKETS FOR THE SP9490

As mentioned above, the case of the **SP9490** is the analog ground and power return. The case of the converter must *not* touch any of the three ground planes on the pc board. Should this occur, the offset of the **SP9490** will change by upwards of 4mV. Again, either have the ground planes on the wiring side of the pc board, or as the internal layers of a multi-layer pc board, or use a socket to mount the **SP9490**.

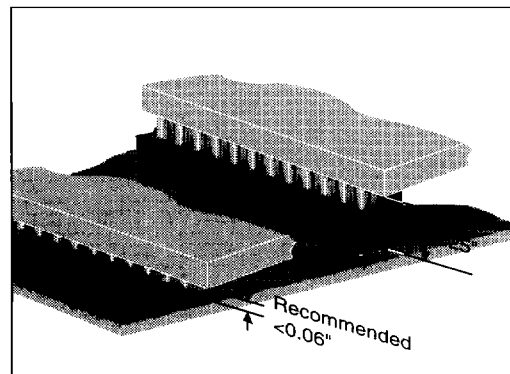


Figure 11. Recommended Board Clearance

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If the **SP9490** is socketed in a pc board, care must be taken to mount the **SP9490** as close to the pc board as possible. Sockets such as the typical test socket depicted in Figure 11 will raise the **SP9490** a quarter-inch or so off the pc board. The contact inductance of these types of sockets can cause a ± 2 LSB or more change in integral linearity. In addition, the noise introduced by this physical arrangement can become significant. A low-profile socketing approach, such as the use of Voltrex type pin sockets (Part Number MC74C), which are soldered into the pc board, provide a minimum clearance between the **SP9490** and the pc board.

POWER SUPPLIES — DISTRIBUTION AND BYPASSING

Single +5V Digital Supply

Ideally, separate ± 5 V analog and ± 5 V digital supplies should be used to power the **SP9490**. However, since most systems have ample +5V digital power supplies, and economics being a prime system design requirement, it is reasonable to attempt to supply both the +5V digital and analog supply pins of the **SP9490** from the same +5V digital supply. Without proper isolation, however, this will have disastrous results. Figure 13 shows the proper use of Murata BNX002 isolator/filters plus heavy bypassing at each +5V analog supply pin. With this approach, the **SP9490** has a reasonable chance of providing 16-bit performance.

+5V Analog and +5V Digital Supplies

If separate +5V analog and +5V digital power supplies are available in the system, then the power supply distribution scheme shown in Figure 14 will provide adequate isolation and bypassing.

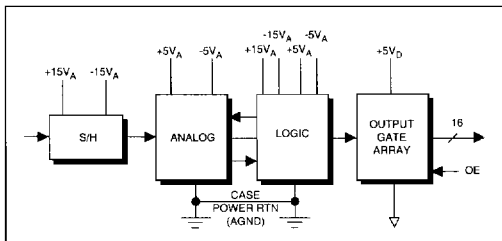


Figure 12. SP9490 Power Distribution

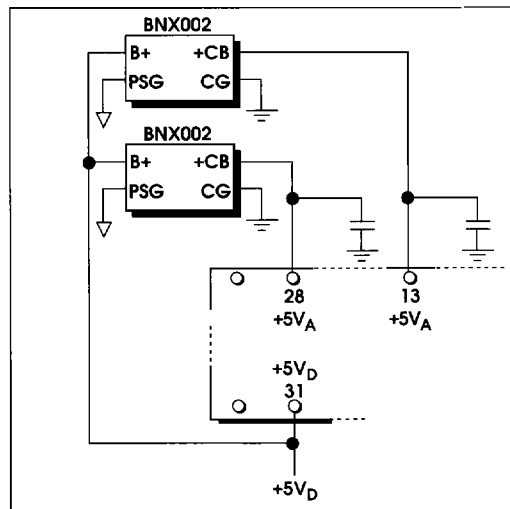


Figure 13. +5V_o Supply Distribution

The -5V Analog Supply

The -5V analog supply requirements of the **SP9490** can be satisfied from a system -5V digital supply if the isolation/bypassing scheme shown in Figure 15 is used.

Bypassing

Every power supply pin on the SP9490 must be bypassed. The largest tantalum or electrolytic capacitor that will physically fit on the pc board should be used, in parallel with a 0.1 μ F ceramic. In Figures 13 through 15, only one capacitor is shown for the sake of clarity. Each pin must use both

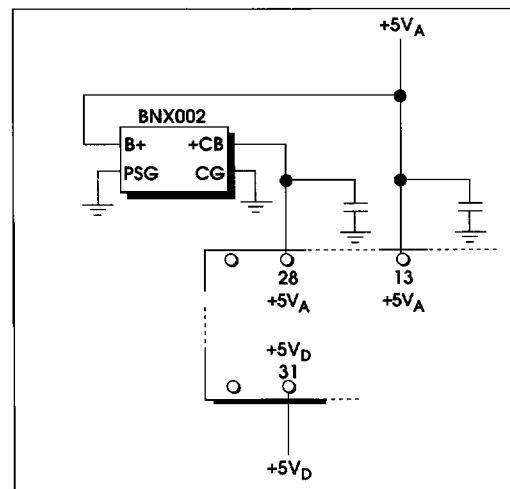


Figure 14. +5V_A & +5V_D Supply Distribution

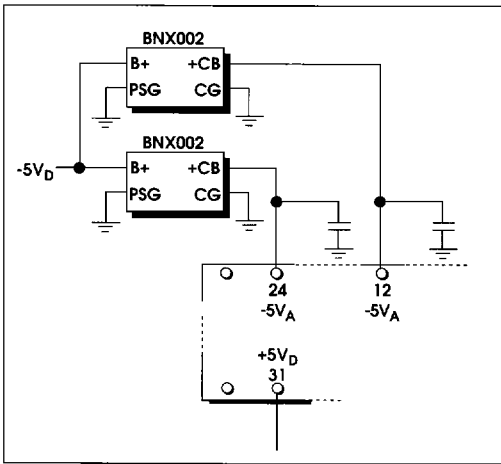


Figure 15. $-5V_D$ Supply Distribution

capacitors for effective bypassing. The capacitors must be both electrically and physically mounted as close to the **SP9490** pin as possible.

OFFSET AND GAIN ADJUST

Figure 16 shows the recommended circuit and shielding techniques for the OFFSET ADJUST on the **SP9490**. To minimize noise pickup on the OFFSET ADJUST input (pin 6), which is a direct line to the summing junction of the input amplifier, pin 6 and

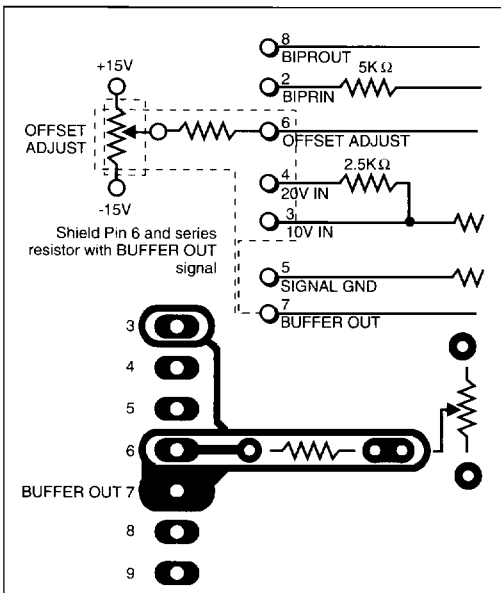


Figure 16. Offset Adjust Circuitry

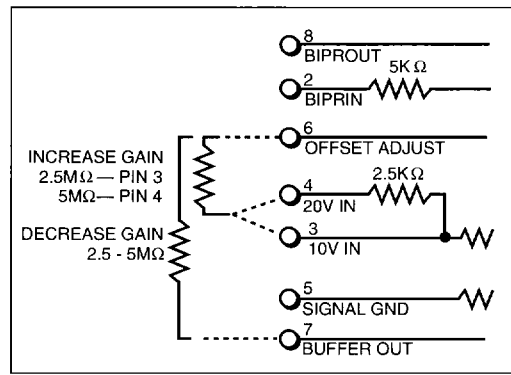


Figure 17. Gain Adjust

the offset adjust circuitry are shielded with the output of the input amplifier. The lead length connected to pin 6 must be as short as possible.

The GAIN ADJUST on the **SP9490** is accomplished by connecting a fixed resistor in parallel with either the series input resistor or the input amplifier feedback resistor depending on whether the gain must be increased or decreased, respectively. The resistor should be a low tolerance, low temperature coefficient. The resistor value should be in the $2.5M\Omega$ range for the 10V and $\pm 5V$ input full scale ranges, and $5M\Omega$ for the $\pm 10V$ and 20V input full scale ranges.

TIMING

Figure 18 shows the nominal timing relationships of various signals during continuous conversions. Temperature-related timing effects are discussed later.

The S/\bar{H} control line (pin 56) provides the sample-and-hold mode control and ADC convert command. It controls the overall throughput of the **SP9490**. The conversion time is fixed at 750ns nominal. For a maximum 1MHz throughput, the S/\bar{H} control need be high (SAMPLE mode) for a minimum of 250ns. As the time allowed for sample acquisition is increased, the overall throughput decreases accordingly.

The READY/BUSY status line (pin 17) provides a convenient, and recommended, signal with which output data can be latched into external registers. The falling edge of this status signal occurs at the least critical time in the overall conversion

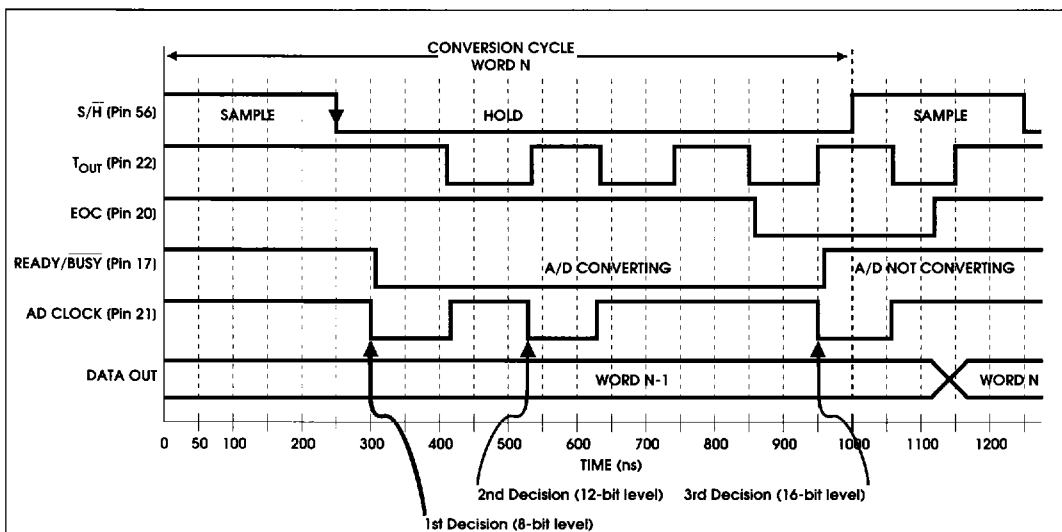


Figure 18. Nominal Timing

process — the S/H has already gone into the HOLD mode, and the converter is making its first conversion decision, which is accurate only to the 8-bit level. Any power supply disturbances resulting from latching the output data will therefore have minimum effect on the conversion results. The A/D CLOCK (pin 21) is shown for reference only. *No connection should be made to this pin, for any reason.*

OUTPUT ENABLE (OE) (pin 48) controls the tri-state output of the SP9490 data latches. The output changes state 15ns typically

both going into or out of the tri-state mode. Leakage current is $\pm 10\mu\text{A}$ in the tri-stated mode at 25°C.

TEMPERATURE EFFECTS ON TIMING

The internal timing of the SP9490 is affected by temperature. A 100°C change in temperature results in a 50ns change in conversion time. Since the conversion time is fixed by the internal logic of the SP9490, trimming of the timing circuit at the anticipated operating temperature is necessary for accurately timed throughput rates.

If the SP9490 is to be operated from 25°C to 40°C, it is unlikely that a trim would have to be made. To achieve the full 1MHz throughput rate at a 90°C case temperature, the timing must be brought back to within its nominal limits.

The temperature coefficient is negative, i.e. as the temperature increases, the internal timing circuit slows down; conversely, as the temperature decreases, the timing circuit speeds up. Figure 19 shows how a resistor connected across the T_{CAP} and T_{OUT} pins (23 and 22 respectively) speeds up the timing circuits, while a capacitor connected from T_{CAP} (pin 23) to analog ground will slow down the timing circuit. Nominal values are 1.8KΩ for the resistor and 68pF for the capacitor.

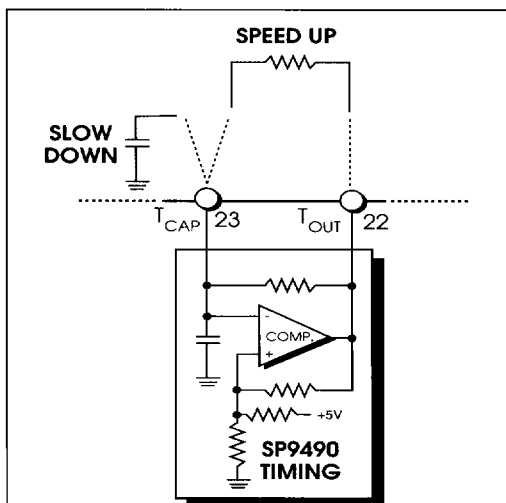


Figure 19. Compensation of Temperature Effects on Timing

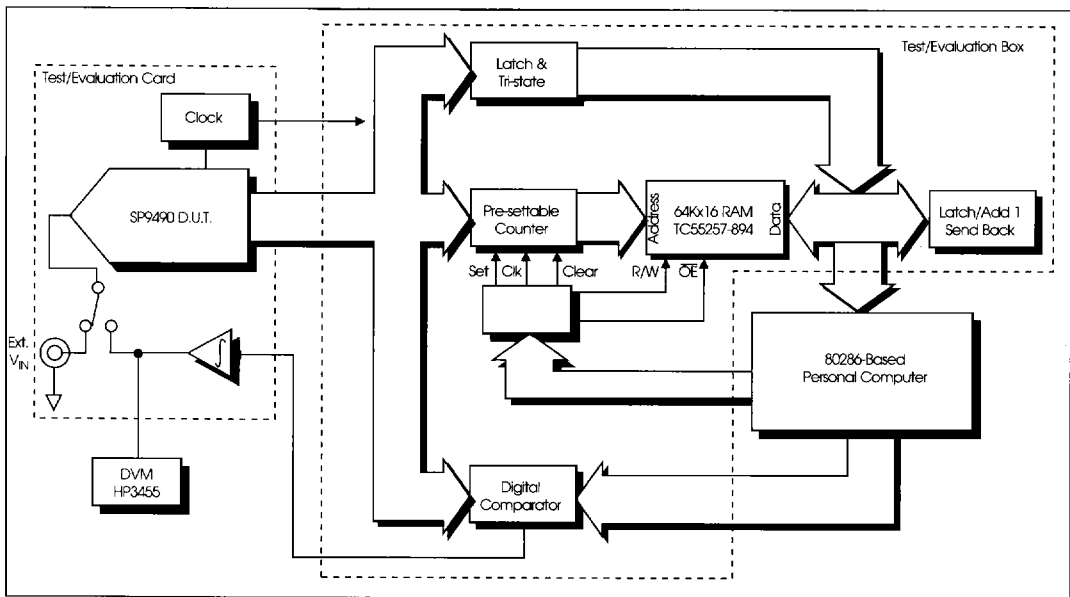


Figure 20. Test/Evaluation System Block Diagram

EVALUATING THE SP9490

The following describes the test methods used at Sipex to evaluate the **SP9490s** performance on a production basis. Each converter is tested on an 80286 CPU-based personal computer-driven test system. With a single insertion, all critical DC and dynamic performance testing are accomplished as described below.

We are certainly not suggesting that a potential user of the **SP9490** must amass a test system such as the one described here in order to determine whether or not the SP9490 is suitable for a design under consideration. However, the information here may suggest an evaluation method that will allow the full performance of the SP9490 to be appreciated. To further assist in the evaluation of the **SP9490**, an evaluation board is available by consulting the factory.

The **SP9490** requires high accuracy, low distortion, DC and dynamic testing in order to fully guarantee specified performance. Dynamic applications such as Magnetic Resonance Imaging require specified FFT data which reflects the response of the SP9490 to a given fundamental input frequency. The dynamic data collected quantifies noise and nonlinearity as a function of frequency. This portion of

production test set for the SP9490 is versatile enough to evaluate different frequencies and dynamic ranges including a Nyquist frequency of 500 kHz at a peak to peak magnitude of 10V, at the 16-bit level.

Static testing of the **SP9490** proves the performance of the part in multiplexed applications such as CAT scanners or Data Acquisition Systems. Linearity, noise, and settling time are key parameters when low frequency or DC measurements are required. Due to the architecture of the SP9490, there are no predictable points along the transfer function where the errors will be the greatest. Thus, all 65,536 codes must be evaluated. Histograms make this type of data analysis possible on a production basis.

The **SP9490** is tested on one test system which incorporates all AC and DC testing. Test time has also been minimized and handling has been reduced. Figure 20 shows the organization of the test system and the basic flow of data.

The test system is made up of three sections. The first is the (IBM®) 286-based computer which controls all the operations and executes all necessary mathematics. The second is the test box which includes a 64K RAM, digital comparators, latches, and

logic control. The third is the DUT test card which includes its own clock and integrator and interfaces directly to the test box. The following discussion will describe the algorithms used for some of the AC and DC testing.

DISTORTION TESTING

Distortion is tested with a $10V_{pp}$ sinewave input at a total conversion time of $1\mu S$. Even at the Nyquist frequency of $500kHz$, the instantaneous rate of change of the input signal does not exceed the capabilities of the sample-and-hold within the **SP9490**. Therefore, the sample acquisition time can be reduced to $250ns$. The A/D conversion time is a constant $700ns$ starting from the falling edge of the S/H control. A $50ns$ delay is added to this for a total conversion time of $1\mu s$.

SNR

Signal to Noise Ratio (SNR) is one of the dynamic tests performed on the **SP9490** on a production basis. The test is carried out by first supplying the **SP9490** with a pure $16\text{-bit } 10V_{pp}$ sinewave, created by a **Sipex**-designed signal generator. The analog input is filtered to remove noise using a

low-pass filter. The **SP9490** continuously converts the sinewave and stores the consecutive digital words at each location of the RAM. The data is taken until a complete FFT record is full. When there is enough data, the RAM is dumped to the CPU where the FFT calculations are carried out. Other AC tests carried out in this manner include Total Harmonic Distortion which represents the total signal-related harmonics, spurious-free dynamic range, and SINAD which is Signal to Noise plus Distortion.

ALL CODES TESTING

All codes testing is performed by using a very slow ramp input that ranges from minus full scale to plus full scale. The 2^{16} consecutive addresses in RAM are associated with each output code of the **SP9490**. The values stored at each location in RAM are cleared to zero at the beginning of the test. As the analog input ramp ranges from -FS to +FS, the digital output code increments from all zeros to all ones. As the digital output of the A/D addresses a location in RAM, the value stored there is incremented. An ideal converter will have the same number of occurrences for each

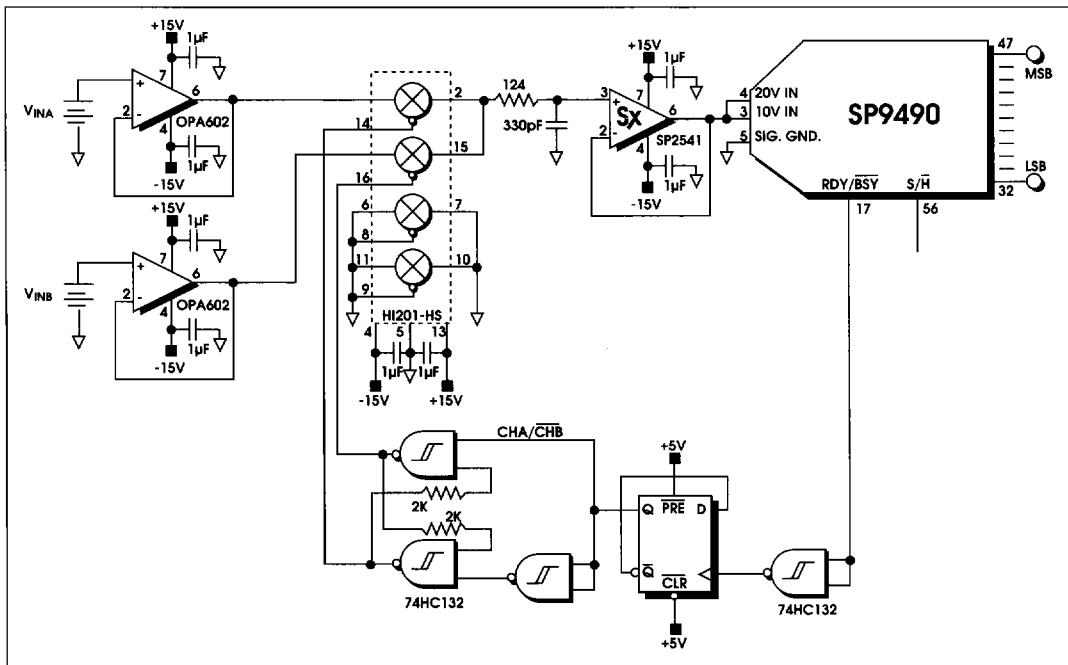


Figure 21. Sample Acquisition Test

code. All the occurrences are added and this sum is divided by 2^{16} to get the ideal number of occurrences for each location, this value is then subtracted from each of the numbers stored in RAM and this difference is divided by 1LSB. The final result represents the Differential Linearity error in LSB's. The DNL error is then accumulated to obtain the Integral Linearity.

DC NOISE

The same algorithm used to calculate linearity is also used to calculate DC noise. This test however takes continuous conversions of a DC input rather than a ramp, and the data is collected such that a bell curve of the codes representing the input is created around the input voltage. The root sum square is taken of all the codes collected. This value multiplied by one LSB is the RMS DC noise.

GAIN AND OFFSET

Since a software-controlled 16-bit accurate voltage source is very expensive and difficult to calibrate, gain and offset are measured using a servo-loop that includes the digital comparators, integrator, and DVM. To measure gain, the code for full scale is written to the digital comparator. This value is compared to the output of the SP9490. If the output of the A/D is less than the code written, then the integrator output (and A/D input) is increased, which increases the digital output of the A/D. The analog input of the **SP9490** will increase until its digital outputs are greater than the code written. The integrator will then try to integrate down until the digital output is again less than the code written. The servo-loop will continue in this manner until the integrator dithers around the voltage that corresponds to the digital code written. The value measured by the DVM at this point is stored in software as the measurement for positive full scale. The same algorithm is used at minus full scale, or at $1/2\text{FSR}$ in the bipolar case. This result is subtracted from the positive full scale value. The resultant value is the gain of the A/D. Offset is simply the value measured at minus full scale.

SAMPLE ACQUISITION ACCURACY

The sample acquisition accuracy test is the worst case scenario for the **SP9490**. It is a dynamic test that stresses the part over a

$10V_{\text{FSR}}$ step. This test closely parallels DAS applications where the user multiplexes the input between several channels. Figure 21 shows the actual circuit used to collect the data for this test.

The circuitry shown is triggered using the READY/BUSY signal (pin 17) from the SP9490. The READY/BUSY signal is high when the A/D is ready to convert, is low when the actual conversion is being carried out, and goes high when the conversion is completed and it is again ready to start a new conversion. The sample-and-hold (S/H) command is created on the DUT test card using a crystal oscillator. This signal controls the S/H and controls when the A/D converts. The S/H control is level-triggered, while the A/D converter is initiated with the falling edge of the same signal. A new input can be sampled with a logic high on the S/H control (pin 56) only when READY/BUSY is high. The S/H control must be high for at least 300ns to allow the S/H sufficient time to acquire the input signal to 16-bit accuracy. After 300ns, the next falling edge will start a conversion. The low level puts the S/H into hold mode. After about 50ns (typical) of delay, the READY/BUSY signal will go low, indicating that the A/D is converting the held signal, and will remain low until the conversion is complete. Data will be valid 25 ns (typical) after the rising edge of EOC (pin 20) and will remain valid until the next rising edge of EOC.

The sample acquisition accuracy test continuously converts a full scale square wave input such that 16 continuous conversions are done at -Full Scale and 16 conversions are done at +Full Scale. The input changes state on the falling edge of the READY/BUSY signal thus ensuring that the S/H is in the hold mode so that the input may change without interfering with the conversion taking place. All of the data points are measured using the above mentioned servo-loop, and the digital codes representing the input are stored in memory. The difference between the maximum and minimum at each level is compared to a $\pm 300\mu\text{V}$ error band, thus confirming successful consecutive conversions at both ends of the input range.

A square wave input is created using an HI201-HS, which is a high speed switch that switches between V_{IN1} and V_{IN2} . The two inputs of the switch are driven by Schmitt triggers (74HC132) which creates a "break before make" situation, minimizing transients as the switch changes levels. The timing circuit for the sample acquisition accuracy test allows for worst case

conditions so that the sample time is increased from 300ns to 350ns. The increase in the sample time allows the S/H enough time to settle after the full scale instantaneous change. This increase is due to the fact that the input changes over a $10V_{pp}$ step virtually instantaneously. The same results can be achieved at a 250ns sample time if the input is limited to $5V_{pp}$.