

Philips Components-Signetics

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Application Specific Product	

80C451/83C451/87C451

CMOS single-chip 8-bit microcontroller

DESCRIPTION

The Philips 8XC451 is an I/O expanded single-chip microcontroller fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes latch-up sensitivity.

The 8XC451 is a functional extension of the 87C51 microcontroller with three additional I/O ports and four I/O control lines. The LCC version has a total of 68 pins. The LCC version has a total of 68 pins. Four control lines associated with port 6 facilitate high-speed asynchronous I/O functions.

The 8XC451 includes a 4k X 8 ROM (83C451) EPROM (87C451), a 128 X 8 RAM, 56 (LCC) or 52 (DIP) I/O lines, two 16-bit timer/counters, a five source, two priority level, nested interrupt structure, a serial I/O port for either a full duplex UART, I/O expansion, or multi-processor communications, and on-chip oscillator and clock circuits. The 80C451 includes all of the 83C451 features except the on-board 4k X 8 ROM.

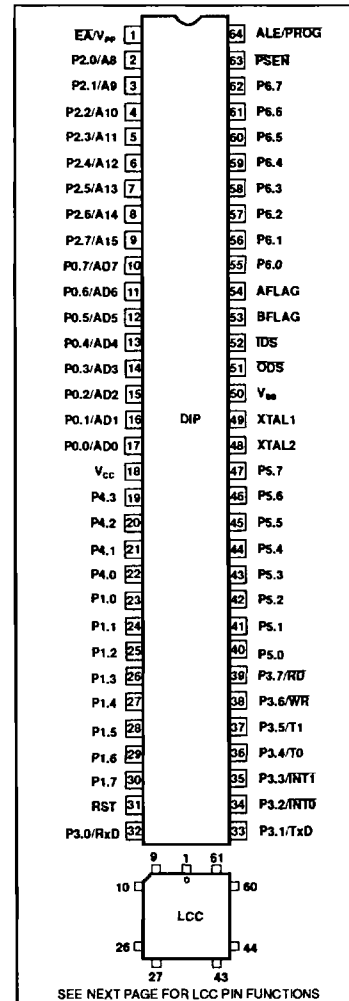
The 87C451 has 4k of EPROM on-chip as program memory and is otherwise identical to the 83C451.

The 8XC451 has two software selectable modes of reduced activity for further power reduction; idle mode and power-down mode. Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. Power-down mode freezes the oscillator, causing all other chip functions to be inoperative while maintaining the RAM contents.

FEATURES

- 80C51 based architecture
- 68-pin LCC and 64-pin DIP packages:
 - Seven 8-bit I/O ports (LCC version)
 - Six 8-bit ports and one 4-bit port (DIP version)
- Port 6 features:
 - 8 data pins
 - 4 control pins
 - Direct MPU bus interface
 - Parallel printer interface
- On the microcontroller:
 - 4k X 8 ROM (83C451)
 - 4k X 8 EPROM (87C451)
 - ROMless version (80C451)
 - 128 X 8 RAM
 - Two 16-bit counter/timers
 - Two external interrupts
- External memory addressing capability
 - 64k ROM and 64k RAM
- Low power consumption:
 - Normal operation: less than 24mA at 5V, 12MHz
 - Idle mode
 - Power-down mode

PIN CONFIGURATION



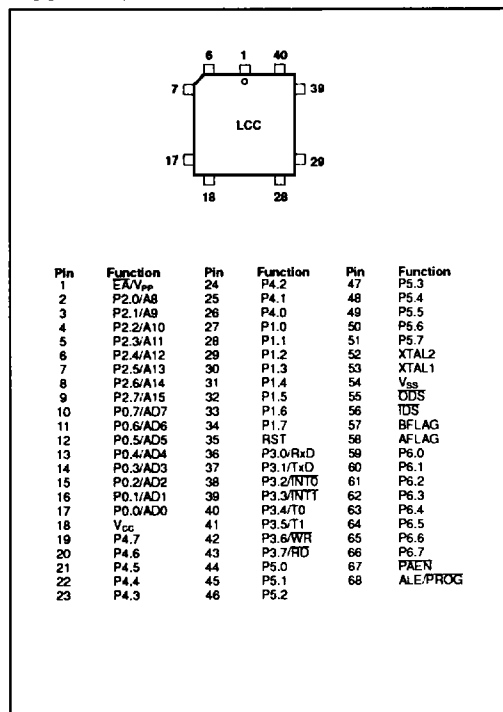
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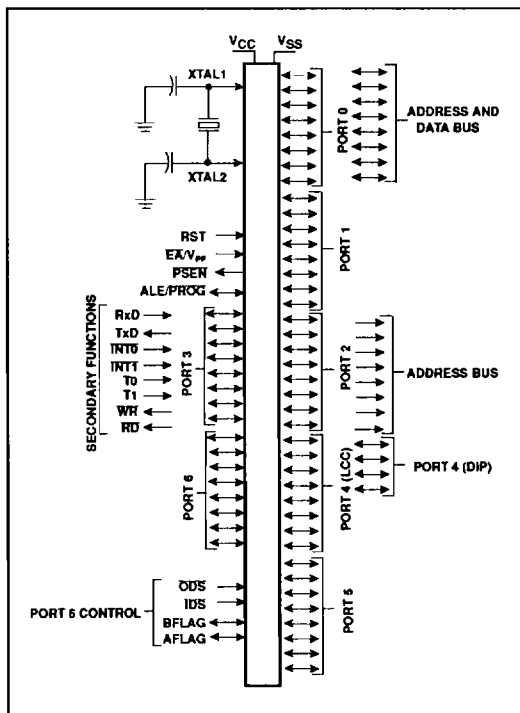
PART NUMBER SELECTION

ROMless	ROM	EPROM	TEMPERATURE °C AND PACKAGE	FREQUENCY
SC80C451CCN64	SC83C451CCN64	SC87C451CCN64	0 to +70, plastic DIP	3.5 to 12MHz
SC80C451CGN64	SC83C451CGN64	SC87C451CGN64	0 to +70, plastic DIP	3.5 to 16MHz
SC80C451CCA68	SC83C451CCA68	SC87C451CCA68	0 to +70, plastic LCC	3.5 to 12MHz
SC80C451CGA68	SC83C451CGA68	SC87C451CGA68	0 to +70, plastic LCC	3.5 to 16MHz
SC80C451ACN64	SC83C451ACN64	SC87C451ACN64	-40 to +85, plastic DIP	3.5 to 12MHz
SC80C451AGN64	SC83C451AGN64	SC87C451AGN64	-40 to +85, plastic DIP	3.5 to 16MHz
SC80C451ACA68	SC83C451ACA68	SC87C451ACA68	-40 to +85, plastic LCC	3.5 to 12MHz
SC80C451AGA68	SC83C451AGA68	SC87C451AGA68	-40 to +85, plastic LCC	3.5 to 16MHz
		SC87C451CCIA	0 to +70, ceramic DIP	3.5 to 12MHz
		SC87C451CGIA	0 to +70, ceramic DIP	3.5 to 16MHz
		SC87C451CCL68	0 to +70, ceramic LCC	3.5 to 12MHz
		SC87C451CGL68	0 to +70, ceramic LCC	3.5 to 16MHz
		SC87C451ACIA	-40 to +85, ceramic DIP	3.5 to 12MHz
		SC87C451ACL68	-40 to +85, ceramic LCC	3.5 to 12MHz
		SC87C451AGIA	-40 to +85, ceramic DIP	3.5 to 16MHz
		SC87C451AGL68	-40 to +85, ceramic LCC	3.5 to 16MHz

LCC PIN FUNCTIONS



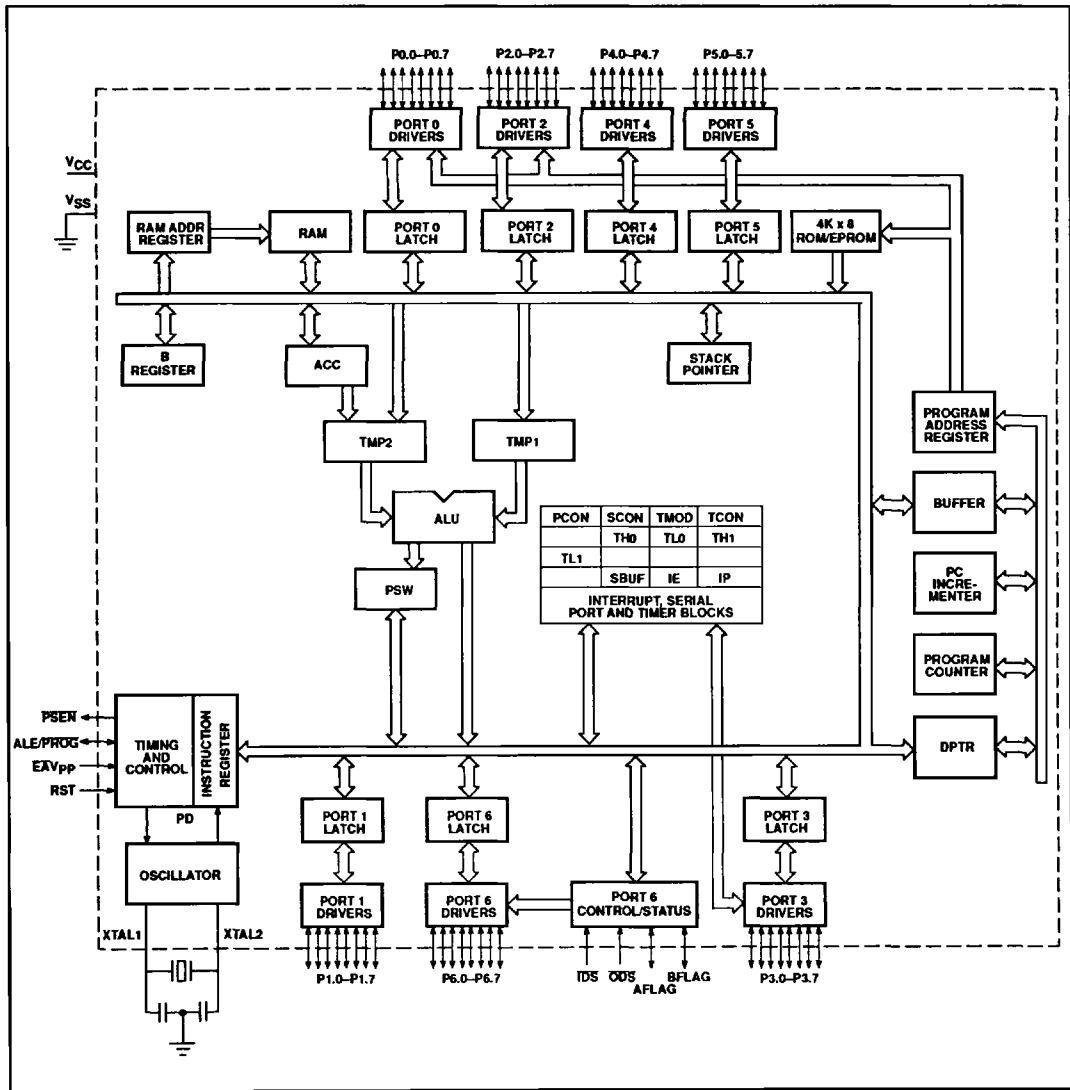
LOGIC SYMBOL



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BLOCK DIAGRAM



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PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	LCC		
V _{SS}	50	54	I	Ground: 0V reference.
V _{CC}	18	18	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0–P0.7	17–10	17–10	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 is also the multiplexed data and low-order address bus during accesses to external memory. External pull-ups are required during program verification. Port 0 can sink/source eight LS TTL inputs.
P1.0–P1.7	23–30	27–34	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 receives the low-order address bytes during program memory verification. Port 1 can sink/source three LS TTL inputs, and drive CMOS inputs without external pull-ups.
P2.0–P2.7	2–9	2–9	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 emits the high-order address bytes during access to external memory and receives the high-order address bits and control signals during program verification. Port 2 can sink/source three LS TTL inputs, and drive CMOS inputs without external pull-ups.
P3.0–P3.7	32–39	36–43	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 can sink/source three LS TTL inputs, and drive CMOS inputs without external pull-ups. Port 3 also serves the special functions listed below:
	32	36	I	RxD (P3.0): Serial input port
	33	37	O	TxD (P3.1): Serial output port
	34	38	I	INT0 (P3.2): External interrupt
	35	39	I	INT1 (P3.3): External interrupt
	36	40	I	T0 (P3.4): Timer 0 external input
	37	41	I	T1 (P3.5): Timer 1 external input
	38	42	O	WR (P3.6): External data memory write strobe
	39	43	O	RD (P3.7): External data memory read strobe
P4.0–P4.3	22–19		I/O	Port 4: Port 4 is a 4/8-bit (DIP/LCC) bidirectional I/O port with internal pull-ups. Port 4 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups.
P4.0–P4.7		26–19	I/O	
P5.0–P5.7	40–47	44–51	I/O	Port 5: Port 5 is a 4/8-bit (DIP/LCC) bidirectional I/O port with internal pull-ups. Port 5 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups.
P6.0–P6.7	55–62	59–66	I/O	Port 6: Port 6 is a specialized 8-bit bidirectional I/O port with internal pull-ups. This special port can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. Port 6 can be used in a strobed or non-strobed mode of operation. Port 6 works in conjunction with four control pins that serve the functions listed below:
	51	55	I	ODS: Output data strobe
	52	56	I	IDS: Input data strobe
	53	57	I/O	BFLAG: Bidirectional I/O pin with internal pull-ups
	54	58	I/O	AFLAG: Bidirectional I/O pin with internal pull-ups
RST	31	35	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal pull-down resistor permits a power-on reset using only an external capacitor connected to V _{CC} .
ALE/PROG	64	68	I/O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. ALE is activated at a constant rate of 1/6 the oscillator frequency except during an external data memory access, at which time one ALE is skipped. ALE can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. This pin is also the program pulse during EPROM programming.
PSEN	63	67	O	Program Store Enable: The read strobe to external program memory. PSEN is activated twice each machine cycle during fetches from external program memory. However, when executing out of external program memory, two activations of PSEN are skipped during each access to external program memory. PSEN is not activated during fetches from internal program memory. PSEN can sink/source eight LS TTL inputs and drive CMOS inputs without an external pull-up. This pin should be tied low during programming.
EA/V _{PP}	1	1	I	Instruction Execution Control/Programming Supply Voltage: When EA is held high, the CPU executes out of internal program memory, unless the program counter exceeds 0FFFH. When EA is held low, the CPU executes out of external program memory. EA must never be allowed to float. This pin also receives the 12.75V programming supply voltage (V _{PP}) during EPROM programming.
XTAL1	49	53	I	Crystal 1: Input to the inverting oscillator amplifier that forms the oscillator. This input receives the external oscillator when an external oscillator is used.
XTAL2	48	52	O	Crystal 2: An output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

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PORTS 4 AND 5

Ports 4 and 5 are bidirectional I/O ports with internal pull-ups. Port 4 is an 8-bit port (LCC version) or a 4-bit port (DIP version). Port 4 and port 5 pins with ones written to them, are pulled high by the internal pull-ups, and in that state can be used as inputs. Port 4 and 5 are addressed at the special function register addresses shown in Table 1.

PORT 6

Port 6 is a special 8-bit bidirectional I/O port with internal pull-ups (see Figure 1). This port can be used as a standard I/O port, or in strobed modes of operation in conjunction with four special control lines: ODS, IDS, AFLAG, and BFLAG. Port 6 operating modes are controlled by the port 6 control status register (CSR). Port 6 and the CSR are addressed at the special function register addresses shown in Table 1. The following four control pins are used in conjunction with port 6:

ODS – Output data strobe for port 6. ODS can be programmed to control the port 6 output drivers and the output buffer full flag (OBF), or to clear only the OBF flag bit in the CSR (output-always mode). ODS is active low for output driver control. the OBF flag can

be programmed to be cleared on the negative or positive edge of ODS.

IDS – Input data strobe for port 6. IDS is used to control the port 6 input latch and input buffer full flag (IBF) bit in the CSR. The input data latch can be programmed to be transparent when IDS is low and latched on the positive transition of IDS, or to latch only on the positive transition of IDS. Correspondingly, the IBF flag is set on the negative or positive transition of IDS.

AFLAG – AFLAG is a bidirectional I/O pin which can be programmed to be an output set high or low under program control, or to output the state of the output buffer full flag. AFLAG can also be programmed to be an input which selects whether the contents of the output buffer, or the contents of the port 6 control status register will output on port 6. This feature grants complete port 6 status to external devices.

BFLAG – BFLAG is a bidirectional I/O pin which can be programmed to be an output, set high or low under program control, or to output the state of the input buffer full flag. BFLAG can also be programmed to input an enable signal for port 6. When BFLAG is used as an enable input, port 6 output drivers

are in the high-impedance state, and the input latch does not respond to the IDS strobe when BFLAG is high. Both features are enabled when BFLAG is low. This feature facilitates the use of the SC8XC451 in bused multiprocessor systems.

CONTROL STATUS REGISTER

The control status register (CSR) establishes the mode of operation for port 6 and indicates the current status of port 6 I/O registers. All control status register bits can be read and written by the CPU, except bits 0 and 1, which are read only. Reset writes ones to bits 2 through 7, and writes zeros to bits 0 and 1 (see Table 2).

CSR.0 Input Buffer Full Flag (IBF) (Read Only)

The IBF bit is set to a logic 1 when port 6 data is loaded into the input buffer under control of IDS. This can occur on the negative or positive edge of IDS, as determined by CSR.2 IBF is cleared when the CPU reads the input buffer register.

CSR.1 Output Buffer Full Flag (OBF)

The OBF flag is set to a logic 1 when the CPU writes to the port 6 output data buffer. OBF is cleared by the positive or negative edge of ODS, as determined by CSR.3.

Table 1. Special Function Register Addresses

REGISTER ADDRESS			BIT ADDRESS								
Name	Symbol	Address	MSB								LSB
Port 4	P4	C0	C7	C6	C5	C4	C3	C2	C1	C0	
Port 5	P5	C8	CF	CE	CD	CC	CB	CA	C9	C8	
Port 6 data	P6	D8	DF	DE	DD	DC	DB	DA	D9	D8	
Port 6 control status	CSR	E8	EF	EE	ED	EC	EB	EA	E9	E8	

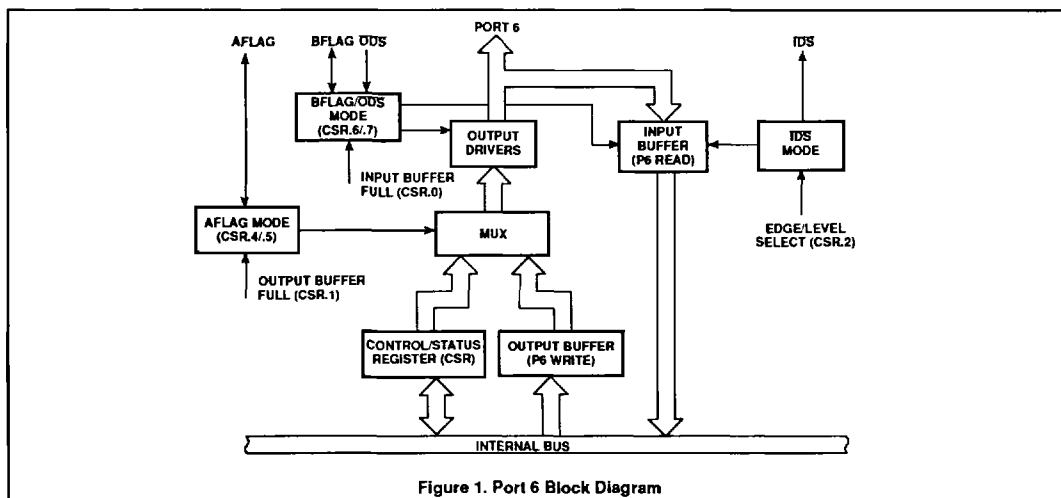


Figure 1. Port 6 Block Diagram

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CSR.2 IDS Mode Select (IDSM) – When CSR.2 = 0, a low-to-high transition on the IDS pin sets the IBF flag. The Port 6 input buffer is loaded on the IDS positive edge. When CSR.2 = 1, a high-to-low transition on the IDS pin sets the IBF flag. Port 6 input buffer is transparent when IDS is low, and latched when IDS is high.

CSR.3 Output Buffer Full Flag Clear Mode (OBFC) – When CSR.3 = 1, the positive edge of the ODS input clears the OBF flag. When CSR.3 = 0, the negative edge of the ODS input clears the OBF flag.

CSR.4, CSR.5 AFLAG Mode Select (MA0, MA1) – Bits 4 and 5 select the mode of operation for the AFLAG pin as follows:

MA1	MA0	AFLAG Function
0	0	Logic 0 output
0	1	Logic 1 output
1	0	OBF flag output (CSR.1)
1	1	Select (SEL) input mode

The select (SEL) input mode is used to determine whether the port 6 data register or the control status register is output on port 6.

When the select feature is enabled, the AFLAG input controls the source of port 6 output data. A logic 0 on AFLAG input selects the port 6 data register, and a logic 1 on AFLAG input selects the control status register.

CSR.6, CSR.7 BFLAG Mode Select (MB0, MB1) – Bits 6 and 7 select the mode opera-

tion as follows:		BFLAG Function
MB1	MB0	
0	0	Logic 0 output
0	1	Logic 1 output
1	0	IBF flag output (CSR.0)
1	1	Port enable (PE)

In the port enable mode, IDS and ODS inputs are disabled when BFLAG input is high. When the BFLAG input is low, the port is enabled for I/O.

SPECIAL FUNCTION REGISTER ADDRESSES

Special function register addresses for the device are identical to those of the 80C51, except for the additional registers listed in Table 1.

Table 2. Control Status Register (CSR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MB1	MB0	MA1	MA0	OBFC	IDSM	OBF	IBF
BFLAG Mode Select		AFLAG Mode Select		Output Buffer Flag Clear Mode	Input Data Strobe Mode	Output Buffer Flag Full	Input Buffer Flag Full
0/0 = Logic 0 output* 0/1 = Logic 1 output* 1/0 = IBF output 1/1 = PE input (0 = Select) (1 = Disable I/O)		0/0 = Logic 0 output* 0/1 = Logic 1 output* 1/0 = OBF output 1/1 = SEL input (0 = Select) (1 = Control/status)		0 = Negative edge of ODS 1 = Positive edge o ODS	0 = Negative edge of IDS 1 = Positive edge o IDS	0 = Output data buffer empty 1 = Output data buffer full	0 = Input data buffer empty 1 = Input data buffer full

NOTE:

*Output-always mode: MB1 = 0, MA1 = 1, and MA0 = 0. In this mode, port 6 is always enabled for output. ODS only clears the OBF flag.

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ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 -40 to +85	°C
Storage temperature range	-65 to +150	°C
Voltage on any other pin to V _{SS}	-0.5 to +6.5	V
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C or -40°C to +85°C, V_{CC} = 5V ±20%, V_{SS} = 0V (80C451, 83C451)T_A = 0°C to +70°C or -40°C to +85°C, V_{CC} = 5V ±10%, V_{SS} = 0V (87C451)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYPICAL ¹	MAX	
V _{IL}	Input low voltage; except EA		-0.5		0.2V _{CC} -0.1	V
V _{IL1}	Input low voltage to EA		0		0.2V _{CC} -0.3	V
V _{IH}	Input high voltage; except XTAL1, RST		0.2V _{CC} +0.9		V _{CC} +0.5	V
V _{IH1}	Input high voltage; XTAL1, RST		0.7V _{CC}		V _{CC} +0.5	V
V _{OL}	Output low voltage; ports 1, 2, 3	I _{OL} = 1.6mA ²			0.45	V
V _{OL1}	Output low voltage; port 0, ALE, PSEN	I _{OL} = 3.2mA ²			0.45	V
V _{OH}	Output high voltage; ports 1, 2, 3, 4, 5, 6	I _{OH} = -60µA	2.4			V
		I _{OH} = -25µA	0.75V _{CC}			V
		I _{OH} = -10µA	0.9V _{CC}			V
V _{OH1}	Output high voltage (port 0 in external bus mode, ALE, PSEN) ³	I _{OH} = -800µA	2.4			V
		I _{OH} = -300µA	0.75V _{CC}			V
		I _{OH} = -80µA	0.9V _{CC}			V
I _{IL}	Logical 0 input current; ports 1, 2, 3, 4, 5, 6	V _{IN} = 0.45V			-50	µA
I _{TL}	Logical 1-to-0 transition current; ports 1, 2, 3	See note 4			-650	µA
I _{LI}	Input leakage current; port 0	V _{IN} = V _{IL} or V _{IH}			±10	µA
I _{CC}	Power supply current: Active mode @ 12MHz ⁵ Idle mode @ 12MHz ⁵ Power down mode	See note 6		11.5	25	mA
				1.3	4	mA
				3	50	µA
R _{RST}	Internal reset pull-down resistor		50		300	kohm
C _{IO}	Pin capacitance ⁷ - DIP package - PLCC package				15	pF
					10	pF

NOTES:

- Typical ratings are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the 0.9V_{CC} specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
- I_{CC}MAX at other frequencies is given by:
Active mode: I_{CC}MAX = 0.94 X FREQ + 13.71
Idle mode: I_{CC}MAX = 0.14 X FREQ + 2.31
where FREQ is the external oscillator frequency in MHz. I_{CC}MAX is given in mA. See Figure 13.
- See Figures 14 through 17 for I_{CC} test conditions.
- C_{IO} applies to ports 1 through 6, AFLAG, BFLAG, XTAL1, XTAL2.

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AC ELECTRICAL CHARACTERISTICS

 $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or -40°C to $+85^\circ\text{C}$, $V_{CC} = 5V \pm 20\%$, $V_{SS} = 0V$ (80C451, 83C451)^{1,2} $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or -40°C to $+85^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$ (87C451)

SYMBOL	FIGURE	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$		Oscillator frequency: Speed Versions SC8XC451 B SC8XC451 C SC8XC451 G			0.5 3.5 3.5	12 12 16	MHz MHz MHz
t_{LHLL}	2	ALE pulse width	127		$2t_{CLCL}-40$		ns
t_{AVLL}	2	Address valid to ALE low	28		$t_{CLCL}-55$		ns
t_{LLAX}	2	Address hold after ALE low	48		$t_{CLCL}-35$		ns
t_{LLIV}	2	ALE low to valid instruction in		234		$4t_{CLCL}-100$	ns
t_{LLPL}	2	ALE low to PSEN low	43		$t_{CLCL}-40$		ns
t_{PLPH}	2	PSEN pulse width	205		$3t_{CLCL}-45$		ns
t_{PLIV}	2	PSEN low to valid instruction in		145		$3t_{CLCL}-105$	ns
t_{PXIX}	2	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	2	Input instruction float after PSEN		59		$t_{CLCL}-25$	ns
t_{AVIV}	2	Address to valid instruction in		312		$5t_{CLCL}-105$	ns
t_{PLAZ}	2	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	3, 4	RD pulse width	400		$6t_{CLCL}-100$		ns
t_{WLWH}	3, 4	WR pulse width	400		$6t_{CLCL}-100$		ns
t_{RLDV}	3, 4	RD low to valid data in		252		$5t_{CLCL}-165$	ns
t_{RHDX}	3, 4	Data hold after RD	0		0		ns
t_{RH0Z}	3, 4	Data float after RD		97		$2t_{CLCL}-70$	ns
t_{LLDV}	3, 4	ALE low to valid data in		517		$8t_{CLCL}-150$	ns
t_{AVDV}	3, 4	Address to valid data in		585		$9t_{CLCL}-165$	ns
t_{LLWL}	3, 4	ALE low to RD or WR low	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	3, 4	Address valid to WR low or RD low	203		$4t_{CLCL}-130$		ns
t_{QVWX}	3, 4	Data valid to WR transition	29		$t_{CLCL}-60$		ns
t_{WHDX}	3, 4	Data hold after WR	33		$t_{CLCL}-50$		ns
t_{RLAZ}	3, 4	RD low to address float		0		0	ns
t_{WHLH}	3, 4	RD or WR high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
Shift Register							
t_{XLXL}	5	Serial port clock cycle time	1.0		$12t_{CLCL}$		μs
t_{QVXH}	5	Output data setup to clock rising edge	700		$10t_{CLCL}-133$		ns
t_{XHDX}	5	Output data hold after clock rising edge	50		$2t_{CLCL}-117$		ns
t_{XHDX}	5	Input data hold after clock rising edge	0		0		ns
t_{XH0V}	5	Clock rising edge to input data valid		700		$10t_{CLCL}-133$	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.

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AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	FIGURE	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
Port 6 input (Input rise and fall times = 5ns)							
t_{FLFH}	8	PE width	270		$3t_{CLCL}+20$		ns
t_{LLH}	8	IDS width	270		$3t_{CLCL}+20$		ns
t_{DVIH}	8	Data setup to IDS high or PE high	0		0		ns
t_{HDX}	8	Data hold after IDS high or PE high	30		30		ns
t_{VfV}	9	IDS to BFLAG (IBF) delay		130		130	ns
Port 6 output							
t_{OLOH}	6	ODS width	270		$3t_{CLCL}+20$		ns
t_{FVDV}	7	SEL to data out delay		85		85	ns
t_{OLDV}	6	ODS to data out delay		80		80	ns
t_{OHZ}	6	ODS to data float delay		35		35	ns
t_{OVFV}	6	ODS to AFLAG (OBF) delay		100		100	ns
t_{FLDV}	6	PE to data out delay		120		120	ns
t_{OHFH}	7	ODS to AFLAG (SEL) delay	100		100		ns
External Clock							
t_{CHCX}	10	High time	20		20		ns
t_{CLCX}	10	Low time	20		20		ns
t_{CLCH}	10	Rise time		20		20	ns
t_{CHCL}	10	Fall time		20		20	ns

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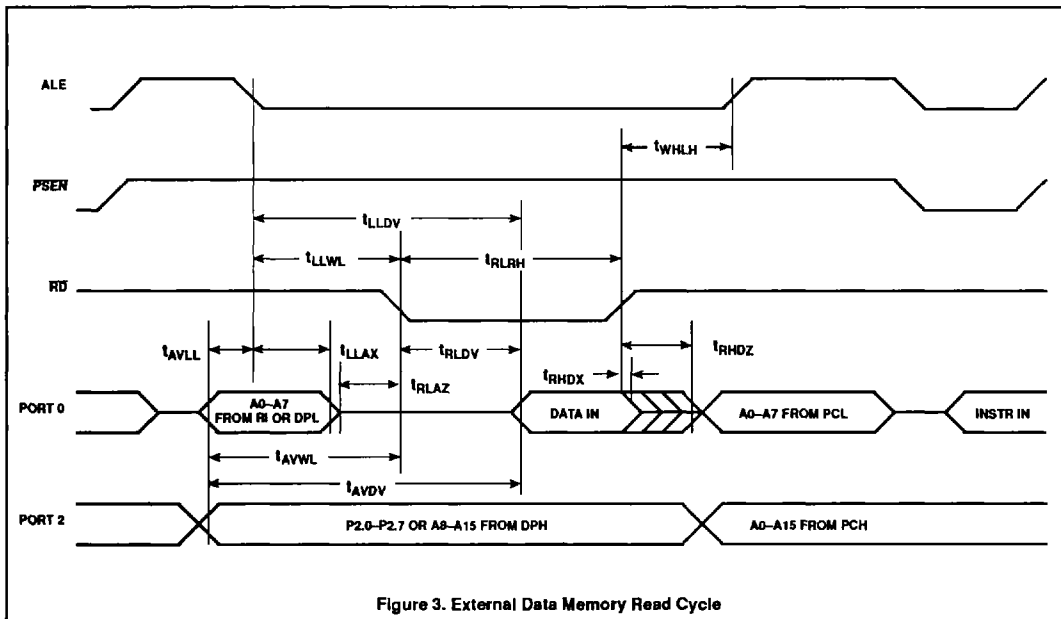
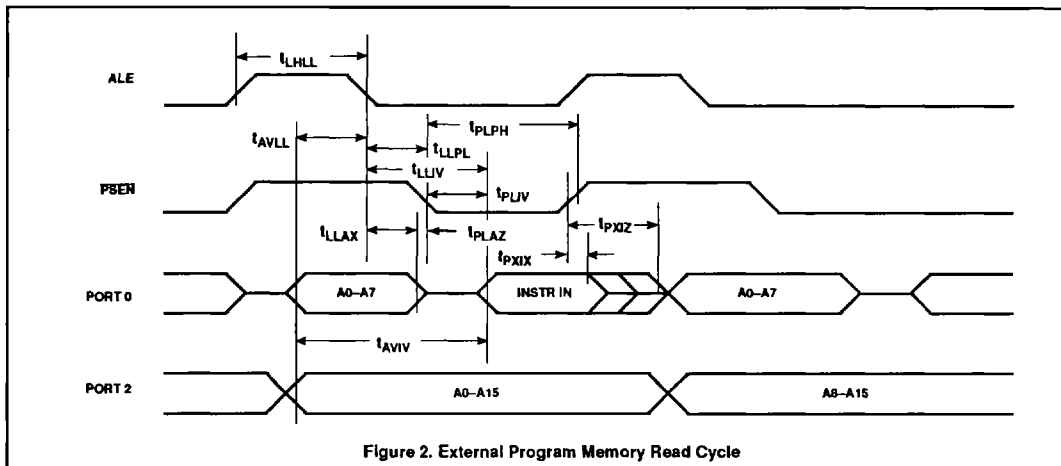
EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

- A - Address
- C - Clock
- D - Input data
- H - Logic level high
- I - Instruction (program memory contents)
- L - Logic level low, or ALE

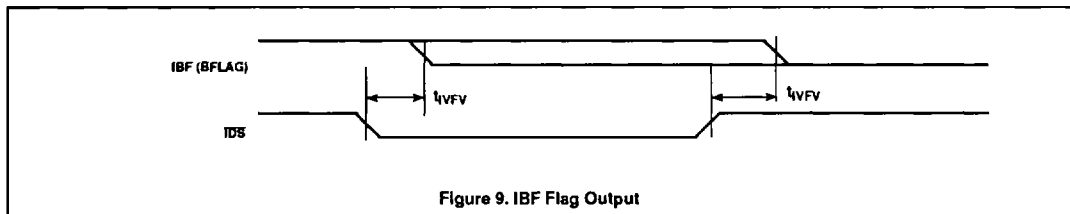
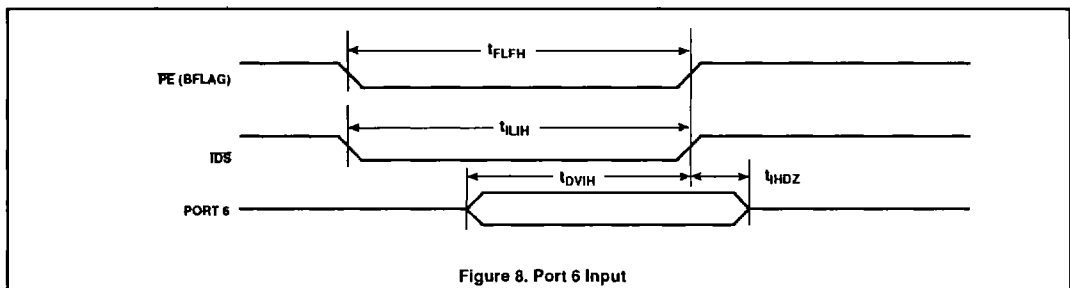
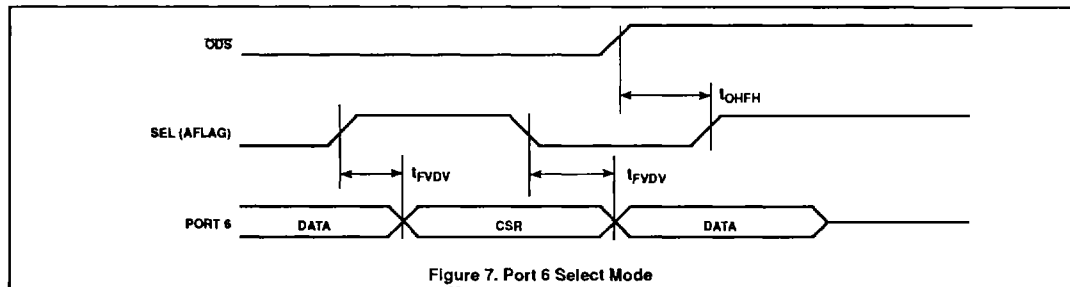
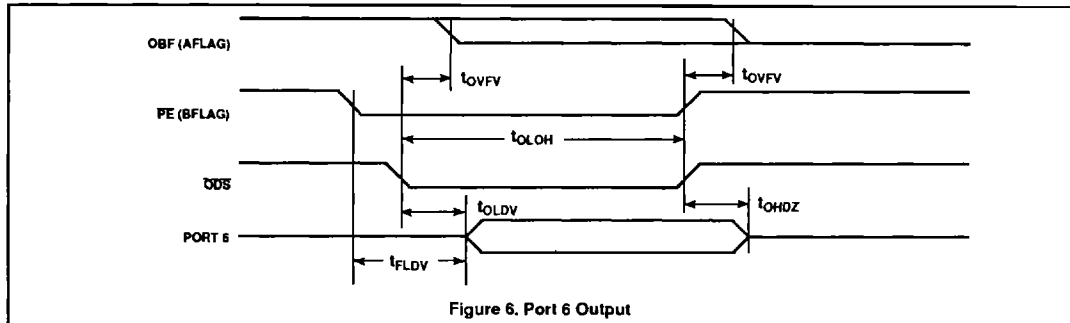
- P - PSEN
- Q - Output data
- R - RD signal
- t - Time
- V - Valid
- W - WR signal
- X - No longer a valid logic level
- Z - Float

Examples: t_{AVLL} = Time for address valid to ALE low.
 t_{LLPL} = Time for ALE low to PSEN low.



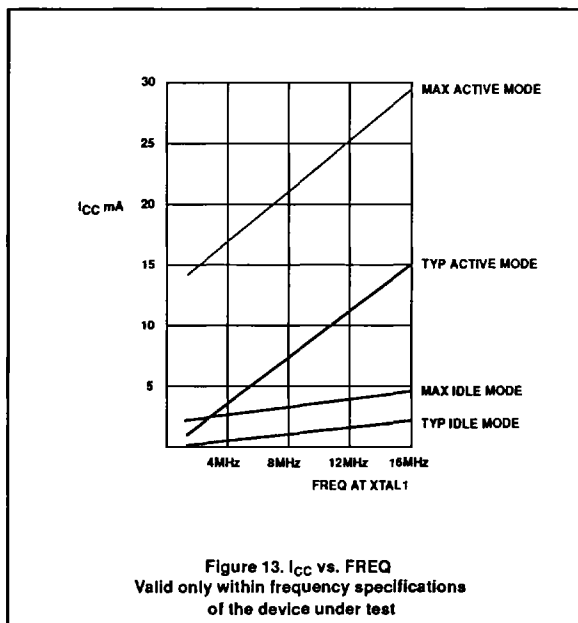
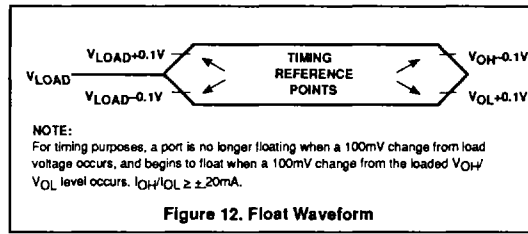
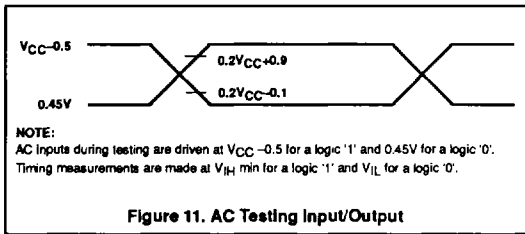
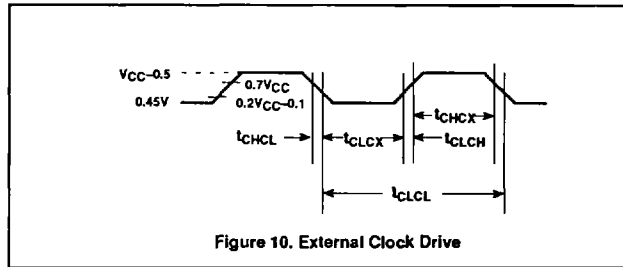
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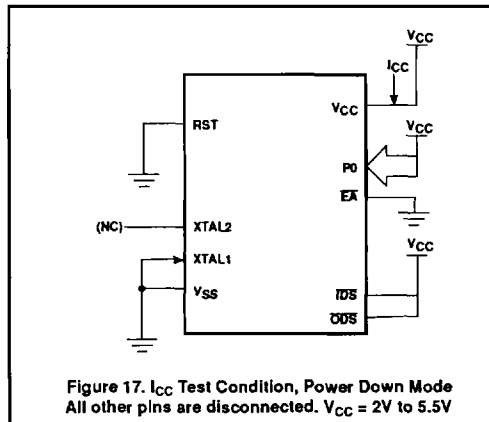
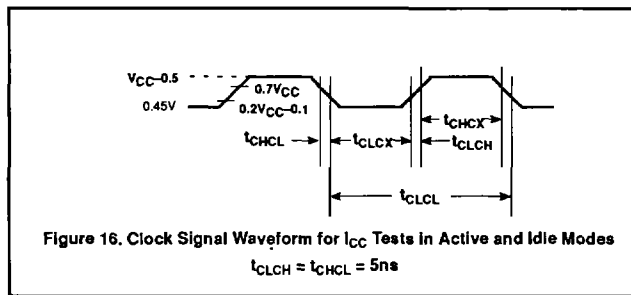
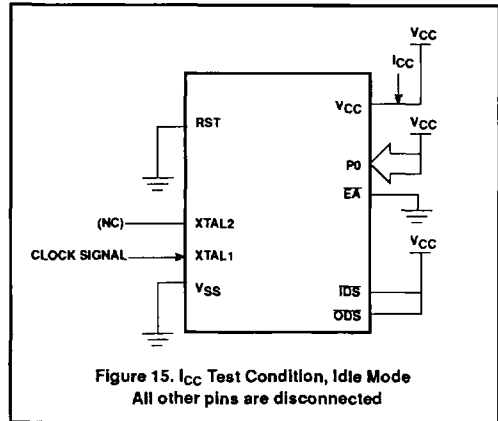
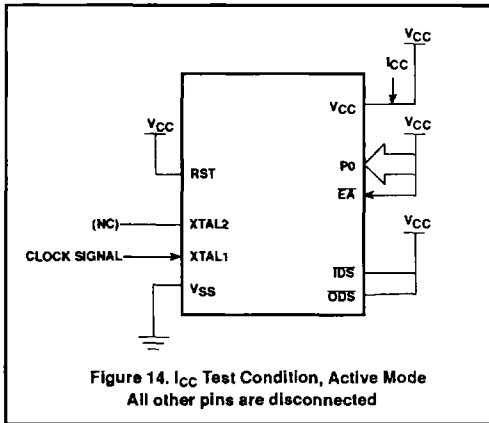
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EPROM CHARACTERISTICS

The 87C451 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C451 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C451 manufactured by Philips Corporation.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 18 and 19. Figure 20 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 18. Note that the 87C451 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 18. The code byte to be programmed into that location is applied to port 0. RST, PSEN and pins of ports 2 and 3 specified in Table 3 are held at the 'Program Code Data' levels indicated in Table 3. The ALE/PROG is pulsed low 25 times as shown in Figure 19.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25 pulse programming sequence using the 'Pgm Lock Bit' levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the $E\bar{A}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 20. The other pins are held at the 'Verify Code Data' levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips

(031H) = 90H indicates 87C451

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

Erase Characteristics

Erase of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345-5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm². Exposing the EPROM to an ultraviolet lamp of 12,000uW/cm² rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erase leaves the array in an all 1s state.

Table 3. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	$E\bar{A}/V_{PP}$	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm lock bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm lock bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:

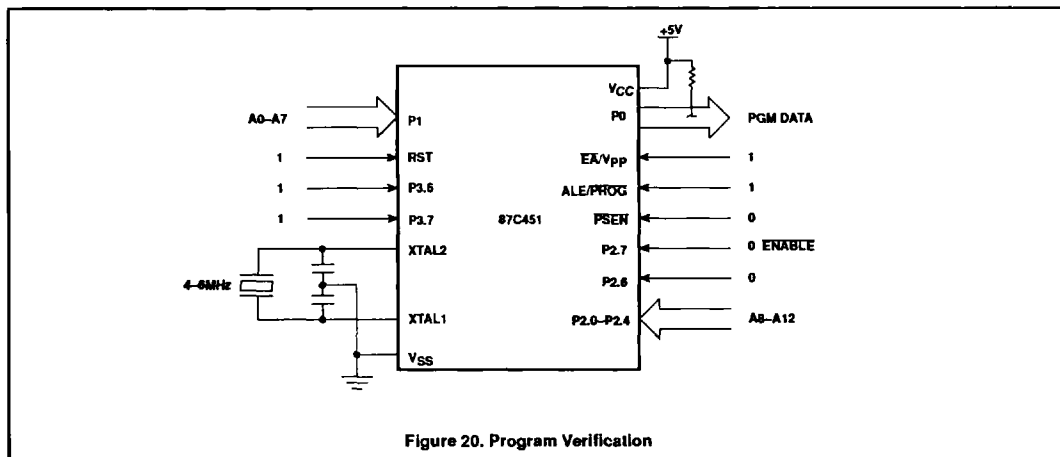
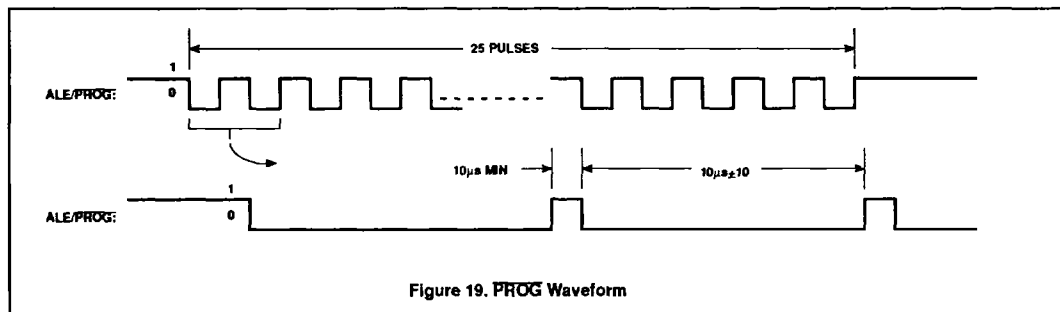
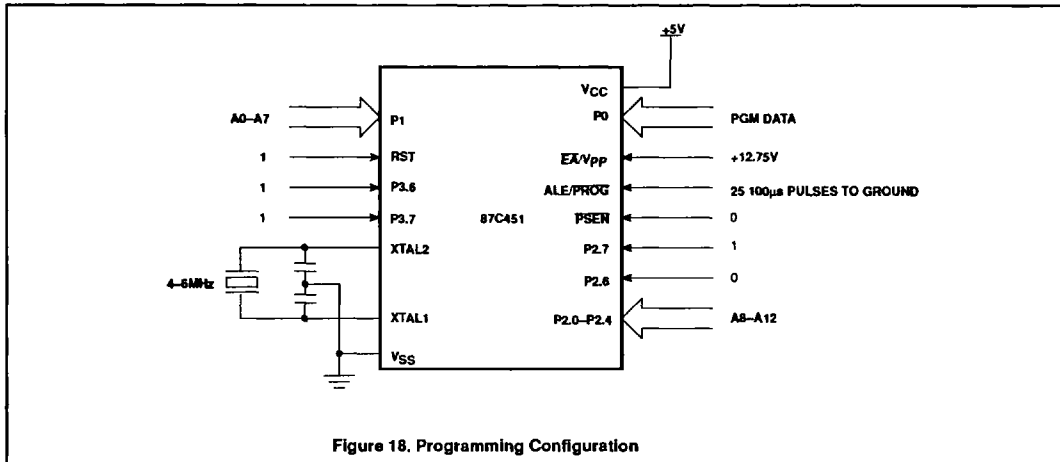
1. '0' = Valid low for that pin, '1' = valid high for that pin.
2. $V_{PP} = 12.75V \pm 0.25V$.
3. $V_{CC} = 5V \pm 10\%$ during programming and verification.

*ALE/PROG receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100 μ s ($\pm 10\mu$ s) and high for a minimum of 10 μ s.

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EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_A = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (See Figure 21)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V _{PP}	Programming supply voltage	12.5	13.0	V
I _{PP}	Programming supply current		50	mA
1/f _{CLCL}	Oscillator frequency	4	6	MHz
t _{AVGL}	Address setup to PROG low	48t _{CLCL}		
t _{GHAX}	Address hold after PROG	48t _{CLCL}		
t _{DVGL}	Data setup to PROG low	48t _{CLCL}		
t _{GHDX}	Data hold after PROG	48t _{CLCL}		
t _{EHSH}	P2.7 (ENABLE) high to V _{PP}	48t _{CLCL}		
t _{SHGL}	V _{PP} setup to PROG low	10		μs
t _{GHSL}	V _{PP} hold after PROG	10		μs
t _{GLGH}	PROG width	90	110	μs
t _{AVQV}	Address to data valid		48t _{CLCL}	
t _{ELQZ}	ENABLE low to data valid		48t _{CLCL}	
t _{EHQZ}	Data float after ENABLE	0	48t _{CLCL}	
t _{GHGL}	PROG high to PROG low	10		μs

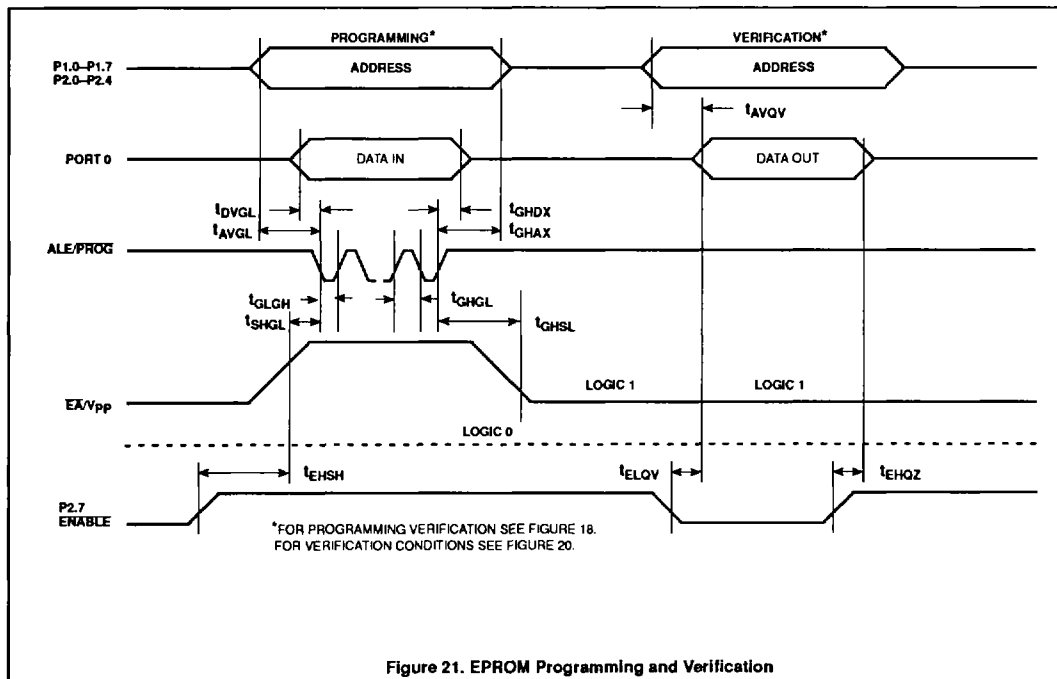


Figure 21. EPROM Programming and Verification