V53C106A FAMILY
HIGH PERFORMANCE, LOW POWER
256K x 4 BIT, STATIC COLUMN MODE
CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C106A	70/70L	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	35 ns	40 ns	50 ns
Min. Static Column Mode Cycle Time, (t_{PC})	40 ns	45 ns	50 ns
Min. Read-Write Cycle Time, (t_{RC})	130 ns	150 ns	180 ns

LOW POWER V53C106AL	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	1.0 mA	1.0 mA	1.0 mA

Features

- 256K x 4 organization
- $\overline{RAS}$ access time: 70, 80, 100 ns
- Low power dissipation for V53C106A-10
  - Operating Current—65 mA max.
  - TTL Standby Current—2.0 mA max.
- Low CMOS Standby Current
  - V53C106A—1.5 mA max.
  - V53C106AL—1.0 mA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Common I/O capability
- 512 refresh cycles each 8 ms
- On-chip substrate bias generator
- Static Column Mode operation for a sustained data rate greater than 25 MHz
- Standard packages are 20 pin Plastic DIP and 26/20 pin SOJ

Description

The V53C106A is a Static Column Mode, 262,144 word by four bit dynamic RAM. It is designed to operate from a single, 5 V ±10% tolerance power supply. Fabricated with Vitelic's VICMOS III technology, the device provides both high performance and high reliability over its operating range. Because it utilizes static circuitry, and its flow-through column address latches allow address pipelining, many critical system timing requirements are relaxed. It is not necessary to toggle $\overline{CAS}$ when in the Static Column Mode. These features make the V53C106A ideally suited for high resolution graphics, DSP, and high performance PC and workstation applications. The 70 ns version is capable of providing zero wait state memory in two memory clock cycle microprocessors running at 25 MHz clock rates.

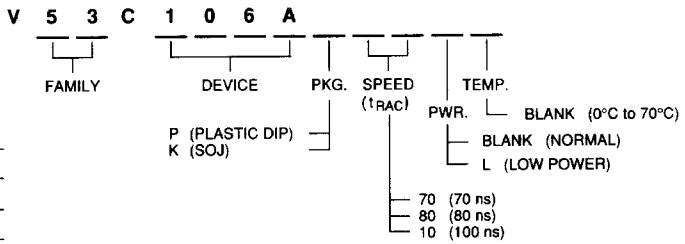
Multiplexed address inputs and 1.0 micrometer design rules permit the V53C106A to be packaged in standard 300 mil plastic 20-pin DIPs and 300 mil plastic 26/20 SOJs.

Refreshing can be accomplished by using $\overline{CAS}$ before $\overline{RAS}$, $\overline{RAS}$-only or normal read or write cycles.

An internal address counter obviates the need for externally supplied addresses during the $\overline{CAS}$ before $\overline{RAS}$ refresh mode. Externally supplied addresses are required during $\overline{RAS}$-only, or normal read or write cycles.

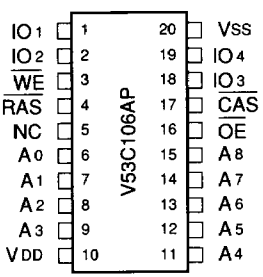
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Power		Temperature Mark
	P	K	70	80	100	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	Blank



Description	*Pkg.*	*Pin Count*
Plastic DIP	P	20
SOJ	K	26/20

20-Pin Plastic DIP PIN CONFIGURATION
Top View



26/20-Pin Plastic SOJ PIN CONFIGURATION
Top View