Integrated Device Technology, Inc.

2 x 16K x 60 DATA/INSTRUCTION CACHE MODULE FOR IDT79R3000 CPU (MULTIPROCESSOR)

IDT7MB6049

FEATURES:

- High Speed 240K-Byte CMOS Static RAM Module con structed to support the IDT79R3000 CPU in a multi processor system as a complete data and instruction cache
- Additional data and instruction address invalidation latches on-board to facilitate use in a multi-processor system
- Operating frequencies to support 12MHz, 16.7MHz, 20MHz, 25MHz, and 33MHz IDT79R3000
- Available in a high density, low profile 120-pin QIP (Quad-In-Line Package)
- Surface mounted SO's on a multilayer epoxy substrate (FR-4)
- Multiple ground pins for maximum noise immunity.
- TTL compatible I/O's
- Single 5V (±10%) power supply

PIN CONFIGURATION[1]

GND	1	61	GND	GND	120	60	Vcc
D(0)	2	62	D(1)	D(58)	119	59	D(59)
D(2)	3	63	D(3)	D(56)	118	58	D(57)
D(4)	4	64	D(5)	D(54)	117	57	D(55)
D(6)	5	65	D(7)	D(52)	116	56	D(53)
$\overline{WE}$(1)	6	66	$\overline{OE}$(1)	$\overline{WE}$(4)	115	55	$\overline{OE}$(4)
$\overline{CS}$(1)	7	67	Vcc	GND	114	54	GND
D(8)	8	68	D(9)	D(50)	113	53	D(51)
D(10)	9	69	D(11)	D(48)	112	52	D(49)
P1A(0)	10	70	P1A(1)	P2A(0)	111	51	P2A(1)
P1A(2)	11	71	P1A(3)	P2A(2)	110	50	P2A(3)
P1A(4)	12	72	P1A(5)	P2A(4)	109	49	P2A(5)
P1LE1	13	73	P1LE2	P2LE1	108	48	P2LE2
P1A(6)	14	74	P1A(7)	P2A(6)	107	47	P2A(7)
P1A(8)	15	75	P1A(9)	P2A(8)	106	46	P2A(9)
P1A(10)	16	76	P1A(11)	P2A(10)	105	45	P2A(11)
P1A(12)	17	77	P1A(13)	P2A(12)	104	44	P2A(13)
$\overline{P1OE}$(1)	18	78	$\overline{P1OE}$(2)	$\overline{P2OE}$(1)	103	43	$\overline{P2OE}$(2)
D(12)	19	79	D(13)	D(46)	102	42	D(47)
D(14)	20	80	D(15)	D(44)	101	41	D(45)
D(16)	21	81	D(17)	D(42)	100	40	D(43)
D(18)	22	82	D(19)	D(40)	99	39	D(41)
$\overline{WE}$(2)	23	83	$\overline{OE}$(2)	$\overline{WE}$(3)	98	38	$\overline{OE}$(3)
GND	24	84	GND	Vcc	97	37	$\overline{CS}$(2)
D(20)	25	85	D(21)	D(38)	96	36	D(39)
D(22)	26	86	D(23)	D(36)	95	35	D(37)
D(24)	27	87	D(25)	D(34)	94	34	D(35)
D(26)	28	88	D(27)	D(32)	93	33	D(33)
D(28)	29	89	D(29)	D(30)	92	32	D(31)
Vcc	30	90	GND	GND	91	31	GND

2796 drw 01

QIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to drawing M26 in the packaging section.

DESCRIPTION:

The IDT7MB6049 is a 240K-Byte high-speed CMOS Static RAM cache module constructed on a multilayer epoxy substrate (FR-4) using 28 (16K x 4) RAM's, 16 IDT74FCT373 latches, and 1 IDT74FCT244.

The IDT7MB6049 is organized as two separate banks of 16K x 60 with the IDT74FCT373's being used as address latches. The two banks of RAM with their associated address latches share a common 14-bit ADDRESS bus and a common 60-bit DATA bus. The chip select, write enable, RAM output enable, and latch enable controls for the two banks are brought out separately, to support inter-leaving access to the two banks of RAM. Also, each bank has two sets of address latches to reduce the capacitance loading on the outputs of the latches; thereby enhancing CPU performance.

The IDTMB6049 supports use in a multi-processor (IDT79R3000 based) system by providing a second address bus and an addtional set of latches for that bus. This bus is used in multi-processor applications to latch an address from a source other than the R3000. This maintains cache coherency by allowing the system to invalidate entries in the data cache. For more details on IDT7MB6049 operation, please refer to Application Note AN-76.

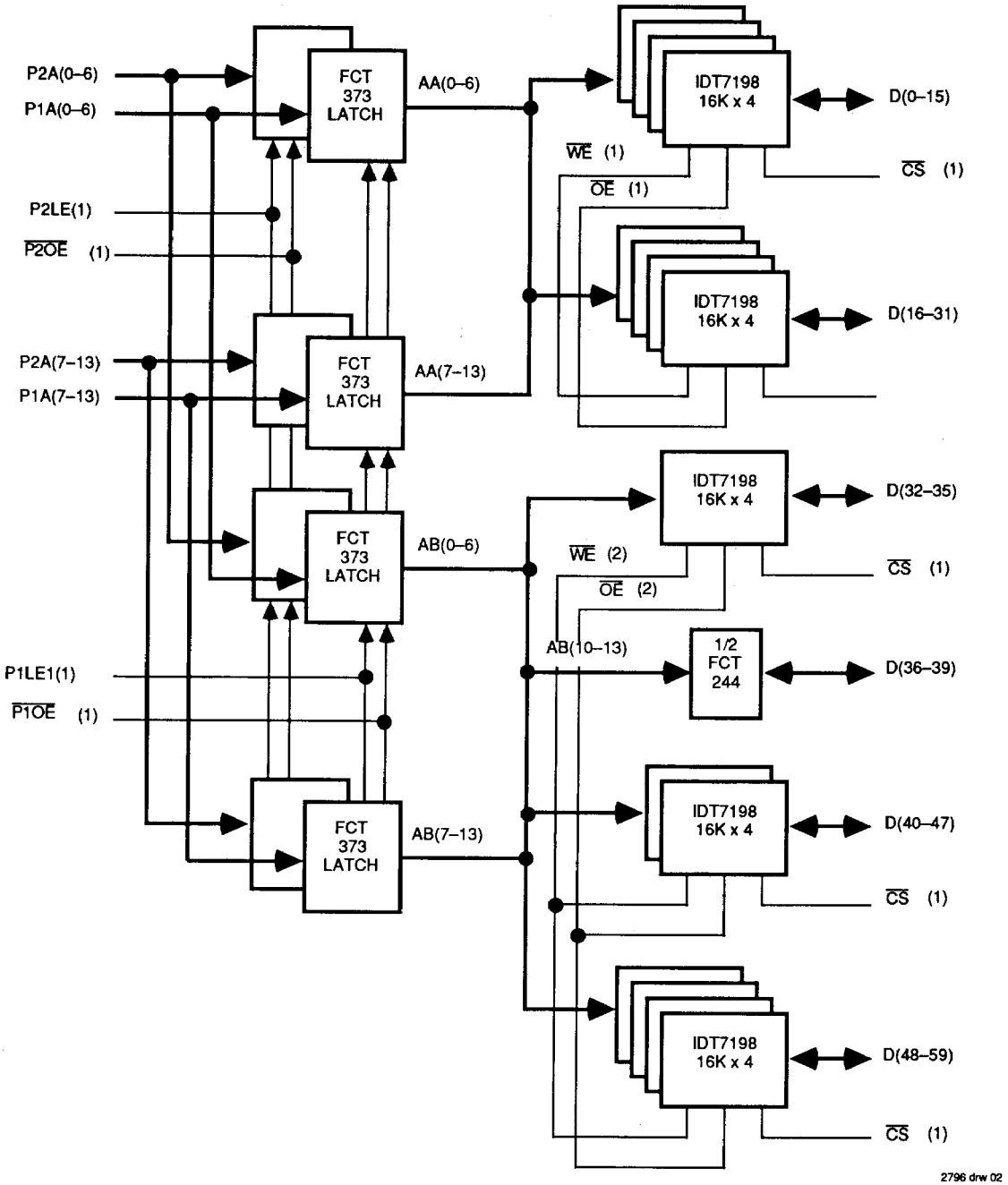
All inputs and outputs of the IDT7MB6049 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

PIN NAMES

D (0)–D (59)	Data Inputs/Outputs
P1A (0)–P1A (13)	Address inputs
P2A (0)–P2A (13)	Invalidate Address Inputs
P1LE1	Data Address Latch Enable
P1LE2	Instruction Address Latch Enable
$\overline{P1OE}$ (1)	Data Address Enable
$\overline{P1OE}$ (2)	Instruction Address Enable
$\overline{P2OE}$ (1)	Invalidate Data Address Enable
$\overline{P2OE}$ (2)	Invalidate Instruction Address Enable
P2LE1 (1)	Invalidate Data Address Latch Enable
P2LE2 (2)	Invalidate Instruction Address Latch Enable
$\overline{CS}$ (1), $\overline{CS}$ (2)	Data, Instruction Cache RAM Selects
$\overline{WE}$ (1) – $\overline{WE}$ (4)	Write Enables
$\overline{OE}$ (1) – $\overline{OE}$ (4)	Output Enables
GND	Ground
Vcc	Power Supply

2796 tbl 01

FUNCTIONAL BLOCK DIAGRAM

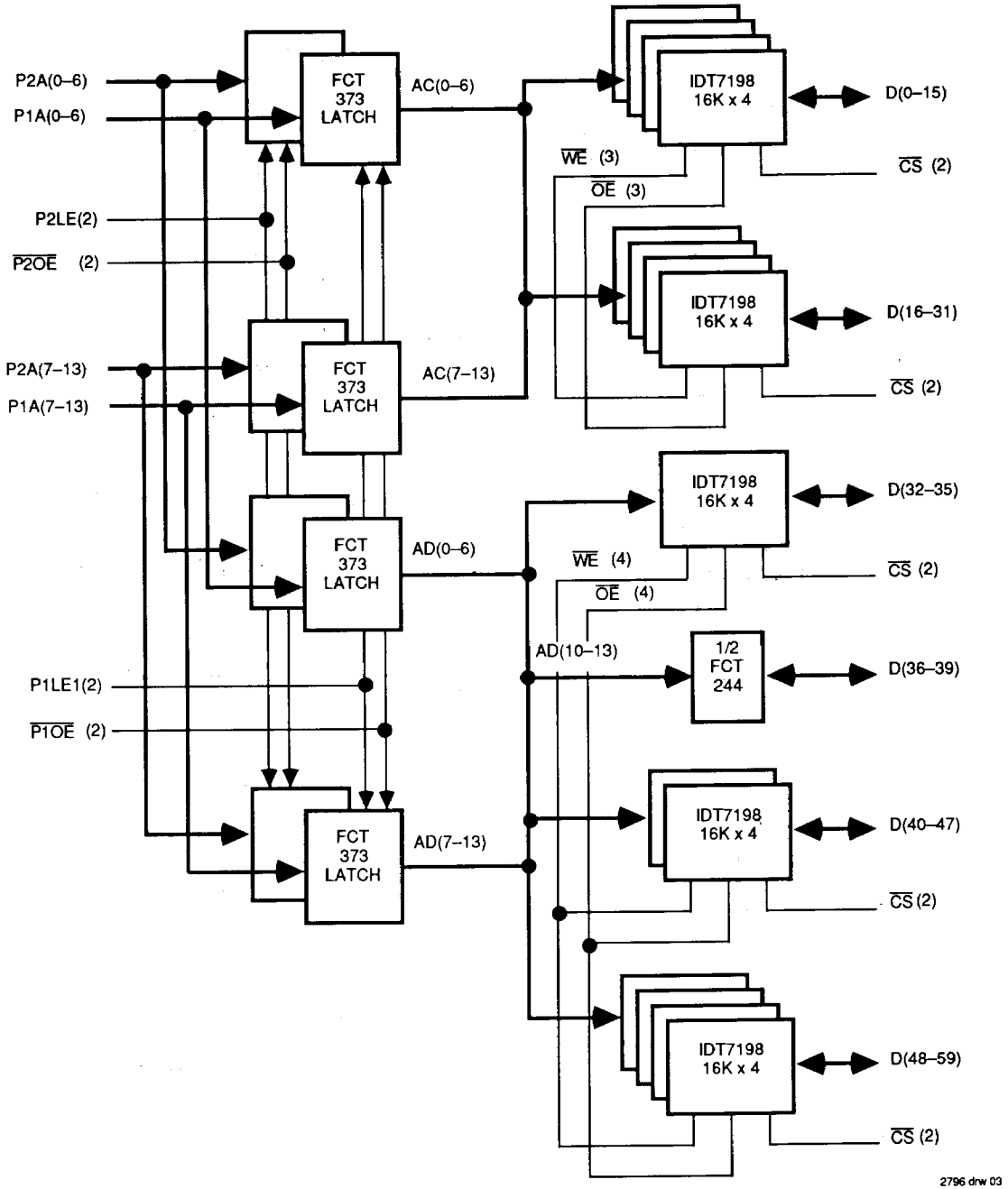


2796 drw 02

DATA CACHE

8

FUNCTIONAL BLOCK DIAGRAM



2796 drw 03

INSTRUCTION CACHE

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to 7.0	V
TA	Operating Temperature	0 to 70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2796 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2796 tbl 03

1. VIL (Min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to 70°C	0V	5.0V ± 10%

2796 tbl 04

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	12MHz		16.7MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
|ILI|	Input Leakage Current	Vcc = Max., VIN = GND to Vcc	—	20	—	20	—	20	—	20	—	20	µA
|ILO|	Output Leakage Current	Vcc = Max., $\overline{CS}$ = VIH, VOUT = GND to Vcc	—	10	—	10	—	10	—	10	—	10	µA
ICC1	Operating Current	f = 0, $\overline{CS}$ = VIL, Vcc = Max., Output Open	—	2350	—	2400	—	2500	—	2850	—	3000	mA
ICC2	Dynamic Operating Current	Vcc = Max., $\overline{CS}$ ≤ VIL, f = fMAX, Output Open	—	2850	—	2900	—	3125	—	3400	—	3600	mA
ISB1	Full Standby Supply Current	$\overline{CS}$ ≥ Vcc 0.2V, VIN >Vcc – 0.2V or < 0.2V	—	450	—	450	—	450	—	600	—	750	mA
ISB	Standby Power Supply Current	$\overline{CS}$ ≥ VIH, Vcc = Max. f = fMAX, Outputs Open	—	1300	—	1425	—	1575	—	1700	—	2000	mA
VOH	Output High Voltage	Vcc = Min., IOH = -4mA	2.4	—	2.4	—	2.4	—	2.4	—	2.4	—	V
VOL	Output Low Voltage	Vcc = Min., IOL = 8mA	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	V

2796 tbl 05

8

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2796 tbl 06

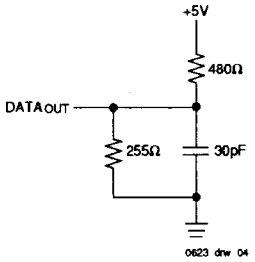
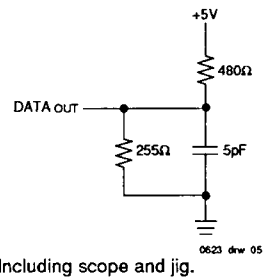


Figure 1. Output Load



* Including scope and jig.

Figure 2. Output Load (for tOLZ, tOHZ)

AC ELECTRICAL CHARACTERISTICS

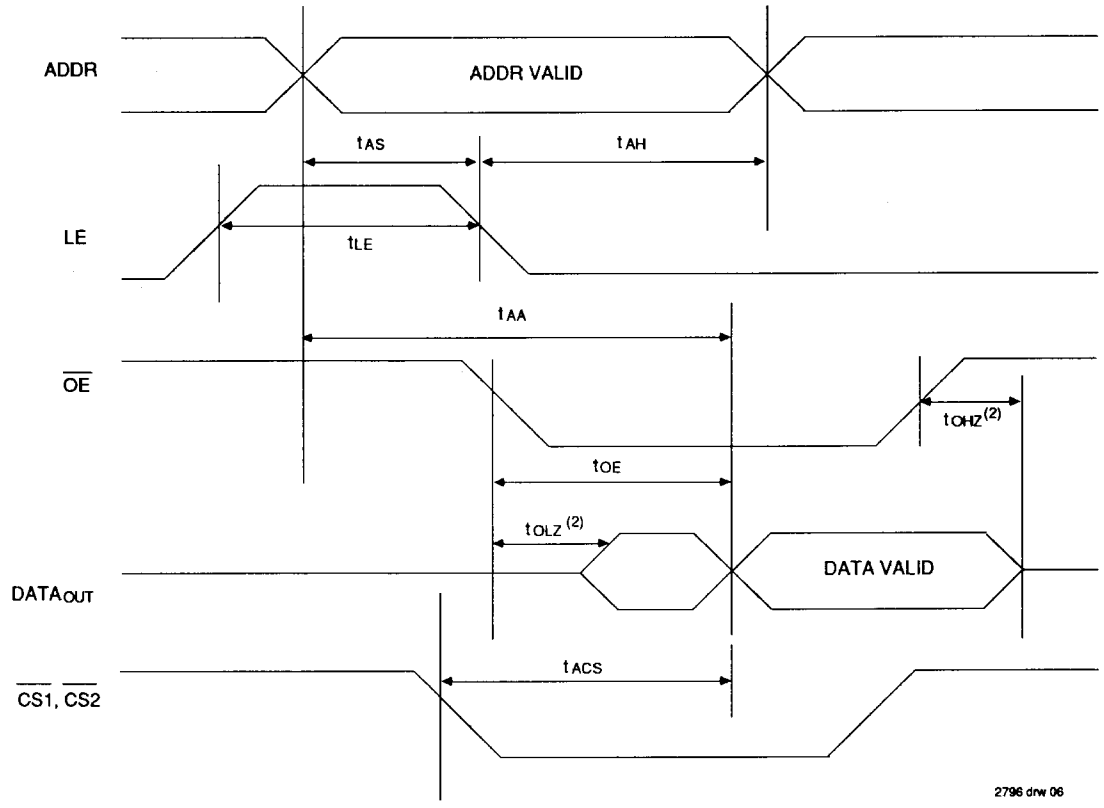
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	12MHz		16.7MHz		20MHz		25MHz		33MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tLE	Latch Enable Width	8	—	6	—	6	—	6	—	6	—	ns
tAS	Address Setup Time to LE	4	—	2	—	2	—	2	—	2	—	ns
tAH	Address Hold Time from LE	3	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AA}[2]	Address Access Time	—	45	—	35	—	30	—	25	—	20	ns
tACS	Chip Select Time	—	40	—	30	—	25	—	20	—	15	ns
t_{OE}[3]	Output Enable Time	—	22	—	17	—	11	—	8	—	5	ns
t_{OHZ}[1]	Output Disable to Output in High Z	2	16	2	14	2	10	2	8	2	6	ns
t_{OLZ}[1]	Output Disable to Output in Low Z	5	—	5	—	5	—	5	—	5	–	ns
Write Cycle												
tLE	Latch Enable Width	8	—	6	—	6	—	6	—	6	—	ns
tAS	Address Setup Time to LE	4	—	2	—	2	—	2	—	2	—	ns
tAH	Address Hold Time from LE	3	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AW}[2]	Address Valid to End of Write	40	—	30	—	25	—	23	—	20	—	ns
tCW	Chip Select to End of Write	35	—	25	—	20	—	18	—	15	—	ns
tWP	Write Pulse Width	30	—	25	—	20	—	17	—	12	—	ns
tDW	Data Valid to End of Write	20	—	13	—	13	—	11	—	8	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{LOE}[4]	Latch Output Enable	—	7	—	7	—	7	—	7	—	7	ns

2796 tbl 07

NOTES:
1. This parameter is guaranteed by design but not tested.
2. LE already asserted.
3. For all $\overline{OE}_{(1)}$, $\overline{OE}_{(2)}$, $\overline{OE}_{(3)}$, $\overline{OE}_{(4)}$
4. For all $\overline{P1OE_1}$, $\overline{P1OE_2}$, $\overline{P2OE_1}$, $\overline{P2OE_2}$

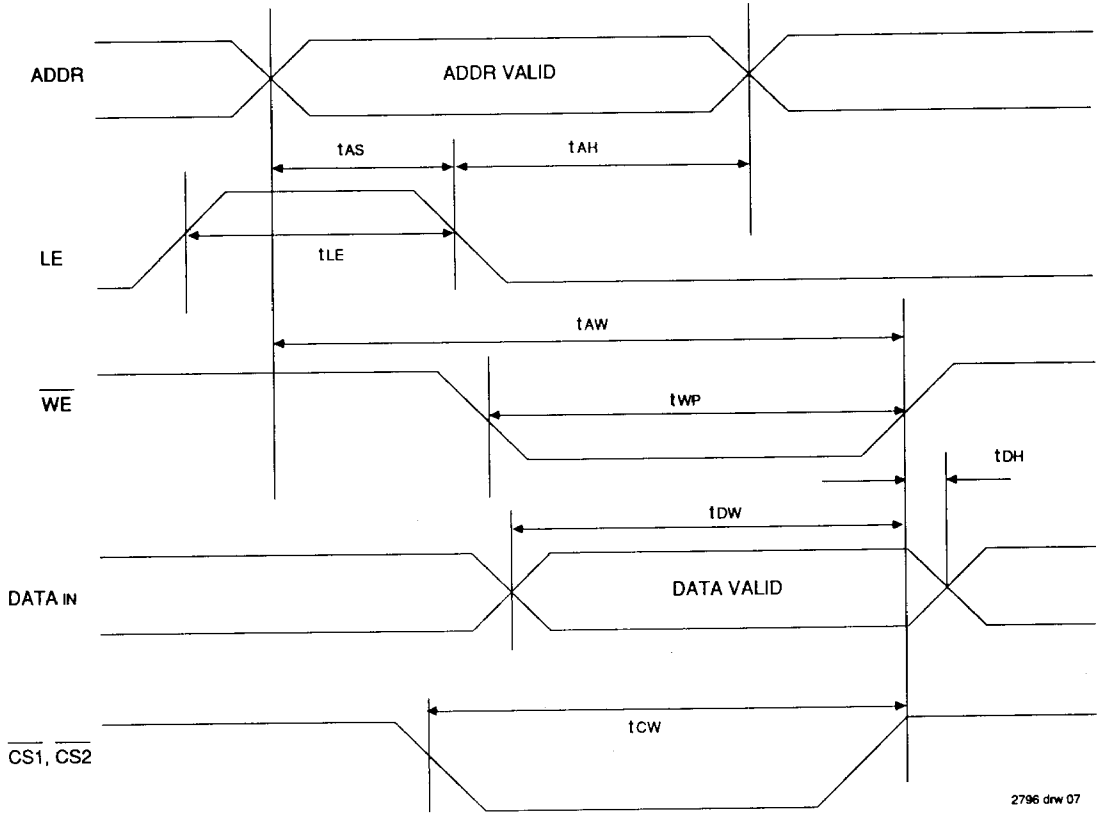
TIMING WAVEFORM OF READ CYCLE



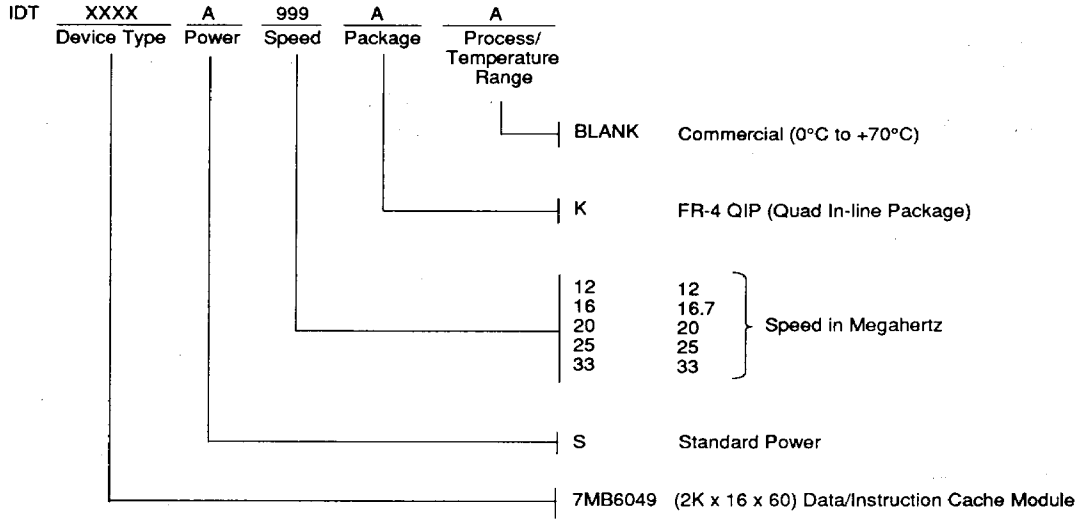
NOTE:
1. This parameter is guaranteed by design but not tested

8

TIMING WAVEFORM OF WRITE CYCLE



ORDERING INFORMATION



8