Integrated Device Technology, Inc.

FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74FCT299
IDT54/74FCT299A
IDT54/74FCT299C

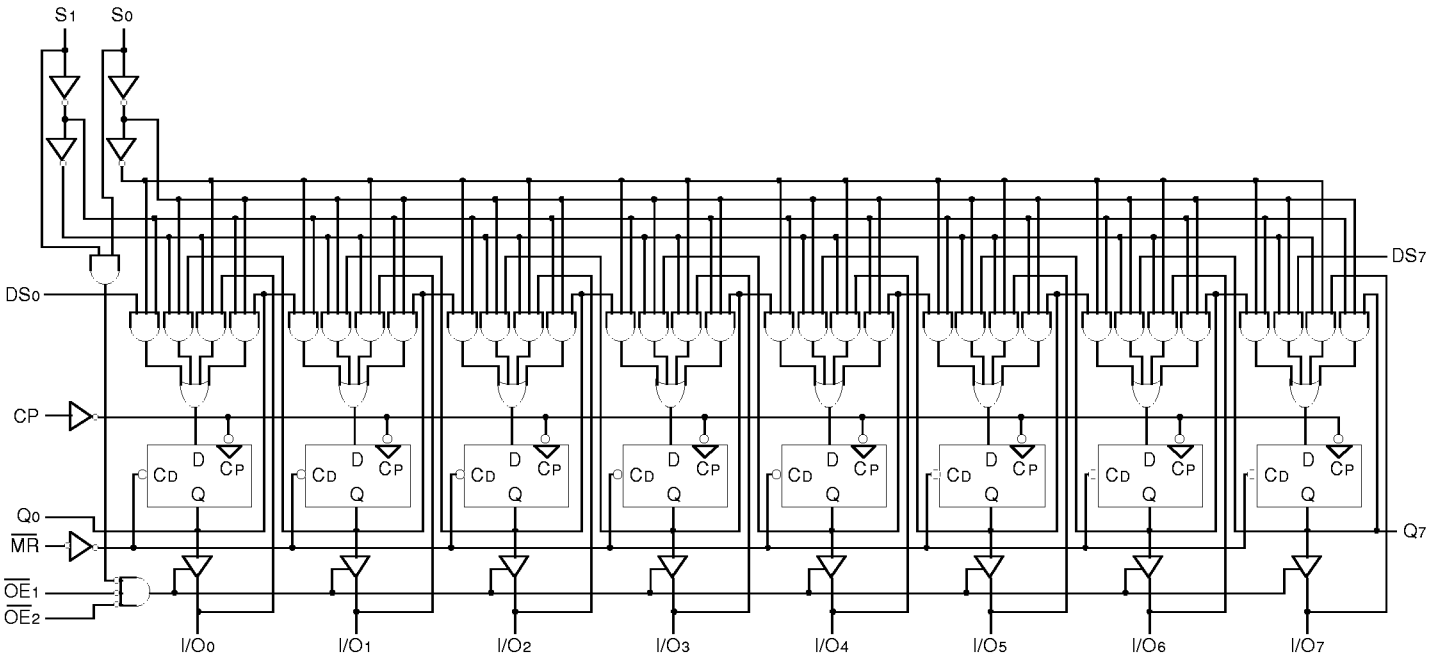
FEATURES:

- IDT54/74FCT299 equivalent to FAST™ speed
- **IDT54/74FCT299A 25% faster than FAST**
- **IDT54/74FCT299C 35% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5μA max.)
- 8-input universal shift register
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86862 is listed on this function. Refer to section 2.

DESCRIPTION:

The IDT54/74FCT299 and IDT54/74FCT299A/C are built using an advanced dual metal CMOS technology. The IDT54/74FCT299 and IDT54/74FCT299A/C are 8-input universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

FUNCTIONAL BLOCK DIAGRAM



2561 drw 01

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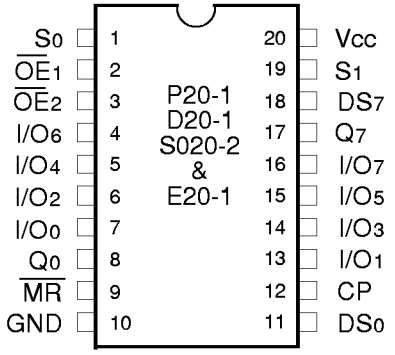
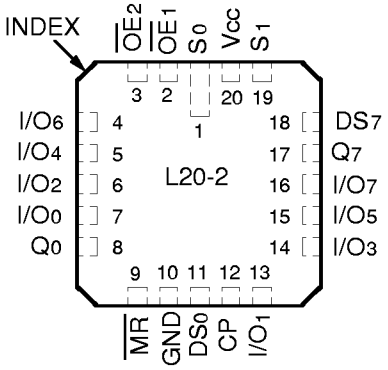
FAST is a registered trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

2561 drw 02

PIN DESCRIPTION

Pin Names	Description
CP	Clock Pulse Input (Active Edge Rising)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O_0–I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
Q_0, Q_7	Serial Outputs

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FUNCTION TABLE(1)

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset Q_0–Q_7 = LOW
H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

NOTE: 2561 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2561 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5 unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2561 tbl 04

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current (Except I/O Pins)		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current (I/O Pins Only)	V_{CC} = Max.	V_I = V_{CC}	—	—	15	µA
			V_I = 2.7V	—	—	15[4]	
I_{IL}	Input LOW Current (I/O Pins Only)		V_I = 0.5V	—	—	–15[4]	
			V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:

2561 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	Vcc = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	Vcc = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	Vcc = Max. Outputs Open $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	Vcc = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		Vcc = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

NOTES: 2561 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

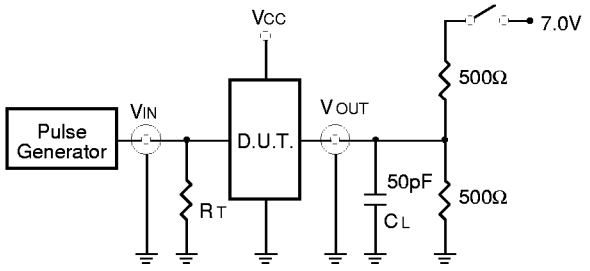
Symbol	Parameter	Condition[1]	IDT54/74FCT299				IDT54/74FCT299A				IDT54/74FCT299C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	14.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		2.0	12.0	2.0	12.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		2.0	10.0	2.0	10.5	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		2.0	15.0	2.0	15.0	2.0	8.7	2.0	11.5	2.0	6.5	2.0	7.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_n$ to I/O_n		1.5	11.0	1.5	15.0	1.5	6.5	1.5	7.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_n$ to I/O_n		1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	6.0	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW S_0 or S_1 to CP		7.5	—	7.5	—	3.5	—	4.0	—	3.5	—	4.0	—	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
t_{SU}	Set-up Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		5.5	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
t_H	Hold Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
t_W	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
t_{REM}	Recovery Time $\overline{MR}$ to CP		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2561 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

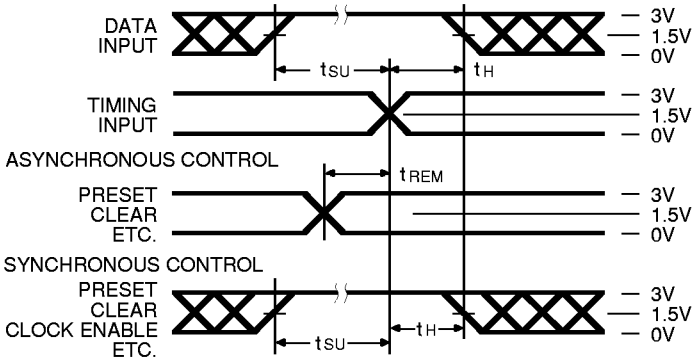
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2561 tbl 08

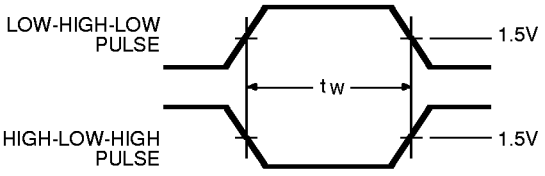
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



PULSE WIDTH



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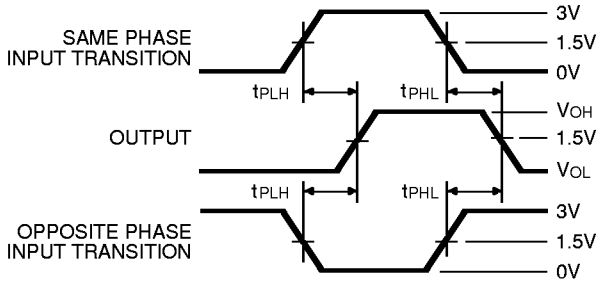
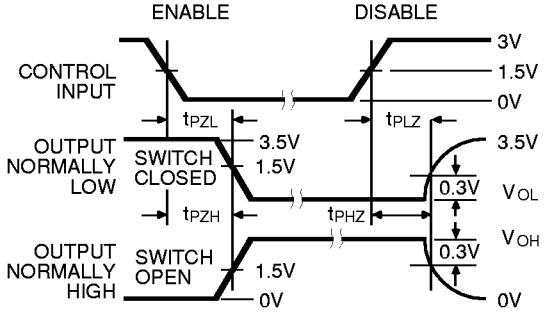


ENABLE AND DISABLE TIMES



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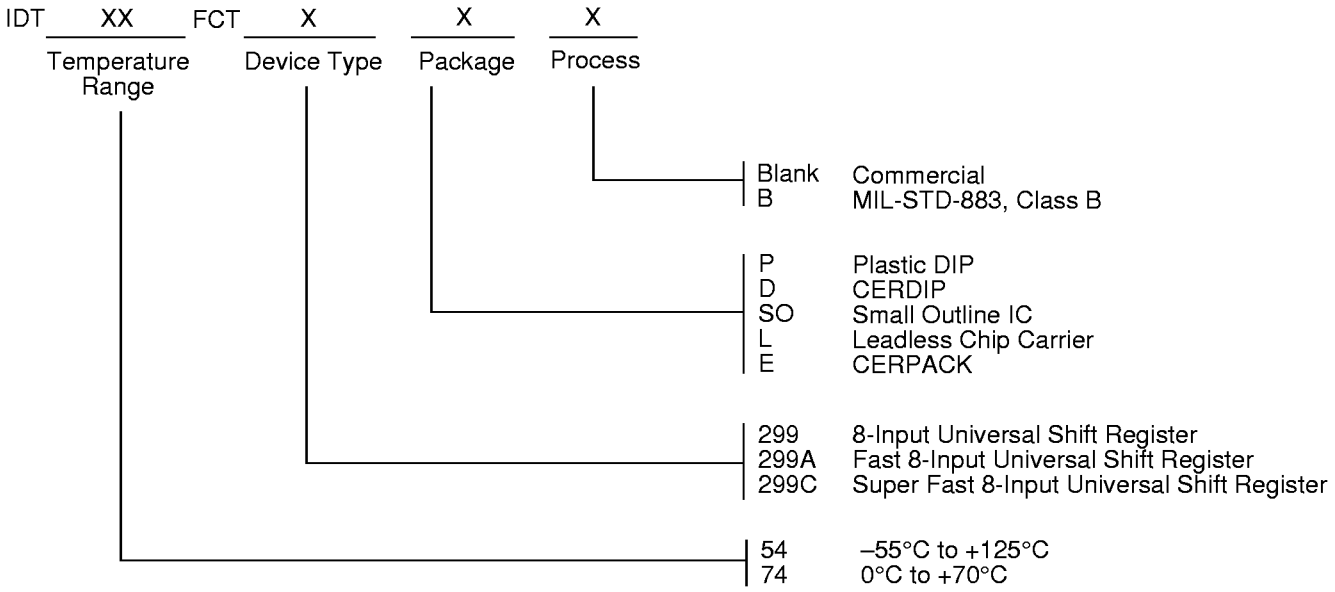
NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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