# HS-C²MOS™ INTEGRATED CIRCUITS

**M54HC4022**
**M74HC4022**

**PRELIMINARY DATA**

## OCTAL COUNTER/DIVIDER

### DESCRIPTION

The M54/74HC4022 is a high speed CMOS OCTAL COUNTER/DIVIDER fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It contains a 4-stage divide-by-8 Johnson counter with 8 decoded outputs (Q0-Q7) and a Carry-out bit. This counter is advanced on the positive edge of clock signal when CLOCK ENABLE input is held low, or is advanced on the negative edge of clock enable signal when CLOCK input is held high, and the selected one of eight outputs goes high. Holding high the CLEAR input, this counter is cleared to its zero state without regard to the other input conditions. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

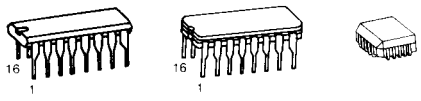
### FEATURES

- High Speed
  $f_{MAX}$ = 42 MHz (Typ) at $V_{CC}$ = 5V
- Low Power Dissipation
  $I_{CC}$ = 4 $\mu$A (Max.) at $T_A$ = 25°C
- High Noise Immunity
  $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (Min.)
- Output Drive Capability
  10 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}| = I_{OL}$ = 4 mA (Min.)
- Balanced Propagation Delays
  $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
  $V_{CC}$ (opr) = 2V to 6V
- Pin and Function compatible with 4022B

### TRUTH TABLE

X: Don't Care

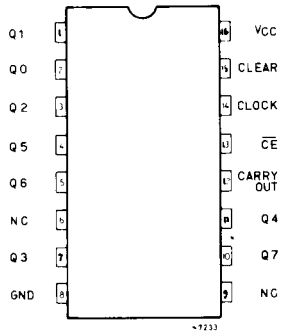
| CLOCK | $\overline{CE}$ | CLEAR | DECODER OUTPUT(H) |
|---|---|---|---|
| X | X | H | Q0 |
| L | X | L | No Change |
| X | H | L | No Change |
| ↓ | L | L | No Change + 1 |
| ↑ | L | L | No Change |
| H | ↓ | L | No Change |
| H | ↓ | L | No Change + 1 |




**B1** Plastic Package | **F1** Ceramic Package | **C1** Chip Carrier

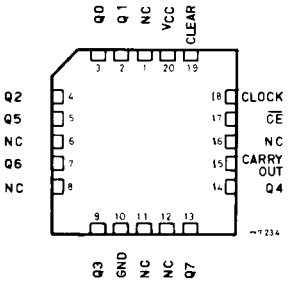
ORDERING NUMBERS: M54HC4022 F1
M74HC4022 B1
M74HC4022 F1
M74HC4022 C1

### PIN CONNECTIONS
(top view)



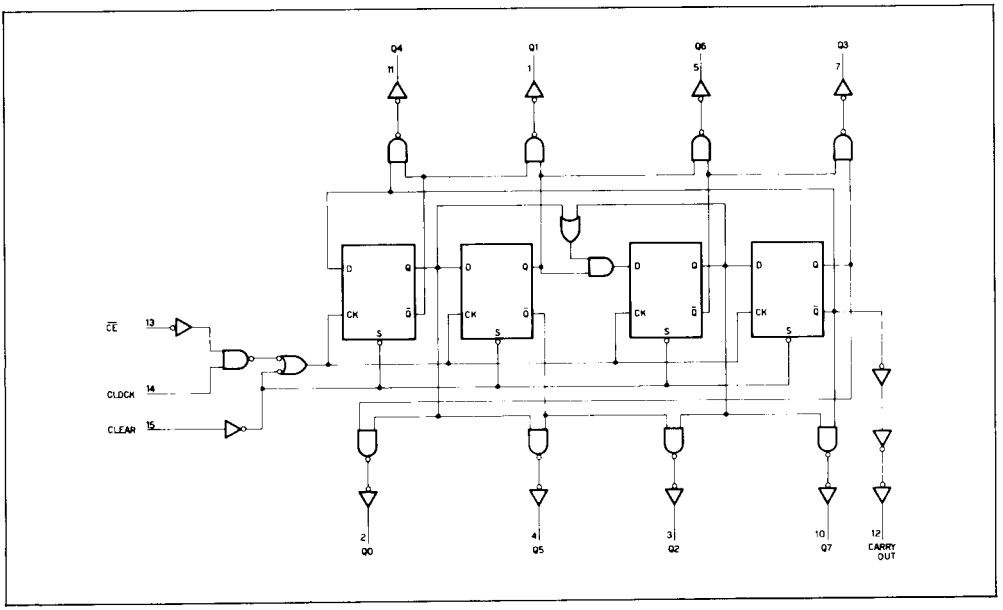

Dual in line

### CHIP CARRIER

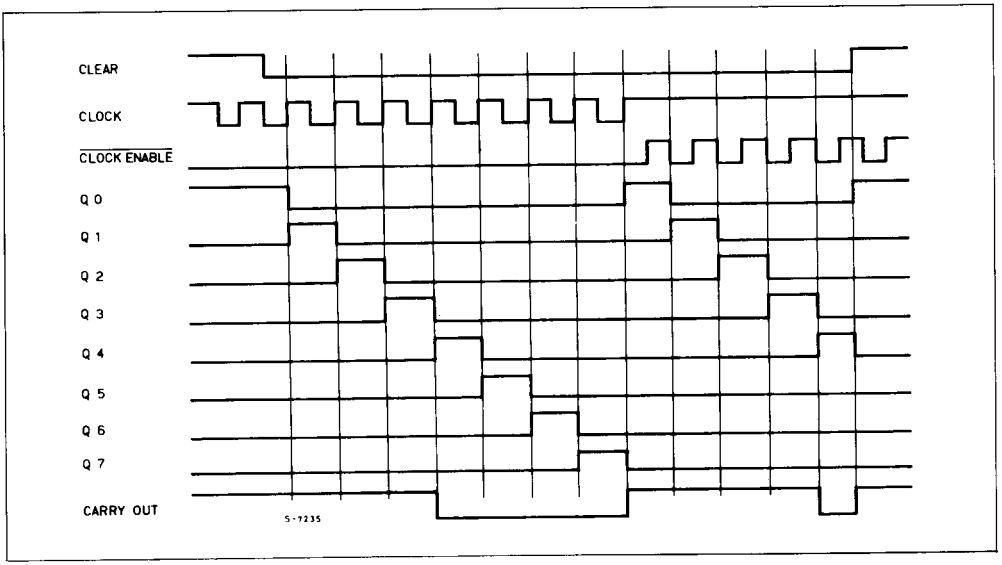



NC = No Internal Connection

## LOGIC DIAGRAM




## TIMING CHART



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 to 7 | V |
| $V_I$ | DC Input Voltage | −0.5 to $V_{CC}$ + 0.5 | V |
| $V_O$ | DC Output Voltage | −0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | ± 20 | mA |
| $I_{OK}$ | DC Output Diode Current | ± 20 | mA |
| $I_O$ | DC Output Source Sink Current Per Output Pin | ± 25 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current | ± 50 | mA |
| $P_D$ | Power Dissipation | 500 (*) | mW |
| $T_{stg}$ | Storage Temperature | −65 to 150 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Limit | | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 2 to 6 | | V |
| $V_I$ | Input Voltage | | 0 to $V_{CC}$ | | V |
| $V_O$ | Output Voltage | | 0 to $V_{CC}$ | | V |
| $T_A$ | Operating Temperature | 74HC Series<br>54HC Series | − 40 to 85<br>−55 to 125 | | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time | $V_{CC}$ = 2 V<br>$V_{CC}$ = 4.5V<br>$V_{CC}$ = 6 V | 0 to 1000<br>0 to 500<br>0 to 400 | | ns |

## DC SPECIFICATIONS

| Symbol | Parameter | $V_{CC}$ | Test Condition | $T_A$ = 25°C 54HC and 74HC | | | −40 to 85°C 74HC | | −55 to 125°C 54HC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $V_{IH}$ | High Level Input Voltage | 2.0<br>4.5<br>6.0 | | 1.5<br>3.15<br>4.2 | —<br>—<br>— | —<br>—<br>— | 1.5<br>3.15<br>4.2 | —<br>—<br>— | 1.5<br>3.15<br>4.2 | —<br>—<br>— | V |
| $V_{IL}$ | Low Level Input Voltage | 2.0<br>4.5<br>6.0 | | —<br>—<br>— | —<br>—<br>— | 0.5<br>1.35<br>1.8 | —<br>—<br>— | 0.5<br>1.35<br>1.8 | —<br>—<br>— | 0.5<br>1.35<br>1.8 | V |

## DC SPECIFICATIONS (Continued)

| Symbol | Parameter | $V_{CC}$ | Test Condition | | $T_A$ = 25°C 54HC and 74HC | | | −40 to 85°C 74HC | | −55 to 125°C 54HC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $V_{OH}$ | High Level Output Voltage | 2.0 | $V_I$ | $I_O$ | 1.9 | 2.0 | — | 1.9 | — | 1.9 | — | V |
| | | 4.5 | $V_{IH}$ | −20 μA | 4.4 | 4.5 | — | 4.4 | — | 4.4 | — | |
| | | 6.0 | or | | 5.9 | 6.0 | — | 5.9 | — | 5.9 | — | |
| | | 4.5 | $V_{IL}$ | −4.0 mA | 4.18 | 4.31 | — | 4.13 | — | 4.10 | — | |
| | | 6.0 | | −5.2 mA | 5.68 | 5.8 | — | 5.63 | — | 5.60 | — | |
| $V_{OL}$ | Low Level Output Voltage | 2.0 | | | — | 0 | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 4.5 | $V_{IH}$ | 20 μA | — | 0 | 0.1 | — | 0.1 | — | 0.1 | |
| | | 6.0 | or | | — | 0 | 0.1 | — | 0.1 | — | 0.1 | |
| | | 4.5 | $V_{IL}$ | 4.0 mA | — | 0.17 | 0.26 | — | 0.33 | — | 0.40 | |
| | | 6.0 | | 5.2 mA | — | 0.18 | 0.26 | — | 0.33 | — | 0.40 | |
| $I_I$ | Input Leakage Current | 6.0 | $V_I$ = $V_{CC}$ or GND | | — | — | ±0.1 | — | ±1 | | ±1 | μA |
| $I_{CC}$ | Quiescent Supply Current | 6.0 | $V_I$ = $V_{CC}$ or GND | | — | — | 4 | — | 40 | | 80 | μA |

## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 15pF, Input $t_r = t_f$ = 6ns)

| Symbol | Parameter | 54HC and 74HC | | | Unit |
|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | | 4 | 8 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (CLOCK-Q, CARRY) | | 21 | 33 | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (CLEAR-Q, CARRY) | | 21 | 33 | ns |
| $f_{MAX}$ | Maximum Clock Frequency | 30 | 48 | | ns |
| $t_{W(L)}$ $t_{W(H)}$ | Minimum Pulse Width (CLOCK) | | 8 | 15 | ns |
| $t_{W(H)}$ | Minimum Pulse Width (CLEAR) | | 9 | 15 | ns |
| $t_s$ | Minimum Set-up Time | | — | 0 | ns |
| $t_h$ | Minimum Hold Time | | 9 | 15 | ns |
| $t_{REM}$ | Minimum Removal Time | | 8 | 15 | ns |

## AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

| Symbol | Parameter | $V_{CC}$ | Test Condition | $T_A$ = 25°C 54HC and 74HC | | | −40 to 85°C 74HC | | −55 to 125°C 54HC | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $t_{TLH}$ $t_{THL}$ | Output Transition Time | 2.0 | | — | 30 | 75 | — | 90 | | | ns |
| | | 4.5 | | — | 9 | 15 | — | 18 | | | |
| | | 6.0 | | — | 8 | 13 | — | 16 | | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time (CLOCK-Q, CARRY) | 2.0 | | — | 100 | 195 | — | 235 | | | ns |
| | | 4.5 | | — | 25 | 39 | — | 47 | | | |
| | | 6.0 | | — | 22 | 34 | — | 40 | | | |
| $t_{PLH}$ $t_{PHL}$ | Progation Delay Time (CLEAR-Q, CARRY) | 2.0 | | — | 100 | 195 | — | 235 | | | ns |
| | | 4.5 | | — | 25 | 39 | — | 47 | | | |
| | | 6.0 | | — | 22 | 34 | — | 40 | | | |
| $f_{MAX}$ | Maximum Clock Frequency | 2.0 | | 5 | 10 | — | 4 | — | | | MHz |
| | | 4.5 | | 25 | 40 | — | 20 | — | | | |
| | | 6.0 | | 29 | 45 | — | 23 | — | | | |
| $t_{W(L)}$ $t_{W(H)}$ | Minimum Pulse Width (CLOCK) | 2.0 | | — | 30 | 75 | — | 90 | | | ns |
| | | 4.5 | | — | 8 | 15 | — | 18 | | | |
| | | 6.0 | | — | 7 | 13 | — | 16 | | | |
| $t_{W(H)}$ | Minimum Pulse Width (CLEAR) | 2.0 | | — | 35 | 75 | — | 90 | | | ns |
| | | 4.5 | | — | 9 | 15 | — | 18 | | | |
| | | 6.0 | | — | 8 | 13 | — | 16 | | | |
| $t_s$ | Minimum Set-up Time | 2.0 | | — | — | 0 | — | 0 | | | ns |
| | | 4.5 | | — | — | 0 | — | 0 | | | |
| | | 6.0 | | — | — | 0 | — | 0 | | | |
| $t_h$ | Minimum Hold Time | 2.0 | | — | 35 | 75 | — | 90 | | | ns |
| | | 4.5 | | — | 9 | 15 | — | 18 | | | |
| | | 6.0 | | — | 8 | 13 | — | 16 | | | |
| $t_{REM}$ | Minimum Removal Time | 2.0 | | — | 30 | 75 | — | 90 | | | ns |
| | | 4.5 | | — | 8 | 15 | — | 18 | | | |
| | | 6.0 | | — | 7 | 13 | — | 16 | | | |
| $C_{IN}$ | Input Capacitance | | | — | 5 | 10 | — | 10 | | | pF |
| $C_{PD}$ (*) | Power Dissipation Capacitance | | | — | 52 | — | — | — | | | pF |

Note (*) $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$