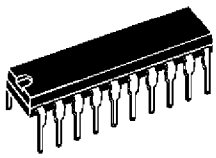
SGS-THOMSON MICROELECTRONICS

ST5421

SID-GCI : S/T INTERFACE DEVICE WITH GCI

PRELIMINARY DATA

- SINGLE CHIP 4 WIRES 192kb/s TRANSCEIVER FULLY COMPLYING WITH CCITT I.430
- ISDN BASIC ACCESS HANDLING 144kb/s 2B + D TRANSMISSION
- GCI COMPATIBLE INTERCHIP INTERFACE
- ADAPTIVE AND FIXED TIMING OPTIONS FOR NT
- CLOCK RESYNCHRONIZER AND DATA BUFFERS FOR NT2
- PROGRAMMABLE S1 AND Q CHANNELS HANDLING ACCORDING TO US ANSI STANDARD FOR LAYER 1 MAINTENANCE
- EASILY INTERFACEABLE WITH ST5451 HDLC & GCI CONTROLLER AND ANY OTHER GCI COMPATIBLE DEVICE



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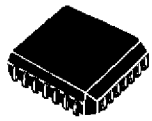
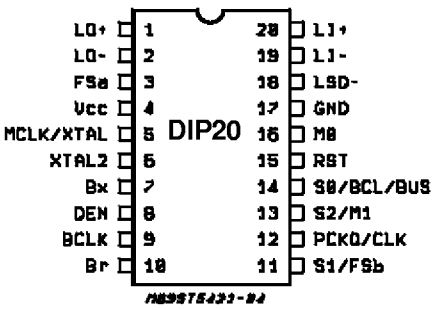


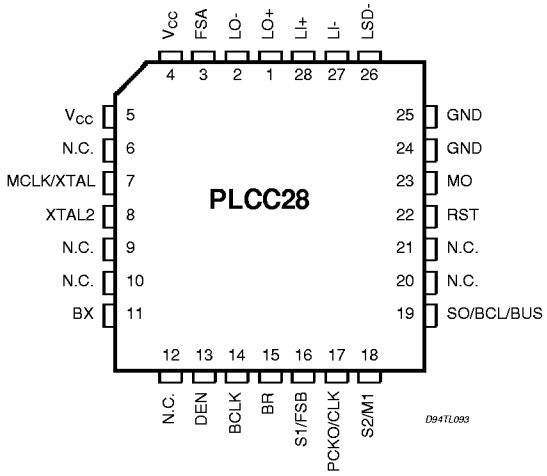
PLCC28

ORDERING NUMBERS:

ST5421CP ST5421CFN

PIN CONNECTIONS (Top views)





DESCRIPTION

The ST5421 (SID-GCI) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is built on SGS-THOMSON HCMOS 3A double metal advanced process, and requires only a single + 5V supply. All functions specified in CCITT recommendation I.430 for ISDN basic access at the 'S' and 'T' interfaces are provided, and the device can be configured to operate either in TE (Terminal Equipment), in NT1 or NT2 (Network Termination) or in PABX line-card device.

GCI interchip interface highly enhances device connection efficiency by multiplexing controls and data on the same bus and requiring only 4 pins. ST5421 implements all the GCI standard functions for Monitor and Control/Indicate channels, supporting up to 8 GCI peripherals in multiplexed mode.

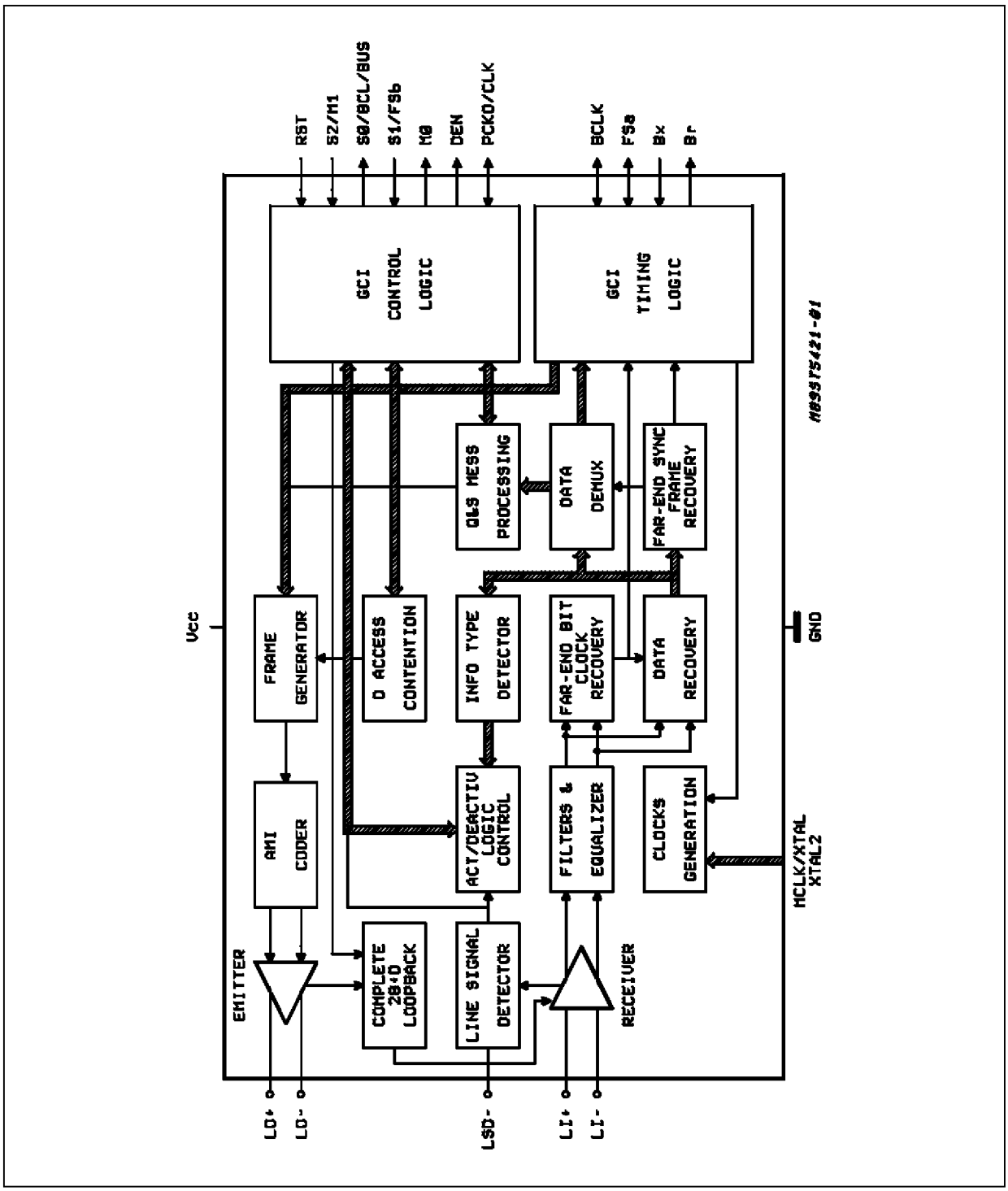
As specified in I.430, full-duplex transmission at 192kb/s is provided on separate transmit and receive twisted wire pairs using inverted Alternate Mark Inversion (AMI) line coding. Various channels are combined to form the 192kb/s aggregate rate, including 2 'B' channels, each of 64kb/s, and 1 'D' channel at 16kb/s. In addition, multiframe transmission is provided in a switchable processing mode based on United State ANSI standard for Layer 1 maintenance. 800 bit/s message oriented data transmission is supported by S1 and Q channels.

DESCRIPTION (Continued)

All I.430 wiring configurations are supported by ST5421 including passive bus for TE's distributed point-to-point and point-to-multipoint extended. Adaptive receive signal processing enables the device to operate with low bit error rate on any of the standard types of cable pairs commonly found in premise wiring installations when tested with the noise sources specified in I.430.

Far-end Clock Resynchronizer automatically selected, data buffer and slave-slave mode allow design of NT2 trunk-card connected to several T interfaces.

BLOCK DIAGRAM



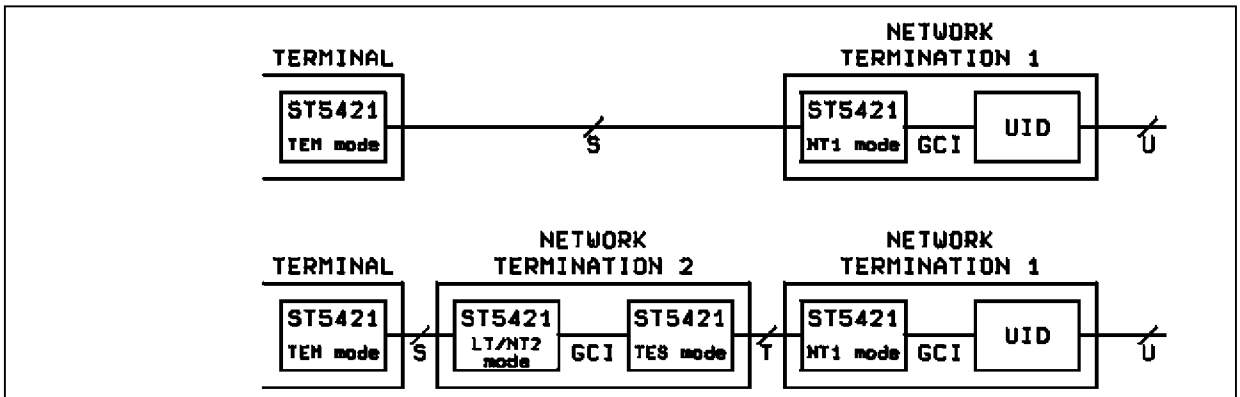
PIN DESCRIPTION

Name	DIP	PLCC	Description
GND	17	24,25	Ground Reference Voltage: all analog and digital signals are referenced to this pin.
V_{CC}	4	4,5	Positive Power Supply Input 5V ($\pm$ 5%) relative to GND
MCLK/XTAL	5	7	Master Clock or Crystal Oscillator Input: this pin requires either a 15.36MHz crystal (parallel resonant with R_S < 100 Ω) to be tied between this pin and XTAL2 or a logic CMOS level 15.36MHz clock from a stable source. When using a 20pF crystal, a total of 33pF load capacitance to GND must also be connected. In NT configurations. MCLK clock input doesn't need to be synchronous with the Network Reference Clock (FSa).
XTAL2	6	8	Crystal Oscillator Output. This pin should be connected to one end of the 15.36MHz crystal, otherwise is not connected. (see MCLK/XTAL).
BCLK	9	14	Bit Clock: this signal determines the data shift rate at GCI. Data is shifted-in on Bx and shifted-out on Br at half the BCLK frequency. When NT/TES mode is selected, BCLK is an input which does not need to be synchronous with the Master Clock input (MCLK). When TEM is selected, BCLK is an output at frequency of 1536kHz. This clock is phase locked to the receive line signal and synchronous with FSa output.
FSa	3	3	Frame Synchronization Clock: 8kHz clock which defines the start of the frame. In GCI slave (NT/TES) FSa is an input used as a network reference clock for S/T line. In GCI master (TEM) is an output applicable as a validation strobe for the first B channel.
S1/FSb	11	16	S1 if M0 = 1; is GCI channel number selection (input). FSb if M0 = 0 and M1 = 0 (TEM): is a data strobe indicating the active slot for the second B channel on the GCI (output). In NT1 mode, M0 = 0; M1 = 1, this pin is not used and must be left floating.
Bx	7	11	Digital Input for GCI Channels: data to be transmitted to S line is shifted-in at half the BCLK frequency on the 2nd falling edge.
Br	10	15	Digital Output for GCI Channel (OPENDRAIN): data is shifted-out at half the BCLK frequency on the transmit rising edges of BCLK. An external pull-up resistor is needed.
DEN	8	13	In TEM mode DEN is an output, normally low, that pulses high to indicate the active time slot for D channel data at the Bx input. It is intended to be gated with BCLK to control the D channel shifting from a layer 2 device (i.e. ST5451) to ST5421 transmit buffer. Using ST5451 HDCL/GCI controller, no external circuitry is needed. In NT/TES mode this pin is not used and must be kept floating.
Not Connected	–	6,9,10, 12,20,21	Leave open on the board.
PCK0/CLK	12	17	PCK0 IN TEM, LT/NT2, NT1 mode: 32 kHz clock output synchronized to GCI clocks. It is intended to synchronize DC/DC converter in TEM mode. CLK in TES mode: is a clock signal open drain output phased-locked to the receive S line signal and applicable as far-end clock reference. Its frequency is 1536kHz compatible with 768kbit/s GCI data rate. An external pull-up resistor is needed.
M0	16	23	M0 = 0: GCI mode selection; Time slot Assigner is selected on GCI channel 0. M0 = 1: GCI in a multiplex mode; S0, S1, S2 pins define the GCI channel number allocated to ST5421. TES/NT2 selection is done with the configuration registers (input).

PIN DESCRIPTION (continued)

Name	DIP	PLCC	Description
S2/M1	13	18	S2 if M0 = 1: GCI channel number selection (input). When M0 = 0 M1 select TEM or NT1 mode: M1 = 0 selects TEM, M1 = 1 selects NT1.
S0/BCL/BUS	14	19	S0 if M0 = 1; GCI channel number selection (input). BCL in TEM; bit clock output at 768kHz compatible with COMBO families ETC5054/57. BUS in NT1; S Bus Configuration Selection: low for fixed timing recovery and high for adaptive timing recovery (input).
RST	15	22	Reset Pin: must be low at Power On Reset; after, a high pulse on this pin reset ST5421 in a state depending on the other configuration pins (input).
LSD-	18	26	Line Signal Detect: open drain output, normally high impedance, pulling low when SID-GCI is powered down and an S line signal is detected. It is applicable to wake up a microprocessor from a low power idle mode. LSD^- output goes back to high impedance when ST5421 is powered up.
LO+, LO-	1,2	1,2	Transmit AMI signal differential outputs to the S/T line transformer; when used with an appropriate 2:1 step down transformer, the line signal conforms to the output pulse masks in CCITT I.430.
LI^-,LI^+	19,20	27,28	Receive AMI signal inputs from the S/T line transformer. They should be connected to an appropriate 1:2 or 1:1 transformer through a line coupling circuit to conform I.430 recommendation. LI^- pin is also the internal voltage reference pin.

Table 1: Pin configurations



	TEM	LT/NT2(1)	TES (1)	NT1
M0	i-0	i-1	i-1	i-0
DEN	o-DEN			
S2/M1	i-M1-0	i-S2	i-S2	i-M1-1
S1/FSb	o-FSb	i-S1	i-S1	Not used
S0/BCL/BUS	o-BCL	i-S0	i-S0	i-BUS
PCKO/CLK	o-PCKO	o-PCKO	o-CLK	o-PCKO

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(1) differentiation between TES and LT/NT2 is done by register programming.
Default value after reset is LT/NT2 in adaptive timing recovery configuration.

FUNCTIONAL DESCRIPTION

POWER ON INITIALIZATION

Following initial application of power, SID-GCI enters the power down de-activated state.
RST input must be tied low during power-on.

After Power on reset, all the internal I.430 circuits including the master oscillator are inactive and in a low power state except for the line signal detection circuit.

After any period of activity a high pulse on RST reset completely SID-GCI.

Configuration mode programming of SID-GCI is done by means of pins polarization and register programming.

NT1 and TEM modes are defined only by means of 2 configuration pins M0, M1 at Power On Reset.

For NT2 and TES modes (M0=1), configuration has to be completed by means of a Control Instruction on Monitor channel prior a Power Up instruction.

POWER UP/DOWN CONTROL

When TEM configuration is selected, ST5421 provides GCI Clocks needed for control channel transfer. Power Up instruction is directly provided by pulling low the Bx data input. SID-GCI then reacts sending GCI clocks. LSD- output pin can be directly connected to Bx data input for providing an automatic Power up when far-end attempts to activate.
After a period of activity, Power down state is normally re-entered by C/I control code DC (1111) while ST5421 is sending C/I indication code DP (0000); then ST5421 send twice C/I indication code DI(1111) before to power down.
It is possible to force immediately power down state by using PDN (0001) C/I control code.

When NT1 configuration is selected, ST5421 is powered up directly by receiving GCI clocks on BCLK and FSa input from the "U" device. The only way to power down ST5421 is to stop BCLK or FSa clock signal inputs.
For example PDN (0001) C/I control code has no effect.

When NT2 or TES configuration is selected, SID-GCI is powered up by the PUP code (0000) on C/I Control Channel. After a period of activity, Power down state is normally reentred by C/I control code DC (1111) while ST5421 is sending C/I indication DI(1111).
It is possible to force immediately Power down state by using PDN (0001) C/I control code. In NT1, NT2 or TES mode, loss of GCI clocks automatically forces the power down state.

POWER UP/DOWN STATE

Following a period of activity in the power up state, power down state may be re-entered as described above. Configuration Registers remain in their current state. They can be changed by the GCI Monitor channel.

The power down transition disables analog and I.430 circuitry, stops the Crystal Oscillator and all the clocks internally generated. Line Signal Detector Circuit remains active allowing LSD-pin to pull low if a receive signal is detected.

Power up transition enables all analog and I.430 circuitry, starts the Crystal oscillator and reset the state machine to the de-activated state. It also inhibits LSD-output.

LINE CODING AND FRAME FORMAT

For both directions of transmission, Alternate Mark Inversion (AMI) coding with inverted binary is used, as illustrated in figure 1.

This coding rule requires that a binary ONE is represented by a 0 current high impedance output, whereas a binary ZERO is represented by a positive or negative-going 100% duty cycle pulse. Normally, binary ZEROs alternate in polarity to maintain a d.c. balanced line signal.

The frame format used in SID-GCI follows CCITT reccommendation in I.430 and illustrated in figure 2. Each complete frame consists of 48 bits, with a line bit rate of 192kbit/s, giving a frame repetition rate of 4kHz. A violation of the AMI coding rule is used to indicate a frame boundary, by using a 0+ bit followed by a 0- balance bit to indicate the start of a frame, and by forcing the first binary zero following the balance bit to be of the same polarity as the balance bit.

In the Network Termination (NT) to Terminal Equipment (TE) transmission direction, the frame contains in addition to the 2B+D basic access data, an echo channel, the E bit, which is used to retransmit the D bits that are received from the TE (s), and three extra channels: FA, M and S bit.

In the TE to NT direction, the frame contains in addition to the 2B + D data, an extra channel, the FA bit.

FA, M and S bits are used to set up a Q multiframe channel in the TE or NT direction, and a S1 multiframe channel from NT to TE. These 800bit/s message oriented channels are structured on the base of the United States ANSI standard specification for layer 1 maintenance.

Figure 1: Inverted AMI Line-coding Rule.

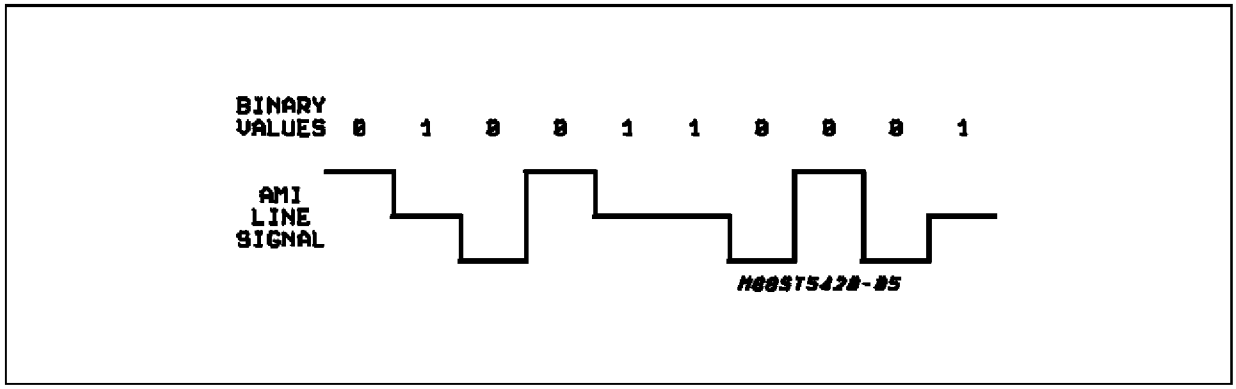
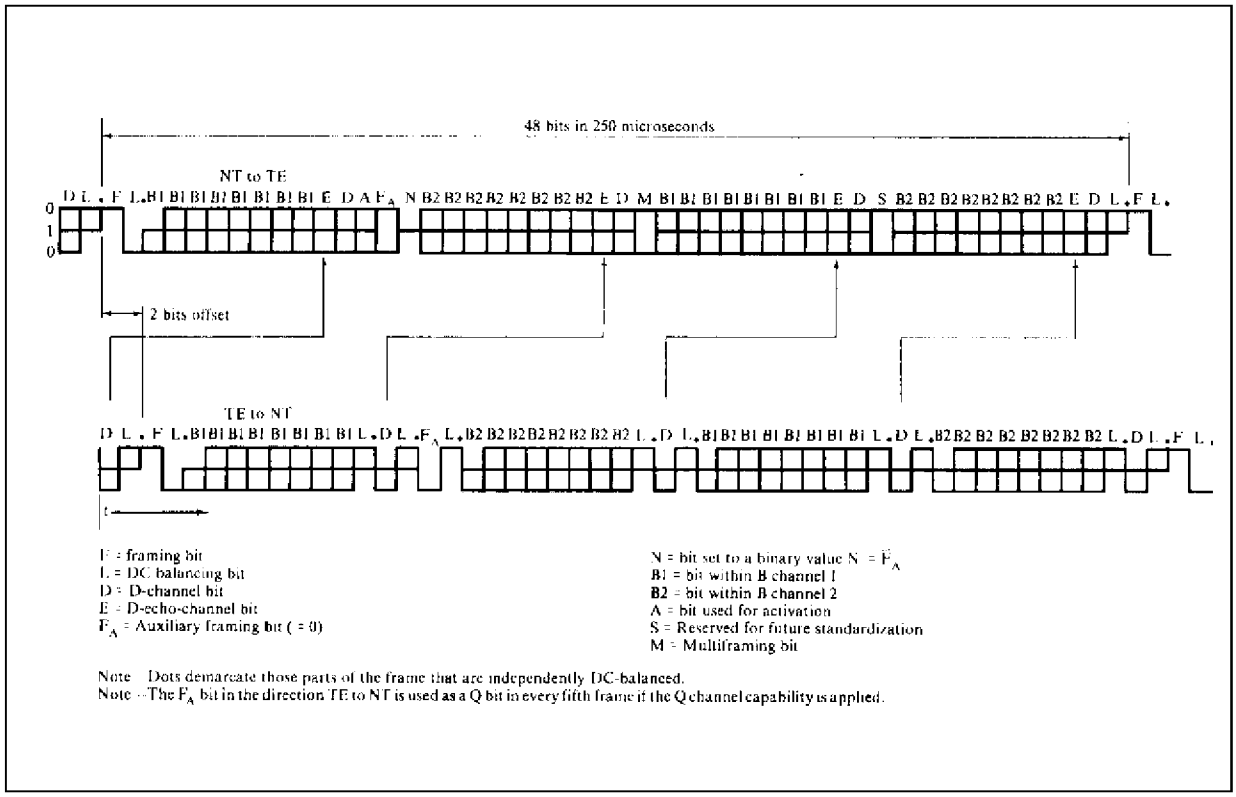


Figure 2: Frame Format



LINE TRANSMIT SECTION

The differential line driver outputs LO+ and LO- are designed to drive a suitable transformer with an external termination resistor. A 2:1 transformer, results in a signal amplitude of 750mV on the line which meets the I.430 pulse shape for all the loads specified.

When driving a binary 1 symbol, the output presents a high impedance in accordance with I.430. When driving a 0+ or 0- symbol, the voltage limited current source is turned on.

Short protection is included in the output stage.

Overvoltage protection is required externally.

Depending on TE or NT selected configuration, 192kbit/s data is transmitted on LO+,LO- by means of clocks respectively locked on the far-end received bit and frame clocks recovered from the line with two bit delay between transmit and receive frame, or locked with a fixed delay on the Frame Sync signal received from FSa input.

LINE RECEIVE SECTION

The receive input signal should be derived via a 1:1 a or 1:2 transformer of the same type used for

the transmit direction. At the front end of the receive section is a continuous filter which limits the noise bandwith. To improve the protection of the line interface and to comply with the receive input impedance specification even if power is lost, it is necessary to add 3 external resistors between the receive transformer and the LI+/LI- pins.

To correct pulse attenuation and distorsion caused by the transmission line in point-to-point and extended passive bus applications, an adaptive equalizer enhances the received pulse shape, thereby restoring a "flat" channel response with maximum eye opening over a wide spread of cable attenuation characteristics.

This equalizer is always enabled when either TE or NT mode adaptive sampling is selected, but is disabled for NT short passive bus applications, when NT mode fixed sampling is selected.

An adaptive threshold circuit maximizes Signal to Noise ratio in the eye at the detector for all loop conditions.

A DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols.

The MCLK input provides the reference clock for the DPLL at 15.36MHz.

When the device is powered down, a Line Signal Detect circuit, able to discriminate a valid line signal from noise, is enabled to detect the presence of incoming data. LSD-output pulls low to wake up the equipment.

GCI INTERFACE

General Description

GCI interface is an European standardized interface to connect ISDN dedicated components in the different configurations of equipment as Terminals, Network Terminations, PBX, etc...

In Terminal Equipments, this interface allows connection between SID-GCI and an associated ST5451 HDLC&GCI Controller used for 16kbit/s D channel processing and SID-GCI control. 64kbit/s B1 and B2 channels are transferred on GCI interface providing direct connection for B channel processing peripherals like Programmable ISDN COMBO ST5080 or extra ST5451 controllers.

In NT2 or PBX line card, GCI interface permits connection of up to 8 SID-GCI onto a common serial multiplexed bus. Each SID-GCI is assigned to one GCI channel selected by hardware configuration.

Figure 3 shows the Frame structure of a GCI channel. One GCI channel is structured in four subchannels:

- B1 channel 8 bits
- B2 channel 8 bits
- Monitor (M) channel 8 bits
- SC channel which is structured as follows:
  - D channel 2 bits
  - C/I channel 4 bits
  - A bit associated with M channel
  - E bit associated with M channel

B1,B2 and D channels are used to transfer 2B + D basic access data.

M channel is used to read and write multiframe S1 and Q channel messages and to configurate SID-GCI. Protocol for byte exchange on the M channel uses the E and A bits.

C/I (Control/Indicate) channel is used to exchange "real time" primitives between the SID-GCI and the Controller as Activation/Deactivation codes.

Physical Description

The interface consists of 4 wires:

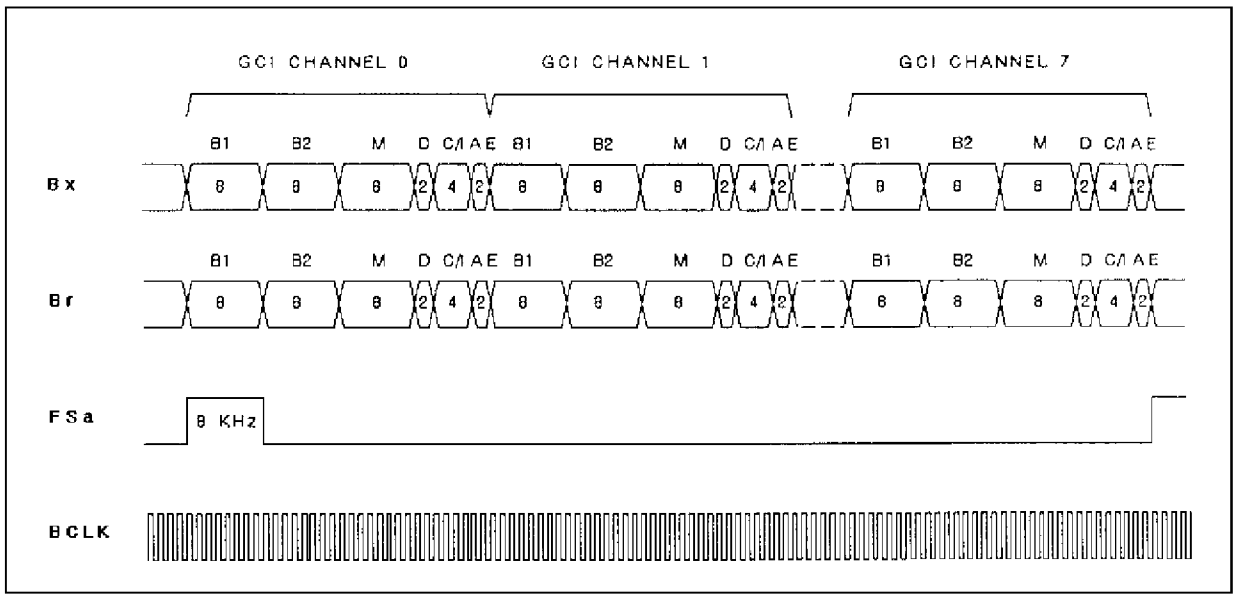
- Input Data: Bx
- Output Data: Br
- Bit Clock: BCLK
- Frame Synchronization: FSa

Data is synchronized by BCLK and FSa signals. The latter insures reinitialization of a time slot counter at each frame beginning. Its rising edge is the reference for the first bit of the first GCI channel. Data is transmitted in both directions at half the BCLK frequency, on the rising edge of BCLK and is sampled 1.5 period after the transmit rising edge. Unused channels are high impedance.

In NT2 or PABX equipments, up to 8 GCI channels (32 bits each) may be multiplexed on Bx and Br links used as a serial bus for several devices. The channel number selection is made by programming pins S0,S1 and S2 according to the following rules:

S2	S1	S0	Channel Number	Timeslots
0	0	0	0	0 -3
0	0	1	1	4 - 7
0	1	0	2	8 - 11
0	1	1	3	12 - 15
1	0	0	4	16 - 19
1	0	1	5	20 - 23
1	1	0	6	24 - 27
1	1	1	7	28 - 31

Figure 3: GCI Interface Structure



BCLK frequency may be any value between 512 and 6176kHz.

In TEM and NT1 configurations, the first GCI channels is automatically selected.

In TEM configuration, due to SID-GCI recovery circuitry, a low jitter should be provided on FSa and BCLK clocks. FSa and BCLK are always in phase. The maximum value of jitter amplitude is a step of 65ns at each GCI frame (125µs). The maximum high frequency jitter amplitude is 130ns pk-pk.

For applications such as the network side of an NT2, eg, a PABX trunk card, TES mode allows the transmission side of SID-GCI to be a slave to the received frame timing while GCI is also in slave mode Elastic buffers which allow any phase relationship between FSa and I.430 frames and a clock resynchroniser circuit absorb jitter and low frequency wander up to at least 18µs pk-pk at frequencies below 10Hz.

Exchange Protocol on the C/I channel

Exchange of information in the C/I channel runs as follows:

Two devices connected on a GCI channel send each other a permanent four bit command code in the C/I field. The same code is sent at a 8kHz frequency as long as the content of the internal C/I register remains unchanged.

Note: as for GCI definition, in case that a command code has to be executed twice, it is necessary that the device, that is sending the commands, sends, after the first code, a NOP before repeting the command for the second time.

When a change of C/I the command is initiated that is recognized by SID-GCI if detected in two consecutive frames.

ST5421 will interpret the new code and send the corresponding control instructions on the S line or switch a local function as long as the corresponding action is required.

An information change received from the S line or a local status change of SID-GCI set a new indication code on the C/I channel. The code is sent at least in 2 consecutive frames.

Table 2 gives the C/I codes meaning. C1 bit is first transmitted. Here after for each mode a list of recognized Control and Indicate codes is given.

TEM mode: Control

0000 (DR) : Deactivation Request
In the Power Up state, DR instruction can be used as a Deactivation Request instruction to force transmission of INFO0 on the S line.

0001 (PDN) : Power Down Request.
PDN instruction forces the device to the Power Down state after that DI (1111) has been sent in two consecutive frames.

0110 (NOP) : No operations.

1000 (AR8) : Activate Request Class 8.
AR8 instruction combines an Activation Request, which initiates the Activation Sequence on the line, and a request to attempt to access the transmit D channel in the high priority class at the S interface after its complete activation.
After activation of the S interface, AI8 indication is sent by ST5421. D channel access attempt is

Table 2: C/I Channel Coding

Code	TEM		LT/NT2		TES		NT1	
C1 C2 C3 C4	Ind.	Com.	Ind.	Com.	Ind.	Com.	Ind.	Com.
0000	DP	DR	TIM	PUP/DR	DP	PUP/DR	TIM	DR
0001	X	PDN	X	PDN	X	PDN	X	X
0010	X	X	X	X	X	X	X	X
0011	EOM	X	X	X	X	X	X	X
0100	EI	X	EI	X	EI	X	EI	FI2
0101	X	X	X	X	X	X	X	X
0110	X	NOP	X	NOP	X	NOP	X	NOP
0111	X	X	X	X	X	X	X	X
1000	AP	AR8	AP	AR	AP	AR	AP	AR
1001	CON	AR10	X	X	X	X	X	X
1010	X	ARL	X	ARL	X	ARL	X	ARL
1011	X	X	X	X	X	X	X	X
1100	AI8	X	AI	FI4	AI	X	AI	FI4
1101	AI10	X	X	X	X	X	X	X
1110	AIL	X	AIL	X	AIL	X	AIL	X
1111	DI	DC	DI	DC	DI	DC	DI	DC

(x) codes reserved

automatically processed for each HDLC frame to be transmitted without need for new Control Instruction.
Except for code EOM, any further indication change on C/I as CON or EI deactivates D channel access attempt at the S interface. A new AR8 instruction is needed to restart the procedure.
Note : A new AR8 instruction means that if the controller was already sending AR8, it has to change first the code sent to ie DC (1111) and after change again to AR8.

1001 (AR10) : Activate Request Class 10.
Same meaning as AR8 command but requesting access to transmit D channel with low priority class.
After activation of the S interface has been completed, AI10 indication is sent by SID-GCI.

1010 (ARL) : Activate Request Loopback.
ARL instruction operates a loopback of 2B + D channels from Bx input to Br output. It may be set when the device is either activated, in which case it is transparent (the composite signal is also transmitted to the line), or when it is deactivated in which case it is non transparent.
Any change from ARL to another C/I command clears the loopback.
When the complete loopback is activated, (AIL) code is sent by SID-GCI.

1111 (DC) : Deactivation Control.
DC instruction allows ST5421 to enter automatically the Power Down state if the S line is deactivated (DP sent by SID-GCI). When S line is not deactivated, DC has no effect.

TEM mode : Indication

0000 (DP) : Deactivation Pending Indication.
DP code indicates ST5421 is powered up and that no identified signal has been detected on the S line. DP indication is sent when one of the following events occur :
- Power Up has been completed and no signal is identified on the line,
- after a period of activity, INFO0 is detected on the S line,
- the device being in status F4, F5, F6, F7 or, F8, a DR instruction is issued.

0011 (EOM) : End of Message.
EOM indicates that the closing flag of a D channel message has been transmitted on S line indicating successfull completion of a packet sending. EOM is sent continuously until receiving of a new AR8 or AR10 command or line status change.
EOM code sending can be disabled via a Monitor channel instruction EID : (see table 3).

0100 (EI) : Error Indication.
EI indicates that a frame loss of has been detected on S line ; is sent when one of the following events occur :
- being in the F6 or F7 states, detection of a loss of frame, (jump to F8).

- being in the F7 state, receiving of INFO2, (jump to F6).

1000 (AP) : Activation Pending.
AP indicates that INFO2 (or INFO4) frames have been identified on the line.
AP indication is sent when one of the following events occur:
- being in F2 deactivated state, detection of INFO2 or INFO4.
- being in the loss framing state F8, detection of INFO2

1001 (CON) : Contention Indication
CON is sent when, during transmission of a packet in the D channel, a received E bit does not match the last transmitted D bit, indicating a lost collision.
D channel access attempt is deactivated at the S interface. A new AR8 or AR10 instruction is needed to restart the procedure.

1100 (AI8) : Activation Indication Class 8.
AI8 is sent when, following an AR8 instruction, the S line is completely activated (state F7). The D channel access procedure is set in the high priority class 8 (or 9).

1101 (AI10) : Activation Indication Class 10.
AI10 is sent when, following an AR10 instruction, the S line is completely activated. The D channel access procedure is set in the low priority class 10 (or 11).

1110 (AIL) : Activation Indication Loopback.
AIL indicates that the complete loopback requested by the instruction ARL is completed.

1111 (DI) : Deactivation Indication.
DI is sent at least in two consecutive frames when, being in the S line deactivated state (DP indication sent by SID-GCI) DC control instruction is received on C/I control channel.
After that, SID-GCI is automatically powered down.

TES mode : Control.

0000 (PUP/DR) : Power Up Request/Deactivation Request.
When in Power Down, Power Up instruction powers up the device in the configuration previously set. When in Power Up, PUP/DR can be used as a Deactivation Request instruction to force the transmission of INFO0 on the line.

0001 (PDN) : Power Down Request.
PDN instruction forces the device to the Power Down state.

0110 (NOP): Some as TEM

1000 (AR) : Activate Request.
AR instruction initiates the Activation Sequence on the line. It is recommended that an AR be delayed at least 2ms after the PUP instruction.

1010 (ARL) : Activate Request Loopback.
Identical to TEM mode.

1111 (DC) : Deactivation Control.
DC instruction allows ST5421 to enter automatically the Power Down state if the S line is deactivated (DI sent by SID-GCI). When S line is not deactivated, DC has no effect.

TES mode : Indication.

0000 (DP) : Deactivation Pending.
DP code indicates ST5421 has been just powered up and no signal has been identified on the line.

0100 (EI) : Error Indication.
Identical to TEM mode.

1000 (AP) : Activation Pending.
Identical to TEM mode.

1100 (AI) : Activation Indication.
AI is sent when, following an AR instruction, the S line is completely activated in state F7.

1110 (AIL) : Activation Indication Loopback.
Identical to TEM mode.

1111 (DI) : Deactivation indication.
DI indication is sent when one of the following events occur:
- After a period of activity, INFO0 is detected on the S line,
- the device beeing in status F4, F5, F6, F7 or F8, DR instructions is issued.

NT1 mode : Control.

0000 (DR) : Deactivation Request.
DR command forces ST5421 through the appropriate deactivation sequence where INFO0 is sent on the line. The device remains in the Power Up state. DI indication is sent.

0100 (FI2) : Force Info 2
Being in the activated state G3, FI2 instruction forces the appropriate sequence to send INFO2 on the line. If the S line is not completely activated, FI2 instruction has no effect.

0110 (NOP): Some as TEM

1000 (AR) : Activation Request.
Being in the inactive Power Up state, sending INFO0, AR instruction forces SID-GCI through the appropriate sequence to send INFO2 on the line. It is recommended that an AR instruction be delayed at least 2ms after setting the GCI clocks.

1010 (ARL): Activate Request Loopback.
Identical to TEM mode.

1100 (FI4) : Force Info 4.
An activation Request being in progress, FI4 instruction allows SID-GCI through the appropriate sequence to send INFO4 on the line.

1111 (DC) : Deactivation Control.
DC instruction has no effect on SID-GCI.

NT1 mode : Indication.

0000 (TIM) : Timing Requested.
Being in Power down state, the LSD- output is pulled low to indicate that the far-end is attempting to activate the S interface. The device requests GCI clock signals. Receiving of GCI clocks powers up the SID-GCI, LSD- is freed, and TIM code is sent on the C/I channel.

0100 (EI) : Error Indication.
EI code indicates that a loss of frame has been detected on the S line, ST5421 being previously activated.

1000 (AP) : Activation Pending.
AP code indicates that INFO1 frames have been identified of the line. The device is waiting for an activate request to send INFO2.

1100 (AI) : Activation Indication.
AI code indicates that the S line is activated. That means it is receiving INFO3.

1111 (DI) : Deactivation Indication.
DI code indicates S line is completely deactivated: the device can be powered down switching off GCI clocks.

1110 (AIL) : Activation Indication Loopback.
Identical to TEM mode.

NT2 mode : Control.

0000 (PUP/DR) Power Up Request/Deactivation Request.
When in Power Down state, PUP code powers up the device in the NT2 configuration previously selected. When in Power Up state DR code forces the appropriate deactivation sequence where INFO0 is sent on the line. SID-GCI remains in Power Up state.

0001 (PDN) : Power Down Request.
Identical to TES mode.

0110 (NOP): Some as TEM

1000 (AR) : Activation Request.
After a PUP instruction, AR forces the appropriate sequence to send INFO2 on the line. It is recommended that AR instruction is sent after receiving TIM indication..
1010 (ARL) : Activation Request Loopback.
Identical to TEM mode.

1100 (FI4) : Force Info 4.
An Activation Request being in progress, FI4 instruction puts ST5421 through the appropriate sequence to send INFO4 on the line.

1111 (DC) : Deactivation Control.
The DC instruction allows to enter the power down state if the S line is deactivated.
DC control has no effect if SID-GCI not sending DI indication.

NT2 mode : Indication.

0000 (TIM) : Timing Requested.
Being in Power down state, LSD- output is pulled low to indicate that far-end is attempting to activate the interface. SID-GCI requests GCI clocks followed by a PUP instruction. After receiving, LSD- is freed and TIM is sent on C/I channel.

0100 (EI) : Error Indication.
Identical to NT1 mode.

1000 (AP) : Activation Pending.
Identical to NT1 mode.

1101 (AI) : Activation Indication.
Identical to NT1 mode.

1110 (AIL) : Activation Indication Loopback.
Identical to TEM mode.

1111 (DI) : Deactivation Indication.
The DI code indicates that the S line is completely deactivated.

EXCHANGE PROTOCOL ON M CHANNEL

Protocol allows a bidirectional transfer of bytes between SID-GCI and a Controller (for example ST5451) with an acknowledgement at each received byte.

Write cycle.
The Controller sends to ST5421 control instruction(s) coded on a single byte. It is possible but optional to write several control instructions in a single message. Control instruction bytes are structured as defined in Table 3.

Read cycle.
When a new validated S1 or Q message is received from the line, the device send a single byte message as defined in table 4. If a new message is received from the S line before the previous is acknowledged by the controller end, this new message is lost.

Exchange protocol.
The exchange protocol is identical for both directions.

The sender uses E bit to indicate that it is sending a M byte while the receiver uses A bit to acknowledge the received byte.

When no message is transferred, E bit and A bit are forced to inactive state (i.e. high impedance).

A transmission is initialized by the sender setting E bit in active state and sending the first byte on M channel in the same frame. Transmission of a message is allowed only if A bit received has been detected inactive in the last two frames.

When the receiver is ready, it validates the received byte internally when it has been detected identical in two consecutive frames. Then, the receiver set first A bit from inactive to active state; it is the pre-acknowledgement, and maintain A bit active at least in the following frame, it is the acknowledgement.
If validation is not possible, the two last bytes received not identical, the receiver abort the message by setting A bit active for one frame only.

A second M byte may be transmitted by the sender turning E bit from active to inactive state and sending the byte in the same frame. The E bit is set inactive for one frame only. If it remains inactive more than one frame, it is an end of message. The second byte may be transmitted only after receiving the pre-acknowledgement of the previous byte (see timing diagram).

The receiver validates the current received byte as for the first one and then set A bit in the next two frames first from active to inactive state (pre-acknowledgement) and from inactive to active (acknowledgement). If the receiver cannot validate (the two bytes received are not identical) it pre-acknowledges normally but let A bit in the inactive state in the next frame which indicates an abort request.

If a message is aborted, ST5421 sends again the complete message until receiving acknowledgement.
A received message is acknowledged or aborted without flow Control.
Figure 4 gives the timing of a write cycle. The most significant bit of a Monitor byte is sent first of the M channel. E & A bits are active low and inactive state on Br is high impedance.

Figure 4: Monitor messaging

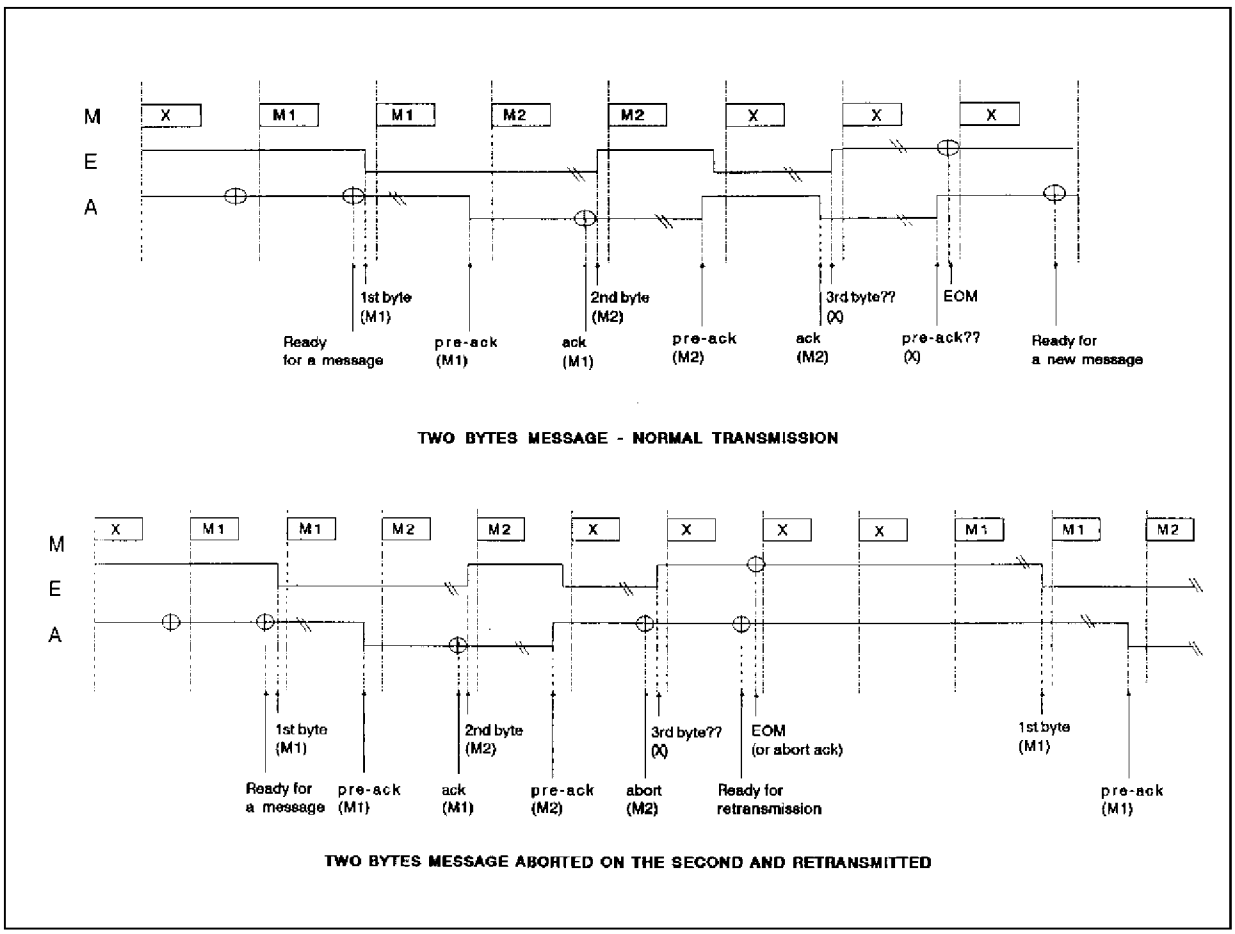


Table 3: Monitor Channel Instruction

Functions	Mnemonic	Bit Number 7	6	5	4	3	2	1	0
Device Mode:									
NT Mode Adaptive Sampling (*)	NTA	0	0	0	0	0	1	0	0
NT Mode Fixed Sampling	NTF	0	0	0	0	0	1	0	1
TE Slave Mode (slave-slave)	TES	0	0	0	0	0	1	1	0
Monitoring Mode Activation	MMA	0	0	0	1	1	1	1	1
TE Master Mode	TEM	0	0	0	0	0	1	1	1
B Channel Configuration:									
B Channel Mapped Direct (*)	BDIR	0	0	0	0	1	1	0	0
B Channel Exchanged	BEX	0	0	0	0	1	1	0	1
B1 Channel Enabled (*)	B1E	0	0	0	1	0	1	0	0
B1 Channel Disabled	B1D	0	0	0	1	0	1	0	1
B2 Channel Enabled (*)	B2E	0	0	0	1	0	1	1	0
B2 Channel Disabled	B2D	0	0	0	1	0	1	1	1
End of Messages Indication:									
EOM Indication Enabled (*)	EIE	0	0	0	1	0	0	0	1
EOM Indication Disabled	EID	0	0	0	1	0	0	0	0
Multiframe Processing:									
Multiframe Disabled (*)	MID	0	0	0	1	0	0	1	1
Multiframe Enabled	MIE	0	0	0	1	0	0	1	0
Disable Three Time Checking	DIS3X	0	0	1	0	1	0	0	1
Enable Three Time Checking (*)	EN3X	0	0	1	0	1	0	0	0
Write Multiframe Message	MFT	0	0	1	1	M1	M2	M3	M4
Loopback Test Mode:									
Clear All loopbacks (*)	CAL	0	0	0	1	1	0	1	1
Loopback B1 on Line Enabled	LB1E	0	0	0	1	1	0	0	0
Loopback B2 on Line Enabled	LB2E	0	0	0	1	1	0	0	1
Loopback 2B+D Enabled (1)	LBS	0	0	0	1	1	0	1	0
Loopback B1 on GCI Enabled	LBB1E	0	0	0	1	1	1	0	0
Loopback B2 on GCI Enabled	LBB2E	0	0	0	1	1	1	0	1

(1) alternate command instruction to ARL (C/I code); but without any status indication pending.
(*) initial state following Power on initialization

Table 4: Monitor Status Messages

Functions	Mnemonic	Bit Number 7	6	5	4	3	2	1	0
Multiframe Receive Register	MFR	0	0	1	1	M1	M2	M3	M4

Monitor channel code description:
Monitor channel code list is given in table 3 and 4.

Device mode.

NTA : NT mode Adaptive sampling.
In NT mode, adaptive sampling should be selected when the device is an NT equipment connected on any wiring configuration up to the maximum specified length for operation. Multiple Terminals, if required, must be grouped within approximately 50 meters one from each other (depending on cable capacitance as indicated in I.430). Transmit section of SID-GCI is phased locked to GCI FSa source.

NTF : NT mode fixed sampling.
In NT mode, fixed sampling should be selected when the device is in a NT equipment connected on a passive bus wiring configuration up to approximately 200 meters in length depending on cable type. In this mode the receiver DPLL is disabled and sampling of the received symbols is fixed to enable multiple Terminals (nominally up to 8) to be connected anywhere along the passive bus. Transmit and Receive section is phased locked to GCI FSa source.

TES : TE mode connected on the T interface.
This mode should be selected when the device is used on the T interface side of an NT2 equipment. I.430 circuitry operates as in TE mode but GCI interface is driven by BCLK and FSa sources providing a slave-slave configuration.

Data buffers and a clock resynchronizer enable

the GCI to function with FSa and BCLK jittering sources. No phase relationship is needed between the line recovered clocks and GCI.

A 1536kHz clock signal output phased locked to the Recevied line signal is delivered on CLK.

CLK output signal is generated only when ST5421 if fully activated (state F7) and no clock signal is detected on that pin by the device during his own selected GCI channel.
Otherwise CLK output remains high impedance.

Note: CLK output is activated immediately on the first bit of the B2 channel (GCI side) and is deactivated immediately if SID-GCI leaves F7 state.

D channel access Control circuitry is disabled. i.e. D channel data at Bx input is continuously transmitted to the line; there is no monitoring of the D echo channel from the network direction.

MMA : Monitoring mode activation.
When ST5421 is configured in TE mode by means of pins M0, M1, the MMA instruction allows to receive and activate on INFO3 frames, while remaining the master of GCI. That configuration can be used for applications such as monitoring the outputs of TEs on a passive bus.
The received 2B+D can then be passively monitored (the line transmit LO+,LO- would not be connected).

TEM : TE Master Mode.
When ST5421 is in TE configuration by means of pins M0, M1, and in the Monitoring Mode Activation by means of the instruction MMA, the TEM instruction set back SID-GCI in the normal TE Master mode.

B channels configuration.

BDIR/BEX B1E/B1D B2E/B2D
BDIR and BEX instructions provide for the exchange of data between the B1 and B2 channels. (Note: when enabling a B channel in conjuction with the BEX command, channels is referenced at the CGI).
When either or both B channels are disabled by means of the B1D or B2D instruction, binary 1 are transmitted on the line regardless of Bx input while Br output is in high impedance state. When enabled by means of B1E and B2E instructions, B channel are transparently transmitted.

End of message indication.

EID/EIE
C/I channel End Of Message code sending can be enabled with instruction EIE and disabled by means of EID.

Multiframe processing.

MFT/MFR/MIE/MID
In the Transmit direction, with the device in TEM or TES mode, data entered in bit positions M1, M2, M3 and M4 of instruction MFT is transmitted to the NT in multiframe bit positions Q1, Q2, Q3 and Q4 respectively. With the device in NT mode, data entered in the M bit positions is transmitted to the TE in multiframe bit positions S11, S12, S13 and S14 respectively. In the Receive direction, when the Multiframe receive data buffer requires servicing, the MFR (see table 4) status message is autonomously sent with M1, M2, M3 and M4 bits representing Q1, Q2, Q3 and Q4 or S11, S12, S13 and S14 bits received from the multiframe respectively.

Multiframe Structure and transmission protocol on the line comply with the ANSI US Standard T1.605.1989. "Basic Access Interface for S and T Reference points - Layer 1 specification".

Multiframe message exchange can be supported by SID-GCI when the line is synchronized : states F6 & F7 in TEM or TES modes and state G3 in NT modes.

The multiframe channel processing must be enabled by an MIE instruction to use these channels.

DIS3X/EN3X

When EN3X is set, a new Multiframe message received from the line is checked and transferred on the M channel when received three times identical.
When DIS3X is set, Multiframe messages are transferred tranparently every superframe.

Loopback test modes

CAL/LBS/LB1E/LB2E/LBB1E/LBB2E
LB1E and LB2E instructions turn each individual B channel from the line receive input back to the line transmit output. They may be set separately or together.
LBB1E and LBB2E instructions turn each individual B channel from GCI input to the GCI output. They may be set separately or together.
CAL instruction clears both loopbacks.
It is not allowed to set or clear a LB1, LB2, LBB1 or LBB2 loopback while a complete loopback is set by means of the C/I instruction ARL. LBS can be used as an alternate command to ARL.

Activation/Deactivation

In NT configuration :

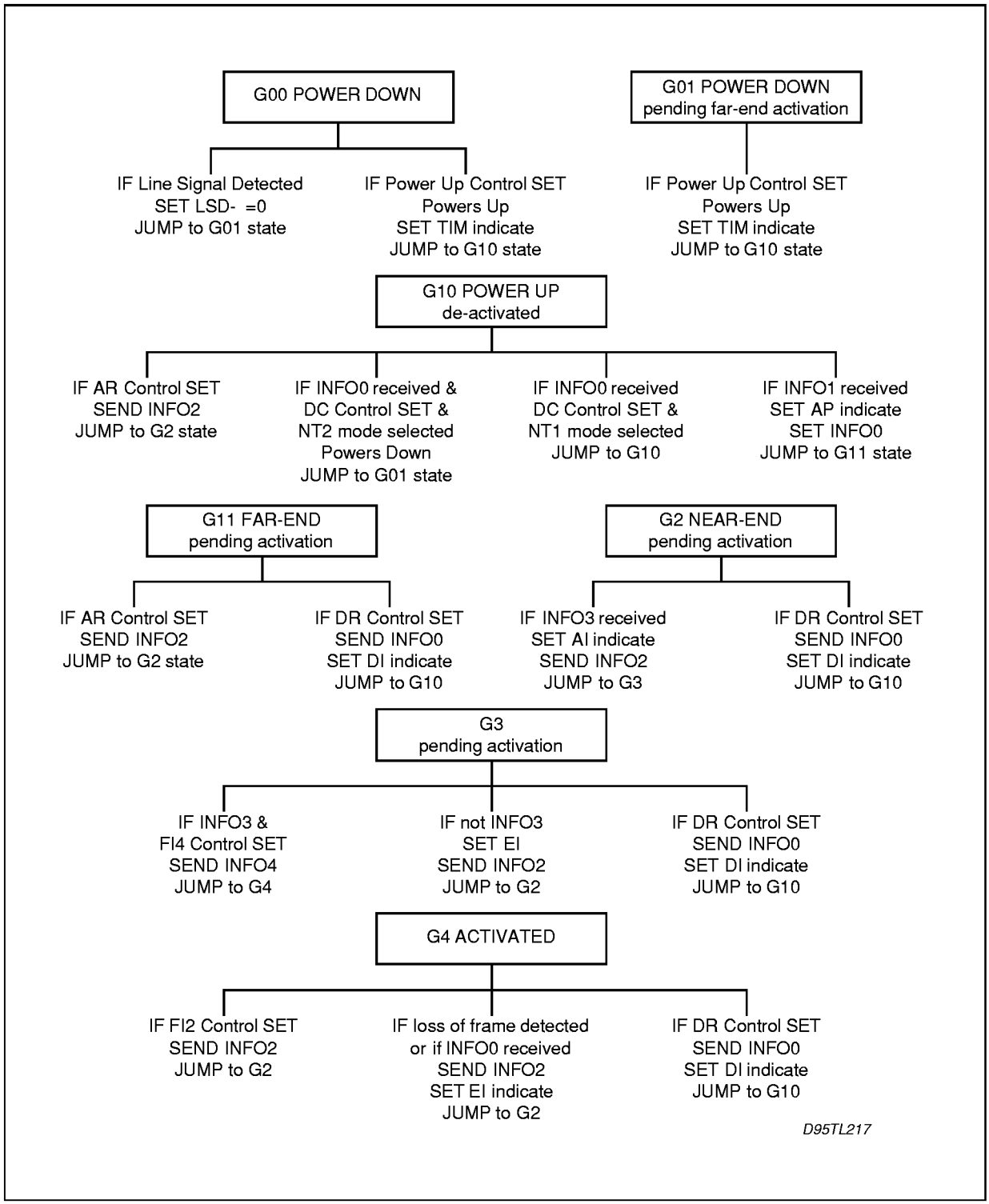
After Power on initialization, ST5421 can be con-

figured in NT1 or NT2 mode, by means of pins and register programming. In NT1, SID-GCI is powered up directly by receiving the GCI clocks on BCLK and FSa inputs. In NT2 mode, the device is powered up by means of PUP code on the C/I Control channel.

Activation may be initiated from either end of the loop.

To operate an activation from the Network, ST5421 must be first powered up by the appropriate procedure followed at least 2ms later by an AR instruction on the C/I channel. Network timing,

Figure 5: Activation Procedure in GCI mode, NT Selected.



FSa, BCLK and MCLK must be present at this time. When activation is initiated by the far-end, SID-GCI being in the Power Down state, a Line Signal Detector circuit pulls low LSD- pin, which can be used to wake up the system. A power Up procedure must be then be issued allowing identification of received signal ie, INFO1 or INFO2. The appropriate procedure is then followed according to I.430.

I.430 recommends that 2 Timers should be available in an NT. An Activation Request should be associated with the start of an external Timer 1 if required. Timer 1 should be stopped when the AI indication is generated following successful activation. If Timer 1 expires before AI is generated, however, Control instruction DR should be written to the device to force deactivation. Timer 2 which is specified to prevent unintentional re-activation, is not required since ST5421 can uniquely recognize INFO1 frames.
Two extra codes are needed for NT1 application: FI4 indicates to the SID-GCI that the U line is activated and allows completion of activation by sending INFO4. FI2 indicates to SID-GCI that the U line has lost synchronization and requests sending of INFO2.

In TEM or TES configuration :
After Power on initialization, ST5421 can be configured in TE or TES power down mode, depending on pins and register configuration setting. In TEM mode, SID-GCI is powered up by pulling low the Bx input. SID-GCI reacts by sending GCI free-running clocks. In TES mode, the SID-GCI is powered up by means of the PUP code on the C/I Control channel.

Activation may be initiated from either end of the loop. To operate an activation from the Terminal, the device must be first powered up by the appropriate procedure followed at least 2ms later by an AR instruction on the C/I channel. When activation is initiated by the far-end, SID-GCI being in the Power Down state, a Line Signal Detector Circuit pulls low the LSD- pin, which can be used to wake up the system. A Power Up procedure must then be issued allowing identification of received signal ie, INFO2. The appropriate procedure is then followed according to I.430.

Figure 6: Activation Procedure in GCI mode, TE Selected

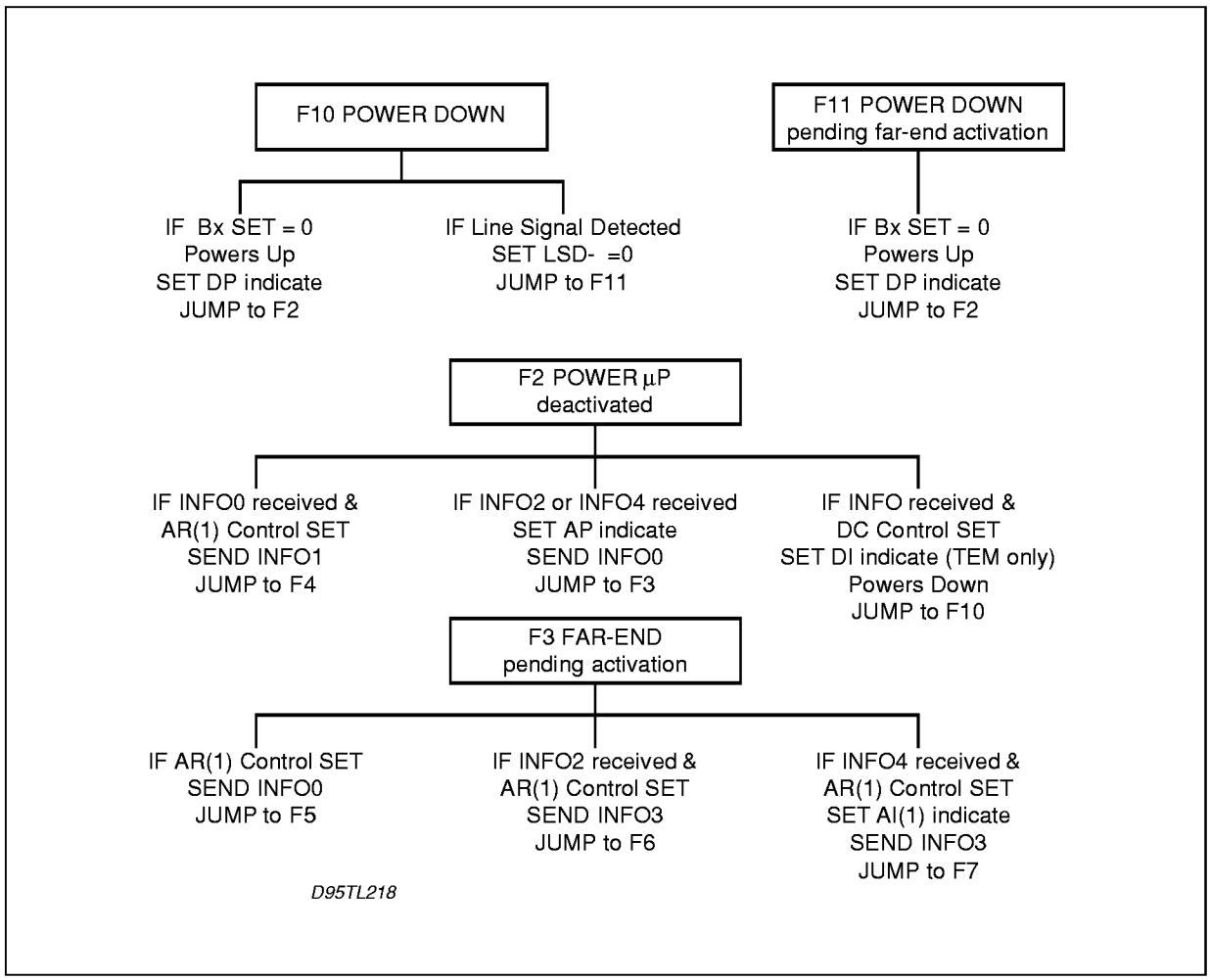
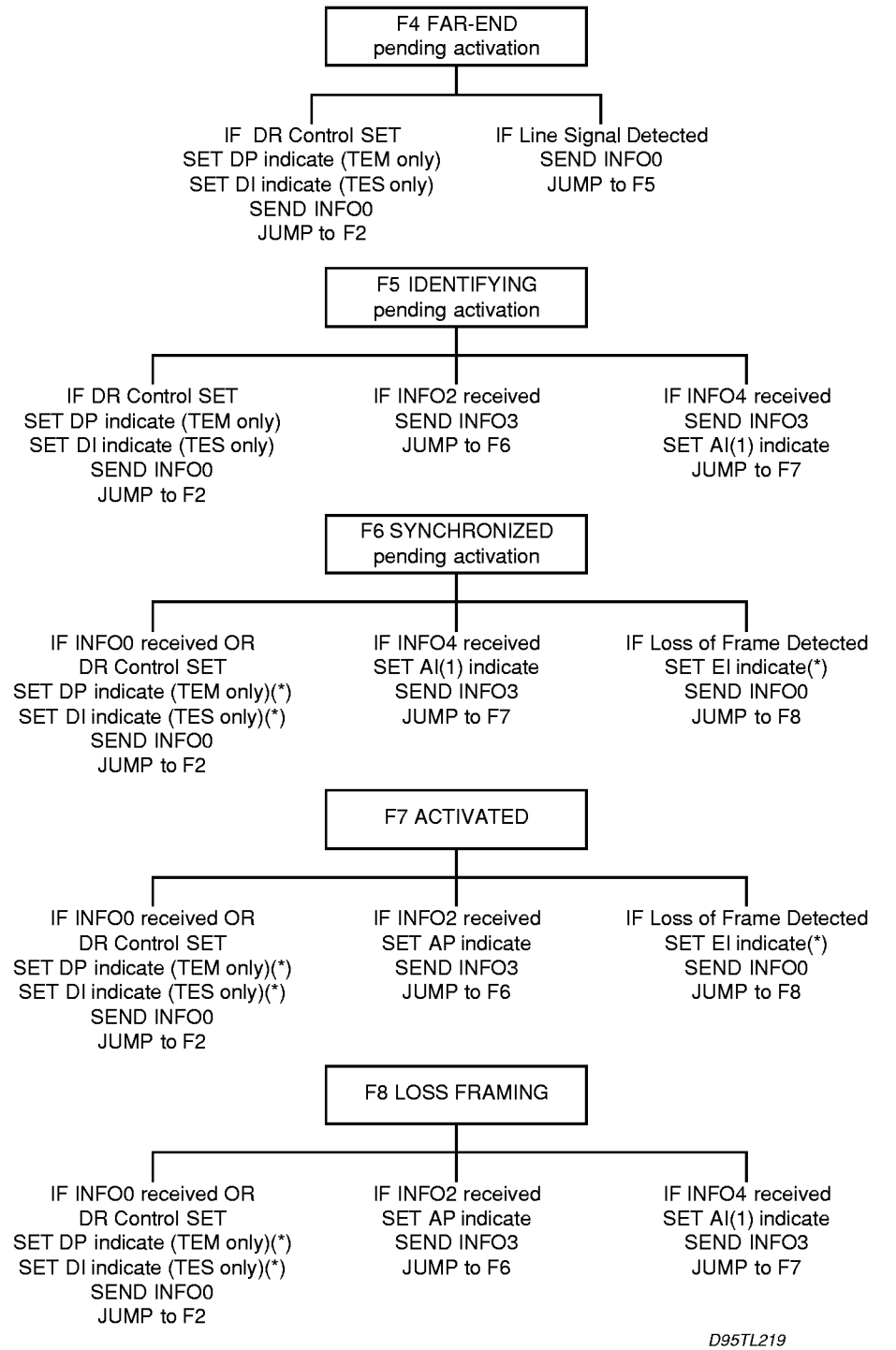


Figure 6: Continued



(1) AR means: AR, AR8 or AR10 while AI means: AI, AI8 or AI18 depending on configuration

(*) In these cases, the indications DP, DI and EI are preceded by an AI indication that stays for a period of time ≤1ms

I.430 recommends that a Timer should be available in a TE. An Activation Request to the SID-GCI should be associated with the start of an external Timer 3 if required.Timer 3 should be stopped when the AI indication is generated following successful activation. Timer 3 expires before AI, AI8 or AI10 is generated, however, Control instruction DR should be written to the device to force de-activation.

D CHANNEL ACCESS IN TEM MODE

A controller device requiring to start transmission of a packet on the line should first prepare the complete message such that the opening Flag is ready to be shifted accross GCI. A Control Instruction AR8 or AR10 will initiate first the Activation Sequence on the line until activation has been completed and then the D channel access sequence according to Priority Class 1 (signalling) or Priority Class 2 (Data packet) respectively.

After line activation, AI8 (or AI10) indication is sent from SID-GCI. Then, DEN output immediately enables to prefetch the opening flag from the controller device into the SID-GCI D channel buffer. Meanwhile, the Priority Counter checks that no other TE connected to the S interface is transmitting in the D channel. This is assured by counting consecutive "1"s in the E bit position of frames received from the NT and comparing the value with the current priority level as specified by I.430. If another TE is active in the D channel, DEN pulses are inhibited once the Opening Flag is in the Transmit buffer to prevent further fetching of Transmit data from the Controller until D channel access is achieved.

As soon as the required number of consecutive E bit "1"s has been counted, the leading 0 of the opening flag is transmitted in the next D bit position to the NT. Then, DEN pulses are re-enabled in order to get new D channel bits. No other instructions are necessary for local flow control between controller and ST5421.

During transmission in the D channel, SID-GCI continues to compare each E bit with the D bit previously transmitted before proceeding to send the next. In case of mis-match, a contention for the previous D bit is assumed to have been won by another TE. Transmission of the current packet therefore ceases and "1"s are transmitted in all following D bit positions. Status indication CON is sent to the controller on C/I channel. DEN output pulses are again inhibited, and D channel access sequence is disabled.

In order to retransmit the lost frame, the controller must begin as before sending a new AR8 (or AR10) ; it has to change first the code sent (ie DI) and after change again to AR8. Successful sending of a transmit frame is detected when the closing Flag is transmitted in the D channel. "1"s are then transmitted in the following D bit positions.

If enabled by the Control Instruction EIE, indication EOM is sent to indicate the End of message.

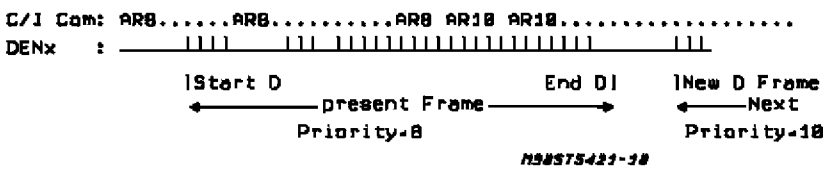
After sending of a transmit frame successfull, SID GCI will automatically perform a new D access sequence if it's still receiving AR8 or AR10 command on C/I channel, otherwise no D access sequence will be done until reception of AR8 or AR10 command.

Any indication change on the C/I channel except EOM indicates deactivation of the D channel access sequence and a new AR8 (or AR10) is needed to restart the procedure.

Note: Users willing to control the D channel access, can use this procedure:
Send AR8 or AR10 until receiving DENx, then remove ARx command code and replace it by an another command (ie DI that is equivalent to a NOP operation if the device is full_activated). At the end of a D frame EOM Indication is received (if EIE is set); when a new D message is prepared an ask for a new D channel access by AR8 or AR10 can be sent.

Users that want to discriminate consecutive D channel access with EOM Indication, are suggested to remove EOM Indication, between 2 D frames, to be able to separate the 2 messages EOM: With the following method: send AR8 (AR10) continuously, until receiving EOM Indication, then send ONCE AR8~ [0111] (AR10~ [0110]) on C/I channel and continue to send the previous code AR8 (AR10); this AR8~ (AR10~) is a kind of EOM aknowledge: the device detect a 'new' primitive AR8 (AR10), stop EOM Indication and replace it by AI8 or AI10 if ST5421 is still full activated.

For application with automatic D channel access and wanting to change the priority class (8 or 10) for D channel, they can use the following procedure:
Assuming that the present D frame is priority class 8 and that the next D frame will be priority class 10, users can change AR8 code to AR10 as soon as they are sure that the present D frame is started, by controlling DENx, anticipating the next D messages before the closing flag of the present D frame. When the automatic D channel access will be performed for next D message, the D channel request will be done with the desired priority class. (see figure below).



MULTIFRAME MAINTENANCE CHANNELS (S1 AND Q WORDS)

Each direction of transmission across the S interface includes a low-speed (800 b/s) channel for loop maintenance accessed via the monitor channel of ST5421. A multiframe structure, consisting of 20 frames on the S interface, is used to synchronize these channels and convey messages coded into 4-bit words, see Table 5. One word is transmitted downstream (NT-to-TE) in the S1 channel, and one word is transmitted upstream (TE-to-NT) in the Q channel every multiframe.

When the device is in NT mode, the MIE command enables both the transmission of the multiframe identification algorithm (reversal of the FA/N bits every 5th frame and M bit set = 1 every 20th frame) and enables the MFR message. The algorithm is present during INFO2 and INFO4 frames. In TE modes this command only enables the MFR message since the device will always search for and synchronize to the multiframing identification bits if NT is sending them. In all modes, at the end of each multiframe the received 4-bit word is decoded to determine if it should generate an MFR interrupt immediately, or be stored until 3 consecutive multiframes have contained the same 4-bit word before a MFR message is generated. Table 5 lists the codes which are 3-times checked. Note, however, that no other action is taken by the ST5421 in response to received codes (e.g. loop-backs are not automotically implemented); the external controller must take the necessary action. This provides the freedom to implement maintenance functions without constrains from the device, and to utilise the unassigned codes for other functions.
It is possible to disable the checking algorithm by setting DIS3X instruction on M channel. There, Multiframe words are transferred transparently on M channel.

The MID command disables the transmission of the Multiframe identification algorithm in NT mode and disables the MFR message in both NT and TE modes. Both the MIE and MID commands can only be written to the device when it is deactivated (either powered-up or powered-down). The Multiframe Transmit Register should also be loaded with the appropriate "idle" messages, by means of an MFT instruction, prior to activation.

Table 5: Codes for Q and S1 channel messages

Message (1)	NT to TE					TE to NT				
	Received at TE				Number of Repetitions Before MFR message (EN3X set)	Received at NT				Number of Repetitions Before MFR message (EN3X set)
	S11	S12	S13	S14		Q1	Q2	Q3	Q4	
Idle (Normal)	0	0	0	0	3	1	1	1	1	3
Loss-of-Power Indication	1	1	1	1	1	0	0	0	0	1
STP Pass	0	0	1	0	3	--	--	--	--	--
STF Fail	0	0	0	1	3	--	--	--	--	--
ST Request (3)	--	--	--	--	--	0	0	0	1	3
STI Indication	0	1	1	1	3	--	--	--	--	--
DTSE-IN	1	0	0	0	1	--	--	--	--	--
DTSE-OUT	0	1	0	0	1	--	--	--	--	--
DTSE-IN & OUT	1	1	0	0	1	--	--	--	--	--
LB1 Request	--	--	--	--	--	0	1	1	1	3
LB1/Indication	1	1	0	1	3	--	--	--	--	--
LB2 Request	--	--	--	--	--	1	0	1	1	3
LB2/Indication	1	0	1	1	3	--	--	--	--	--
LB1/2Request (2)	--	--	--	--	--	0	0	1	1	3
LB1/2Indication	1	0	0	1	3	--	--	--	--	--
Loss-of-Received Signal Indication	1	0	1	0	3	--	--	--	--	--
Unassigned	All other codes				1	All other codes				1

Notes:
(1) No autonomous action is taken by ST5421 in response to received messages. Where appropriate, the external controller must respond with a command or other action.
(2) The code "0011" will be received by an NT1 when the LB1 and LB2 requests are transmitted by two different TEs (NT2s) on a Passive Bus.
(3) The code "0001" will be received by an NT1 when ST Request and any other code (except LP) is sent simultaneously by two or more TEs on a Passive Bus.

Figure 7: ISDN Telephone Set Application (non isolated)

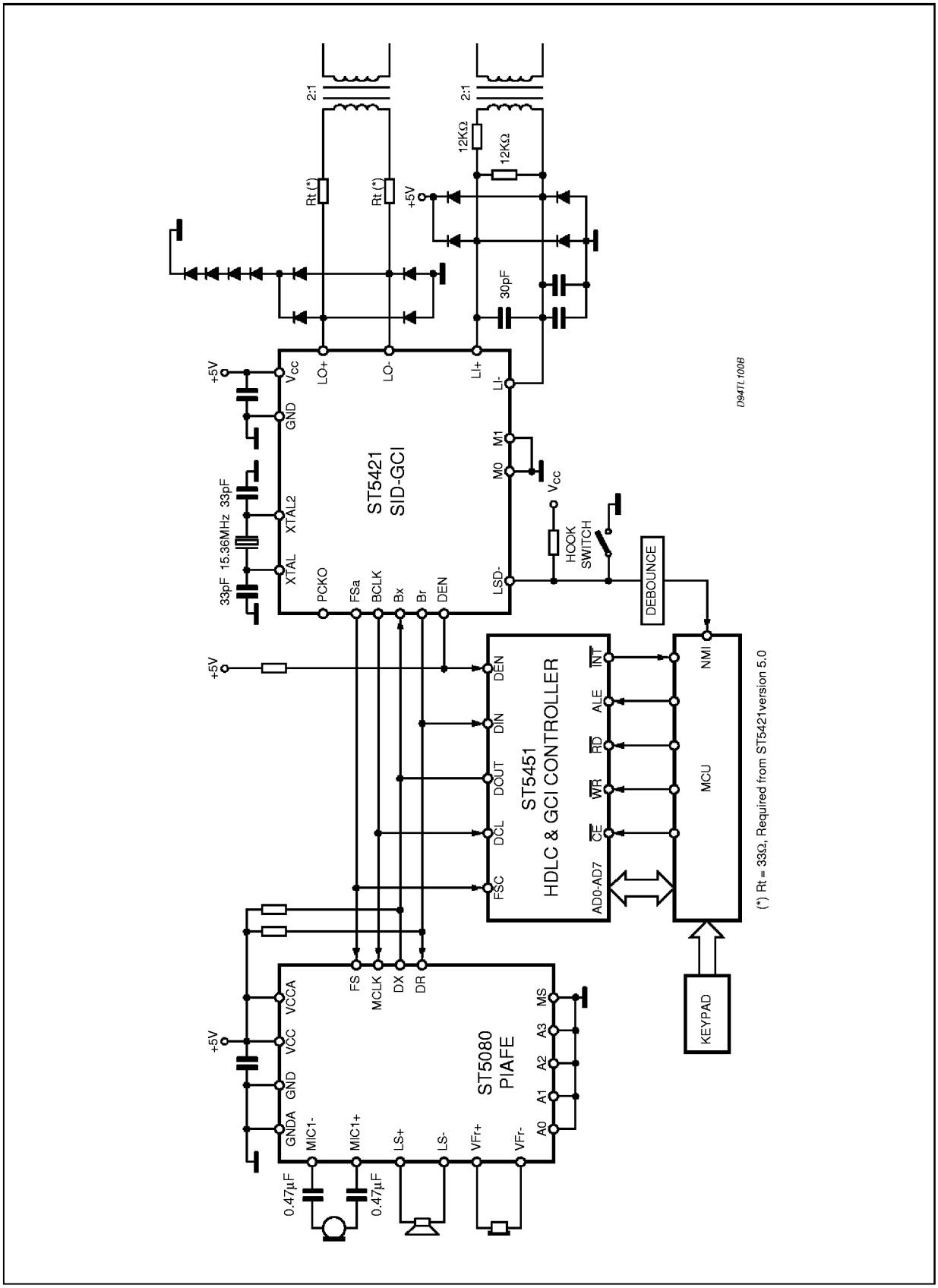
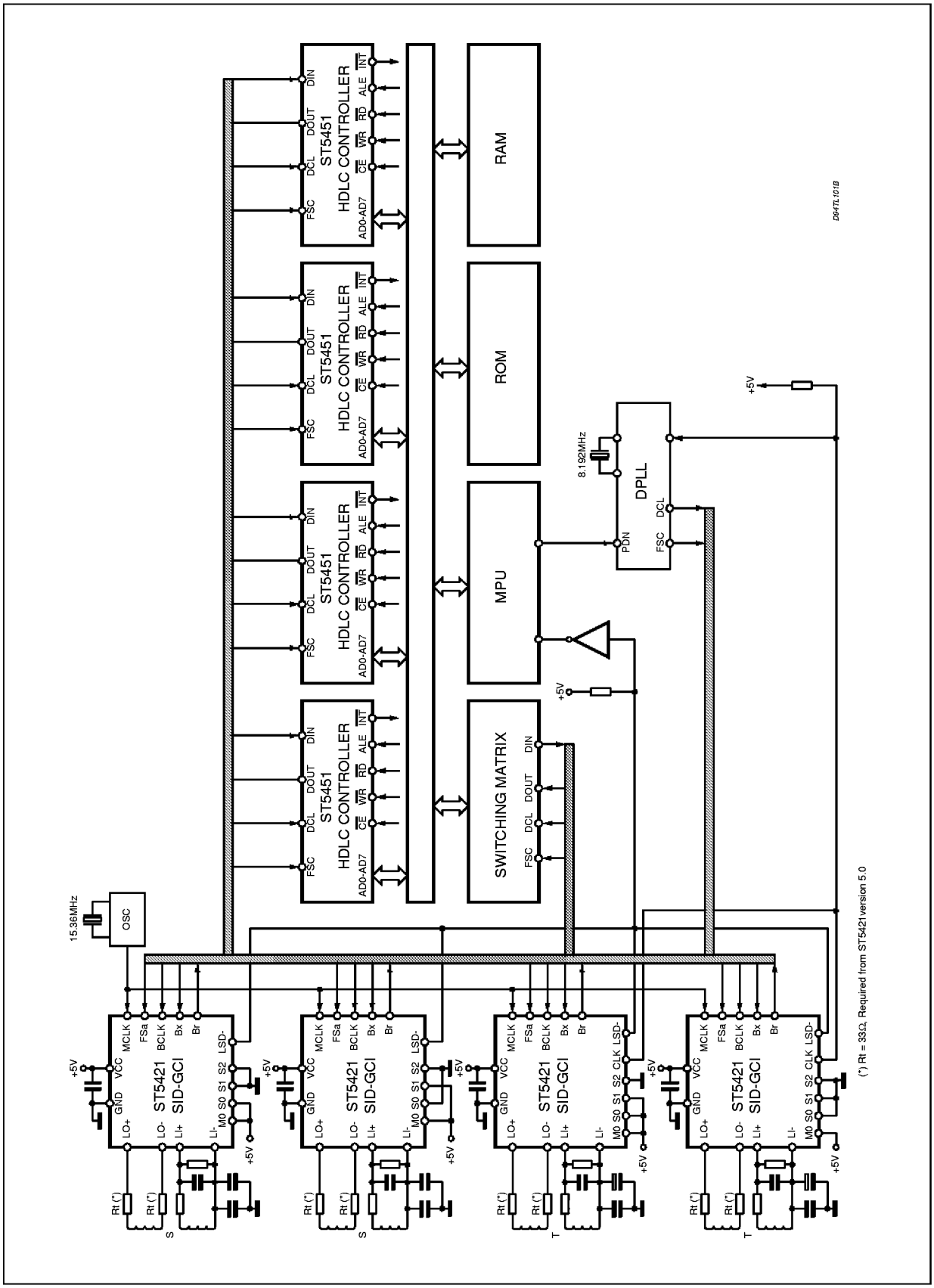


Figure 8: NT2 Application GCI Compatible



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
V_{CC} to GND	7	V
Voltage at Bx, Br	V_{CC} + 1 to GND - 1	V
Voltage at any Digital Input (except Bx)	V_{CC} + 1 to GND - 1	V
Current at any Digital Input (except Br)	± 50	mA
Current at Lo	± 100	mA
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering 10s)	300	°C

ELECTRICAL CHARACTERISTICS (unless specified otherwise: V_{CC} = 5V ±5%, T_A = 0 °C to 70°C; typical characteristics are specified at V_{CC} = 5V, T_A = 25°C. All signals are referenced to GND).

DIGITAL INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All Digital Inputs			0.8	V
V_{IH}	Input High Voltage	All Digital Inputs	2.2			V
V_{ILX}	Input Low Voltage	MCLK/XTAL input			0.5	V
V_{IHX}	Input High Voltage	MCLK/XTAL input	V_{CC}-0.5			V
V_{OL}	Output Low Voltage	Br: I_L = 3.2 mA All other Digital Outputs: I_L = ±1mA			0.4	V
V_{OH}	Output High Voltage	Br: I_L = 3.2 mA All other Digital Outputs: I_L = ±1mA	2.4 2.4			V V
I_{IL}	Input Low Current	Any Digital Input, GND < VIN < V_{IL}	-10		+10	µA
I_{IH}	Input High Current	Any Digital Input, VIH < V_{IN} < V_{CC}	-10		+10	µA
I_{OZ}	Output Current in HIGH Impedance (tri-state)	All Digital Tri-state I/Os	-10		+10	µA

LINE INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{LI}	Differential Input Resistance	GND < LI_+, LI- < V_{CC}	200			kΩ
C_{LLO}	Load Capacitance	From LO+ to LO-			200	pF
	Transmit Pullse Amplitude	R1 = 212Ω between LO+ and LO- (1)	1.484	1.585	1.696	Vpk
	Transmite Pulse Unbalance	O+ relative to O-			5	%
	Input Amplitude	Differential Between LI+ and LI-	±175			mV
V_{OS}	Differential Offset Voltage at L_{O+}, L_{O-}	Driving Binary 1s, 220Ω between LO+ and LO-	-20		20	mV

POWER DISSIPATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{cc0}	Power Down Current	All Outputs Open-circuit			900	µA
I_{ccnt}	Active Current (2)	NT/TES not transmitting		12	13	mA
I_{ccntt}	Active Current (3)	NT/TES transmitting			21	mA
I_{ccte}	Active Current (2)	TEM not transmitting		17	18	mA
I_{cctet}	Active Current (3)	TEM transmitting			26	mA

(1) This specification garanties compliance with CCITT1430 recommendation concerning the pulse templates. Winding resistors for the transformer is assumed to be represented by an extra 12Ω load added to the 200Ω corresponding to the 50Ω load reflected back through the 1:2 transformer.

(2) Measured with an external 15.36MHz clock applied on pin XTAL1, XTAL2 being left unconnected.

(3) Same condition as in (2) assuming worst case line current on 50Ω.

ELECTRICAL CHARACTERISTICS (continued)

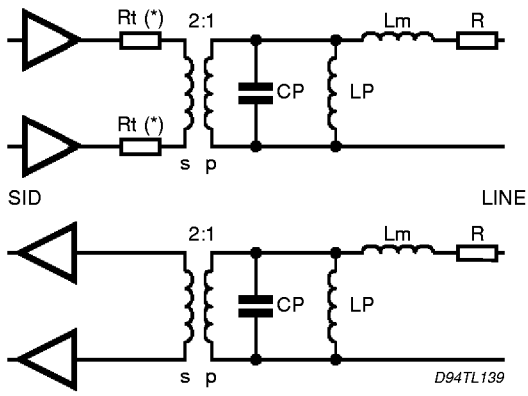
MASTERCLOCK

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	MCLK Frequency			15.36		MHz
	MCLK Frequency Tolerance		-100		100	ppm
	MCLK Input Clock Jitter				50	ns pk-pk
	Timing Recovery Jitter	BCLK Output Relative to MCLK at TE	-130		130	ns
t_{MH}, t_{ML}	Clock Pulse width High and Low of MCLK	$V_{IH} = V_{CC}$ -0.5V, V_{IL} = 0.5V	20			ns
t_{MR}, t_{MF}	Rise Time and Fall Time of MCLK	Used as a logical input			10	ns

TRANSFORMER MODEL (all values are to be measured at 10kHz)

		Min.	Typ.	Max.	Unit
1:N	Primary to Secondary Turn Ratio	1.98	2	2.02	%
Rp	Primary Winding Resistance		2		Ω
Rs	Secondary Winding Resistance		4		Ω
R	Primary Total Resistance		3		Ω
Lp	Primary Inductance	22	30	37.5	mH
Lm	Primary Inductance with Secondary Shorted		16	20	mH
Cp	Primary Capacitance with Secondary Open			25	pF

Figure 9: Transmit & Receive Transformer Model

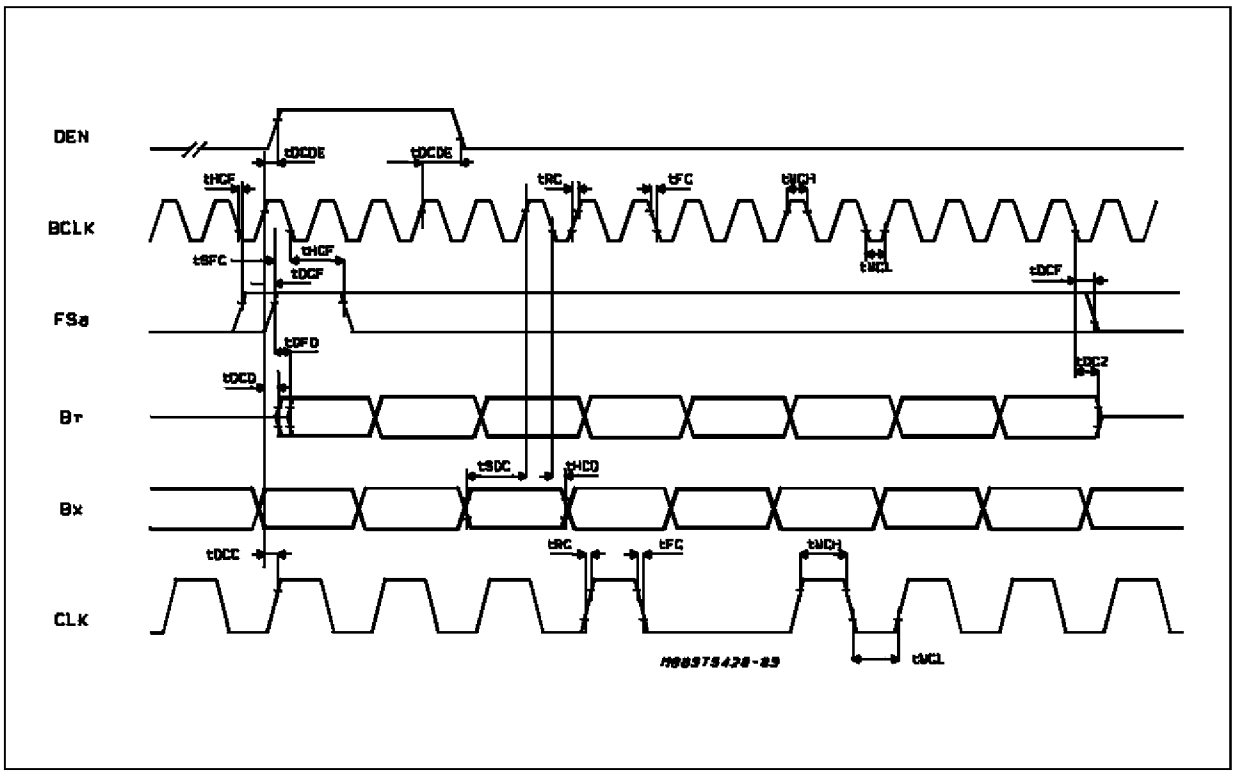


(*) Rt = 33Ω, Required from ST5421version 5.0

TIMING SPECIFICATIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DCDE}	Delay Time BCLK High to DEN Transition	TE Mode only			30	ns
t_{HCF}	Hold Time BCLK Trans. to FSa Transition		0			ns
t_{RC}, t_{FC}	Rise & Fall Time BCLK				15	ns
t_{WCH}, t_{WCL}	BCLK width High & Low		60			ns
t_{SFC}	Setup Time FSa High to BCLK Low		70		BCLK -50	ns
t_{DCF}	Delay Time BCLK High to FSa HIGH	TE Mode only			30	ns
t_{DCD}	Delay Time BCLK High to DATA Valid		20		80	ns
t_{DFD}	Delay Time FSa High to Data Valid	Load 100pF. Apply only if FSa rises later than BCLK rising edge			80	ns
t_{DCZ}	Delay Time BCLK Low Data Invalid		50		120	ns
t_{SDC}	Setup Time Data Valid to BCLK Low		30			ns
t_{HDC}	Hold Time BCLK Low to Data Invalid		20			ns
t_{DCC}	Delay Time BCLK High to CLK High	TE and TES side modes only	0		30	ns

Figure 10: GCI Mode



APPLICATIONS INFORMATION

While the pins of ST5421 SID-GCI device are well protected against electrical misuse, it is recommended that the standard CMOS practise of applying GND to the device before any other connections, should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A power supply decoupling capacitor of 0.15F should be connected from this common point to V_{CC} as close as possible to the device pins.

CRYSTAL OSCILLATOR

The clock source for ST5421 may be provided with a commercially available crystal or an external clock source meeting the frequency requirements as explained in the following sections.

CRYSTAL SPECIFICATION

ST5421 SID-GCI clock source may be either a quartz crystal operating in parallel mode or an external signal source at 15.36MHz. The complete oscillator (crystal plus the oscillator circuit) must meet a frequency tolerance specification of ±50ppm total to comply with the CCITT I.430 specification for TE applications.The frequency tolerance limits span the conditions of full operating temeprature range (commercial or industrial) and effects due to aging and part parameter variations.

The crystal is connected between pin 5 (MCLK/XTAL) and pin 6 (XTAL2), with a 33pF total capacitance from each pin to ground. The external capacitors must be mica or high-Q ceramic type. The use of NPO (Negative Positive Zero coefficient) capacitors is highly recommended to ensure tight tolerance over the operating temperature range. The 33pF capacitance includes the external capacitor plus any trace and lead capacitance on the board. Nominal frequency of 15.360MHz, frequency tolerance (accuracy, temperature and aging) less than 1.60ppm, with Rs = 150, CL= 20pF, parallel mode, C0 (shunt capacitance) 7pF.An external circuit may be driven directly from the pin XTAL2 (pin 6) provided that the load presented is greater than 50K shunted by a total of 33pF of capacitance. Crystal oscillator board layout is critical and should be designed with short traces that do not run parallel when in close proximity (to minimize coupling between adjacent pins). On multi-layered boards a ground layer should be used to prevent coupling from signals on adjacent board layers. Ground traces on either side of the high frequency trace also helps isolate the noise pickup.

EXTERNAL OSCILLATOR CONFIGURATION

An external 5V drive clock sourcxed may be connected to the MCLK (pin 5) input pin of ST5421. The nominal frequency should be 15.36MHz with a tolerance of 1 80ppm. The ST5421 SID provides a load of about 7pF at the MCLK input pin.

LINE TRANSFORMER REQUIREMENTS

The electrical characteristics of the pulse transformer for the ISDN "S" interface are defined to meet the output and input signal and the line isolation and characteristics as defined in CCITT reccommednation I.430. The transformer provides isolation for the line card or terminal from the line it lasi provides a means to transfer power to the terminalb over the S-loop via the "phantom" circuit created by center-tapping the line side windings. A transformer is used both at the transmit and the receive end of the loop. These notes specify the tolerances of a transformer that is employed with ST5421 to meet the CCITT recommendation on output pulse mask and impedance requirements.

LINE TRANSFORMER RATIO

The transmit and th receive transformers can be the same (with a winding ratio of 1:2) or optionally, the receive transformer could have a transformer ratio of 1:1. The primary of the transformer is connected to the S loop while the secondary is connected to the device.

EXTERNAL PROTECTION CIRCUITRY

Precautions are to be taken to ensure that ST5421 SID-GCI is protected against electrical surges and other interferences due to electromagnetic fields, power line faults and lightening discharge that may occur in the transmission medium. Protection circuits that are external to the device are recommended on both the primary and secondary sides of the line transformer.

DC BIAS CAPACITORS FOR ANALOG REFERENCE

Two decoupling capacitors (0.1µF mica) and 10µF (electrolytic) are connected between pin 19 of the device and its ground connection. These capacitors decouple the midpoint of a two-resistor potential divider (inside the device) and provide an internally buffered reference for the analog circuitry.

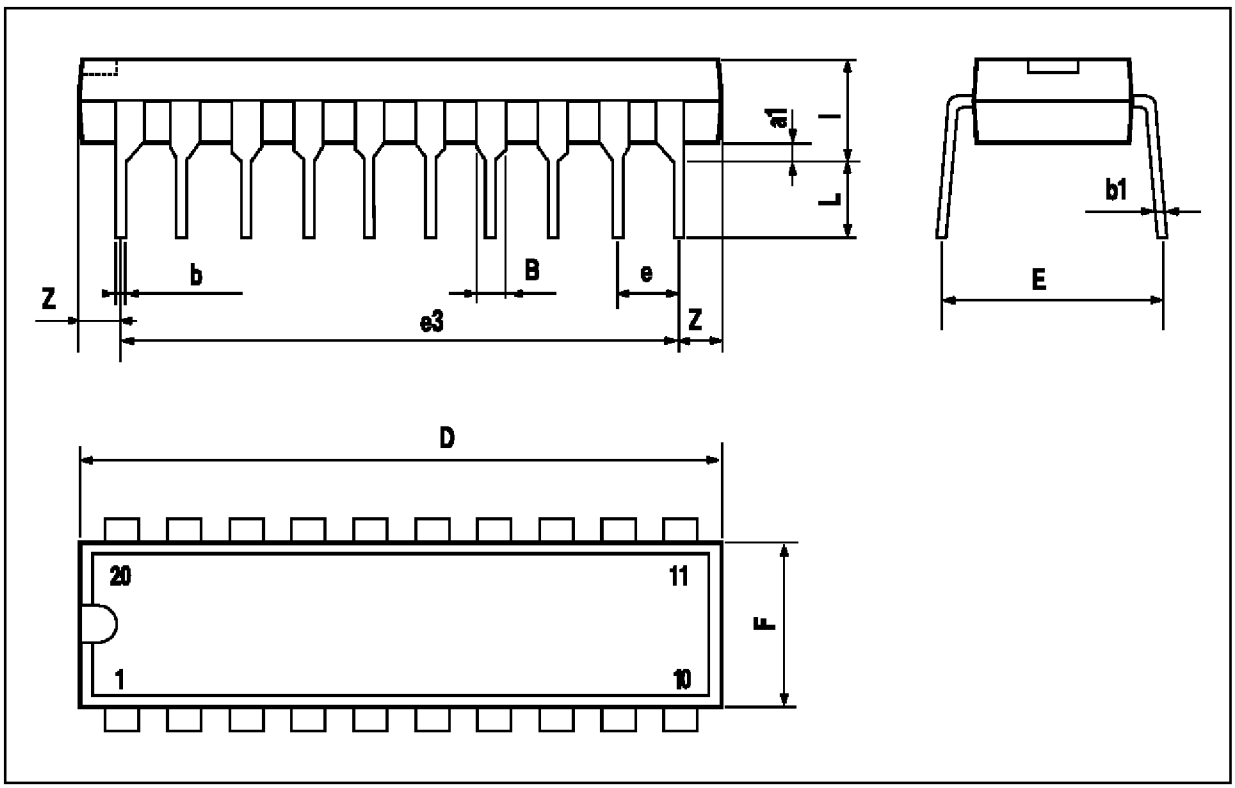
ST5421 EXCEEDING I.430 TRANSMISSION REQUIREMENTS

This ST5421 is designed with the goal of substantially exceeding the transmission performance requirements as specified in the I.430. This is made possible in the ST5421 SID design by employing superior analog front end designs. For example, in the receive path, an analog prefiter removes <200kHz noise signals, which is then followed by an adaptive line equalizer to accomodate varying line conditions with superior performance. A continuously tracking adaptive threshold circuit provides the slicing levels for the detection circuits for correct interpretation of transmission bits even on long lossy loops. This implementation results in longer ranges of S interface cables compared to I.430 requirements.

The version 4.1 of the ST5431 has shown ESD weakness on LO+ and LO- pins: these pins only up to 400V. All other pins are passing SGS-THOMSON Internal Quality Standards (2k volts; Human body model; mil. std. 883 meth. 3015).

DIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



PLCC28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045