MN74HC221/MN74HC221S

Dual Monostable Multivibrators with Clear

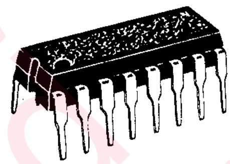
■ Outline

The MN74HC221/MN74HC221S is constituted by 2-circuit monostable multivibrators supported by the high speed silicon gate CMOS technique.

The trigger input triggers the respective multivibrator at the falling edge of the A input, rise of the B input, and rising edge of the CLR input, and once triggered, the output is kept in the monostable mode for a fixed period of time by the external resistor and condenser unless the level of the CLR input is set to "L".

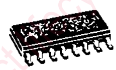
Owing to the silicon gate CMOS process, these multivibrators have realized low power consumption and high noise immunity equivalent to those of a standard CMOS and the operation speed as high as an LS TTL. The MN74HC221/MN74HC221S can directly drive ten LS TTL inputs. To protect the input and output against electrostatic breakdown, a resistor and a diode are used for the V_{CC} and the GND. The pin configuration and the function are the same as those of the standard 54LS/74LS logic family.

P-3



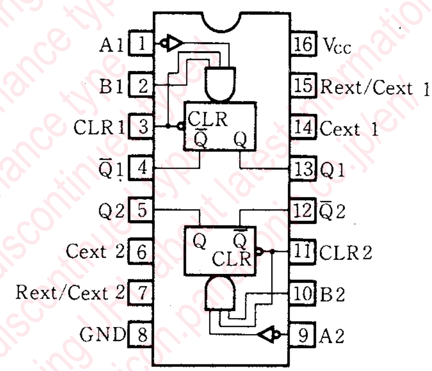
16-pin plastic DIL package

P-4



16-pin PANAFLAT package (SO-16D)

Pin Configuration

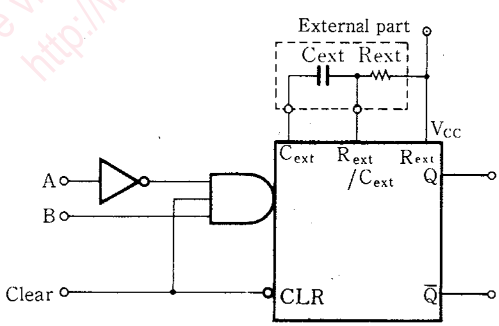


■ Truth Table

Input			Output	
CLEAR	A	B	Q	Q̄
L	×	×	L	H
×	H	×	L	H
×	×	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

Note) H : High level
 : Low level
× : "H" or "L" either will do.
↓ : Trading from "H" to "L"
↑ : Leading from "L" to H"
⊓ : One piece of "H" level pulse
⊔ : One piece of "L" level pulse

■ Logic Diagram



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■ Absolute Maximum Ratings

Item			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5~+7.0	V
Input output voltage			V_I, V_O	$-0.5 \sim V_{CC}+0.5$	V
Input protective diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature			T_{stg}	−65~+150	°C
Power dissipation	MN74HC221	Ta=−40~+60°C	P_D	400	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC221S	Ta=−40~+60°C	P_D	275	mW
		Ta=+60~+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Recommended Operating Conditions

Item	Symbol	V_{CC}(V)	Rating	Unit
Operating power supply voltage	V_{CC}		2.0~6.0	V
Input output voltage	V_I, V_D		$0 \sim V_{CC}$	V
Operating temperature	T_A		−40~+85	°C
Input rise, fall time A, CLR	tr, tf	2.0	0~1000	ns
		4.5	0~5000	ns
		6.0	0~400	ns
Outer fitting timing resistance	Rext		5~1000	kΩ
Outer fitting timing capacitance	Cext		No limit	pF
Wiring capacitance	Rext/Cext		0~50	pF

■ DC Characteristics (GND=0V)

Item	Symbol	V_{CC} (V)	Test Condition V_I	V_O	Unit	Ta=25°C min.	typ.	max.	Ta=−40~+85°C min.	max.	Unit
Input voltage high level	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input voltage low level	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output voltage high level	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.92			3.84		
		6.0		−5.2	mA	5.48			5.34		
Output voltage low level	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.26		0.33	
		6.0		5.2	mA			0.26		0.33	
Input leakage current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
R_{ext}/C_{ext} pin leakage current	I_{OZ}	6.0	$V_I=V_{IH}$ or V_{IL}, $V_O=V_{CC}$ or GND					±0.5		±5.0	μA
Static supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time≦6ns, C_L=50pF)

Item	Symbol	V_{CC} (V)	Test Condition	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Output rise time	t_{TLH}	2.0			27	75		95	ns
		4.5			10	15		19	
		6.0			8	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			8	15		19	
		6.0			6	13		16	
Propagation time A, B, CLR→Q, (L→H)	t_{PLH}	2.0			76	250		315	ns
		4.5			28	50		63	
		6.0			20	43		54	
Propagation time A, B, CLR→$\overline{Q}$, (H→L)	t_{PHL}	2.0			83	250		315	ns
		4.5			29	50		63	
		6.0			22	43		54	
Propagation time CLR→Q, $\overline{Q}$ (L→H)	t_{PLH}	2.0			47	150		190	ns
		4.5			16	30		38	
		6.0			15	26		33	
Propagation time CLR→Q, $\overline{Q}$ (H→L)	t_{PHL}	2.0			44	150		190	ns
		4.5			15	30		38	
		6.0			15	26		33	
Minimum output pulse width	$t_{W(OUT)}$	2.0	Cext=0 Rext=5kΩ		—				ns
		4.5			78				
		6.0			—				
Output pulse width*	$t_{W(OUT)}$	2.0	Cext=1000pF Rext=10kΩ		—				μs
		4.5			4.8				
		6.0			—				
Input pulse width A, B	$t_{W(IN)}$	2.0				100		125	ns
		4.5			9	20		25	
		6.0				34		21	
Input pulse width CLR	$t_{W(IN)}$	2.0				200		250	ns
		4.5			21	40		50	
		6.0				34		43	

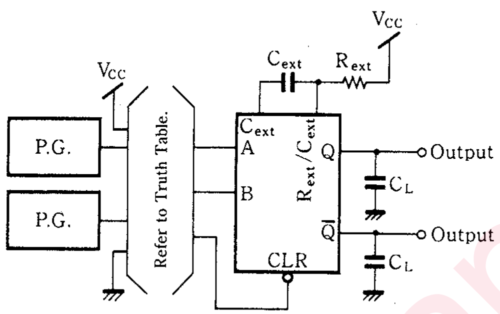
* Output pulse width $t_{W(out)}$ meets to the following formula when C_{ext}>1000pF
$t_{W(out)} \approx 0.3\ C_{ext} \cdot R_{ext}$

■ Caution in Use

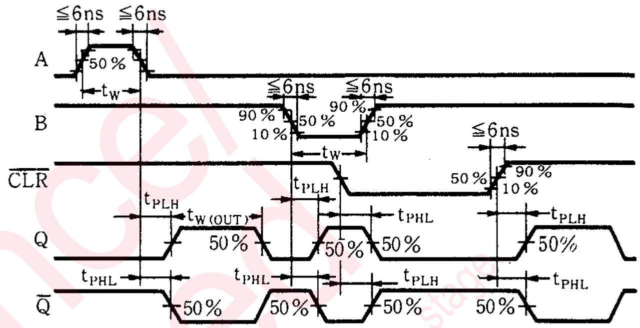
When using one circuit only, make CLR Low, R_{ext}/C_{ext}, C_{ext}, Q, $\overline{Q}$ openand keep other input pins High or Low.

- Switching time measuring circuit and waveforms

1. Measuring circuit

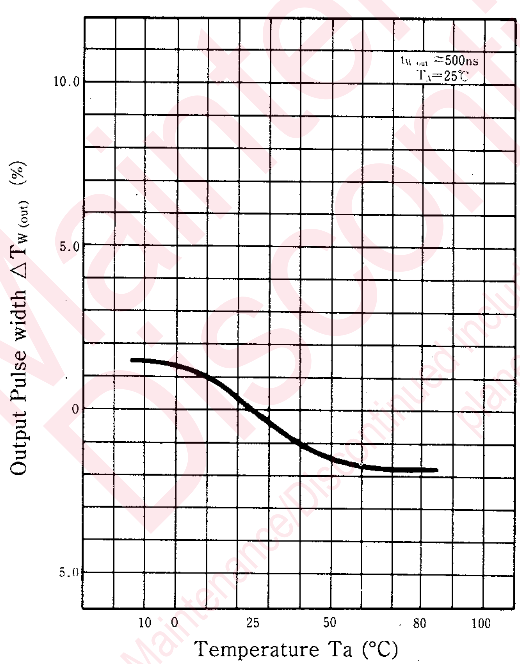


2. Switching waveforms



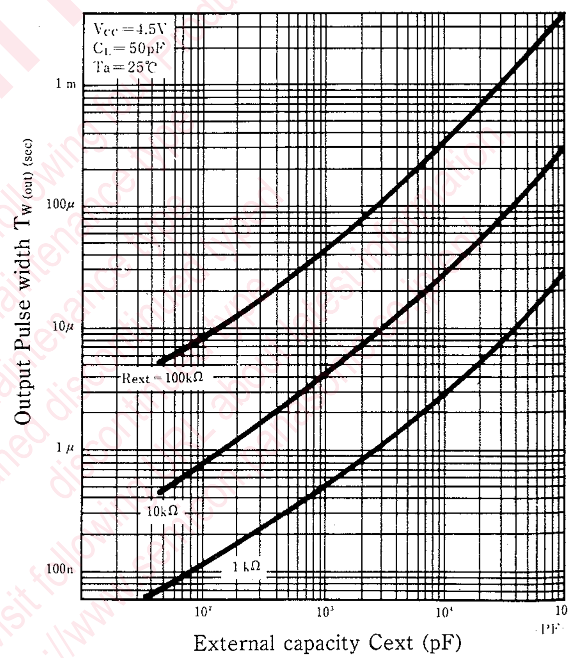
(Fig.1)

$\Delta T_{W\,(out)}$ · Ta characteristics



(Fig.2)

$T_{W\,(out)}$ · Cext characteristics



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