SSI 34D441
Data Synchronizer & Write Precompensator Device

July, 1990

DESCRIPTION

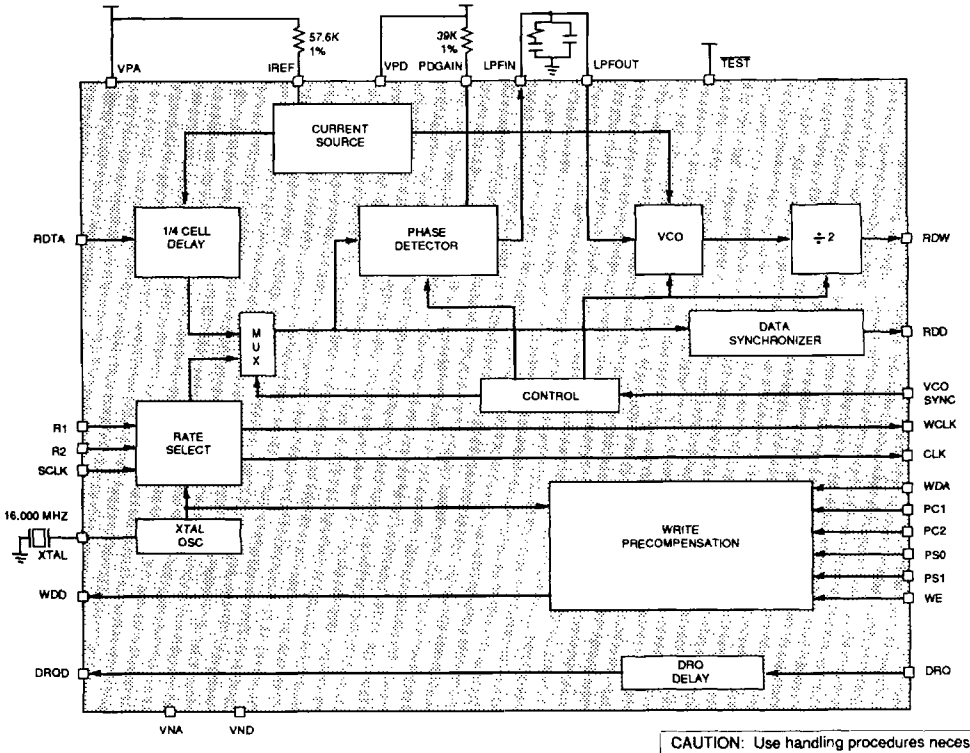
The SSI 34D441 floppy disk data synchronizer/write precompensator performs read-data synchronization and write data precompensation of MFM encoded data for high performance floppy disk drive systems. The SSI34D441 is optimized for use with the NEC μPD765A/ μPD7265 controller family.

The SSI 34D441 contains an analog phase-lock-loop for read data synchronization, a crystal controlled reference oscillator, write precompensation circuitry, and a delay function for the DRQ signal. It employs silicon gate CMOS technology for low power consumption. The SSI34D441 requires a +5V power supply and is available in 28-pin PDIP and 28-pin PLCC packages.

FEATURES

- **Ideal for operation with NEC μPD765A/μPD7265**
- **Fast acquisition analog PLL for precise read data synchronization**
- **No adjustments or trims needed to external components**
- **Programmable data rate, up to 1 Mbit/s**
- **Internal crystal controlled oscillator**
- **Selectable write precompensation intervals**
- **Programmable write clock**
- **DRQ (Data DMA Request) delay function**
- **Low power CMOS, +5V operation**
- **28-pin PDIP and 28-pin PLCC**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

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FUNCTIONAL DESCRIPTION

CRYSTAL OSCILLATOR

The crystal controlled oscillator uses a 16.000 MHz crystal cut for fundamental series mode resonance. Its frequency is divided down and used throughout the 34D441. The device requires only one pin for the crystal input; the other crystal pin is connected to digital ground. An external source (TTL level) can also be used to drive the chip via this pin, if desired.

RATE-SELECT

The rate-select section generates the various write-data frequencies (WCLK), and one of the two alternative clock rates (CLK), as shown in Table 1. In addition, this section provides a time base for the read-data circuitry. The CLK and WCLK signals have their rising edges synchronized. The WCLK signal has a pulse width of 250 ns.

TABLE 1: WRITE-DATA CLOCK FREQUENCIES

R2	R1	WCLK	DATA RATE	SCLK	CLK
1	0	250 kHz	125 kHz	1	8 MHz
0	0	500 kHz	250 kHz	0	4 MHz
0	1	1 MHz	500 kHz		
1	1	2 MHz	1 MHz		

DRQ DELAY

This circuit is used to delay the leading edge of the DRQ signal, which is generated by the NEC 765 before it is sent to the DMA controller. The output pulse appearing at DRQD has its leading edge delayed by six to eight CLK pulses. The DRQ pulse is at least nine CLK pulses wide. The falling edge of the input clears the DRQD pulse.

DATA SEPARATOR

This circuit consists of several blocks, which include the one-shot, VCO, IREF, and the read-path circuitry. Read-data synchronization is accomplished with a fast acquisition phase-lock-loop (PLL). The input data from the disk drive, RDTA, is phase locked with the VCO. The synchronized read data and the VCO (divided by two) are available for external data extraction at the RDD and RDW pins, respectively.

Changing the state of VCOSYNC causes the VCO to be stopped and restarted in phase with the PLL reference, which can be either the internal crystal oscillator or the RDTA input data. Restarting the VCO in phase with the input prevents the PLL from locking to harmonics and insures short lock times. (See Figure 1.)

The one-shot is used to shape the input read data. The IREF block provides reference currents to both the VCO and the One-Shot circuits. Current for the current source block is set by an external resistor connected to the IREF pin. The rate pins R1 and R2 are used to select between various frequencies. The Read-Path circuitry includes the phase detector, charge pump, data synchronizer and control logic circuitry.

The data synchronizer separates the data and clock pulses using windows derived from the VCO output. Using a VCO running at twice the expected input data frequency allows accurate centering of these windows about the expected bit positions. The phase detector controls the charge pump which causes current pulses to flow in or out of the phase-lock-loop filter. The amount of current to be sourced or sunk by the charge pump is controlled by an external resistor connected to the PDGAIN pin. This feature can be used to change the phase detector gain, KPD, which is given by:

$I_{PDGAIN}/2\pi$ [A/rad]

The output read data pulse, RDD, is at least 62.5 ns wide.

WRITE PATH

The WDD output is a re-synchronized version of the input MFM write data (WDA) which has been time shifted, if needed, to reduce interbit interference. The amount of precompensation, as well as the direction of the pulse shifting, is controlled by the external signals PC1, PC2, PS0 and PS1. Table 2 describes the precompensation signals. The output buffer for the precompensated write data (WDD) is capable of sinking 24 mA. The write path circuitry is also used to multiplex the output of the one-shot to the WDD pin for test purposes.

TABLE 2: PRECOMPENSATION DESCRIPTION

PC2	PC1	PRECOMPENSATION INTERNAL	PS0	PS1	SHIFT
0	0	±62.5 ns	0	1	Normal (no shift)
1	0	±125 ns	0	1	Late (delay)
0	1	±187.5 ns	1	0	Early (advance)
1	1	±250 ns	1	1	Invalid (no Shift)

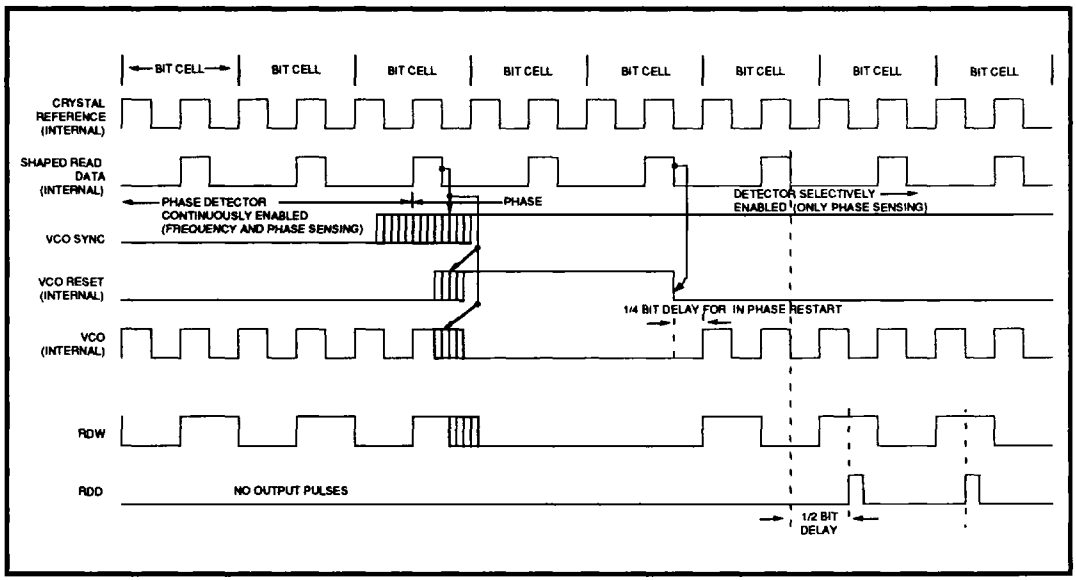

FIGURE 1: PLL Locking Sequence

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PIN DESCRIPTIONS

<table>
<tr><th>NAME</th><th>PIN NO.</th><th>DESCRIPTION</th></tr>
<tr><td>R1, R2</td><td>3, 4</td><td>Used to set the following conditions: write data clock rate (WCLK), one-shot output pulse width, and the (VCO) voltage - controlled oscillator frequency.
<table>
<tr><th>R2</th><th>R1</th><th>DATA RATE</th><th>NOMINAL WCLK</th><th>VCO FREQ</th></tr>
<tr><td>1</td><td>0</td><td>125 kHz</td><td>250 kHz</td><td>250 kHz</td></tr>
<tr><td>0</td><td>0</td><td>250 kHz</td><td>500 kHz</td><td>500 kHz</td></tr>
<tr><td>0</td><td>1</td><td>500 kHz</td><td>1 MHz</td><td>1 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1 MHz</td><td>2 MHz</td><td>2 MHz</td></tr>
</table></td></tr>
<tr><td>SCLK</td><td>5</td><td>This pin sets the clock frequency CLK
<table>
<tr><th>SCLK</th><th>CLK</th></tr>
<tr><td>0</td><td>4 MHz</td></tr>
<tr><td>1</td><td>8 MHz</td></tr>
</table></td></tr>
<tr><td>PC2, PC1</td><td>6, 7</td><td>Used to set the amount of write-data precompensation.
<table>
<tr><th>PC1</th><th>PC2</th><th>PRECOMPENSATION INTERVAL (ns)</th></tr>
<tr><td>0</td><td>0</td><td>±62.5</td></tr>
<tr><td>0</td><td>1</td><td>±125</td></tr>
<tr><td>1</td><td>0</td><td>±187.5</td></tr>
<tr><td>1</td><td>1</td><td>±250</td></tr>
</table></td></tr>
<tr><td>DRQ</td><td>8</td><td>Accepts DRQ signal from NEC 765 controller to delay it.</td></tr>
<tr><td>$\overline{\text{TEST}}$</td><td>10</td><td>Should be a logic high for normal operation. When $\overline{\text{TEST}}$ is low, the WDD pin outputs the one-shot pulse.</td></tr>
<tr><td>RDTA</td><td>11</td><td>Accepts the MFM encoded read data pulses from the read amplifier circuits.</td></tr>
<tr><td>VCOSYNC</td><td>18</td><td>Selects the reference input to the PLL. Selects a reference frequency equal to WCLK when low, and the incoming read data (RDTA), when high.</td></tr>
<tr><td>WDA</td><td>25</td><td>Accepts write data from the controller. This data is resynchronized and precompensated before being sent to the drive.</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

<table>
<tr><th>NAME</th><th>PIN NO.</th><th>DESCRIPTION</th></tr>
<tr><td>PS0, PS1</td><td>26, 27</td><td>Pins to determine whether to precompensate write data pulses, and to advance or delay the leading edge of pulses.
<table>
<tr><th>PS0</th><th>PS1</th><th>SHIFT</th></tr>
<tr><td>0</td><td>1</td><td>Normal (no shift)</td></tr>
<tr><td>0</td><td>1</td><td>Late (delay)</td></tr>
<tr><td>1</td><td>0</td><td>Early (advance)</td></tr>
<tr><td>1</td><td>1</td><td>Invalid (no shift)</td></tr>
</table></td></tr>
<tr><td>WE</td><td>28</td><td>When high, causes data to be output at the WDD pin. When WE is low, write data (WDD) is low.</td></tr>
<tr><td>VPD</td><td>2</td><td>+5V Digital supply</td></tr>
<tr><td>VND</td><td>24</td><td>Digital ground for chip</td></tr>
<tr><td>VPA</td><td>12</td><td>+5V analog supply (isolated +5V source having very little noise).</td></tr>
<tr><td>VNA</td><td>13</td><td>Analog ground</td></tr>
<tr><td>DRQD</td><td>9</td><td>Output for the delayed DRQ signal from the NEC 765. Only the leading edge of the input signal is delayed.</td></tr>
<tr><td>RDW</td><td>19</td><td>This is a square wave output generated by the VCO which provides a read data window to be used by the NEC 765 controller to separate the read-data and read-clock transitions. RDW has the same frequency as the nominal data rate.</td></tr>
<tr><td>RDD</td><td>20</td><td>This signal consists of pulses that indicate flux reversals present on the floppy disk that could indicate either clock or data information. The leading edge of each RDD pulse will appear in the center of window defined by the RDW signal.</td></tr>
<tr><td>WCLK</td><td>21</td><td>This signal is the write clock for the controller device. All write signals output by the NEC 765 controller, are related to WCLK.</td></tr>
<tr><td>CLK</td><td>22</td><td>This signal is used by the NEC 765 controller and associated devices. The CLK signal has a 50% duty cycle and the rate is set by SCLK.</td></tr>
<tr><td>WDD</td><td>23</td><td>This open-drain output provides re-synchronized and precompensated write data in accordance with settings on PC1,PC2, and PS0, PS1 pins. The leading edge of WDD shall be used to define data. When $\overline{\text{TEST}}$ is low, this pin will output the one-shot pulses.</td></tr>
<tr><td>XTAL</td><td>1</td><td>Single input pin for the 16 MHz crystal oscillator. Other side of crystal to go to digital ground. Option of providing an external 16MHz signal with TTL compatible logic levels and a 40% to 60% duty cycle.</td></tr>
<tr><td>IREF</td><td>14</td><td>Used to set the internal reference current generated for the one-shot and VCO. Desired current shall be derived from a 1% tolerance 57.6 kΩ resistor connected between the analog 5 volt supply and this pin.</td></tr>
</table>

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PIN DESCRIPTIONS (Continued)

NAME	PIN NO.	DESCRIPTION
LPFOUT	15	Control voltage input of the VCO, and also for the connection of loop-filter output. Control voltage shall range approximately from 0.7 to 4.5 volts.
LPFIN	16	Output pin for the current pulses from charge pump that the were converted from voltage pulses generated by phase detector. This pin is typically connected to LPFOUT, and an RC low pass loop filter network connected to the analog ground.
PDGAIN	17	Used to set the current level to be sunk or sourced by the charge-pump. A 39K ohm resistor connected between this pin and the digital 5 volt supply VPD, shall provide a 100 µA current to the charge-pump. Some other resistor values and their corresponding currents are given below:

R_{PDGAIN}	I_{PDGAIN}
15K	225 µA
22K	160 µA
30K	120 µA
46K	80 µA

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Storage Temperature	-40 to +120	°C
Ambient Operating Temperature, TA	0 to +70	°C
Supply Voltages, VPD, VPA	-0.5 to +7.0	VDC
Voltage Applied to Logic inputs	-0.5 to +7.0	VDC
Voltage Supplied to Logic Outputs	-0.5 to +5.5	VDC
Maximum Power Dissipation	750	mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Ambient Temperature, TA		0		70	°C
Power Supply Voltage, VPD, VPA		4.75	5	5.25	VDC
High Level Input Voltage, VIH	Power supply = 4.75V	2.0			V
Input Current High, IIH	Power supply =4.75V VIH = 2.4V			20	µA
Low Level Input Voltage, VIL	Power supply = 4.75V			0.8	V
Input Current Low, IIH	Power supply = 5.25V VIL = 0.4V			-20	µA
High Level Output Voltage, VOH	Power supply = 4.75V IOH=4 mA	2.4			V
Low Level Output Voltage All others, VOL	Power supply = 4.75V IOL = 8 mA			0.4	V
Short Circuit Output Current WDD only IOS (to positive supply)	Power supply = 5.25V	20		150	mA

DC CHARACTERISTICS (Unless otherwise specified, power supplies = 4.75V to 5.25V, TA = 0 to 70°C, R_{IREF} = 57.6 kΩ ± 1%, R_{PDGAIN} = 39 kΩ ± 5%, XTAL = 16 MHz crystal in series resonance.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current Analog, IVPA	Power supply = 5.25V 51 MHz data rate			10	mA
Supply Current Digital, IVPD	Power supply = 5.25V 1 MHz data rate			6	mA
Short Circuit Output Current (to ground) All others, IOS	Power supply = 5.25V	30		100	mA

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DYNAMIC CHARACTERISTICS AND TIMING (Load Capacitance = 50 pF)

DATA DETECTION CHARACTERISTICS (See Figure 2)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TRDDW RDTA pulse width		25			ns
TRDWP RDW period	R1 = 0, R2 = 1		8		µs
	R1 = 0, R2 = 0		4		µs
	R1 = 1, R2 = 0		2		µs
	R1 = 1, R2 = 1		1		µs

DATA DETECTION CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRDWW	RDW pulse width high or low	Same R1, R2 as above		TRDWP / 2		µs
TRDW	RDD pulse width		62.5		187.5	ns
TRDDD	Propagation Delay from RDW transition to RDD positive edge	Same R1, R2 as above	0.025	TRDWP / 4		µs

DRQ CHARACTERISTICS (See Figure 2)

TDLY	Propagation delay from DRQ positive edge to DRQD positive edge	SCLK = 1	0.75		1.0	µs
		SCLK = 0	1.50		2.0	µs
TDRLL	Propagation delay from DRQ negative edge to DRQD negative edge				50	ns

CRYSTAL CHARACTERISTICS

TXTALP	Crystal oscillator frequency period			62.5		ns

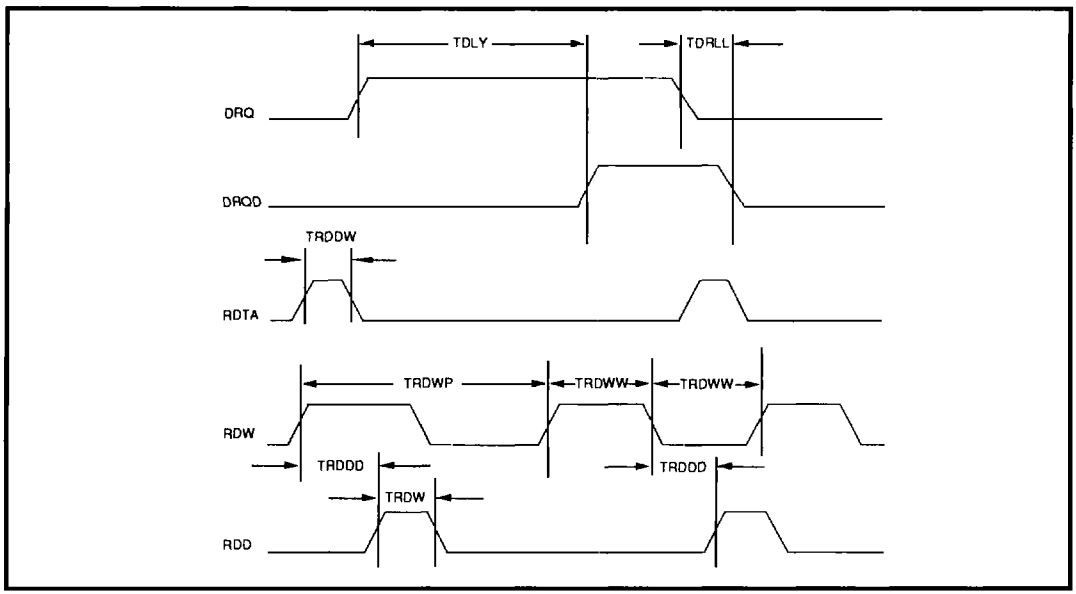

FIGURE 2: Timing Diagram

PHASE-LOCK-LOOP CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCO frequency range	Nominal frequency set by R1, R2, see Table 1	±20		±40	%
KVCO VCO gain	R2=1, R1=0		$0.5x10^6$		rad/s/V
	R2=0, R1=0		$0.96x10^6$		rad/s/V
	R2=0, R1=1		$1.75x10^6$		rad/s/V
	R2=1, R1=1		$2.98x10^6$		rad/s/V
KPD phase detector gain	RPDGAIN = 39kΩ ± 1%		15.9		µA/rad
VCO phase reset error				±0.2	rad
Number of RDW periods delay from RDTA to RDD			0.5		
Number of RDW periods VCO may be disabled during reference switching				3	

REFERENCE CLOCK (See Figure 3)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TC	CLK period	SCLK = 1		125		ns
		SCLK = 0		250		ns
TCO	CLK pulse width low or high			TC/2		ns
TCR	CLK rise time				15	ns
TCF	CLK fall time				15	ns

WRITE PRECOMPENSATION SWITCHING CHARACTERISTICS (See Figure 3)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TCY	WCLK period	R1 = 0, R2 = 1		4		µs
		R1 = 0, R2 = 0		2		µs
		R1 = 1, R2 = 0		1		µs
		R1 = 1, R2 = 1		0.5		µs
TO	WCLK pulse width	All combinations of R1, R2		250		ns
TR	WCLK rise time				15	ns
TF	WCLK fall time				15	ns

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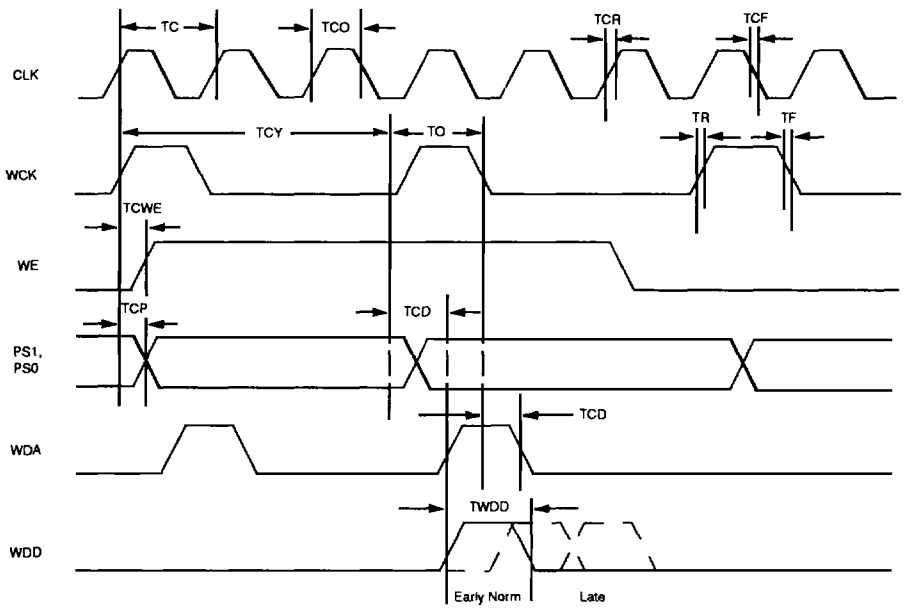
WRITE PRECOMPENSATION SWITCHING CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TCWE Propagation delay from WCLK positive edge to WE positive edge		10		100	ns
TCP Propagation delay from WCLK positive edge to PS0, PS1 transition		10		100	ns
TCD Propagation delay from WCLK positive edge to WDA negative edge		10		100	ns
TWDD WDD pusle width		62.5			ns



Note 1: Not to scale.
Note 2: Read data waveforms do not show delay between RDIA and RDW.
Note 3: Write data waveforms do not show WDD precompensation by exact amounts specified.
Note 4: WCLK and CLK have their rising edges synchronized.

FIGURE 3: Switching Characteristics

APPLICATION

LOOP FILTER

The element in the phase lock loop which controls the loop dynamics is known as the loop filter. Acquisition time, data margin, and data tracking can be optimized by the loop filter selection. One possible loop filter configuration is shown in Figure 4, where the function of C_1 is as an integrating element. The larger the capacitance of C_1, the longer will be the lock time. If the capacitance is too small, the loop will tend to track high frequency jitter. The role of the resistor R is to reduce the phase shift induced by C_1. This is necessary since the loop will oscillate at the frequency where the gain is unity. The capacitor C_2 will suppress high frequency transients when switching occurs. This capacitor will have a minimal effect of the loop response if it is small compared to C_1 (typically, $C_2 = C_1/19$).

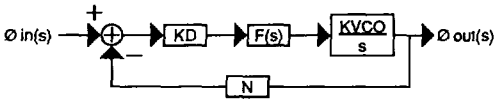
The loop filter transfer function is:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1\left(1 + sC_2R + \frac{C_2}{C_1}\right)}$$

if $C_2 < C_1$
then,

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1}$$

The phase lock loop can be described as:



where,

KD = phase detector gain [A/rad]
F(s) = Filter impedance [V/A]
$\frac{KVCO}{s}$ = oscillator transfer function [rad/s V]
N = ratio of reference input frequency vs. VCO output frequency.

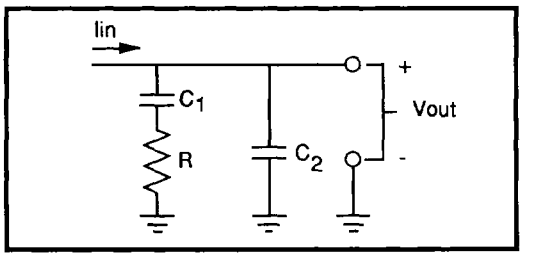


FIGURE 4: Loop Filter

Therefore, the closed loop transfer function is now:

$$T(s) = \frac{Ø\ out(s)}{Ø\ in(s)} = \frac{G(s)}{1 + G(s)H(s)} =$$

$$\frac{KD \times KVCO\left(\frac{1 + sRC_1}{C_1}\right)}{s^2 + s(N \times KD \times KVCO \times R) + \frac{N \times KD \times KVCO}{C_1}}$$

now we can put the characteristic equation (denominator) in the form:

$$s^2 + 2s\zeta\omega_n + \omega_n^2$$

$$\therefore \omega_n^2 = \frac{N \times KD \times KVCO}{C_1} \text{ and } \zeta = \frac{N \times KD \times KVCO \times R}{2\omega_n}$$

which results in:

$$C_1 = \frac{N \times KD \times KVCO}{\omega_n^2}$$

$$R = \frac{2\zeta\omega_n}{N \times KD \times KVCO} \text{ and } C_2 = \frac{C_1}{19}$$

For a $\zeta = 0.8$, the relationship between ω_n and lock time is:

$$\omega_n = \frac{4.5}{\text{lock time}}$$

Therefore, the loop filter components C_1, C_2, and R can be evaluated for a required lock time and coding scheme (N) frequency relationship to the VCO frequency.

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LOOP FILTER (Continued)

For data rates of 250 Kbits/s, the bit cell is 4 µs long. A lock time of 3 bytes translates into:

lock time = 3 x 8 x 4 = 96 µs

Therefore:

$$\omega_n = \frac{4.5}{96\,us} = 47\,Krad/s$$

$$C_1 = \frac{15.9 \times 10^{-6} \times 0.96 \times 10^{6}}{2 \times (47 \times 10^{3})^2} = 3500\,pF$$

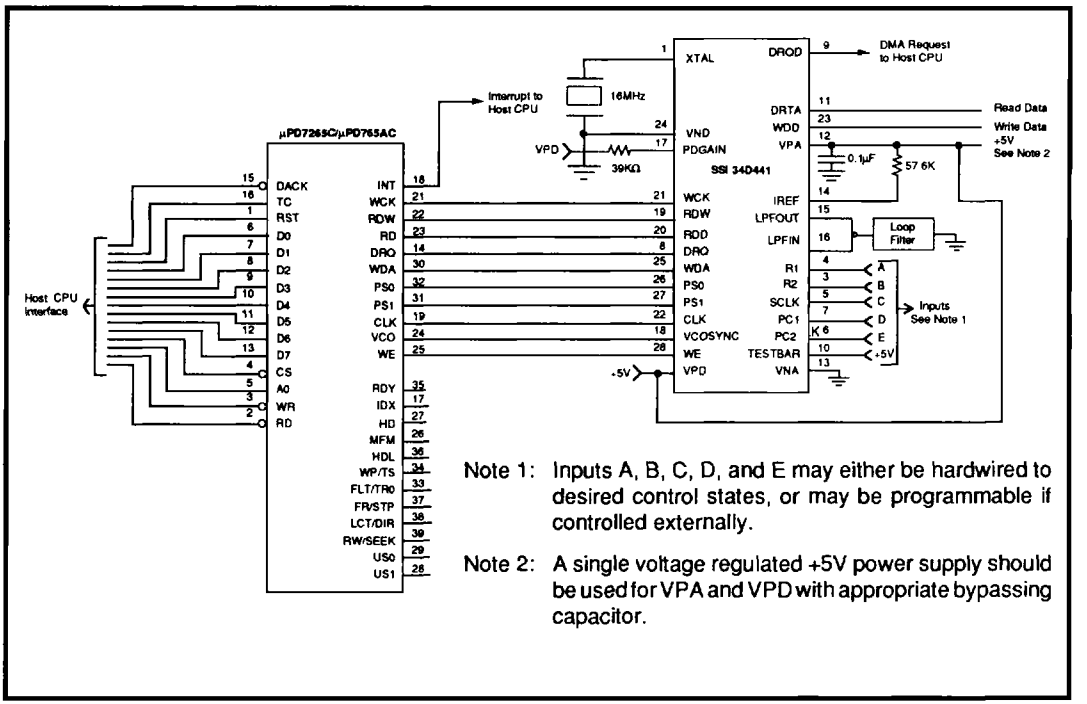
$$R = \frac{2 \times 0.8}{47 \times 10^{3} \times 3.5 \times 10^{-9}} = 9.8\,K\Omega$$

$$C_2 = \frac{C_1}{19} = 184\,pF$$

Table 3 lists suggested loop filter component values for various data rates. These values represent only a starting point for the design of the filter and they may be changed to meet the performance requirements of the system.

TABLE 3:

DATA RATE	LOCK TIME	LOOP FILTER
125 kHz	192 µs	R = 10 kΩ, C_1 = 6800 pF C2 = 360 pF
250 kHz	96 µs	R = 10 kΩ, C_1 = 3300 pF C_2 = 180 pF
500 kHz	46 µs	R = 11 kΩ, C_1 = 1500 pF C_2 = 82 pF
1 MHz	24 µs	R = 13 kΩ, C_1 = 680 pF C_2 = 39 pF



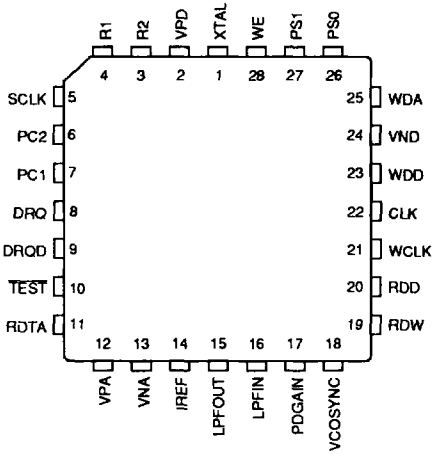
Note 1: Inputs A, B, C, D, and E may either be hardwired to desired control states, or may be programmable if controlled externally.

Note 2: A single voltage regulated +5V power supply should be used for VPA and VPD with appropriate bypassing capacitor.

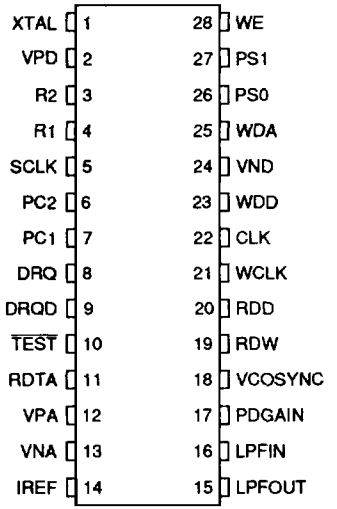
FIGURE 5: Application Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



28-lead PLCC
PLCC pinouts are the same as the 28-pin DIP



600-mil
28-pin DIP

THERMAL CHARACTERISTICS: θja

28-lead PLCC	55°C/W
28-pin PDIP	65°C/W

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ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 34D441 28-pin PDIP	SSI 34D441-CP	34D441-CP
SSI 34D441 28-pin PLCC	SSI 34D441-CH	34D441-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457