

## N-channel 600 V, 0.175 $\Omega$ typ., 18 A MDmesh™ M2 EP Power MOSFET in a TO-220 package

Datasheet - production data

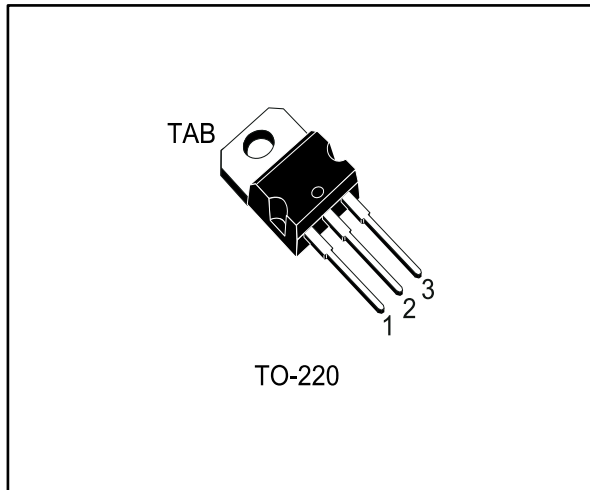
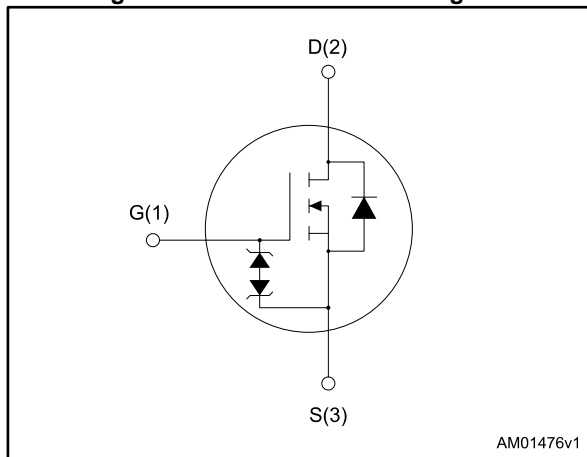


Figure 1: Internal schematic diagram



### Features

Order code	$V_{DS}$ @ $T_{Jmax}$	$R_{DS(on)}$ max.	$I_D$
STP25N60M2-EP	650 V	0.188 $\Omega$	18 A

- Extremely low gate charge
- Excellent output capacitance ( $C_{OSS}$ ) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- Tailored for Very High Frequency Converters ( $f > 150$  kHz)

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 EP enhanced performance technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STP25N60M2-EP	25N60M2EP	TO-220	Tube

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## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
	2.2 Electrical characteristics (curves).....	6
<b>3</b>	<b>Test circuits .....</b>	<b>9</b>
<b>4</b>	<b>Package mechanical data .....</b>	<b>10</b>
	4.1 TO-220 type A package information.....	11
<b>5</b>	<b>Revision history .....</b>	<b>13</b>

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	18	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	72	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature		

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area.

<sup>(2)</sup> $I_{SD} \leq 18\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

<sup>(3)</sup> $V_{DS} \leq 480\text{ V}$

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.83	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	3.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ ; $V_{DD} = 50\text{ V}$ )	200	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 9\text{ A}$		0.175	0.188	$\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{ISS}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1090	-	pF
$C_{OSS}$	Output capacitance		-	56	-	pF
$C_{RSS}$	Reverse transfer capacitance		-	1.6	-	pF
$C_{OSS\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	255	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 18\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> : "Gate charge test circuit")	-	29	-	nC
$Q_{gs}$	Gate-source charge		-	6	-	nC
$Q_{gd}$	Gate-drain charge		-	12	-	nC

**Notes:**

<sup>(1)</sup> $C_{OSS\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{OSS}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7: Switching Energy**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{(off)}$	Turn-off energy (from 90% $V_{GS}$ to 0% $I_D$ )	$V_{DD} = 400\text{ V}$ , $I_D = 2\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	7	-	$\mu\text{J}$
		$V_{DD} = 400\text{ V}$ , $I_D = 4\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	8	-	$\mu\text{J}$

Table 8: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 9\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> : "Switching times test circuit for resistive load" and <a href="#">Figure 20</a> : "Switching time waveform")	-	15	-	ns
$t_r$	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off-delay time		-	61	-	ns
$t_f$	Fall time		-	16	-	ns

Table 9: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		72	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 18\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 18\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 17</a> : "Test circuit for inductive load switching and diode recovery times")	-	360		ns
$Q_{rr}$	Reverse recovery charge		-	5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	28		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 18\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 17</a> : "Test circuit for inductive load switching and diode recovery times")	-	445		ns
$Q_{rr}$	Reverse recovery charge		-	6.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	29		A

**Notes:**

<sup>(1)</sup> Pulse width is limited by safe operating area

<sup>(2)</sup> Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.2 Electrical characteristics (curves)

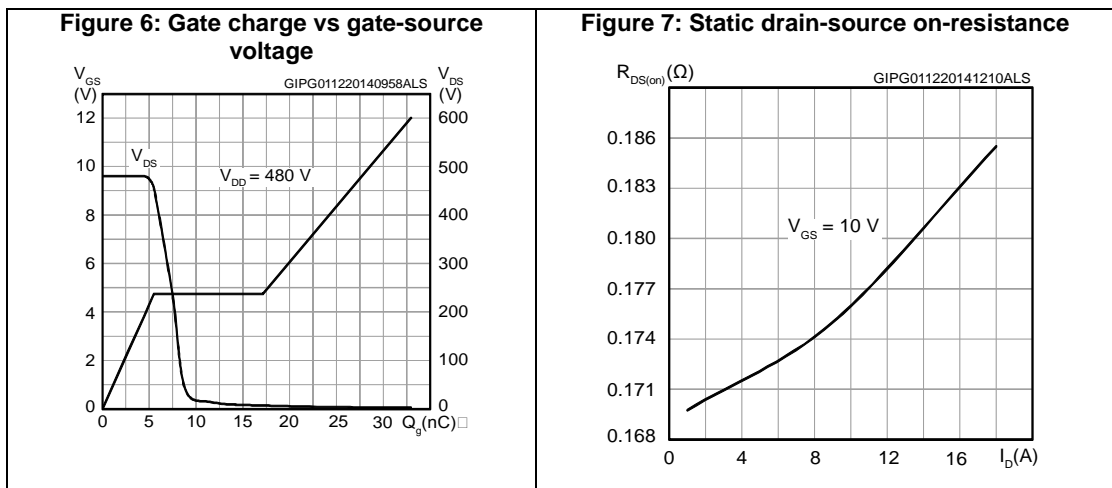
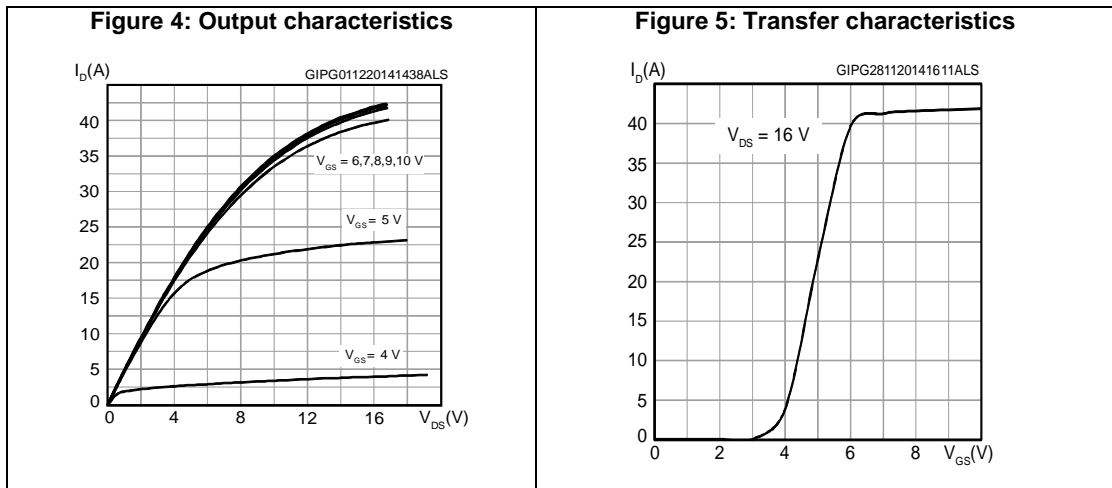
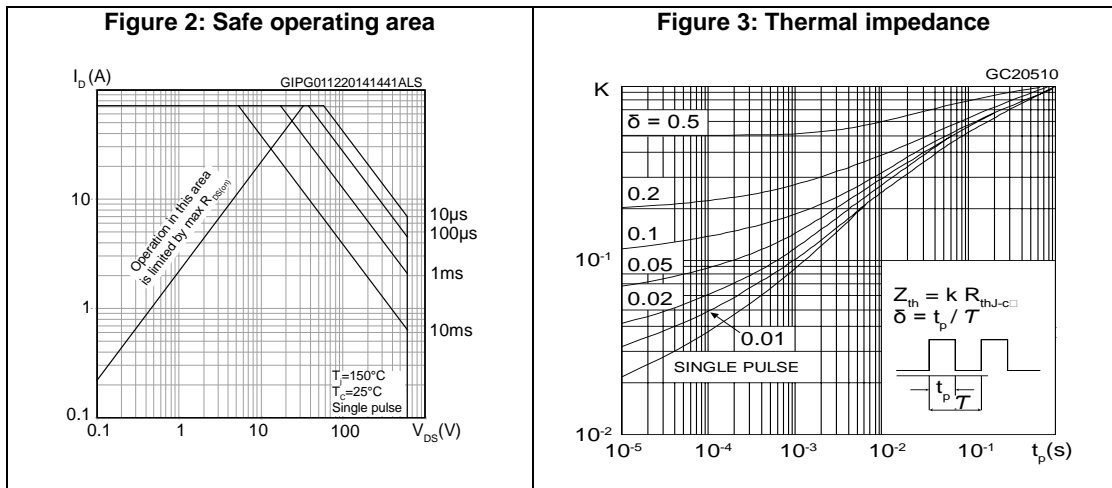


Figure 8: Capacitance variations

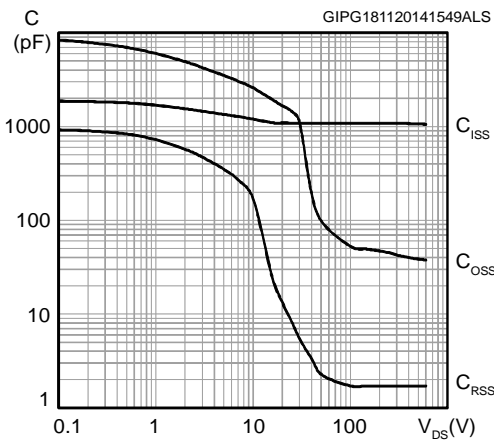


Figure 9: Output capacitance stored energy

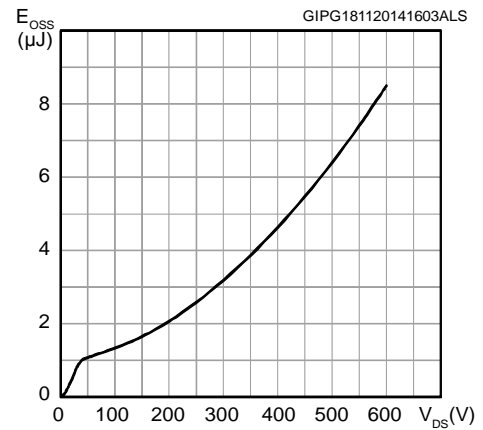


Figure 10: Turn-off switching loss vs drain current

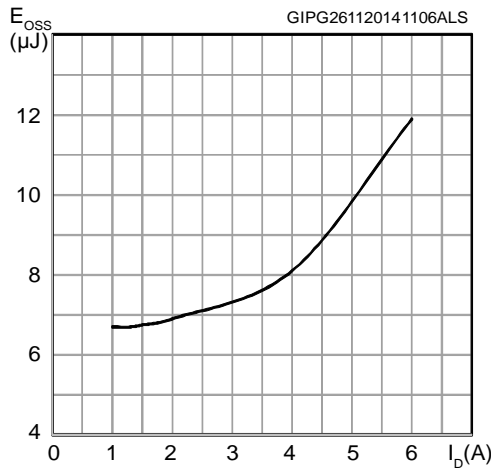


Figure 11: Normalized gate threshold voltage vs temperature

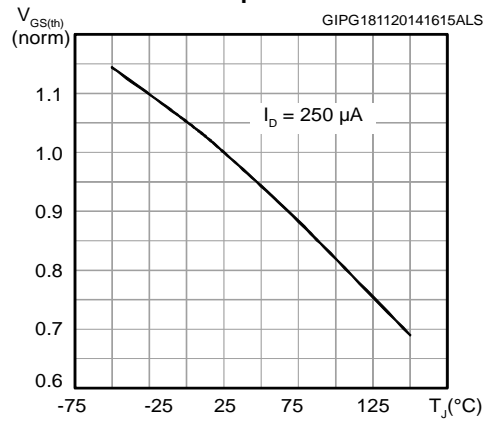


Figure 12: Normalized on-resistance vs temperature

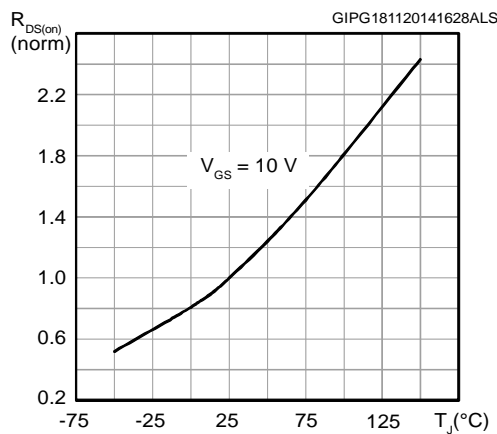
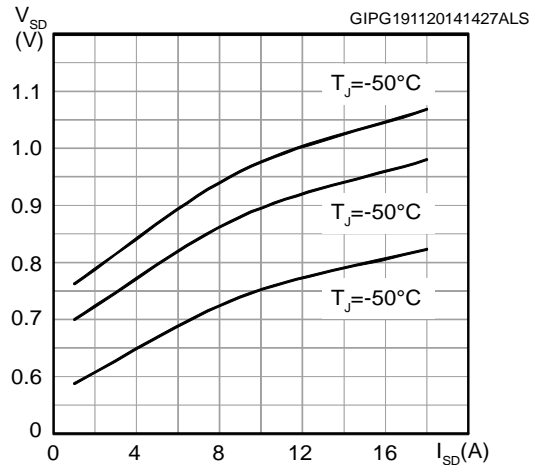
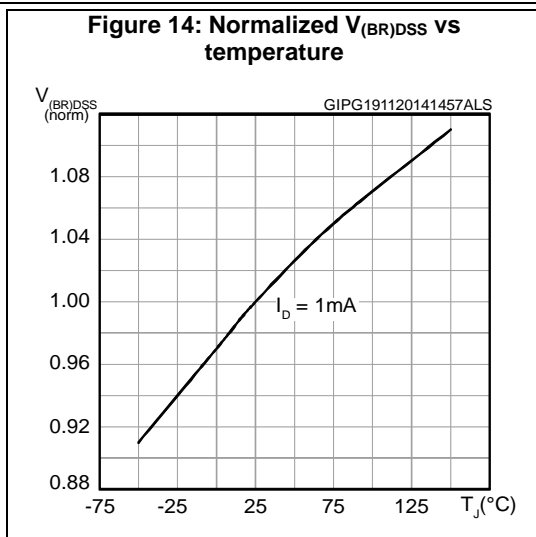


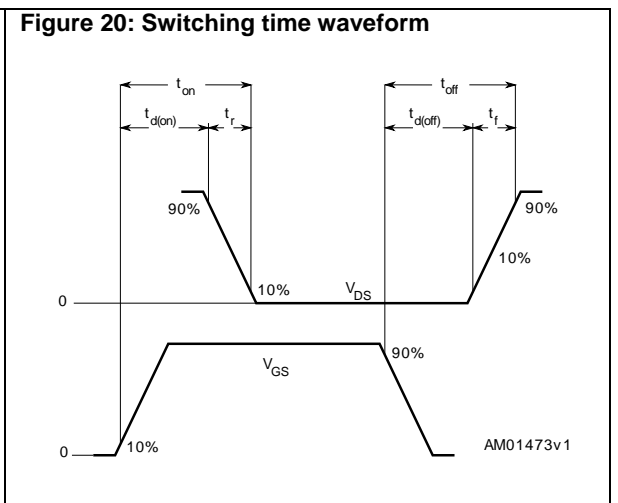
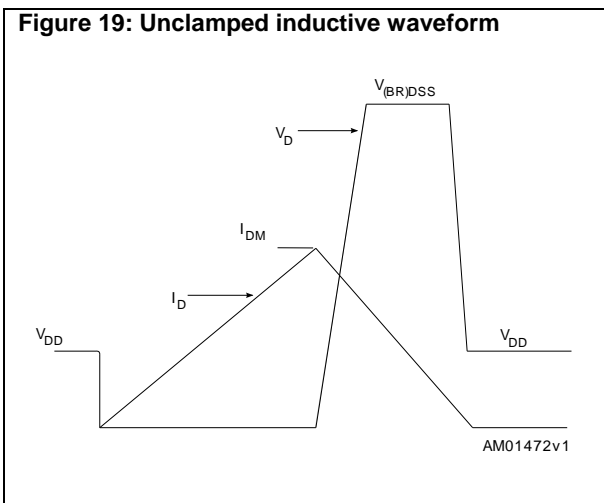
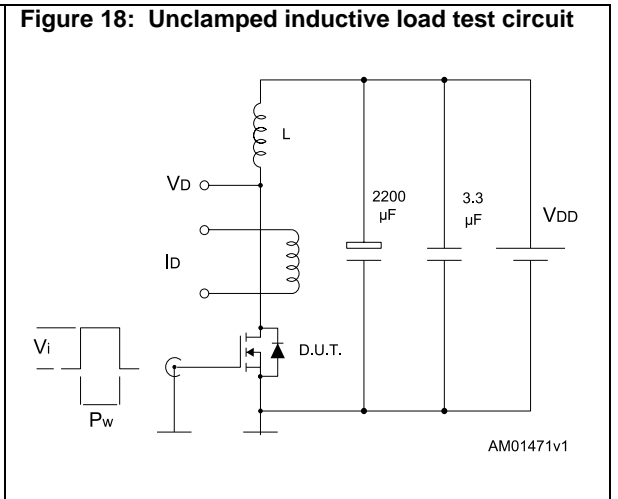
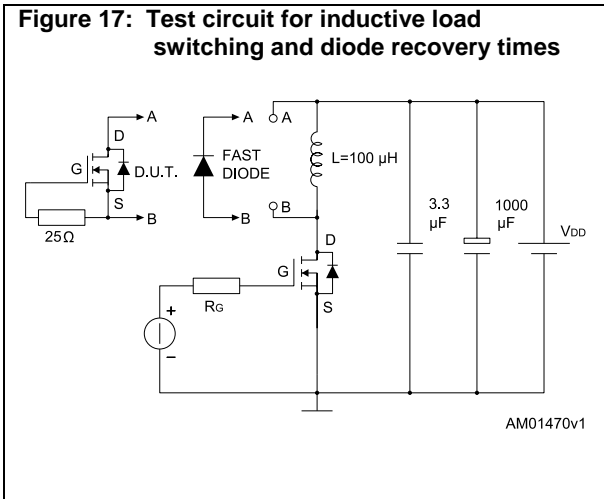
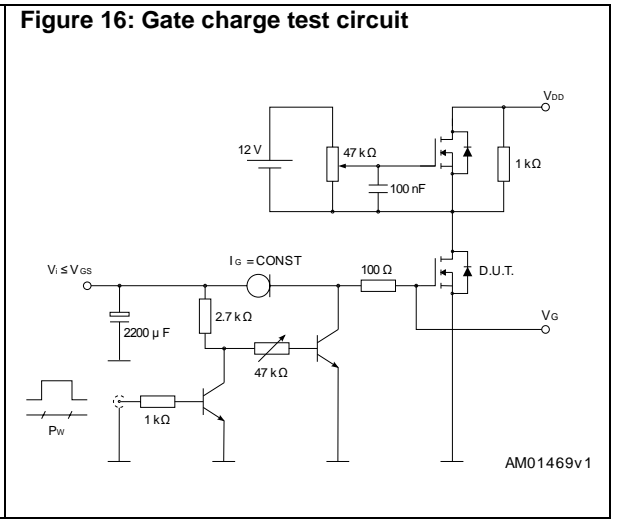
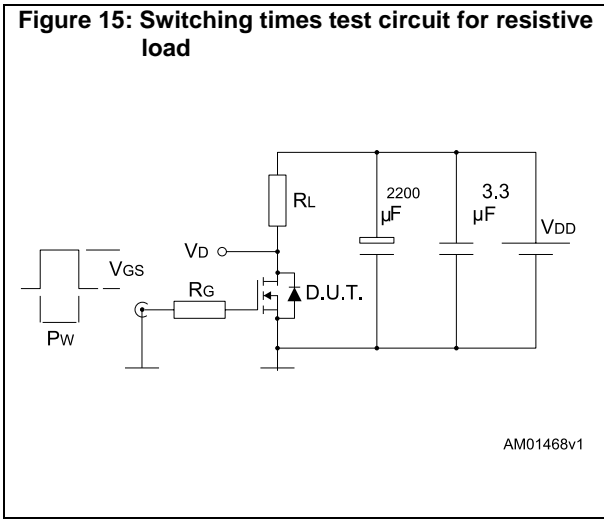
Figure 13: Source-drain diode forward characteristics







### 3 Test circuits



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 TO-220 type A package information

Figure 21: TO-220 type A package outline

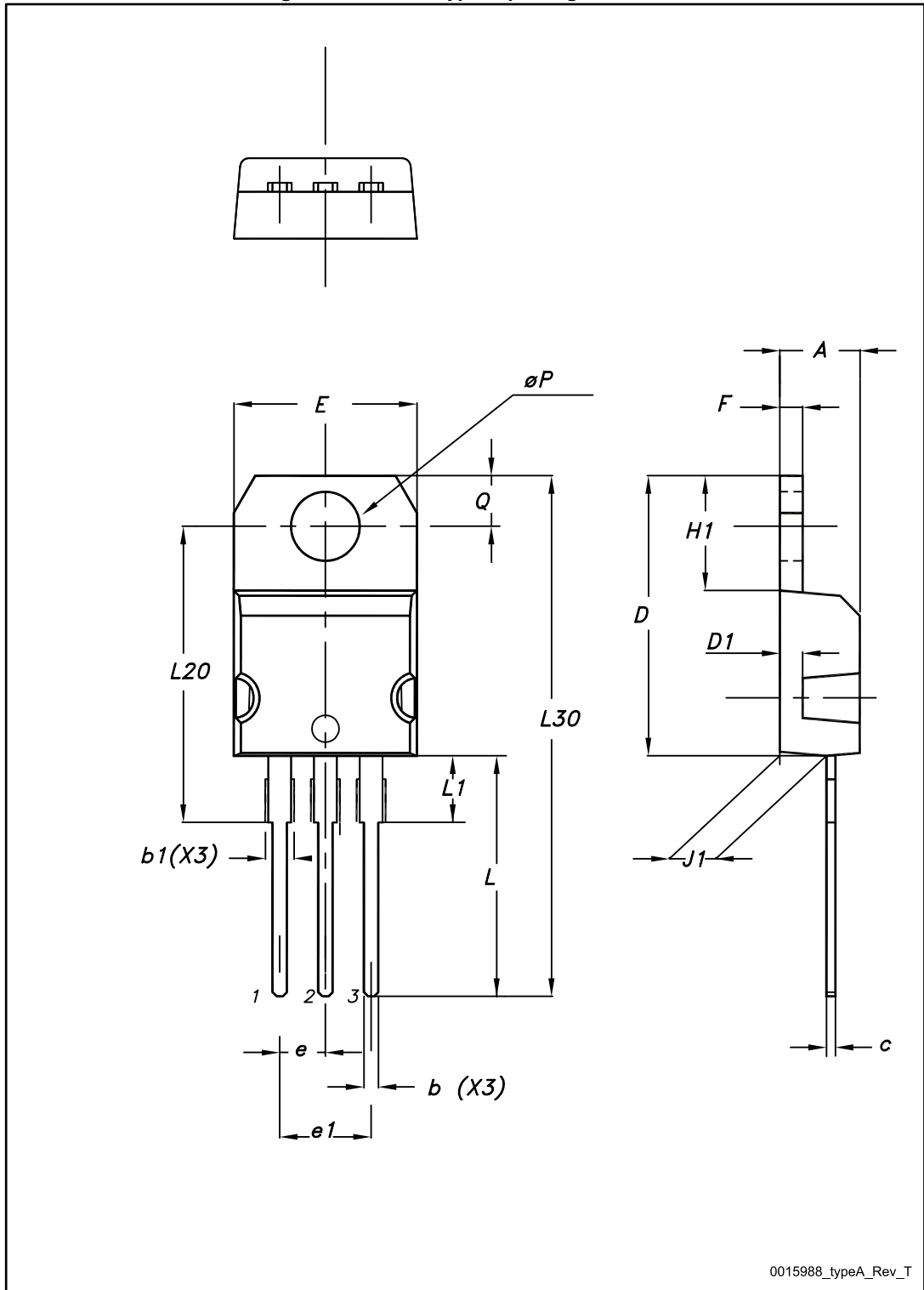


Table 10: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
01-Dec-2014	1	First release.
12-Jan-2015	2	Updated product status from "preliminary data" to "production data".

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