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FUJITSU

DATA SHEET

MB85385-60/-70/-80

CMOS 16M x 9 Fast Page Mode DRAM Module

CMOS 16,777,216 x 9 Bit Fast Page Mode DRAM Module

The Fujitsu MB85385 is a fully decoded CMOS Dynamic Random Access Memory (DRAM) module consisting of nine MB8116100 devices.
The MB85385 is optimized for those applications requiring high speed, high performance and large memory storage.
The operation and electrical characteristics of the MB85385 are the same as the MB8116100 which features fast page mode operation. For ease of memory expansion, the MB85385 is offered in a 30-pad Single In-line Memory Module package (SIMM).

See page 8.

MSS-30P-P12

See page 9.

MSS-30P-P16

PRODUCT LINE & FEATURES

Parameter	MB85385-60	MB85385-70	MB85385-80
$\overline{RAS}$ Access Time	60ns max.	70ns max.	80ns max.
Random Cycle Time	110ns max.	130ns max.	150ns max.
Address Access Time	30ns max.	35ns max.	40ns max.
$\overline{CAS}$ Access Time	15ns max.	17ns max.	20ns max.
Fast Page Mode Cycle Time	40ns max.	45ns max.	50ns max.
Power Dissipation • Operating mode	4950mW max.	4455mW max.	3960mW max.
• Standby mode	99mW max.(TTL level) / 49.5mW max.(CMOS level)		

- Organization:
  16,777,216 words x 9 bits
- Memory:
  MB8116100, 9 pcs
- Decoupling Capacitor:
  0.22 µF, 9 pcs
- Package and Ordering Information:
  30-pad SIMM, order as
  MB85385-xxPJPBK
  (PJPBK = Gold pad)
  MB85385-xxPTPB
  (PTPB = Solder pad)

PIN ASSIGNMENT
(TOP VIEW)

VCC	1
$\overline{CAS}$	2
DQ0	3
A0	4
A1	5
DQ1	6
A2	7
A3	8
VSS	9
DQ2	10
A4	11
A5	12
DQ3	13
A6	14
A7	15
DQ4	16
A8	17
A9	18
A10	19
DQ5	20
$\overline{WE}$	21
VSS	22
DQ6	23
A11	24
DQ7	25
Q8	26
$\overline{RAS}$	27
$\overline{CAS8}$	28
D8	29
VCC	30

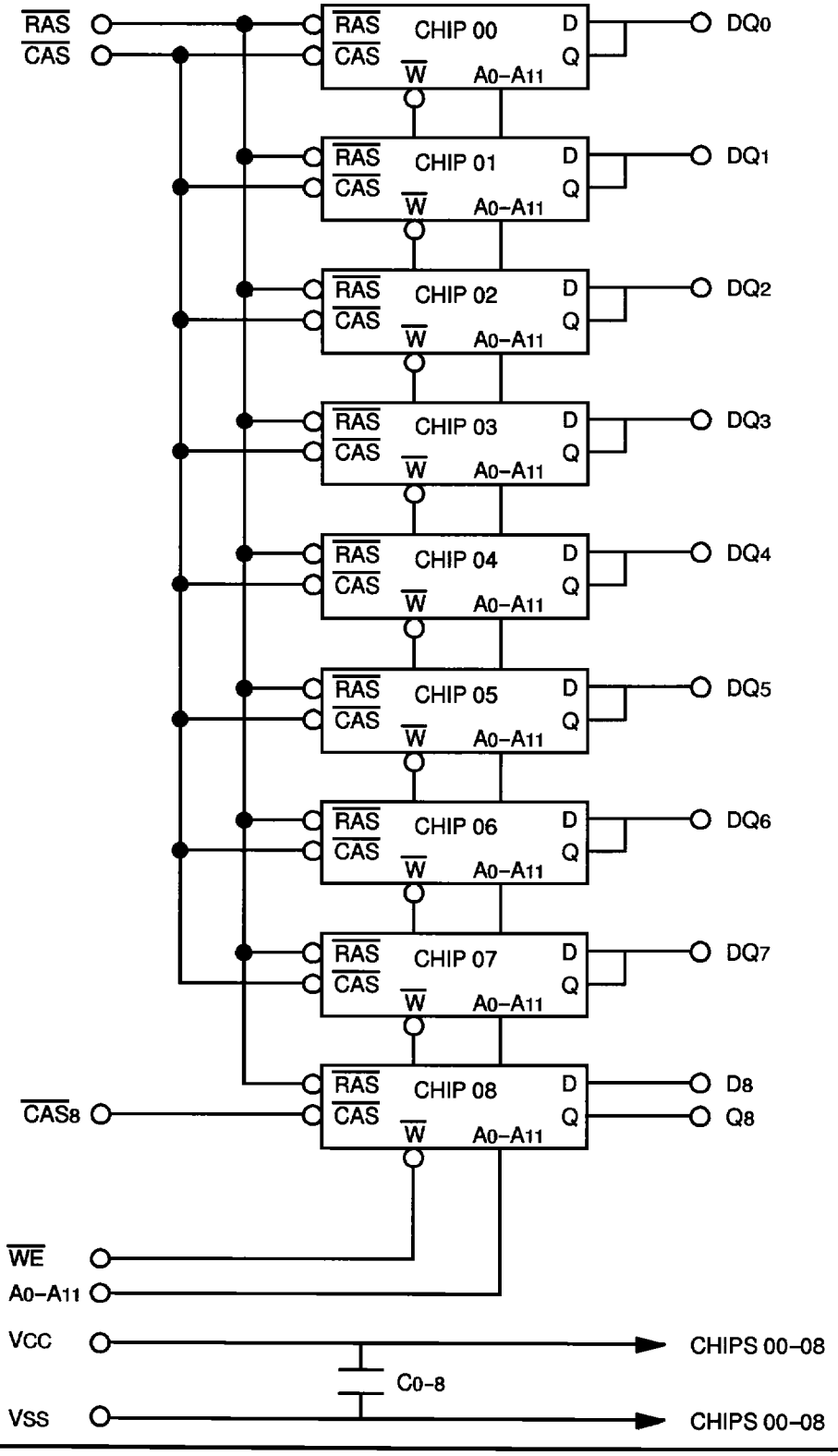
ABSOLUTE MAXIMUM RATINGS (See NOTE.)

Parameter	Symbol	Values	Unit
Supply Voltage	VCC	−1.0 to +7.0	V
Input Voltage	VIN	−1.0 to +7.0	V
Output Voltage	VOUT	−1.0 to +7.0	V
Short Circuit Output Current	IOUT	±50	mA
Power Dissipation	PD	9.0	W
Storage Temperature	TSTG	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A11	C_{IN1}	—	45	pF
Input Capacitance, $\overline{RAS}$	C_{IN2}	—	41	pF
Input Capacitance, $\overline{CAS}$	C_{IN3}	—	41	pF
Input Capacitance, $\overline{WE}$	C_{IN4}	—	44	pF
Input Capacitance, $\overline{CAS}$8	C_{IN5}	—	6	pF
Input Capacitance, D8	C_{IN6}	—	7	pF
I/O Capacitance, DQ0 to DQ7	C_{DQ}	—	14	pF
Output Capacitance, Q8	C_{OUT}	—	10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
	VSS	0	0	0	V
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V
Input Low Voltage, all inputs	V_{IL}	−0.5 *1	—	0.8	V
Operating Temperature	T_A	0	25	70 *2	°C

Notes: *1 The device will withstand undershoots to the −2.0V level with a maximum pulse width of 10ns.
*2 Maximum ambient temperature is permissible under certain conditions. See Fig. 2&3.

Fig. 2 – DERATING CURVE (Normal Cycle)

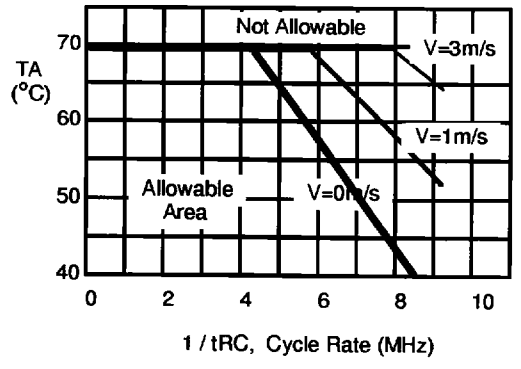
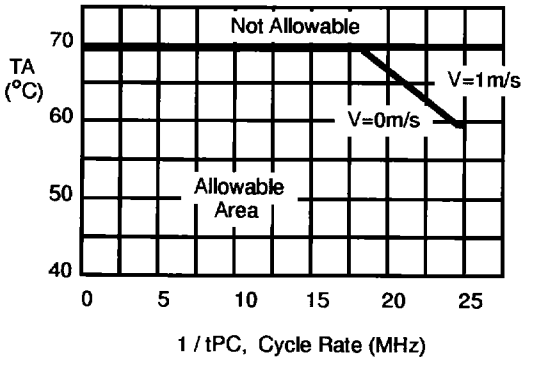


Fig. 3 – DERATING CURVE (Fast Page Cycle)



DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Paramter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output High Voltage	1	VOH	IOH = −5 mA	2.4	—	—	V
Output Low Voltage	1	VOL	IOL = 4.2 mA	—	—	0.4	V
Input Leakage Current	$\overline{CAS}$8, D8	IIL	0 V ≤ VIN ≤ 5.5V; 4.5 V ≤ VCC ≤ 5.5 V VSS = 0 V; All other pins not under test = 0 V	−10	—	10	µA
	Others			−90	—	90	µA
Output Leakage Current		IOL	0 V ≤ VOUT ≤ 5.5 V; Data out disabled	−10	—	10	µA
Operating Current (Average Power Supply Current) 2	MB85385-60	ICC1	$\overline{RAS}$ & $\overline{CAS}$ cycling; tRC = min	—	—	900	mA
	MB85385-70					810	mA
	MB85385-80					720	mA
Standby Current (Power Supply Current)	TTL level	ICC2	$\overline{RAS}$ = $\overline{CAS}$ = VIH	—	—	18	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ VCC−0.2V			9	mA
Refresh Current #1 (Average Power Supply Current) 2	MB85385-60	ICC3	$\overline{CAS}$ = VIH, $\overline{RAS}$ cycling; tRC = min	—	—	900	mA
	MB85385-70					810	mA
	MB85385-80					720	mA
Fast Page Mode Current 2	MB85385-60	ICC4	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; tPC = min	—	—	900	mA
	MB85385-70					810	mA
	MB85385-80					720	mA
Refresh Current #2 (Average Power Supply Current) 2	MB85385-60	ICC5	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; tRC = min	—	—	900	mA
	MB85385-70					810	mA
	MB85385-80					720	mA

Notes:

1. Referenced to VSS.
2. ICC depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   ICC depends on the number of address change as $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   ICC1, ICC3 and ICC5 are specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   ICC4 is specified at one time of address change during one Page cycle.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB85385-60		MB85385-70		MB85385-80		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		tREF	—	65.6	—	65.6	—	65.6	ms
2	Random Read/Write Cycle Time		tRC	110	—	130	—	150	—	ns
3	Read-Modify-Write Cycle Time	17	tRWC	130	—	152	—	175	—	ns
4	Access Time from $\overline{RAS}$	4, 7	tRAC	—	60	—	70	—	80	ns
5	Access Time from $\overline{CAS}$	5, 7	tCAC	—	15	—	17	—	20	ns
6	Column Address Access Time	6, 7	tAA	—	30	—	35	—	40	ns
7	Output Hold Time		tOH	3	—	3	—	3	—	ns
8	Output Buffer Turn on Delay Time		tON	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	8	tOFF	—	15	—	17	—	20	ns
10	Transition Time		tT	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		tRP	40	—	50	—	60	—	ns
12	$\overline{RAS}$ Pulse Width		tRAS	60	100000	70	100000	80	100000	ns
13	$\overline{RAS}$ Hold Time		tRSH	15	—	17	—	20	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		tCRP	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	9, 10	tRCD	20	45	20	53	20	60	ns
16	$\overline{CAS}$ Pulse Width		tCAS	15	—	17	—	20	—	ns
17	$\overline{CAS}$ Hold Time		tCSH	60	—	70	—	80	—	ns
18	$\overline{CAS}$ Precharge Time (C-B-R Refresh)	15	tCPN	10	—	10	—	10	—	ns
19	Row Address Setup Time		tASR	0	—	0	—	0	—	ns
20	Row Address Hold Time		tRAH	10	—	10	—	10	—	ns
21	Column Address Setup Time		tASC	0	—	0	—	0	—	ns
22	Column Address Hold Time		tCAH	15	—	15	—	15	—	ns
23	Column Address Hold Time from $\overline{RAS}$		tAR	35	—	35	—	35	—	ns
24	$\overline{RAS}$ to Column Address Delay Time	11	tRAD	15	30	15	35	15	40	ns
25	Column Address to $\overline{RAS}$ Lead Time		tRAL	30	—	35	—	40	—	ns
26	Column Address to $\overline{CAS}$ Lead Time		tCAL	30	—	35	—	40	—	ns
27	Read Command Setup Time		tRCS	0	—	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{RAS}$	12	tRRH	0	—	0	—	0	—	ns
29	Read Command Hold Time Referenced to $\overline{CAS}$	12	tRCH	0	—	0	—	0	—	ns
30	Write Command Setup Time	13	tWCS	0	—	0	—	0	—	ns
31	Write Command Hold Time		tWCH	15	—	15	—	15	—	ns
32	Write Hold Time from $\overline{RAS}$		tWCR	35	—	35	—	35	—	ns
33	$\overline{WE}$ Pulse Width		tWP	15	—	15	—	15	—	ns
34	Write Command to $\overline{RAS}$ Lead Time		tRWL	15	—	17	—	20	—	ns
35	Write Command to $\overline{CAS}$ Lead Time		tCWL	15	—	17	—	20	—	ns

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB85385-60		MB85385-70		MB85385-80		Unit
				Min	Max	Min	Max	Min	Max	
36	DIN Setup Time		tDS	0	—	0	—	0	—	ns
37	DIN Hold Time		tDH	15	—	15	—	15	—	ns
38	Data Hold Time from $\overline{RAS}$		tDHR	35	—	35	—	35	—	ns
39	$\overline{RAS}$ to $\overline{WE}$ Delay Time	17	tRWD	60	—	70	—	80	—	ns
40	$\overline{CAS}$ to $\overline{WE}$ Delay Time	17	tCWD	15	—	17	—	20	—	ns
41	Column Address to $\overline{WE}$ Delay Time	17	tAWD	30	—	35	—	40	—	ns
42	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time Low (Refresh Cycle)		tRPC	5	—	5	—	5	—	ns
43	$\overline{CAS}$ Setup Time (C-B-R Refresh)		tCSR	0	—	0	—	0	—	ns
44	$\overline{CAS}$ Hold Time (C-B-R refresh)		tCHR	10	—	12	—	15	—	ns
45	$\overline{WE}$ Setup Time from $\overline{RAS}$	16	tWSR	0	—	0	—	0	—	ns
46	$\overline{WE}$ Hold Time from $\overline{RAS}$	16	tWHR	10	—	10	—	10	—	ns
47	DIN to $\overline{CAS}$ Delay Time		tDZC	0	—	0	—	0	—	ns
48	Fast Page Mode $\overline{RAS}$ Pulse Width		tRASP	—	100000	—	100000	—	100000	ns
49	Fast Page Mode Read/Write Cycle Time		tPC	40	—	45	—	50	—	ns
50	Fast Page Mode Read-Modify-Write Cycle Time	17	tPRWC	60	—	67	—	75	—	ns
51	Access Time from $\overline{CAS}$ Precharge	7, 14	tCPA	—	35	—	40	—	45	ns
52	Fast Page Mode $\overline{CAS}$ Precharge Time		tCP	10	—	10	—	10	—	ns
51	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		tRHCP	35	—	40	—	45	—	ns
52	Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	17	tCPWD	35	—	40	—	45	—	ns

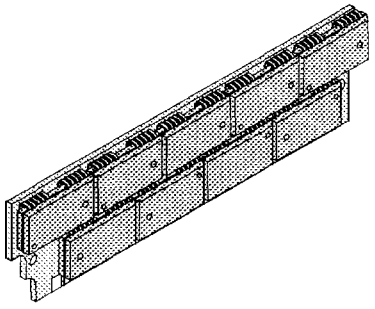
Notes:

1. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ -before-$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.
2. AC characteristics assume tT = 5ns.
3. VIH (min) and VIL (max) are reference levels for measureing the timing of input signals. Also, transition times are measured between VIH (min) and VIL (max).
4. Assumes that tRCD ≤ tRCD (max), tRAD≤ tRAD (max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will be increased by the amount that tRCD exceeds the value shown.
5. If tRCD≥ tRCD (max), tRAD≥ tRAD (max), and tASC≥ tAA- tCAC - tT, access time is tCAC.
6. If tRAD≥ tRAD (max) and tASC≤ tAA- tCAC - tT, access time is tAA.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. tOFF is specified that output buffer change to high impedance state.
9. Operation within the tRCD (max) limit ensures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, access time is controlled exclusively by tCAC or tAA.
10. tRCD (min) = tRAH (min)+ 2tT + tASC (min).
11. Operation within the tRAD (max) limit ensures that tRAC (max) can be met. tRAD (max) is specified as a reference point only; if tRAD is greater than the specified tRAD (max) limit, access time is controlled exclusively by tCAC or tAA.
12. Either tRRH or tRCH must be satisfied for a read cycle.
13. If tWCS > tWCS (min), the data output pin will remain in the high-Z state through the entire cycle.
14. tCPA is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if tCP becomes long, tCPA also becomes longer than tCPA (max).
15. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.
16. Assumes that test mode function.
17. This parameter is specified for parity bit only.

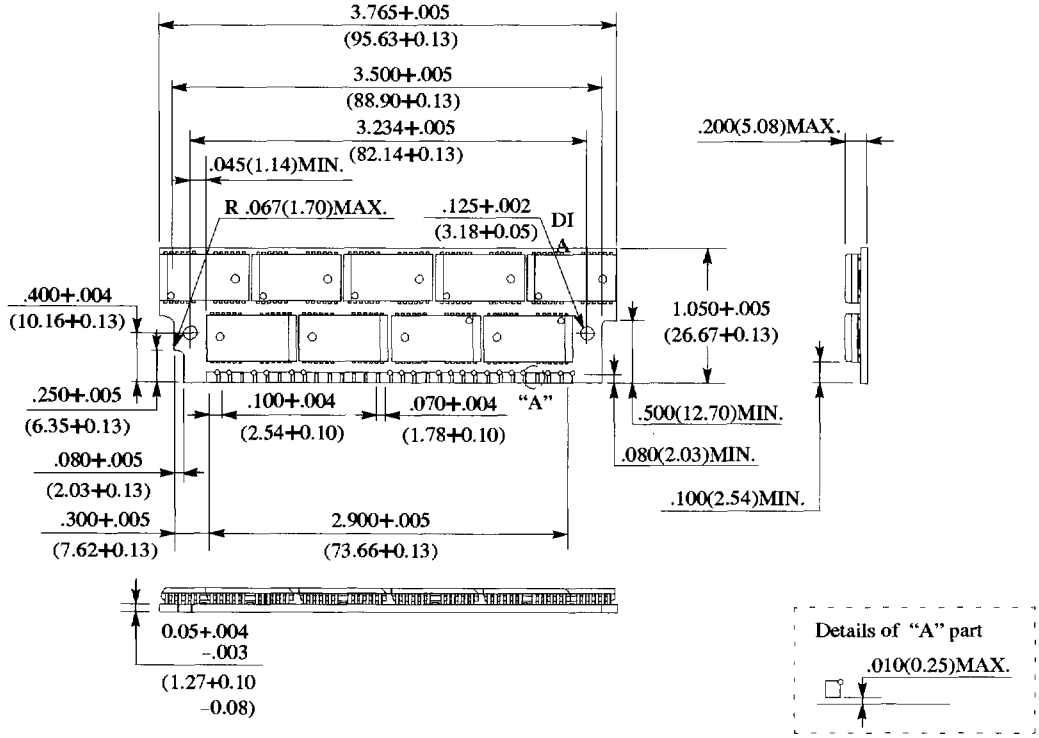
*Source: See MB8116100 Data Sheet for details on the electricals.

PACKAGE DIMENSIONS

(Suffix : PJPBK)



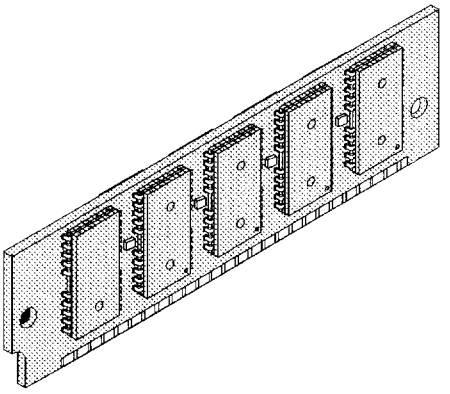
SINGLE IN-LINE TYPE MODULE 30 PIN PLASTIC
(MSS-30P-P12)



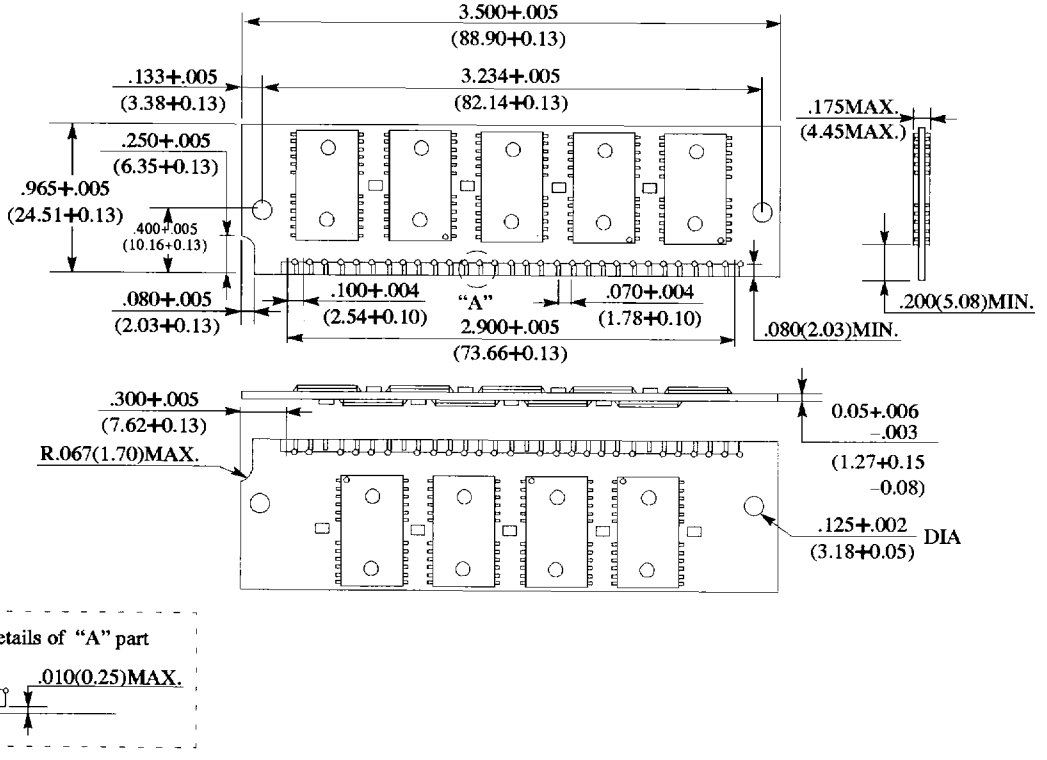
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : PTPB)



SINGLE IN-LINE TYPE MODULE 30 PIN PLASTIC
(MSS-30P-P16)



Dimensions in
inches (millimeters)

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