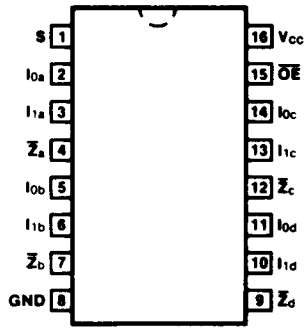
HD74AC258/HD74ACT258 • Quad 2-Input Multiplexer with 3-State Output

Description

The HD74AC258/HD74ACT258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a High on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

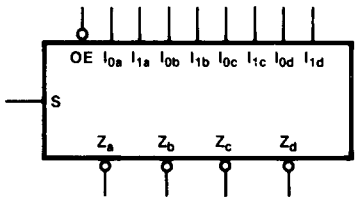
- Multiplexer Expansion by Tying Outputs Together
- Inverting 3-State Outputs
- Outputs Source/Sink 24 mA
- HD74ACT258 has TTL-Compatible Inputs

Pin Assignment



(Top View)

Logic Symbol



Pin Names

S	Common Data Select Input
$\overline{OE}$	3-State Output Enable Input
I_{0a}—I_{0d}	Data Inputs from Source 0
I_{1a}—I_{1d}	Data Inputs from Source 1
$\overline{Z}_a$—$\overline{Z}_d$	3-State Inverting Data Outputs

Functional Description

The HD74AC258/HD74ACT258 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is Low, the I_{0x} inputs are selected and when Select is High, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The HD74AC258/HD74ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$\overline{Z}_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Z}_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$\overline{Z}_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

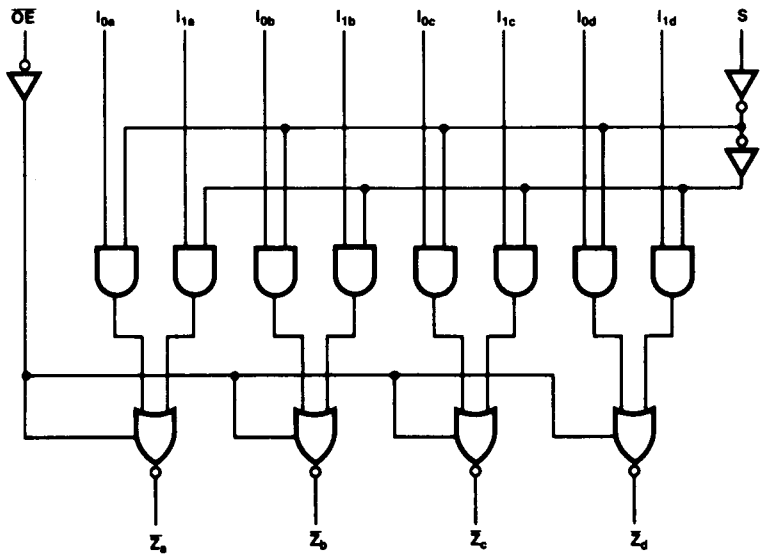
When the Output Enable input ($\overline{OE}$) is High, the outputs are forced to a high impedance state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Input		Outputs
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input (HD74ACT258)	1.5	mA	V_{IN} = V_{CC} − 2.1V, V_{CC} = 5.5V, Ta = Worst Case

AC Characteristics: HD74AC258

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay In to $\overline{Zn}$	3.3	1.0	6.0	9.5	1.0	11.0	ns
		5.0	1.0	4.5	7.5	1.0	8.5	
t_{PHL}	Propagation Delay In to $\overline{Zn}$	3.3	1.0	5.0	8.5	1.0	9.5	ns
		5.0	1.0	4.0	6.5	1.0	7.0	
t_{PLH}	Propagation Delay S to $\overline{Zn}$	3.3	1.0	7.5	12.0	1.0	14.0	ns
		5.0	1.0	6.0	9.5	1.0	10.5	
t_{PHL}	Propagation Delay S to $\overline{Zn}$	3.3	1.0	7.5	11.5	1.0	13.0	ns
		5.0	1.0	5.5	9.0	1.0	10.0	
t_{PZH}	Output Enable Time	3.3	1.0	6.0	9.5	1.0	10.5	ns
		5.0	1.0	4.5	7.5	1.0	8.5	
t_{PZL}	Output Enable Time	3.3	1.0	5.5	9.0	1.0	10.0	ns
		5.0	1.0	5.5	7.0	1.0	8.0	
t_{PHZ}	Output Disable Time	3.3	1.0	5.5	10.0	1.0	11.5	ns
		5.0	1.0	5.5	8.0	1.0	9.0	
t_{PLZ}	Output Disable Time	3.3	1.0	5.5	9.0	1.0	10.0	ns
		5.0	1.0	5.0	7.0	1.0	8.0	

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: HD74ACT258

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay In to $\overline{Z}$n	5.0	1.0	6.5	8.5	1.0	9.5	ns
t_{PHL}	Propagation Delay In to $\overline{Z}$n	5.0	1.0	5.5	7.5	1.0	8.0	ns
t_{PLH}	Propagation Delay S to $\overline{Z}$n	5.0	1.0	7.5	10.5	1.0	11.5	ns
t_{PHL}	Propagation Delay S to $\overline{Z}$n	5.0	1.0	7.0	9.5	1.0	11.0	ns
t_{PZH}	Output Enable Time	5.0	1.0	6.5	8.5	1.0	9.5	ns
t_{PZL}	Output Enable Time	5.0	1.0	6.5	8.5	1.0	9.5	ns
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	9.0	1.0	10.0	ns
t_{PLZ}	Output Disable Time	5.0	1.0	6.0	8.0	1.0	9.0	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	55.0	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

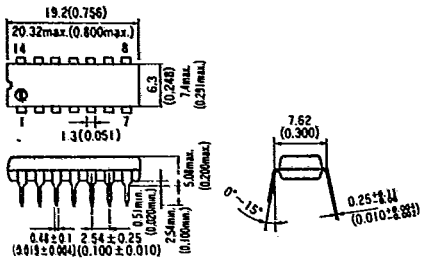
• Package code of Advanced CMOS Logic

HD74AC XXXX P

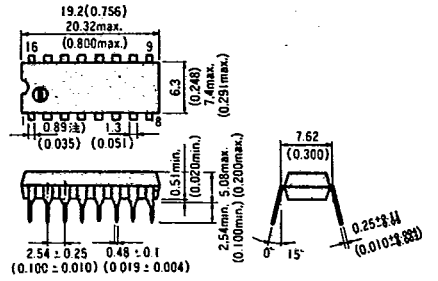
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

14 Pin type



16 Pin type



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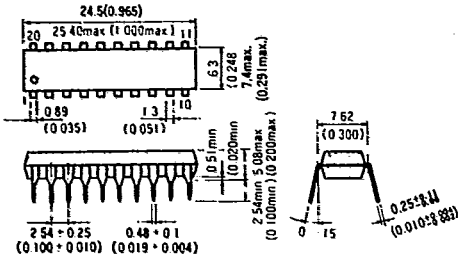
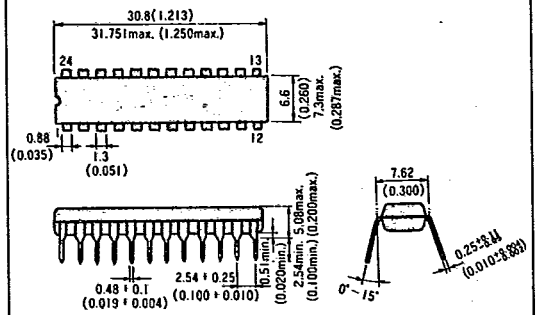


24 Pin type



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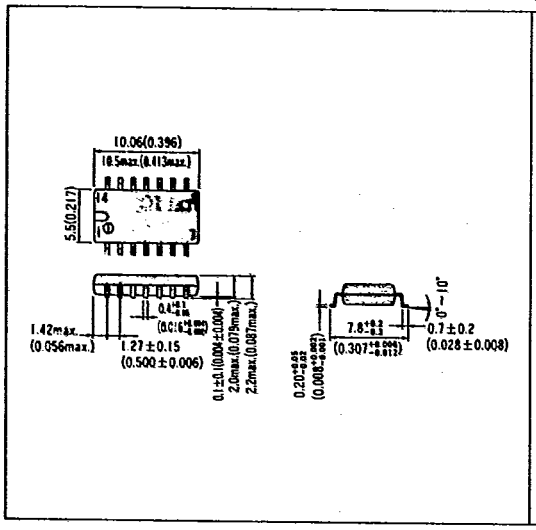
Package Information

Small Outline Package [Unit: mm (inch)]

14 Pin type



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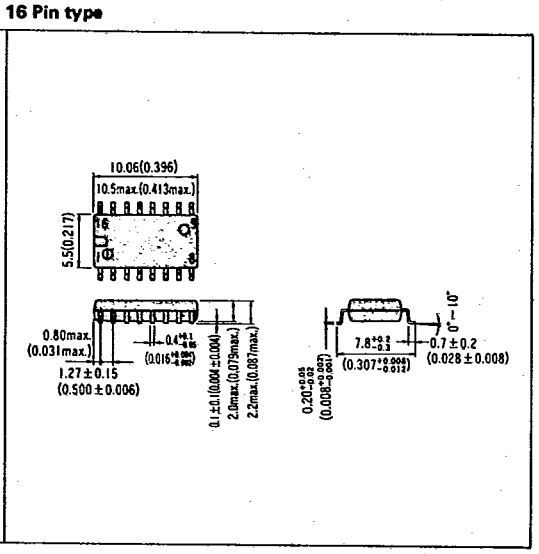

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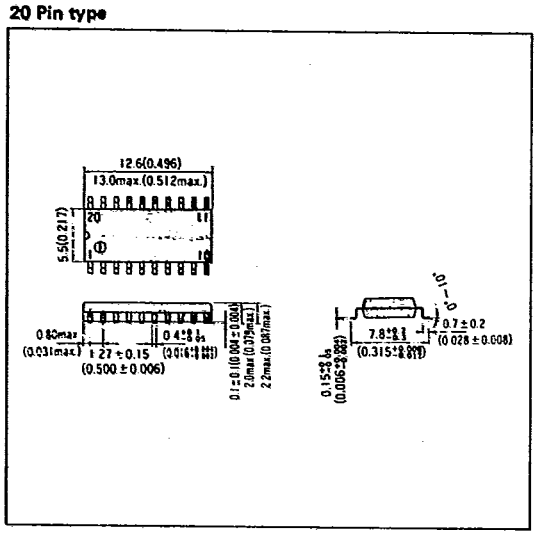

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