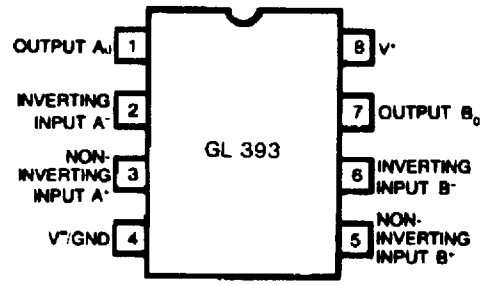
GL393/393A
LOW POWER, LOW OFFSET VOLTAGE DUAL COMPARATORS

Description

The GL393 consists of two independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected pnp input stage allows the input common-mode voltage to include ground.

Pin Configuration



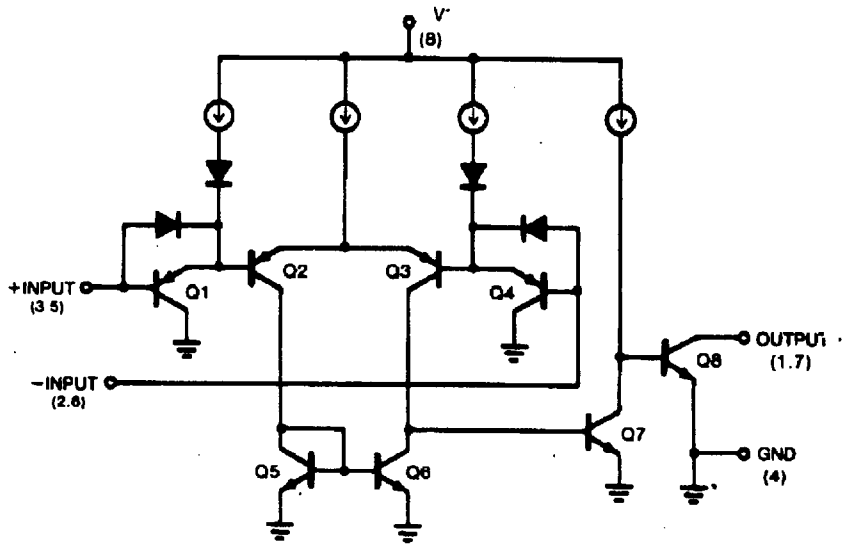
Features

- **Single Supply Operation +2.0V to +36V**
- **Dual Supply Operation ±1.0V to ±18V**
- **Compatible with All forms of Logic**
- **Allow Comparison of Voltages Near Ground Potential**
- **Low Current Drain 400 μA TYP**
- **Low Input Bias Current 25nA TYP**
- **Low Input Offset Current ±5 nA TYP**
- **Low Offset Voltage ±2mV**

Absolute Maximum Ratings

Supply Voltage, V⁺	+36V or ±18V
Differential Input Voltage	36V
Input Voltage Range	−0.3V to +36V
Power Dissipation	500mW
Input Current (V_{IN}<−0.3V)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature	260°C

Shematic Diagram



Electrical Characteristics: $V^+ = 5V$ $T_A = 25°C$, unless otherwise specified)

PARAMETER	Test Conditions	GL393			GL393A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	At out. switch point $V_O = 1.4$; $R_s = 0$		±2	±5		±1	±2	mV
	$V_{REF} = 1.4V$ $0°C \leq T_A \leq 70°C$			9			4	
Input Bias Current (1)	Output in linear range		25	250		25	250	nA
	$0°C \leq T_A \leq 70°C$			400			400	
Input Offset Current			±5	±50		±5	±50	nA
	$0°C \leq T_A \leq 70°C$			±150			±150	
Input Common-Mode Voltage Range (2)		0		V^+-1.5	0		V^+-1.5	V
	$0°C \leq T_A \leq 70°C$	0		V^+-2	0		V^+-2	
Supply Current	$R_L = \infty$		0.4	1		0.4	1	mA
Supply Current	$V_{CC} = 30V$, $R_L = \infty$			2.5			2.5	mA
Voltage Gain	$R_L \geq 15K\Omega$, $V^+ = 15V$	93	106		93	106		dB
Large Signal Response Time	V_{IN} = TTL logic swing; $V_{REF} = +1.4V$; $R_L = 5.1K\Omega$ $V_{RL} = 5V$		300			300		ns
Response Time (3)	$V_{RL} = 5V$; $R_L = 5.1k\Omega$		1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geq 1V$; $V_{IN(+)} = 0V$; $V_O \leq 1.5V$	6	16		6	16		mA
Output Saturation	$V_{IN(-)} \geq 1V$ $V_{IN(+)} = 0V$		150	400		150	400	mV
	$I_{sink} \leq 4mA$ $0°C \leq T_A \leq 70°C$			700			700	
Output Leakage	$V_{IN(+)} \geq 1V$ $V_{IN(-)} = 0V$		0.1			0.1		nA
	$0°C \leq T_A \leq 70°C$			1000			1000	
Differential Input Voltage	All $V_{IN} \geq 0V$ (or V^- if split supply is used) $0°C \leq T_A \leq 70°C$			V^+			V^+	V

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This conditions is not destructive providing the input current is limited to less than 50mA.

(3) The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300 nsec can be obtained.

Typical Performance Curves

Figure 1– Supply Current

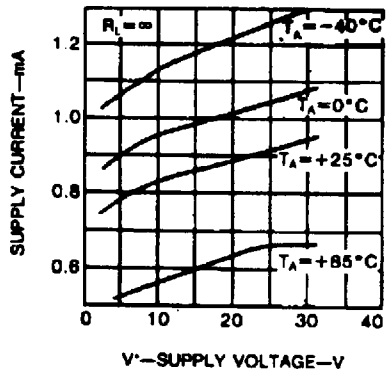


Figure 2– Input Current

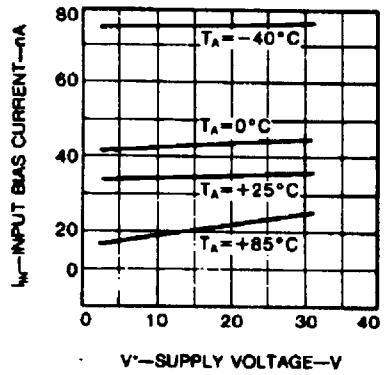


Figure 3–Output Saturation Voltage

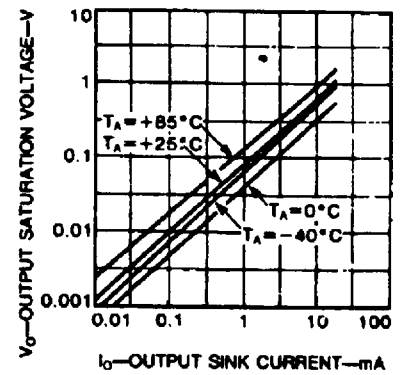


Figure 4 – Response Time for Various Input Overdrives Negative Transition

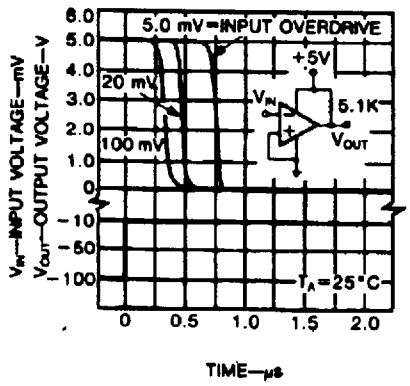
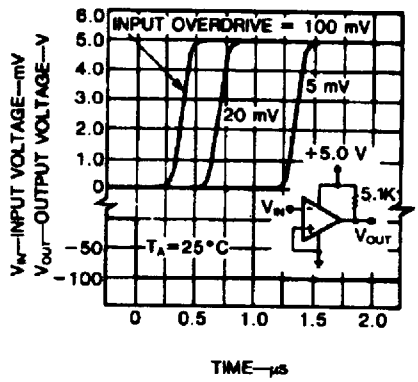


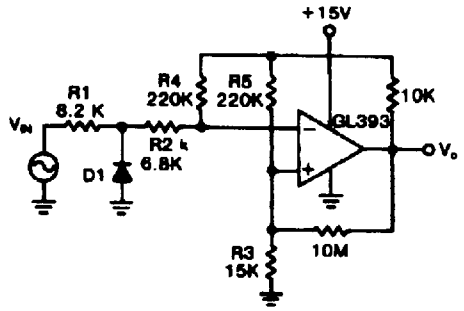
Figure 5– Response Time for Various Input Overdrives Positive Transition



Applications

These dual comparators feature high gain, wide band width characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capactiance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10kΩ should be used. The addition of positive feedback (<10mV) is also recommended. It is good design practice to ground all unused pins. Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than −0.3V should not be used.

Figure 6-Zero Crossing Detector (Single Supply)



D1 prevents input from going negative by more than 0.6V

R1+R=R3

$R3 \leq \frac{R5}{10}$ for small error in zero crossing

Figure 7-Zero Crossing Detector (Split Supplies)

$V_{IN\ MIN} \approx 0.4$ peak for 1% phase distortion ($\Delta\theta$)

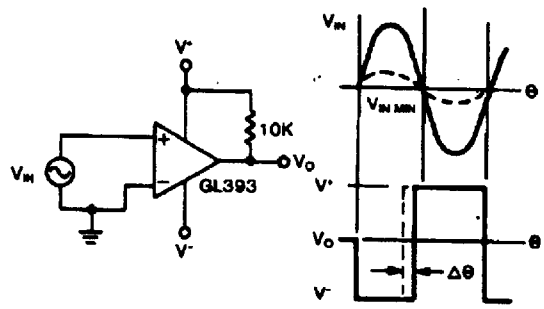


Figure 8-Free-Running Square-Wave Oscillator

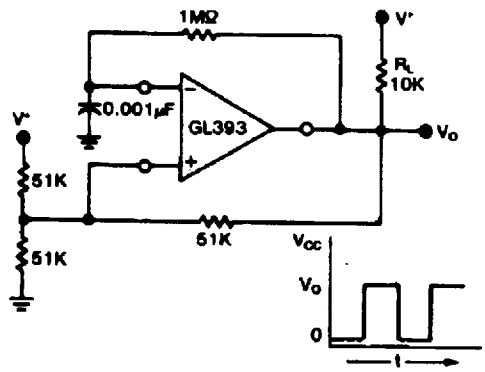
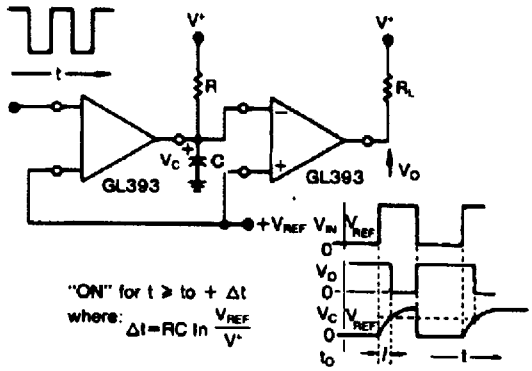


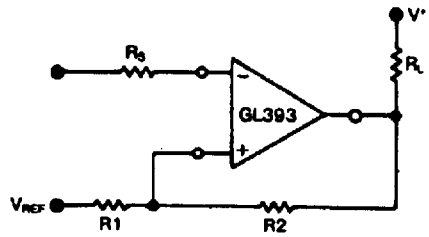
Figure 9-Time Delay Generator



"ON" for $t \geq t_o + \Delta t$

where: $\Delta t = RC \ln \frac{V_{REF}}{V^+}$

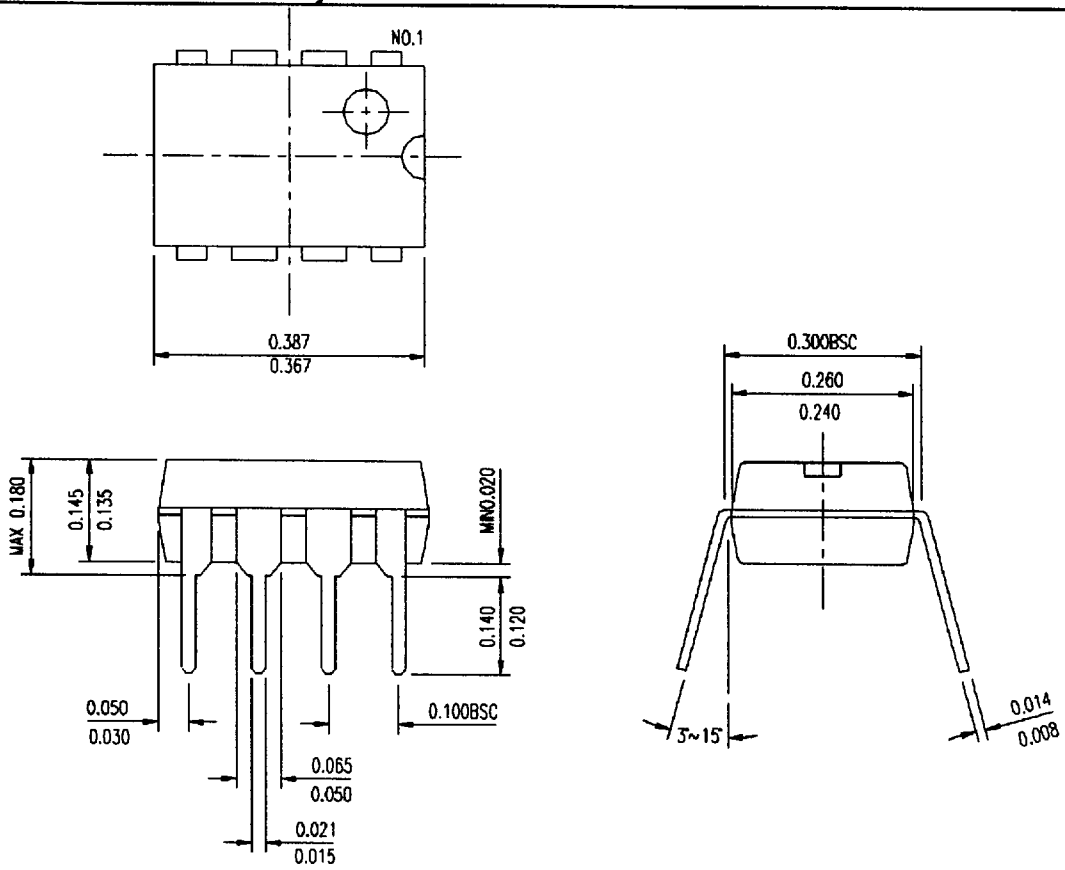
Figure 10-Comparator With Hysteresis



$R_S = R1 \parallel R2$

$$V_{th1} = V_{REF} + \frac{(V_{CC} - V_{REF})\ R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{REF} + \frac{(V_{REF} - V_{O\ Low})\ R1}{R1 + R2 + R_L}$$


NO.1
0.387
0.367
MAX 0.180
0.145
0.135
MIN0.020
0.140
0.120
0.050
0.030
0.100BSC
0.065
0.050
0.021
0.015
0.300BSC
0.260
0.240
3~15°
0.014
0.008