HM10S611G

240Ch. , 64 Gray Scale Color
TFT LCD SOURCE DRIVER

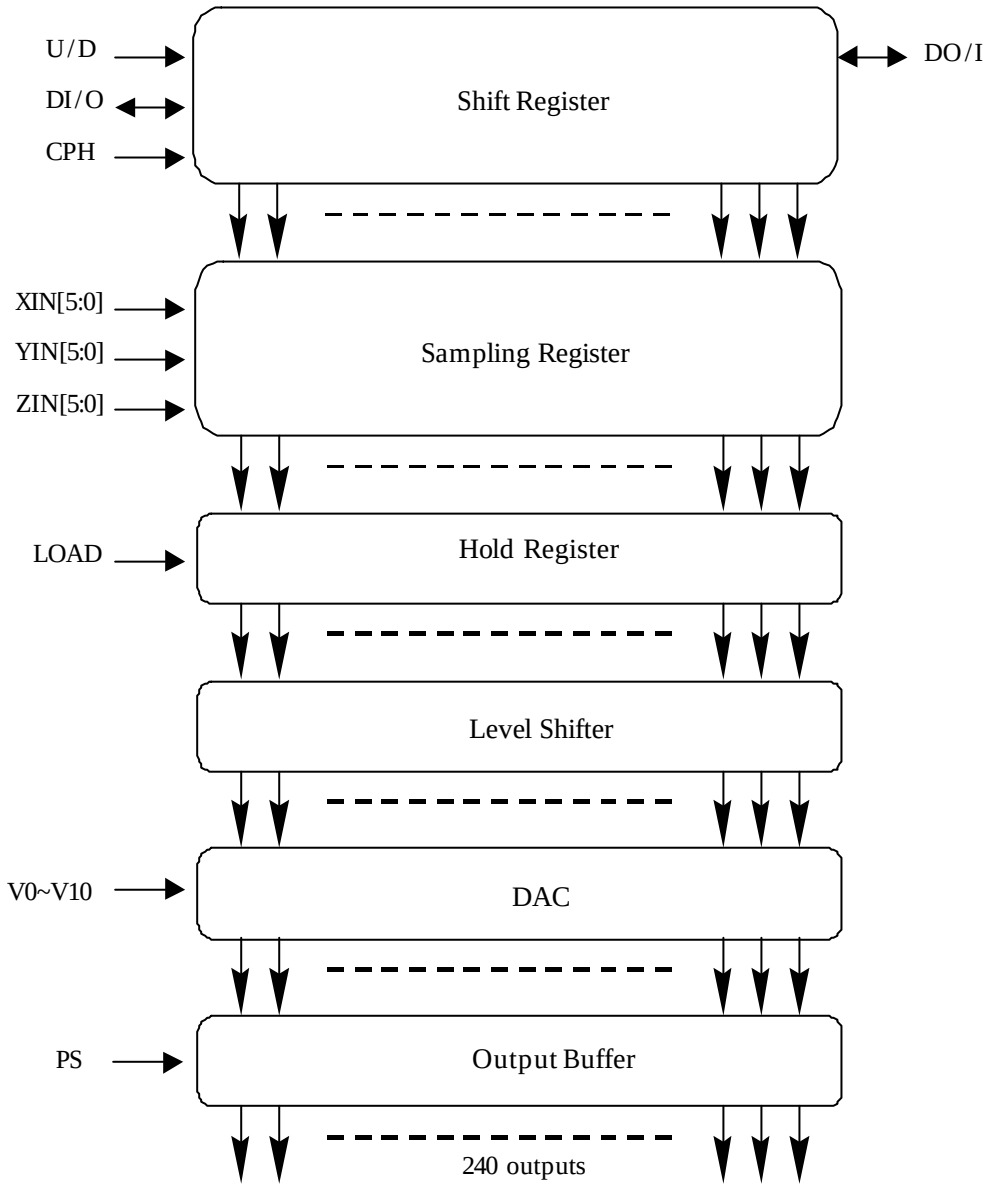
1. OVERVIEW

The driver is 6bit, 240 channel column designed for low power TFT LCD Panel applications. The driver's alternative shift direction makes it easy to integrate the chip on the panel.

2. FEATURES

- 6-bit graphic data , internal DAC
- 240 outputs to driving liquid crystal panel
- 11 external reference voltages to support gamma correction
  - Only 2 reference voltages of ends can support gamma correction
- Maximum 30MHz operation
- Support cascade connection
- Support output for LCD driving direction
- Digital supply voltage, DVDD, 2.5 ~ 3.6 V
- Analog supply voltage, AVDD, 5.0±0.5V
- P-type silicon substrate, CMOS process

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

PIN	I/O	FUNCTION	
XIN[5:0] YIN[5:0] ZIN[5:0]	I	Image Data	The data inputs consist of 6-bit for three each channels. At the rising edge of CPH, each 6-bit data for three adjacent channels are loaded in parallel.
DI/O DO/I	I/O	Chip Enable	Start pulse I/O of address shift register. U/D = H, DI/O : input DO/I : output U/D = L, DO/I : input DI/O : output
U/D	I	Shift Direction	Controls the direction in which the data is loaded into the input register. When U/D = 'H', the data are loaded from channel output X01,Y01,Z01 to output X80, Y80, Z80. When U/D = 'L', the data are loaded from channel output X80, Y80, Z80 to output X01,Y01,Z01.
CPH	I	Clock	The clock synchronizes the 18-bit (three 6-bit channels) data sampling, and synchronizes the internal control logic of the HM10S611G. All data is loaded and moved on at rising edge of CPH.
AVDD	I	Analog Power	Power supply for analog block.
DVDD	I	Digital Power	Power supply for digital block.
VSS	I	Ground	Common ground
V10 ~ 0	I	γ - Correction Voltage	Reference voltage for γ correction of DAC circuit.
LOAD	I	Load Pulse	LOAD pulse transfer the data from sampling register to hold register. The transfer happens after finishing to load the 6bit data into sampling register for all each channels. Then a analog voltage outputs from output buffer as soon.
X01 ~ X80 Y01 ~ Y80 Z01 ~ Z80	O	LCD Panel Drive	LCD Panel Driving Terminal Analog Voltage Output
TESTB	I	Test pin	TESTB pin is tied to DVDD
PS	I	Power Save	Power saving mode. PS = " L " : Normal operation PS = " H " : Hi-Z state (Output Buffer is disable)

5. FUNCTIONAL DESCRIPTIONS

5.1 Data Input

DI/O,DO/I = "H" is loaded into the address shift register on the rising edge of CPH(n).

18bit(6bit x X,Y,Z) data are loaded into sampling register on the rising edge of CPH(n+1).

When LOAD = "H" after the rising edge of CPH(n+80), the data in each sampling register are transfered to hold register and the HM10S611G outputs analog voltage signal through output buffer.

5.2 Extension of Output

By cascade connection of this device, Enlargement of driving data is available and as a result it can be used to a larger size screen.

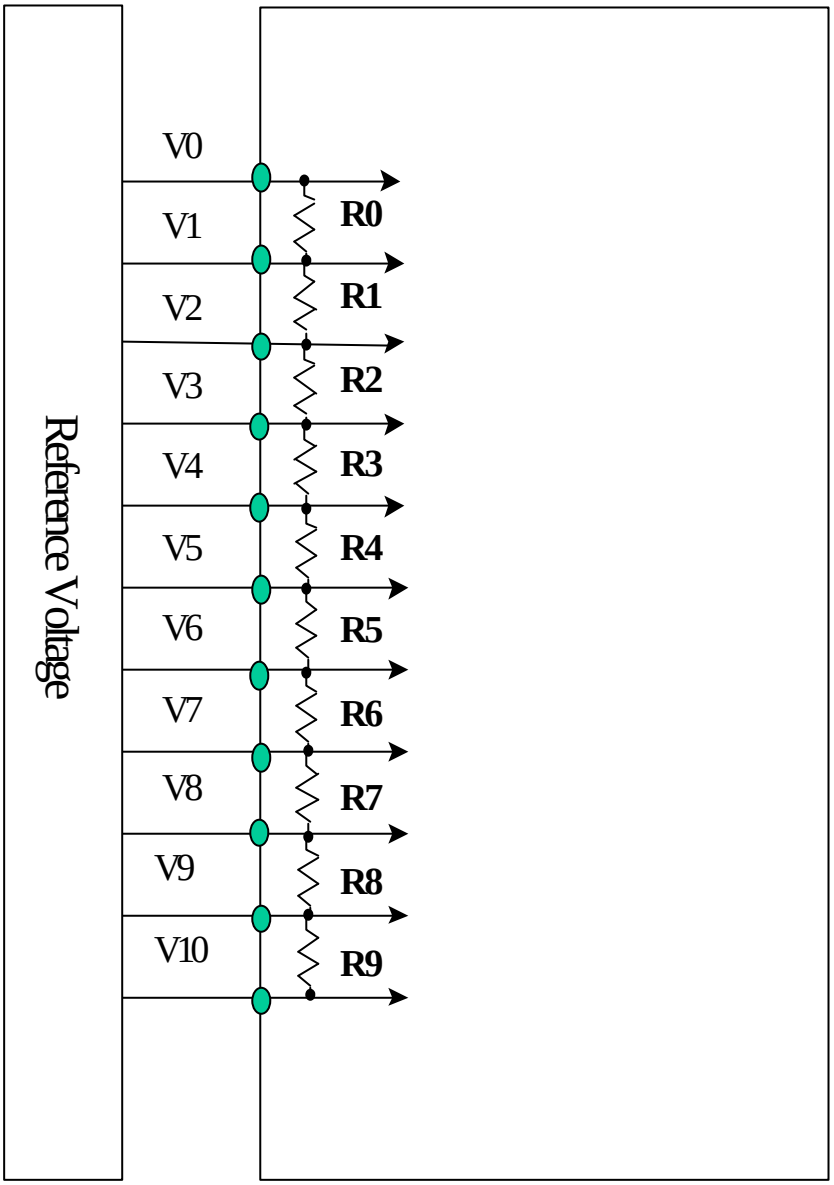
א U/D = " L "

DI/O pin of the former chip is connected to DO/I pin of the next chip. The other input pins except DI/O and DO/I is connected commonly to each device.

ℑ U/D = " H "

DO/I pin of the former chip is connected to DI/O pin of the next chip. The other input pins except DO/I and DI/O is connected commonly to each device

5.3 g - Correction Input Circuit



5.4 Input Data Value and Output Voltage

Output voltage is determined by input data value and 11 reference voltage (V10 ~ V0).

And The relationship between input data value and output voltage is as follows.

(1) Reference voltage input for γ - Correction (V10 ~ V0)

This external voltage is reference voltage extracted from panel characteristics.

(2) Contents of image data

MSB					LSB
wIN5	wIN4	wIN3	wIN2	wIN1	wIN0

| <----------> | <----------> |

Voltage selection for γ - Correction (Vn ~ Vn+1)

D/A conversion (Divide Vn ~ Vn+1 into 7 or 8)

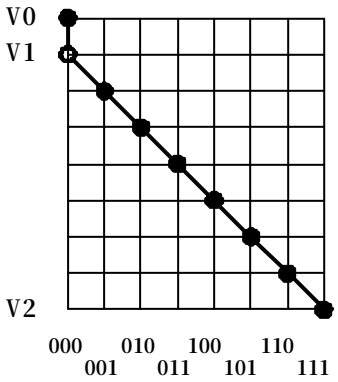
** w in wIN5 ~ 0 is one of X,Y,Z.

- γ - Correction Voltage

wIN5	wIN4	wIN3	γ-Correction Voltage
0	0	0	V0 or V1~V2
0	0	1	V2~V3
0	1	0	V3~V4
0	1	1	V4~V5
1	0	0	V5~V6
1	0	1	V6~V7
1	1	0	V7~V8
1	1	1	V8~V9 or V10

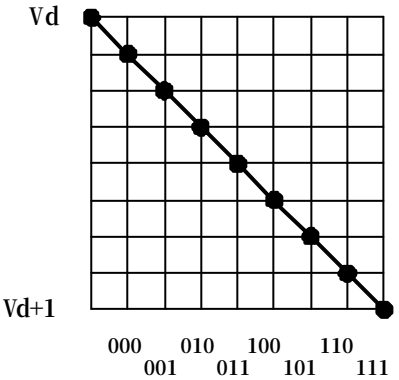
- D/A Conversion

(wIN5,wIN4,wIN3)=(0.0.0)



(wIN2,wIN1,wIN0)

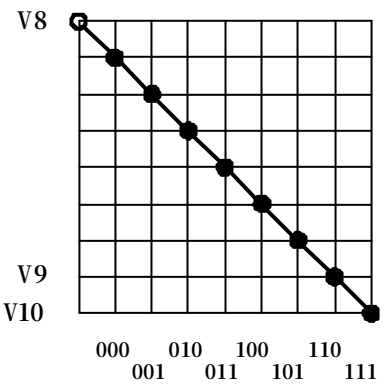
(wIN5,wIN4,wIN3)=(0.0.1) ~ (1,1,0)



(wIN2,wIN1,wIN0)

*d=2~7

(wIN5,wIN4,wIN3)=(1,1.1)



(wIN2,wIN1,wIN0)

Relation with Input Data & Output Voltage

Input Data	Output Voltage
0	V0
No Data	V1
1	V2+(V1-V2) * 6/7
2	V2+(V1-V2) * 5/7
3	V2+(V1-V2) * 4/7
4	V2+(V1-V2) * 3/7
5	V2+(V1-V2) * 2/7
6	V2+(V1-V2) * 1/7
7	V2
8	V3+(V2-V3) * 7/8
9	V3+(V2-V3) * 6/8
A	V3+(V2-V3) * 5/8
B	V3+(V2-V3) * 4/8
C	V3+(V2-V3) * 3/8
D	V3+(V2-V3) * 2/8
E	V3+(V2-V3) * 1/8
F	V3
10	V4+(V3-V4) * 7/8
11	V4+(V3-V4) * 6/8
12	V4+(V3-V4) * 5/8
13	V4+(V3-V4) * 4/8
14	V4+(V3-V4) * 3/8
15	V4+(V3-V4) * 2/8
16	V4+(V3-V4) * 1/8
17	V4
18	V5+(V4-V5) * 7/8
19	V5+(V4-V5) * 6/8
1A	V5+(V4-V5) * 5/8
1B	V5+(V4-V5) * 4/8
1C	V5+(V4-V5) * 3/8
1D	V5+(V4-V5) * 2/8
1E	V5+(V4-V5) * 1/8

Input Data	Output Voltage
1F	V5
20	V6+(V5-V6) * 7/8
21	V6+(V5-V6) * 6/8
22	V6+(V5-V6) * 5/8
23	V6+(V5-V6) * 4/8
24	V6+(V5-V6) * 3/8
25	V6+(V5-V6) * 2/8
26	V6+(V5-V6) * 1/8
27	V6
28	V7+(V6-V7) * 7/8
29	V7+(V6-V7) * 6/8
2A	V7+(V6-V7) * 5/8
2B	V7+(V6-V7) * 4/8
2C	V7+(V6-V7) * 3/8
2D	V7+(V6-V7) * 2/8
2E	V7+(V6-V7) * 1/8
2F	V7
30	V8+(V7-V8) * 7/8
31	V8+(V7-V8) * 6/8
32	V8+(V7-V8) * 5/8
33	V8+(V7-V8) * 4/8
34	V8+(V7-V8) * 3/8
35	V8+(V7-V8) * 2/8
36	V8+(V7-V8) * 1/8
37	V8
38	V9+(V8-V9) * 6/7
39	V9+(V8-V9) * 5/7
3A	V9+(V8-V9) * 4/7
3B	V9+(V8-V9) * 3/7
3C	V9+(V8-V9) * 2/7
3D	V9+(V8-V9) * 1/7
3E	V9
3F	V10

5.6 g - Correction Resistor Ratio

R0	R1	R2	R3	R4	R5	R6	R7	R8	R9
1.00	2.00	2.77	1.50	0.90	0.84	0.66	0.84	1.42	1.05

6. ABSOLUTE MAXIMUM RATING

Parameter		Symbol	Value	Unit
Supply Voltage Range	DVDD	DVDD	-0.3 ~ + 6.5	V
	AVDD	AVDD	-0.3 ~ + 6.5	V
Input Voltage Range	V0 ~ V10	VI	-0.3 ~ + AVDD +0.3	V
	Others	VI	-0.3 ~ + DVDD +0.3	V
Output Voltage Range	DI/O, DO/I	VO	-0.3 ~ + DVDD +0.3	V
	X01 ~ X80 Y01 ~ Y80 Z01 ~ Z80	VO	-0.3 ~ + AVDD +0.3	V
Storage Temp. Range		Tstg	-55 ~ + 125	℃

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7. RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	DVDD		2.5		3.6	V
	AVDD		4.5		5.5	V
Reference voltage (Note)	V0 ~ V10		0		AVDD	V
Output Load	C_L				150	pF/PIN
Clock	f_{CPH}		DC		30	MHz
Operating Temp.	Topr		-20		75	℃

Note : Relation of each reference voltage

$VSS \leq V0 \leq V1 \leq V2 \leq V3 \leq V4 \leq V5 \leq V6 \leq V7 \leq V8 \leq V9 \leq V10 \leq AVDD$,

$AVDD \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V6 \geq V7 \geq V8 \geq V9 \geq V10 \geq VSS$

8. ELECTRICAL CHARACTERISTICS

8.1 DC Characteristics

(VSS = 0 , DVDD = 2.5 ~ 3.6V , AVDD = 5.0±10%V, Ta = -20℃~ +75℃)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	PIN
Input Low Current	I_{ILL1}				10	μA	Note1
	I_{ILL2}				400	μA	TESTB
Input High Current	I_{IH}				10	μA	Note2
Input Low Voltage	V_{IL}		VSS		0.3x DVDD	V	Note3
Input High Voltage	V_{IH}		0.7x DVDD		DVDD	V	
Output Low Voltage	V_{OL}	I_{OL}=0.1mA	VSS		VSS + 0.5	V	DI/O
Output High Voltage	V_{OH}	I_{OH}=-0.1mA	DVDD– 0.5		DVDD	V	DO/I
Current Consumption (operating)	DIDD1	Note4		0.4	1	mA	DVDD- VSS
Current Consumption (standby)	DIDD2	Note5			1	mA	DVDD– VSS
Current Consumption (operating)	AIDD1	Note4		3.4	4.5	mA	AVDD– VSS
Current Consumption (standby)	AIDD2	Note5			4.5	mA	AVDD– VSS
Current Consumption (Power save)	AIDD3	Note6			100	μA	AVDD- VSS
Output voltage range	V_{OUT}		VSS + 0.1		AVDD - 0.1	V	X01 ~ X80
Pin to pin variation	V_{DO}		-20		20	mV	Y01 ~ Y80
Output off current	I_{OFF}	Note6			10	μA	Z01 ~ Z80

Note1, XIN0~XIN5, YIN0~YIN5, ZIN0~ZIN5, DI/O, DO/I, CPH, LOAD, PS, U/D

Note2, XIN0~XIN5, YIN0~YIN5, ZIN0~ZIN5, DI/O, DO/I, CPH, LOAD, PS, U/D, TESTB

Note3, XIN0~XIN5, YIN0~YIN5, ZIN0~ZIN5, DI/O, DO/I, CPH, LOAD, PS

Note4, DVDD=3.6V, AVDD=5.5V, f_{CPH} = 30MHz, 1H = 100 μs, No Load

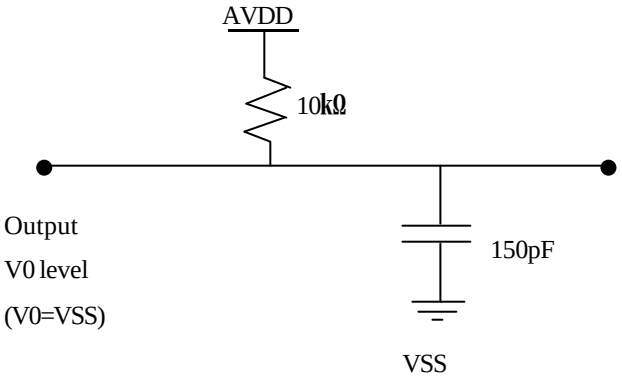
Note5, AVDD=5.5V, f_{CPH} = 30MHz, 1H = 100 μs, DI/O : "Low"

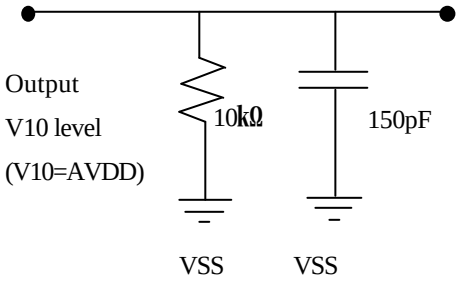
Note6, AVDD=5.5V, PS="High", f_{CPH} = 30MHz, 1H = 100 μs, DI/O : "Low"

8.2 AC Characteristics

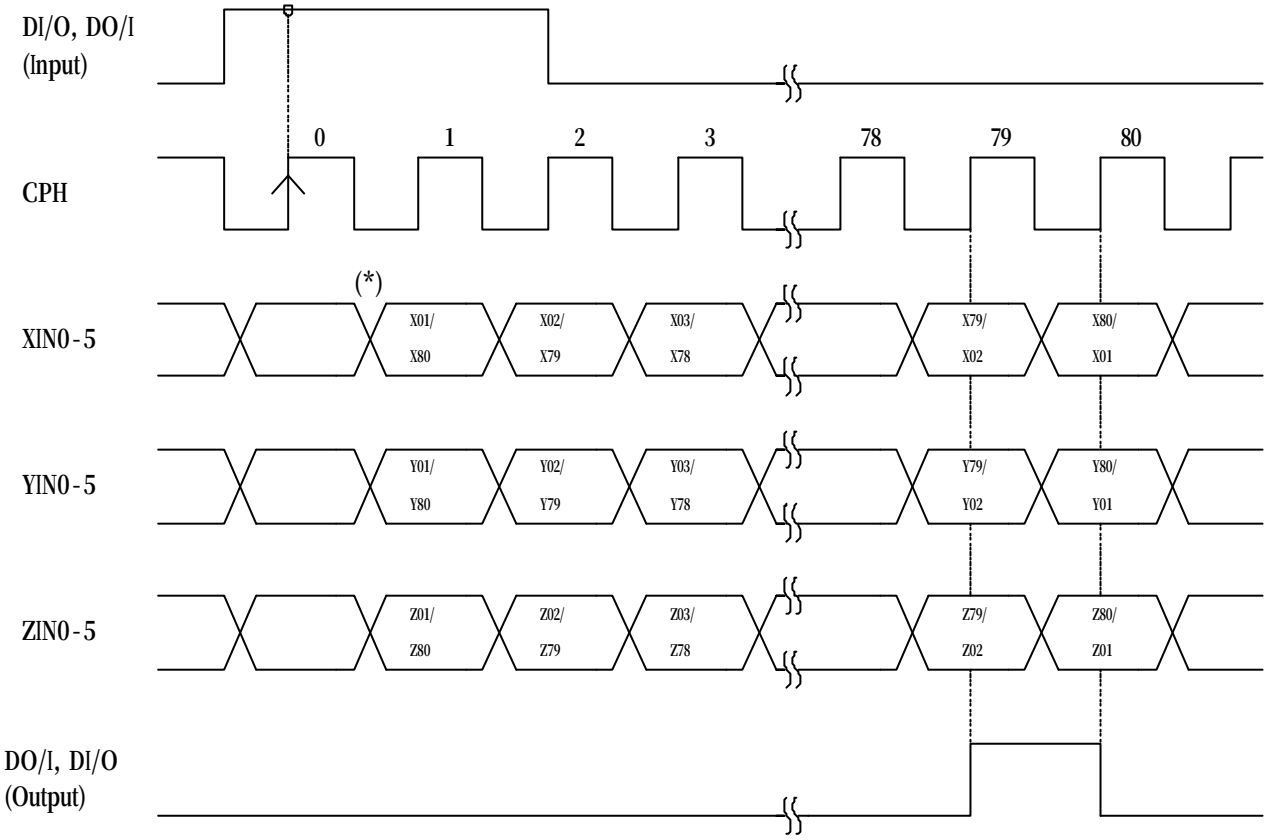
Parameter	Symbol	Condition	Min	Typ	Max	Unit
CPH pulse width, H	tCWH		4			ns
CPH pulse width, L	tCWL		4			ns
Enable setup time	tsDI		4			ns
Enable hold time	thDI		0			ns
Data setup time	tsDD		4			ns
Data hold time	thDD		0			ns
LOAD time	tsLD1		33			ns
Output delay time 1	tpdDO	C_L=15pF	3		12	ns
Output delay time 2	tpdDX	C_L=150pF			14	µs
Output off delay time	tOFF	Note7			15	µs
Output on delay time	tON	Note7			15	µs

Note7, Test Circuit



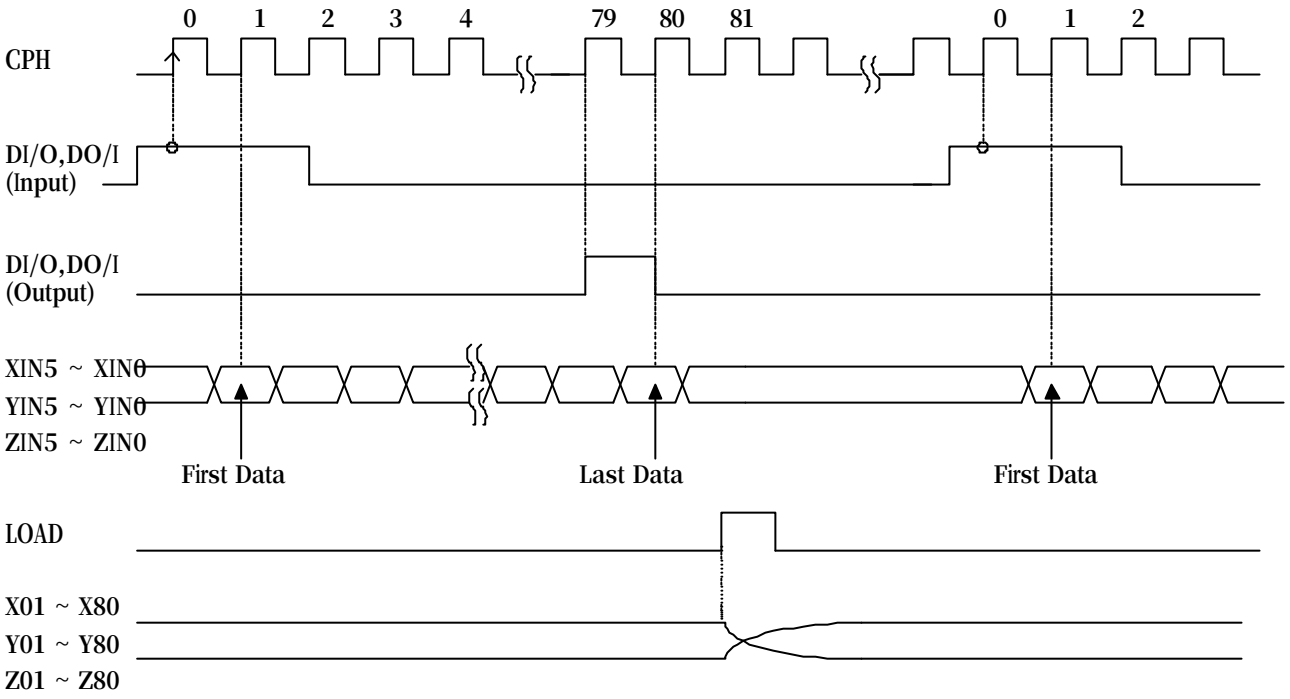


Timing Diagram 1

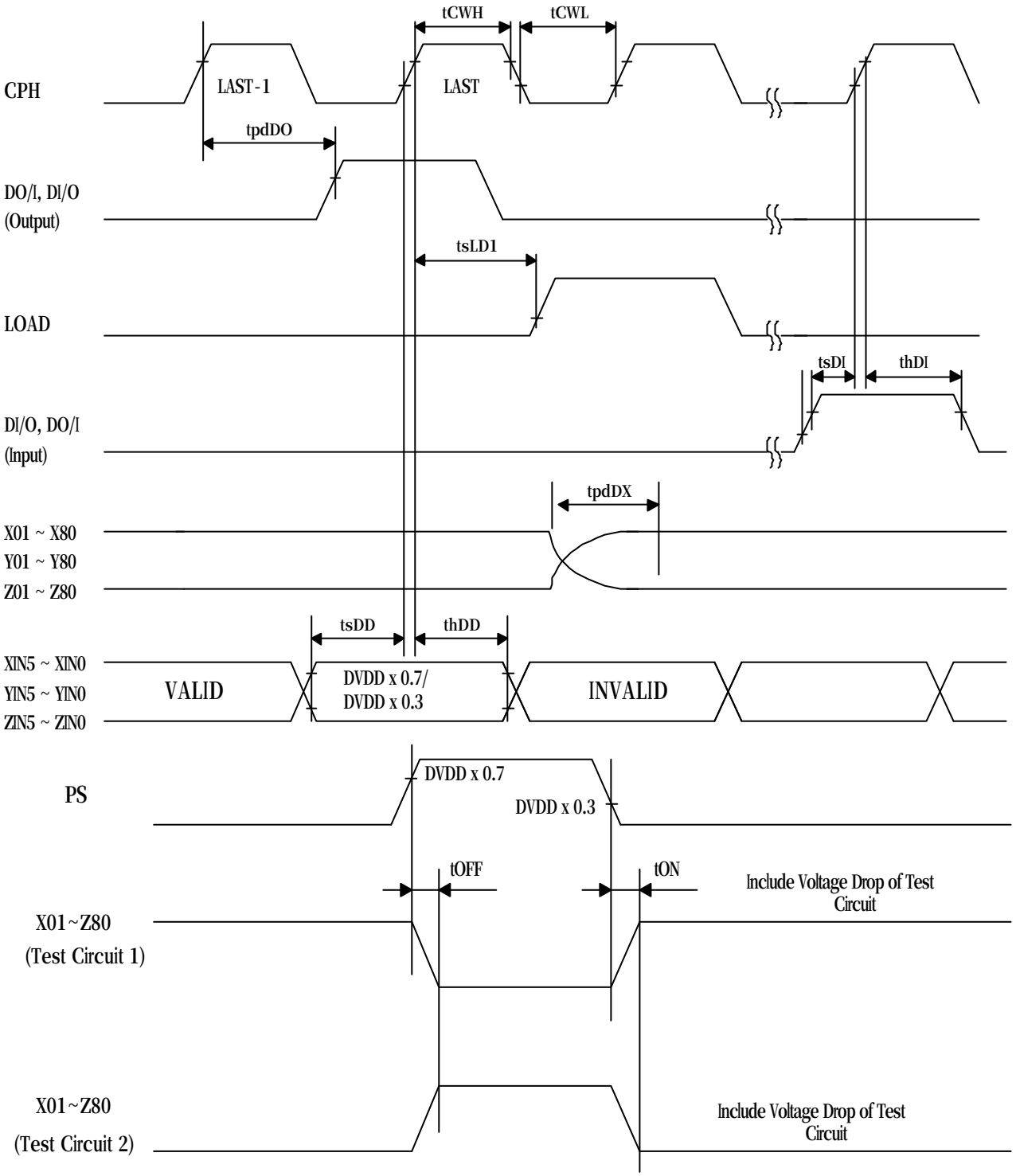


(*) X01→U/D="H"
X80→ U/D="L"

Timing Diagram 2



Timing Diagram 3



9. PAD Configuration