National Semiconductor

PRELIMINARY

MM58250 Infrared Transmitter

General Description

The infrared transmitter is designed to drive an infrared LED (only one external npn transistor is required) with data encoded in a pulse-width-modulated (pwm) format. To get a better signal-to-noise-ratio the pwm scheme amplitude modulates a 38kHz carrier. The data to be transmitted is input in two ways. The primary data input mode (MS = 1) is through a 4-by-8 single-contact keyboard which is interpreted by on-chip logic. The second input mode (MS = 0) is the direct input mode. In this mode a five-bit parallel word and a load pulse are applied to the inputs. The five-bit word is then converted to the pwm format and transmitted.

The chip is designed for battery operation, so it employs a number of power-saving techniques. The chip is implemented in CMOS, so the supply current required by the logic is low. The oscillator can be disabled, allowing the stand-by current to be less than 1 μA. Although the continuous transmission of the data stream is possible, the repetition rate of the continuous transmission is restricted, and the majority of the codes transmittable are repeated only three times. (Twelve outputs can be repeated continuously for analog functions such as volume and channel scanning).

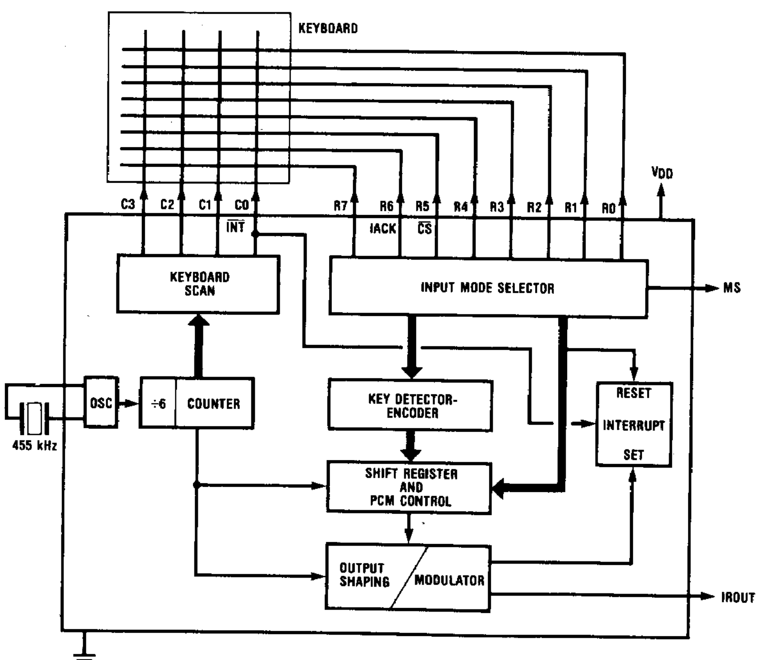
Features

- Up to 32 functions decoded and transmitted
- Single-contact scanned keyboard
- Low standby current (CMOS)
- 455kHz on-chip oscillator
- Wide power supply range (3V-10V)
- Keyboard or direct load modes
- Direct load mode TTL compatible
- 38kHz carrier for improved signal-to-noise-ratio
- High current output stage
- Compatible with MM54251 infrared receiver

Applications

- TV remote control transmitter
- 5-bit wireless asynchronous transmitter
- Intended for use with MM54251

Block Diagram



TL/F/6149-1

Absolute Maximum Ratings

Voltage at Any Pin	$-0.3V$ to $V_{DD}+0.3V$
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500 mW
V_{DD}-V_{SS}	12V
Lead Temperature (Soldering, 10 seconds)	300°C
DC Current at IR Output	− 20 mA

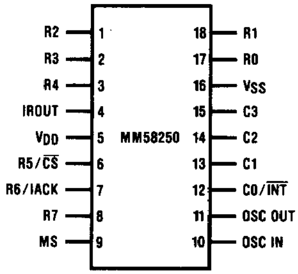
Electrical Characteristics

$V_{DD} = 3.0V$ to 10V, $T_A = \pm 0°C$ to 70°C unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supply V_{DD} Supply Voltage V_{DD} Supply Current (Active) V_{DD} Supply Current (Standby) Oscillator Frequency*		3.0	 455	10 5 1	V mA μA kHz
IR Output Voltage Logic "0" Logic "1"	150μA Sink 10 mA Source	 $V_{DD}-1.4$		0.6	V V
IR Output Current (Note: no short-circuit protection)	$V_{DD}-1.4V$	− 10		− 20	mA
Input Levels Logic "0" Logic "1"	MS = 0, $4.5 \leq V_{DD} \leq 5.5$ Direct Mode	 2.4		0.5	V V
Input Current R_0-R_6, MS R_7	MS = 0, $4.5V \leq V_{DD} \leq 5.5V$ Direct Mode $0V \leq V_{IN} \leq V_{DD}$ $V_{IN} = 0.4V$	− 1 0.06		1.0 0.6	μA mA
Input Current R_0-R_7 MS	MS = 1, $3.0V \leq V_{DD} \leq 10V$ Keyboard Mode $V_{IN} = 0.4V$ $0V \leq V_{IN} \leq V_{DD}$	0.024 − 1		1.6 1	mA μA
Output Current C_0-C_1 Logic "1" Source "1" Source Logic "0" Sink "0" Sink	MS = 1 $V_{DD} = 3V$, $V_{OUT} = V_{DD}-1V$ $V_{DD} = 10V$, $V_{OUT} = V_{DD}-1V$ $V_{DD} = 3V$, $V_{OUT} = 0.4V$ $V_{DD} = 10V$, $V_{OUT} = 0.5V$	− 40 − 150 260 1.6			μA μA μA mA
Output Current $C_0/\overline{Int}$ (Open Drain) Logic "1" Logic "0"	MS = 0, $4.5V \leq V_{DD} \leq 5.5V$ $0 \leq V_{OUT} \leq V_{DD}$ $V_{OUT} = 0.4V$	 2.5		1	μA mA

*Determined by external components.

Connection Diagram



TL/F/6149-2

Order Number MM58250N
See NS Package N18A

Pin Definitions

Mode Select (MS): This pin selects between the two modes of the MM58250's operation.

MS = "0": Parallel input mode. This mode is designed to allow five bits of data to be written to the MM58250 in a parallel fashion with all the appropriate handshaking signals required to facilitate interfacing a microprocessor.

MS = "1": Keyboard input mode. Data is input from a keyboard configured as a matrix of four column conductors and eight row conductors separated at each point of the matrix by a single contact.

R_0/-R_7/:

Keyboard Mode (MS = 1):

R_0/-R_7/: Act as row inputs for a scanned column keyboard. Internal to the MM58250, these are encoded such that if just one input is low during a scan of the column outputs, (see the discussion of pins C_0/-C_3/) a parallel-in-serial-out transmit buffer is loaded with the binary representation of the low row input and the scanning column. (The binary number loaded is equal to the decimal number in the pin name, i.e. binary 5 is stored for the R_5 input.) In addition R_3/-R_5/ cause the MM58250 to continuously transmit the data stored in its transmit buffer (see Figure 6) as long as a switch closure exists.

Parallel Mode (MS = 0):

R_0/-R_4/: These five inputs act as a parallel, non-inverting, 5-bit data entry path.

R_5/-CS/: This active low input is used to latch in the data at the R_0/-R_4/ inputs, as well as beginning the transmit cycle. The part will continue to transmit as long as this input is low and continue to transmit two to three transmit cycles after the input switches to logic "1", depending on where (see Figures 7 and 8) in the transmit cycle the logic change occured. (Note: the data on R_0/-R_4/ should be held stable a minimum of 60ms.)

R_6/-IACK: This input is used to reset the INT/ signal. It is active high. (See Figure 7)

R_7/: R_7/ enables two functions that were designed to facilitate the testing of the MM58250 quickly that might prove useful to some users.

The divide-by-six prescaler can be by-passed by apply ing a logic "0" to R_7/ when R_6/ = "1" and MS = "0". Th by-pass is implemented by setting an RS-flip-flop tha controls the multiplexing of the main clock line from th output of the divide-by-six prescaler to the output of th oscillator, by-passing the divide-by-six prescaler. Th RS-flip-flop is reset by the main internal reset which i made active at the end of the transmit cycle, *begu before* the by-pass was activated. If the MM58250 i waiting for a new input, switching R_7/ low will have n effect.

The second special mode forces the main internal rese active. This causes the chip to load in new data to b transmitted and initializes the chip to the beginning o the word cycle it was currently in or in the word cycl folowing it, depending on where in the word cycle th reset occurred. If a transmit cycle has been complete this mode has no effect. A transmit cycle consists o three word cycles. If no new data is loaded, th MM58250 will go into its idle state within 45ms. Se Figures 9-11 for examples of how to use these features

C_0/-C_3/:

Keyboard Mode (MS = 1):

C_0/-C_3/: These outputs are normally low when MM5825 is waiting for a new input contact closure to occur. contact closure causes the low signal on the column in puts to be passed to the appropriate row input. This in put going low initiates the transmit cycle. As th transmit cycle begins, the oscillator is enabled an begins to oscillate within 6ms. As soon as the oscillato is enabled all the column outputs are switched to th logic "1" state. 40.9ms later, as clocked by the on-chi oscillator, these outputs are individually switched t the logic "0" state (see Figure 5) and the row inputs ar sampled. If the sampling of the row inputs does no show any of these inputs low (see Figure 6b), th transmit cycle is aborted. If any of the row inputs is low the binary representation of the low row input and th binary representation of the low column output ar stored in the transmit buffer. If the low row input wa R_0/, R_1/, R_2/, R_6/, or R_7/ the outputs C_0/-C_3/ all switch low so internal logic can detect when all keyboard switche have been opened. This feature allows the MM58250 t terminate transmission after three iterations (se Figure 6a) of the output data, even when a contac closure exists longer than the time required to transmi the data three times.

Parallel Mode (MS = 0):

C_0/-C_3/: In the parallel mode only one of the column outputs is still used. This output is used as the C_0/ strobe in the keyboard mode. It is used in this mode as an active low processor interrupt (INT/). This output is designed t drive one TTL input with a 10k pullup resistor. It is reset b the IACK pin. When R_5/$\overline{CS}$ is a logic 1, this signal goes lov after the last transmission is complete.

IROUT: This is the output that provides the drive signa for the transmission (see Figures 3 and 4). IROUT pro vides at least 10mA of current, sufficient to drive a single npn transistor hard enough to provide the 200mA of drive current for the infra-red diodes. The data is output in a serial mode with a start bit and a stop bit brack eting the five data bits. The pwm format used has a 1.6ms bit time with a 75% duty cycle for a '1' and a 25% duty cy cle for a '0'. The start and stop bits are zeros.

Timing Specification

Input Timing	Min.	Max.	Units
Microprocessor Mode			
Data Set-up Time	0		s
Data Hold Time	50		ms
$\overline{CS}$ (minimum pulse width)	250		ns
IACK (minimum pulse width)	250		ns
Keyboard Mode			
Switch Bounce		40	ms
Output Timing			
Oscillator Start up (Subject to external components)		9	ms

All of the following data is based on an oscillator frequency = 455 kHz and will vary as the oscillator frequency varies.

Timing Diagrams

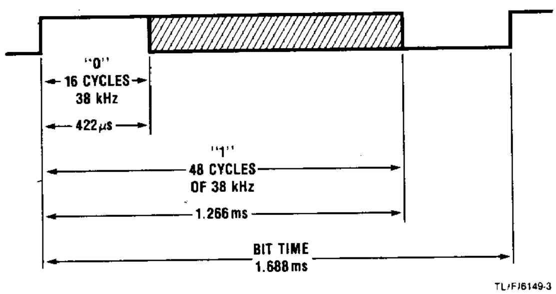


Figure 2. Bit Timing

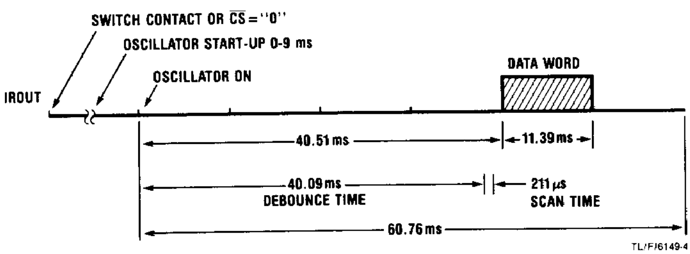


Figure 3. 1/3 Transmit Cycle

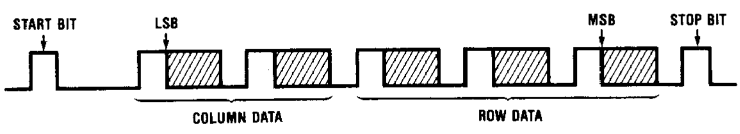


Figure 4. Data Word

Timing Diagrams (Continued)

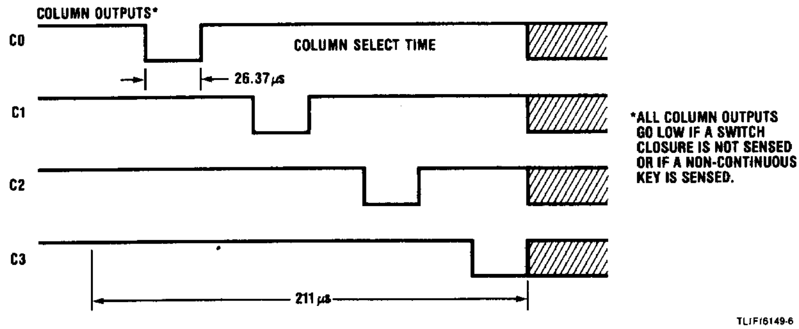


Figure 5. Column Scan Timing

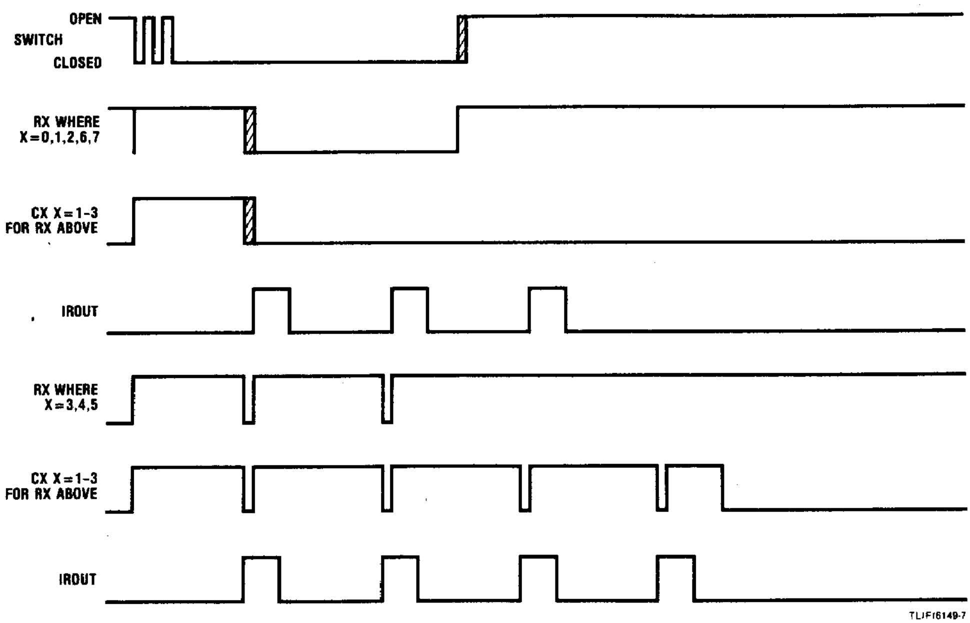


Figure 6a. Typical Transmit Cycles

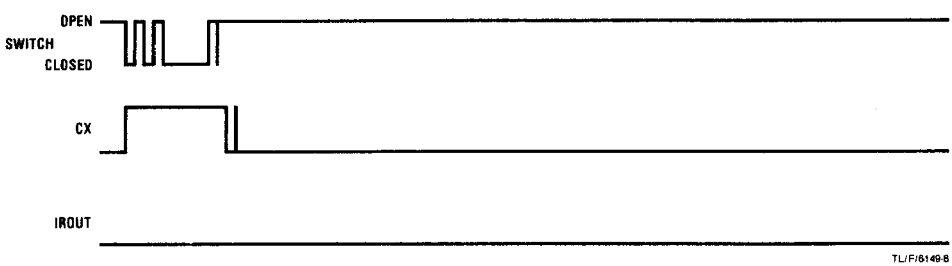


Figure 6b. Aborted Transmit Cycle

Timing Diagrams (Continued)

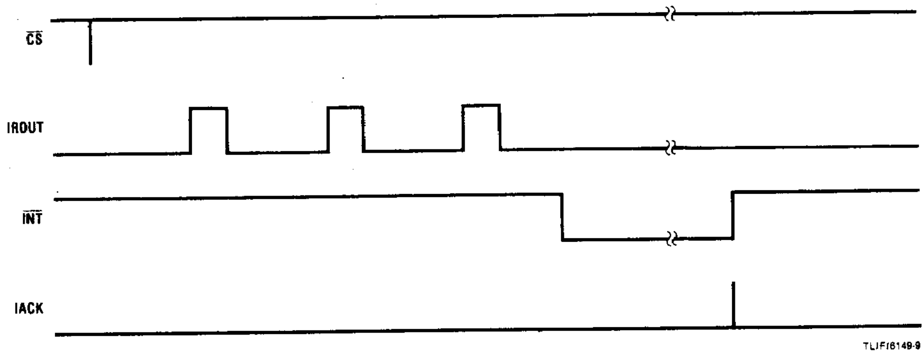


Figure 7. Interrupt Timing

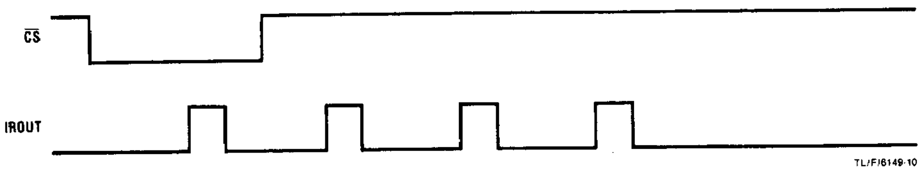


Figure 8. Typical Microprocessor Transmit Cycle

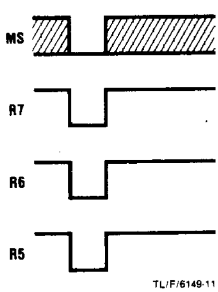


Figure 9. Reset Chip to Beginning of Transmit Cycle

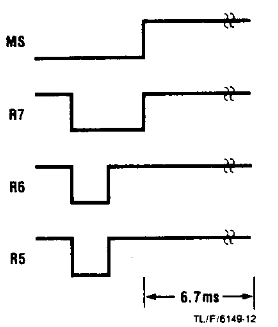


Figure 10. Complete Reset

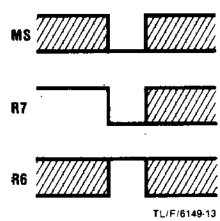


Figure 11. 6X Speed up of Transmit Cycle

Transmitter Functions

#	Code					Row								Column				Function	Note
	16	8	4	2	1	0	1	2	3	4	5	6	7	0	1	2	3		
0	0	0	0	0	0	x								x				0 Direct Entry	1
1	0	0	0	0	1	x									x			1 Direct Entry	1
2	0	0	0	1	0	x										x		2 Direct Entry	1
3	0	0	0	1	1	x											x	3 Direct Entry	1
4	0	0	1	0	0		x							x				4 Direct Entry	1
5	0	0	1	0	1		x								x			5 Direct Entry	1
6	0	0	1	1	0		x									x		6 Direct Entry	1
7	0	0	1	1	1		x										x	7 Direct Entry	1
8	0	1	0	0	0			x						x				8 Direct Entry	1
9	0	1	0	0	1			x							x			9 Direct Entry	1
10	0	1	0	1	0			x								x		Memory Up	1
11	0	1	0	1	1			x									x	On/Off	1
12	0	1	1	0	0				x					x				Slow Up	2
13	0	1	1	0	1				x						x			Slow Down	2
14	0	1	1	1	0				x							x		Search Up	2
15	0	1	1	1	1				x								x	Mute	2
16	1	0	0	0	0					x				x				Analog I Down	2
17	1	0	0	0	1					x					x			Analog I Up	2
18	1	0	0	1	0					x						x		Analog II Down	2
19	1	0	0	1	1					x							x	Analog II Up	2
20	1	0	1	0	0						x			x				Analog III Down	2
21	1	0	1	0	1						x				x			Analog III Up	2
22	1	0	1	1	0						x					x		Analog IV Down	2
23	1	0	1	1	1						x						x	Analog IV Up	2
24	1	1	0	0	0							x		x				Not Defined	1
25	1	1	0	0	1							x			x				
26	1	1	0	1	0							x				x			
27	1	1	0	1	1							x					x		
28	1	1	1	0	0								x	x					
29	1	1	1	0	1								x		x				
30	1	1	1	1	0								x			x			
31	1	1	1	1	1								x				x		

Note 1: Three transmissions.

Note 2: Continuous transmission.

Typical Applications

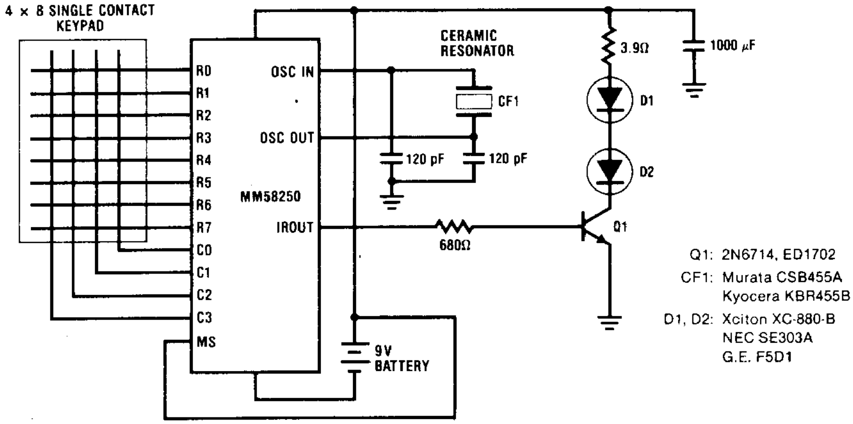


Figure 12.

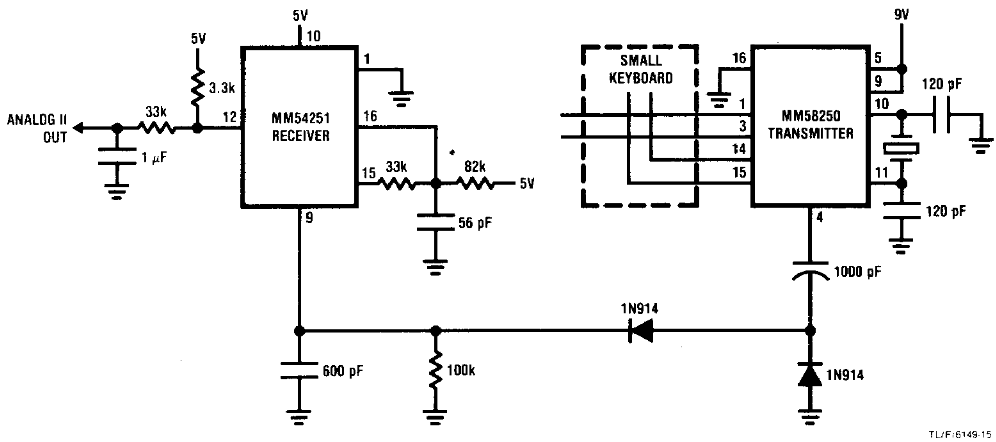


Figure 13. Quick Checkout Circuit