Z8038(FIO)

128 Byte FIFO I/O Port

DISTINCTIVE CHARACTERISTICS

- **Asynchronous FIFO Interface** — 128-byte FIFO provides bidirectional CPU to CPU or peripheral interface.
- **Expandable in Length and Width** — FIOs can be connected in parallel for wider words, can be cascaded for deeper stacks.
- **2-Wire and 3-Wire handshake logic** — Control logic on chip for interlocked two-wire handshake as well as three-wire scheme used in IEEE-488.
- **Pattern matching logic on chip** — FIO can detect a data pattern and interrupt CPU.
- **Byte count available to software** — An on-chip register which contains the actual number of bytes in the FIFO can be read by the software to determine stack status.

GENERAL DESCRIPTION

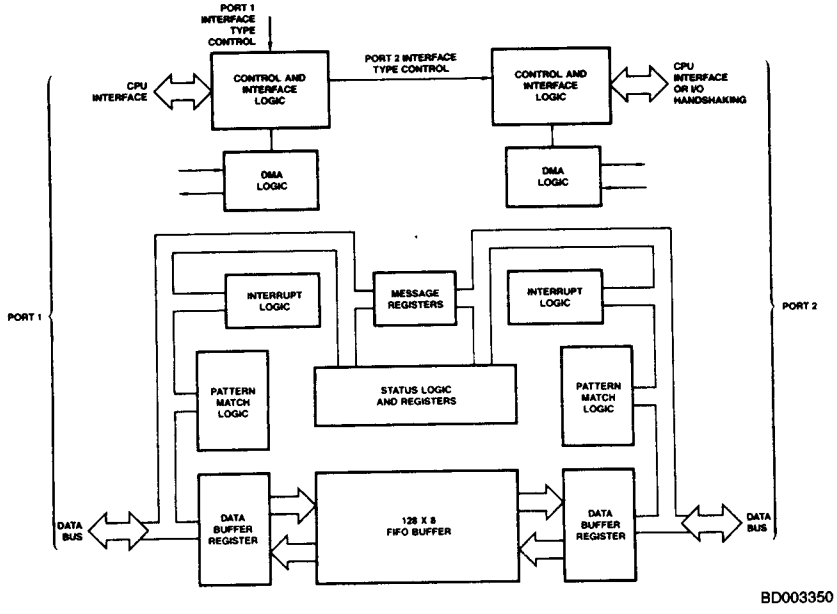
The Z8038* FIO provides an asynchronous 128-byte FIFO buffer between two CPUs or between a CPU and a peripheral device. This buffer interface expands to a 16-bit or wider data path and expands in depth to add as many Z8060 FIFOs (and an additional FIO) as are needed.

The FIO manages data transfers by assuming Z-BUS, non-Z-BUS microprocessor (a generalized microprocessor interface), Interlocked 2-Wire Handshake, and 3-Wire Handshake operating modes. These modes interface dissimilar CPUs or CPUs and peripherals running under differing speeds or protocols, allowing asynchronous data transactions and improving I/O overhead by as much as two orders of magnitude.

The FIO supports the Z-BUS interrupt protocols, generating seven sources of interrupts. Each interrupt source can be enabled or disabled, and can also place an interrupt vector on the port address/data lines.

The data transfer logic of the FIO has been specially designed to work with DMA (Direct Memory Access) devices for high-speed transfers. The FIO also supports the variably sized block length, improving system throughput when multiple variable length messages are transferred amongst several sources.

FIO BLOCK DIAGRAM



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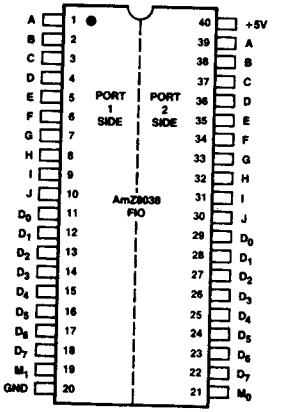
CONNECTION DIAGRAM
Top View

D-40, P-40



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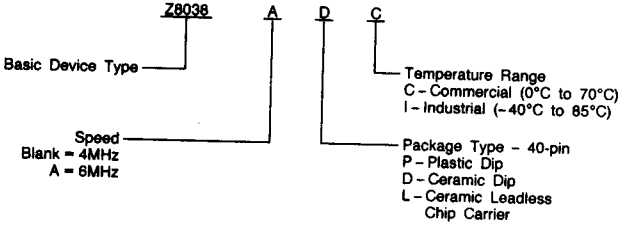
Note: Pin 1 is marked for orientation

ORDERING INFORMATION

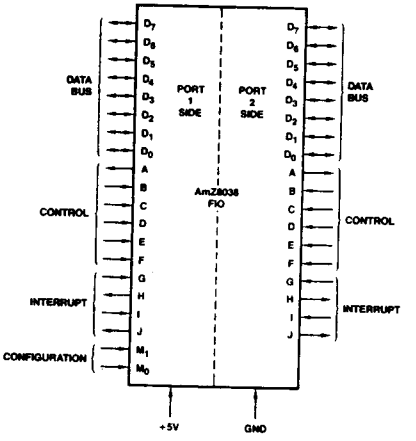
AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
Z8038	DC, PC, DI, ADC, APC

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.



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Pin Functions

PIN DESCRIPTION

Pin Signals	Pin No.		Name	Description
PINS COMMON TO BOTH SIDES				
M_0	21		M_0	M_1 and M_0 program Port 1 side CPU interface
M_1	19		M_1	
+5 Vdc	40		+5 Vdc	DC power source
GND	20		GND	DC power ground
Pin Signals	**Pin No. Port 1**	**Pin No. Port 2**	**Name**	**Description**
Z-BUS LOW BYTE MODE				
AD_0-AD_7 (Address/Data)	11-18	29-22	D_0-D_7	Multiplexed bidirectional address/data lines, Z-BUS compatible.
$\overline{REQ}/\overline{WAIT}$ (Request/Wait)	1	39	A	Output, active Low, REQUEST (ready) line for DMA transfer, WAIT line (open-drain) output for synchronized CPU and FIO data transfers.
$\overline{DMASTB}$ (Direct Memory Access Strobe)	2	38	B	Input, active Low. Strobes DMA data to and from the FIFO buffer.
$\overline{DS}$ (Data Strobe)	3	37	C	Input, active Low. Provides timing for data transfer to or from FIO.
$R/\overline{W}$ (Read/Write)	4	36	D	Input, active High signals CPU read from FIO; active Low signals CPU write to FIO.
$\overline{CS}$ (Chip Select)	5	35	E	Input, active Low. Enables FIO. Latched on the rising edge of $\overline{AS}$.
$\overline{AS}$ (Address Strobe)	6	34	F	Input, active Low. Addresses, $\overline{CS}$ and $\overline{INTACK}$, are sampled while $\overline{AS}$ is Low.
$\overline{INTACK}$ (Interrupt Acknowledge)	7	33	G	Input, active Low. Acknowledges an interrupt. Latched on the rising edge of $\overline{AS}$.
IEO (Interrupt Enable Out)	8	32	H	Output, active High. Sends interrupt enable to lower priority device IEI pin.
IEI (Interrupt Enable In)	9	31	I	Input, active High. Receives interrupt enable from higher priority device IEO signal.
$\overline{INT}$ (Interrupt)	10	30	J	Output, open drain, active Low. Signals FIO interrupt request to CPU.
Z-BUS HIGH BYTE MODE				
AD_0-AD_7 (Address/Data)	11-18	29-22	D_0-D_7	Multiplexed bidirectional address/data lines, Z-BUS compatible.
$\overline{REQ}/\overline{WAIT}$ (Request/Wait)	1	39	A	Output, active Low, REQUEST (ready) line for DMA transfer, $\overline{WAIT}$ line (open-drain) output for synchronized CPU and FIO data transfers.
$\overline{DMASTB}$ (Direct Memory Access Strobe)	2	38	B	Input, active Low. Strobes DMA data to and from the FIFO buffer.
$\overline{DS}$ (Data Strobe)	3	37	C	Input, active Low. Provides timing for transfer of data to or from FIO.
$R/\overline{W}$ (Read/Write)	4	36	D	Input, active High. Signals CPU read from FIO; active Low signals CPU write to FIO.
$\overline{CS}$ (Chip Select)	5	35	E	Input, active Low. Enables FIO. Latched on the rising edge of $\overline{AS}$.
$\overline{AS}$ (Address Strobe)	6	34	F	Input, active Low. Addresses, $\overline{CS}$ and $\overline{INTACK}$, are sampled while $\overline{AS}$ is Low.
A_0 (Address Bit 0)	7	33	G	Input, active High. With A_1, A_2, and A_3, addresses FIO internal registers.
A_1 (Address Bit 1)	8	32	H	Input, active High. With A_0, A_2, and A_3, addresses FIO internal registers.
A_2 (Address Bit 2)	9	31	I	Input, active High. With A_0, A_1, and A_3, addresses FIO internal registers.
A_3 (Address Bit 3)	10	30	J	Input, active High. With A_0, A_1, and A_2, addresses FIO internal registers.

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PIN DESCRIPTION (Cont.)

Pin Signals	Pin No. Port 1	Pin No. Port 2	Name	Description
NON-Z-BUS MODE				
D_0-D_7 (Data)	11-18	29-22	D_0-D_7	Bidirectional data bus.
$\overline{REQ}/\overline{WT}$ (Request/Wait)	1	39	A	Output, active Low. REQUEST (ready) line for DMA transfer, $\overline{WAIT}$ line (open-drain) output for synchronized CPU and FIO data transfer.
$\overline{DACK}$ (DMA Acknowledge)	2	38	B	Input, active Low. DMA acknowledge.
$\overline{RD}$ (Read)	3	37	C	Input, active Low. Signals CPU read from FIO.
$\overline{WR}$ (Write)	4	36	D	Input, active Low. Signals CPU write to FIO.
$\overline{CE}$ (Chip Select)	5	35	E	Input, active Low. Used to select FIO.
C/$\overline{D}$ (Control/Data)	6	34	F	Input, active High. Identifies control byte on D_0-D_7. Active Low identifies data byte on D_0-D_7.
$\overline{INTACK}$ (Interrupt Acknowledge)	7	33	G	Input, active Low. Acknowledges an interrupt.
IEO (Interrupt Enable Out)	8	32	H	Output, active High. Sends interrupt enable to lower priority device IEI pin.
IEI (Interrupt Enable In)	9	31	I	Input, active High, Receives interrupt enable from higher priority device IEO signal.
$\overline{INT}$ (Interrupt)	10	30	J	Output, open drain, active Low. Signals FIO interrupt to CPU.

Pin Signals	Pin No.	Mode	Name	Description
PORT 2 - I/O PORT MODE				
D_0-D_7 (Data)	29-22	2-Wire HS* 3-Wire HS	D_0-D_7	Bidirectional data bus.
RFD/$\overline{DAV}$ (Ready for Data/Data Available)	39	2-Wire HS 3-Wire HS	A	Output, RFD active High. Signals peripherals that F IO is ready to receive data. $\overline{DAV}$ active Low signals that FIO is ready to send data to peripherals.
$\overline{ACKIN}$ (Acknowledge Input)	38	2-Wire HS	B	Input, active Low. Signals FIO that output data is received by peripherals or that input data is valid.
$\overline{DAV}$/DAC (Data Available/Data Accepted)	38	3-Wire HS	B	Input, $\overline{DAV}$ (active Low) signals that data is valid on bus. DAC (active High) signals that output data is accepted by peripherals.
FULL	37	2-Wire HS	C	Output, open drain, active High. Signals that FIO buffer is full.
DAC/RFD (Data Accepted/Ready for Data)	37	3-Wire HS	C	Direction controlled by internal programming. Both active High. DAC (an output) signals that FIO has received data from peripheral; RFD (an input) signals that the listeners are ready for data.
EMPTY	36	2-Wire HS 3-Wire HS	D	Output, open drain, active High. Signls that FIFO buffer is empty.
$\overline{CLEAR}$	35	2-Wire HS 3-Wire HS	E	Programmable input or output, active Low. Clears all data from FIFO buffer.
DATA DIR (Data Direction)	34	2-Wire HS 3-Wire HS	F	Programmable input or output. Active High signals data input to Port 2; Low signals data output from Port 2.
IN_0	33	2-Wire HS 3-Wire HS	G	Input line to D_0 of Control Register 3.
OUT_1	32	2-Wire HS 3-Wire HS	H	Output line from D_1 of Control Register 3.
$\overline{OE}$ (Output Enable)	31	2-Wire HS 3-Wire HS	I	Input, active Low. When Low, enables bus drivers. When High, floats bus drivers at high impedance.
OUT_3	30	2-Wire HS 3-Wire HS	J	Output line from D_3 of Control register 3.

*Handshake

ARCHITECTURE

The FIO is a universal interface between two independent systems operating asynchronously. Conceptually it consists of two programmable interfaces connected by a 128-byte FIFO buffer and a pair of message registers, as shown in Figure 1.

Each port contains 8 lines used for data and for programming the FIO, and 10 lines used for various control functions. The function and timing relationships of the 10 control lines change completely according to the type of interface the port is programmed to be. Either port can be programmed to interface directly to a Z8000 CPU Bus (Z-bus) or to an 8080 type bus (8080, 8085, Z80). The 10 control lines perform the functions needed for read and write strobes, DMA control, and interrupt handling. The port 2 side can also be programmed for interface to peripheral; in this case, the 10 lines are used for handshaking, direction control, and cascading.

The two sides are connected by the FIFO buffer and the message registers. The buffer is used to move data between the two ports. Since it is a FIFO, reads and writes can occur simultaneously and independently. Each port is tied to its own system interface, with the FIFO providing reliable data transfer between them. The message registers are used to transmit information between the two ports without going through the FIFO. They (one going each direction) are intended for control words being sent from one CPU to another.

The CPU interface includes a vectored interrupt capability which covers all the ways in which a transfer might be terminated. The CPU, therefore, can set up the FIO to communicate with a peripheral or another CPU, and then not deal with the FIO until an interrupt occurs. Interrupts can be programmed to occur if any of these conditions takes place:

Buffer Empty
Buffer Full
Overflow/Underflow
Byte Count Match
Data Pattern Match
Data Direction Change
Message Present

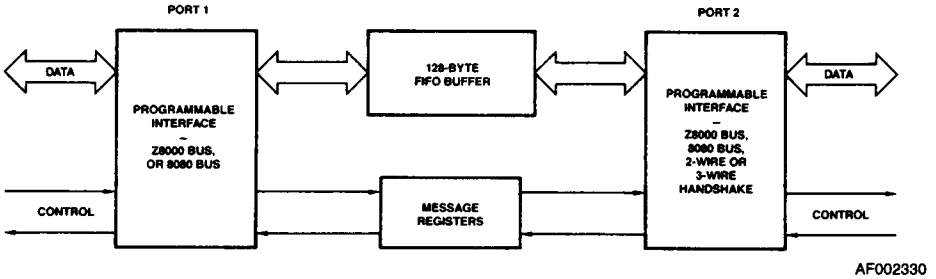


Figure 1. FIO Concept

DETAILED DESCRIPTION

OPERATING MODES

Ports 1 and 2 operate in any of twelve combinations of operating modes, listed in Table 2. Port 1 functions in either the Z-BUS or non-Z-BUS microprocessor modes, while Port 2 functions in Z-BUS, non-Z-BUS, Interlocked 2-Wire Handshake, and 3-Wire Handshake modes. Table 1 describes the signals and their corresponding pins in each of these modes.

The pin diagrams of the FIO are identical, except for two pins on the Port 1 side, which select that port's operating mode. Port 2's operating mode is programmed by two bits in Port 1's Control register 0. Table 2 describes the combinations of operating modes; PIN DESCRIPTION describes the control signals mapped to pins A–J in the five possible operating modes.

RESET

The FIO can be reset under either hardware or software control by one of the following methods:

- By forcing both $\overline{AS}$ and $\overline{DS}$ LOW simultaneously in Z-BUS mode (normally illegal).
- By forcing $\overline{RD}$ and $\overline{WR}$ LOW simultaneously in non-Z-BUS mode.
- By writing a 1 to the Reset bit in Control register 0 for software reset.

In the Reset state, all control bits are cleared to 0. Only after clearing the Reset bit (by writing a 0 to it) can the other command bits be programmed. This action is true for both sides of the FIO when programmed as a CPU interface.

TABLE 1. PIN ASSIGNMENTS

Control Signal Pins	Z-BUS Low Byte	Z-BUS High Byte	Non-Z-BUS	Port 2 Only	
				Interlocked HS Port	3-Wire HS Port
A	$\overline{REQ}/\overline{WT}$	$\overline{REQ}/\overline{WT}$	$\overline{REQ}/\overline{WT}$	RFD/$\overline{DAV}$	RFD/$\overline{DAV}$
B	$\overline{DMASTB}$	$\overline{DMASTB}$	$\overline{DACK}$	$\overline{ACKIN}$	$\overline{DAV}$/DAC
C	$\overline{DS}$	$\overline{DS}$	$\overline{RD}$	FULL	DAC/RFD
D	R/$\overline{W}$	R/$\overline{W}$	$\overline{WR}$	EMPTY	EMPTY
E	$\overline{CS}$	$\overline{CS}$	$\overline{CE}$	$\overline{CLEAR}$	$\overline{CLEAR}$
F	$\overline{AS}$	$\overline{AS}$	C/$\overline{D}$	DATA DIR	DATA DIR
G	$\overline{INTACK}$	A_0	$\overline{INTACK}$	IN_0	IN_0
H	IEO	A_1	IEO	OUT_1	OUT_1
I	IEI	A_2	IEI	OE	OE
J	$\overline{INT}$	A_3	$\overline{INT}$	OUT_3	OUT_3

For proper system control, when Port 1 is reset, Port 2 is also reset. In addition, all Port 2's outputs are floating and all inputs are ignored. To initiate the data transfer, Port 2 must be enabled by Port 1. The Port 2 CPU can determine when it is enabled by reading Control register 0, which reads "floating" data bus if not enabled and "01_H" if enabled.

TABLE 2. OPERATING MODES

MODE	M_1	M_0	B_1*	B_0*	Port 1	Port 2
0	0	0	0	0	Z-BUS Low Byte	Z-BUS Low Byte
1	0	0	0	1	Z-BUS Low Byte	Non-Z-BUS
2	0	0	1	0	Z-BUS Low Byte	3-Wire Handshake
3	0	0	1	1	Z-BUS Low Byte	2-Wire Handshake
4	0	1	0	0	Z-BUS High Byte	Z-BUS High Byte
5	0	1	0	1	Z-BUS High Byte	Non-Z-BUS
6	0	1	1	0	Z-BUS High Byte	3-Wire Handshake
7	0	1	1	1	Z-BUS High Byte	2-Wire Handshake
8	1	0	0	0	Non-Z-BUS	Z-BUS Low Byte
9	1	0	0	1	Non-Z-BUS	Non-Z-BUS
10	1	0	1	0	Non-Z-BUS	3-Wire Handshake
11	1	0	1	1	Non-Z-BUS	2-Wire Handshake

*Bits 3 and 2 of Control register 0. Read/Write from Port 1, Read-only from Port 2.

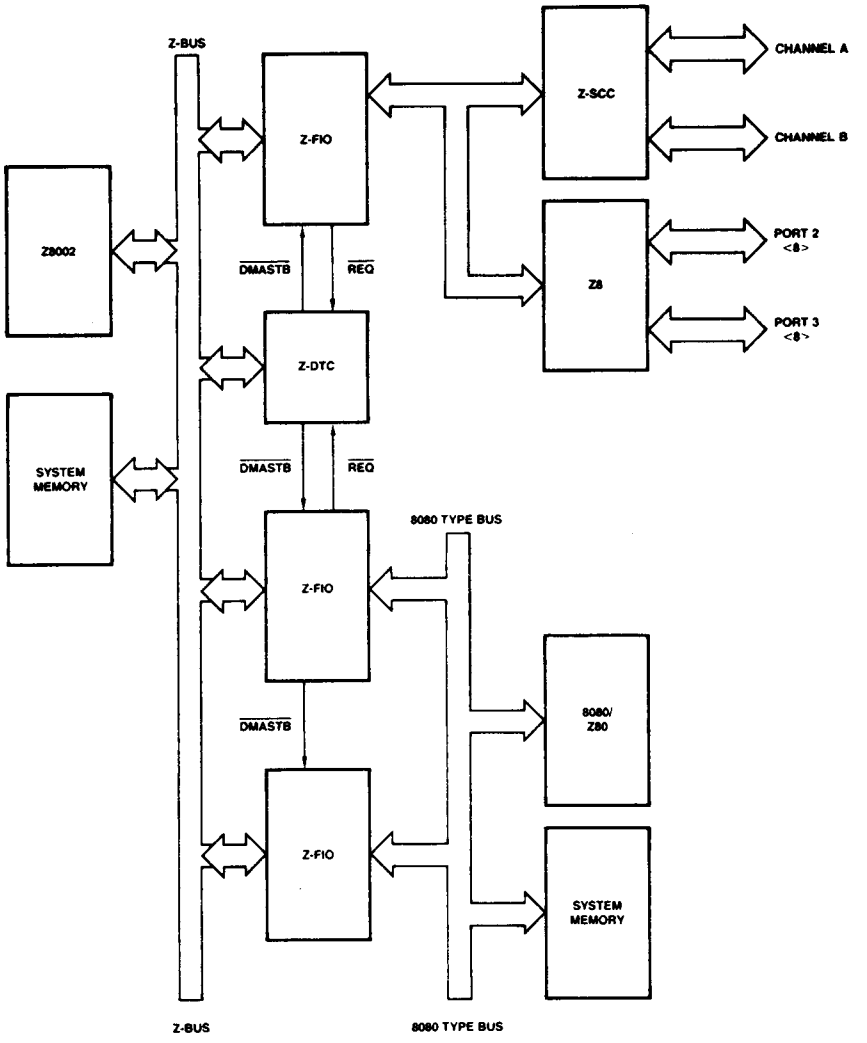


Figure 2. CPU to CPU Configuration

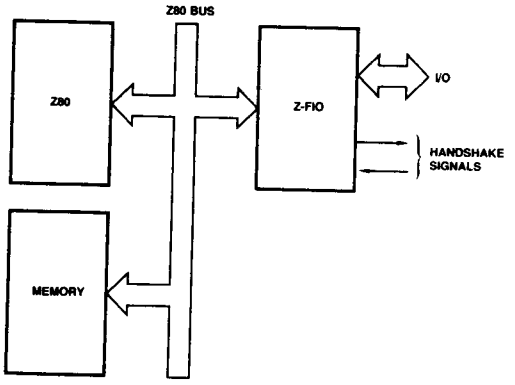


Figure 3. CPU to I/O Configuration

CPU INTERFACES

The FIO is designed to work with both Z-BUS and non-Z-BUS-type CPUs, on both Port 1 and Port 2. The Z-BUS configuration interfaces CPUs with time-multiplexed address and data information on the same pins. The Z8001, Z8002, and Z8 are examples of this type of CPU. The AS (Address Strobe) pin is used to latch the address and chip select information sent out by the CPU. The R/$\overline{W}$ (Read/Write) pin and the $\overline{DS}$ (Data Strobe) pin are used for timing reads and writes from the CPU to the FIO (Figures 4 and 5).

The non-Z-BUS configuration is used for CPUs where the address and data buses are separate. Examples of this type of CPU are the Z80 and 8080. The $\overline{RD}$ (Read) and $\overline{WR}$ (Write) pins are used to time reads and writes from the CPU to the FIO (Figures 7 and 8). The C/$\overline{D}$ (Control/Data) pin is used to directly access the FIFO buffer (C/$\overline{D}$ = 0) and to access the other registers (C/$\overline{D}$ = 1). Read and write to all registers except the FIFO buffer[1] are the two-step operations, described as follows (Figure 6). First, write the address of the register to be accessed with C/$\overline{D}$ = 1. The address goes into a pointer register, and the FIO switches to state 1. The next read or write with C/$\overline{D}$ = 1 will be to the register pointed to. Continuous status monitoring can be performed by continuous Control Read operations (C/$\overline{D}$ = 1).

[1]The FIFO buffer can also be accessed by this two-step operation.

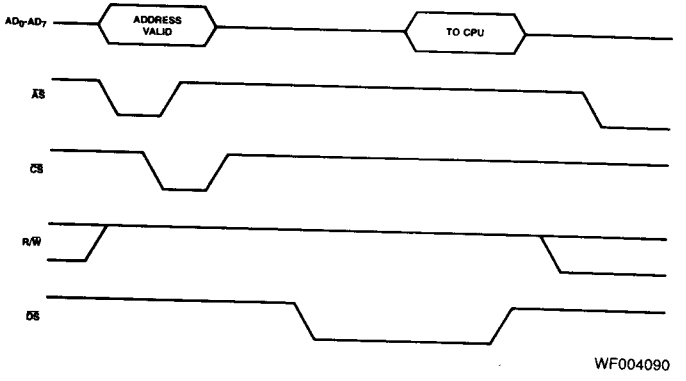


Figure 4. Z-BUS Read Cycle Timing

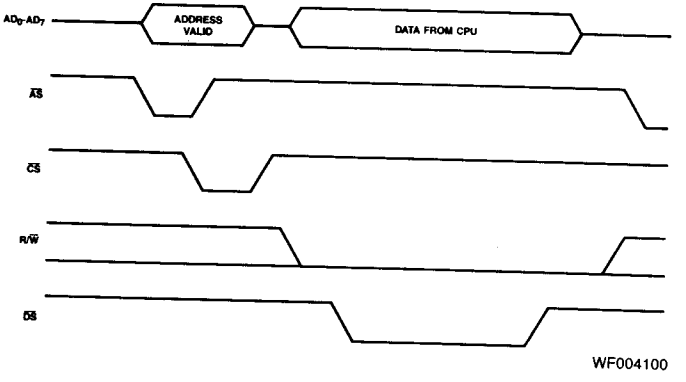


Figure 5. Z-BUS Write Cycle Timing

Refer to page 7-1 for Essential Information on Military Devices

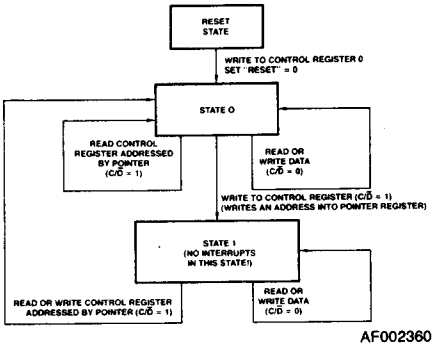


Figure 6. In Non-Z-BUS Mode, Control Registers are Accessed by First Writing the Address of the Register, then Reading or Writing the Contents of the Addressed Register.

WAIT OPERATION

When data is output from the CPU, the REQ/WT/ (WAIT) pin is active (LOW) only when the FIFO buffer is full, the chip is selected, and FIFO buffer is addressed. WAIT goes inactive when the FIFO buffer is not full.

When data is input to the CPU, the REQ/WT pin becomes active (LOW) only when the FIFO buffer is empty, the chip is selected, and the FIFO buffer is addressed. WAIT goes inactive when the FIFO buffer is not empty.

INTERRUPT OPERATION

The FIO supports Zilog's prioritized daisy chain interrupt protocol for both Z-BUS and non-Z-BUS operating modes.

Each side of the FIO has seven sources of interrupt. The priorities of these devices are fixed in the following order (highest to lowest): Mailbox message, Change in Data Direction, Pattern Match, Status Match, Overflow/Underflow Error, Buffer Full, and Buffer Empty. Each interrupt source has three bits that control how it generates the interrupt. These bits are Interrupt Pending (IP), Interrupt Enable (IE) and Interrupt Under Service (IUS).

In addition, each side of the FIO has an interrupt vector and four bits controlling the FIO interrupt logic. These bits are Vector Includes Status (VIS), Master Interrupt Enable (MIE), Disable Lower Chain (DLC) and No Vector (NV).

A typical Interrupt Acknowledge cycle for Z-BUS operation is shown in Figure 9 and for non-Z-BUS operation in Figure 10. The only difference is that in Z-BUS mode, INTACK is latched by AS, and in non-Z-BUS mode, INTACK is not latched.

When MIE = 1, reading the vector always includes status, independent of the state of the VIS bit. In this way, when VIS = 0, all information can be obtained with one additional read, thus conserving vector space. When MIE = 0, reading the vector register returns the unmodified base vector so that it can be verified.

In non-Z-BUS mode, IPs do not get set while in State 1. Therefore, to minimize interrupt latency, the FIO should be left in State 0.

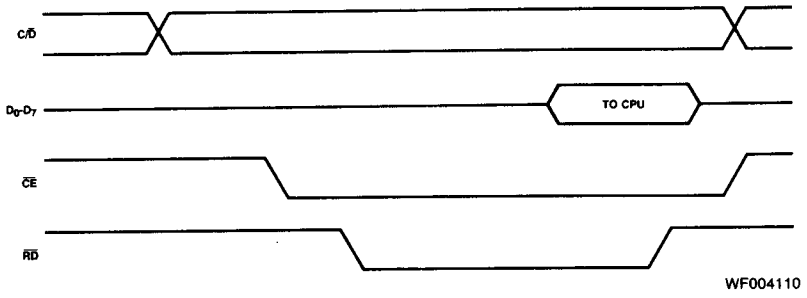


Figure 7. Non-Z-BUS Read Cycle Timing

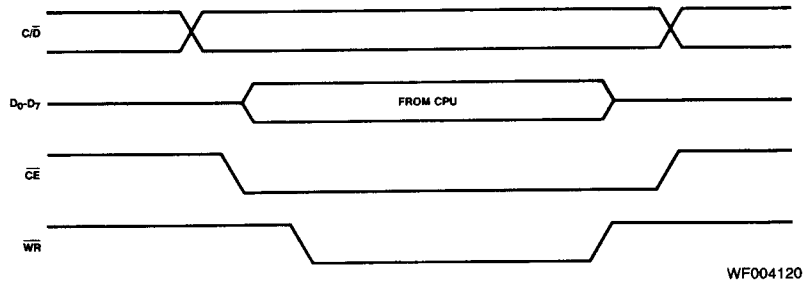


Figure 8. Non-Z-BUS Write Cycle Timing

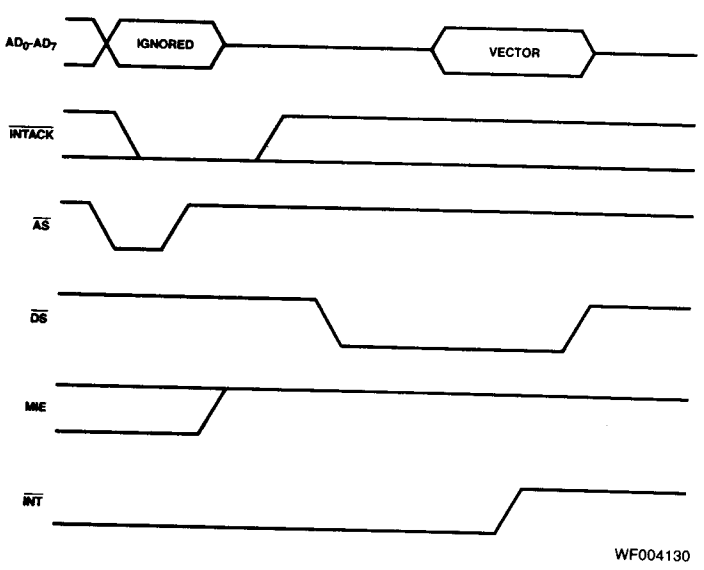


Figure 9. Z-BUS Interrupt Acknowledge Cycle

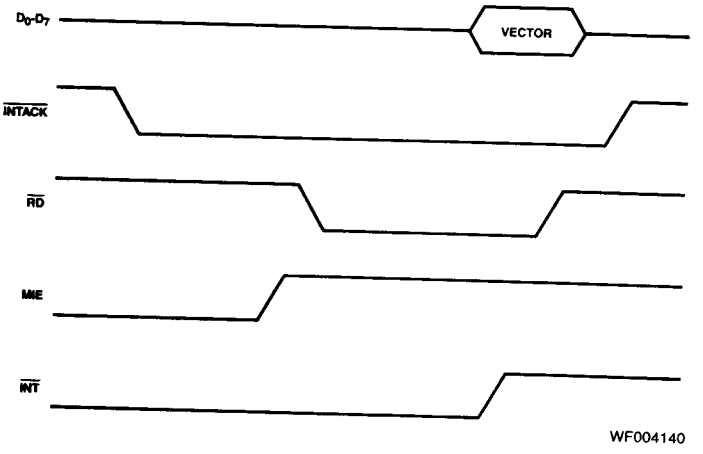


Figure 10. Non-Z-BUS Interrupt Acknowledge Cycle

CPU TO CPU OPERATIONS

DMA Operation

The FIO is particularly well suited to work with a DMA in both Z-BUS and non-Z-BUS modes. A data transfer between the FIO and system memory can take place during every machine cycle on both sides of the FIO simultaneously.

In Z-BUS mode, the $\overline{\text{DMASTB}}$ pin (DMA Strobe) is used to read or write into the FIFO buffer. The R/$\overline{\text{W}}$ (Read/Write) and $\overline{\text{DS}}$ (Data Strobe) signals are ignored by the FIO; however, the $\overline{\text{CS}}$ (Chip Select) signal is not ignored and therefore must be kept valid. Figures 11 and 12 show typical timing.

In Non-Z-BUS mode, the $\overline{\text{DACK}}$ pin (DMA Acknowledge) is used to tell the FIO that its DMA request is granted. After $\overline{\text{DACK}}$ goes Low, every read or write to the FIO goes into the FIFO buffer. Figures 13 and 14 show typical timing.

The FIO provides a special mode to enhance its DMA transfer capability. When data is written into the FIFO buffer, the $\overline{\text{REQ}}$/$\overline{\text{WT}}$ ($\overline{\text{REQUEST}}$/$\overline{\text{WAIT}}$) pin is active (LOW) until the FIFO buffer is full. It then goes inactive and stays inactive until the number of bytes in the FIFO buffer is equal to the value programmed into the Byte Count Comparison register. Then the $\overline{\text{REQUEST}}$ signal goes active and the sequence starts over again (Figure 15).

When data is read from the FIO, the $\overline{\text{REQ}}$/$\overline{\text{WT}}$ pin ($\overline{\text{REQUEST}}$/$\overline{\text{WAIT}}$) is inactive until the number of bytes in the FIFO buffer is equal to the value programmed in the Byte Count Comparison register. The $\overline{\text{REQUEST}}$ signal then goes active and stays active until the FIFO buffer is empty. When empty, $\overline{\text{REQUEST}}$ goes inactive and the sequence starts over again (Figure 16).

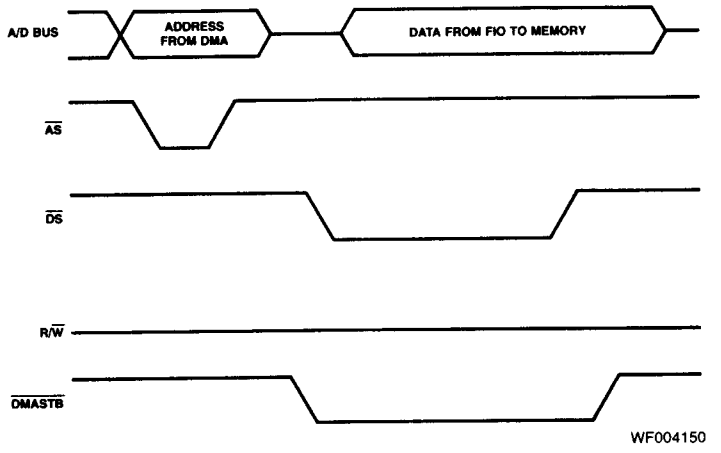


Figure 11. Z-BUS FIO to Memory Data Transaction

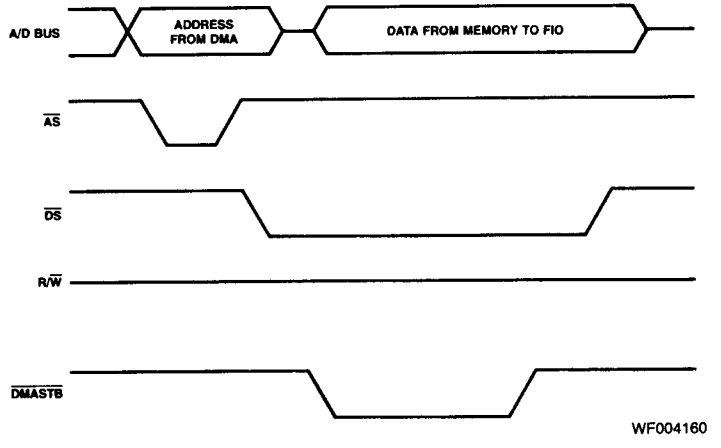


Figure 12. Z-BUS Memory to FIO Data Transaction

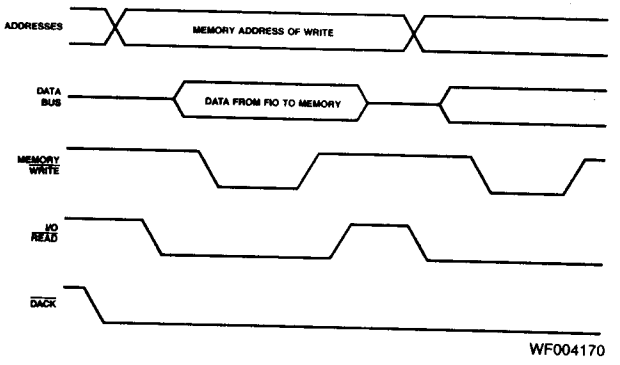


Figure 13. Non-Z-BUS FIO to Memory Transaction

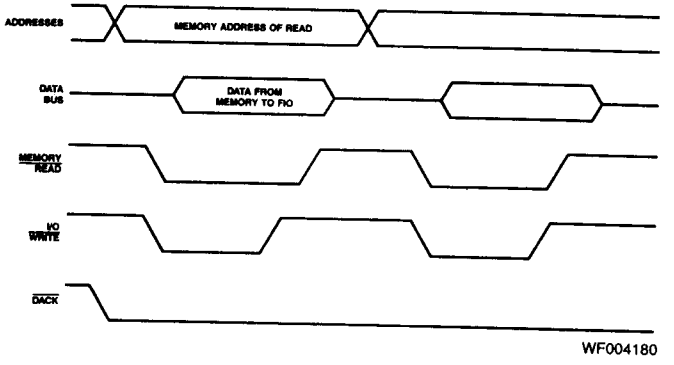
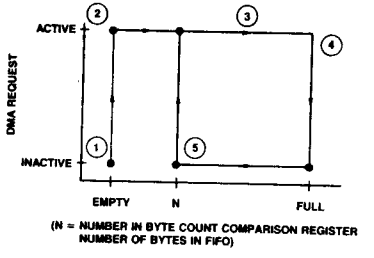
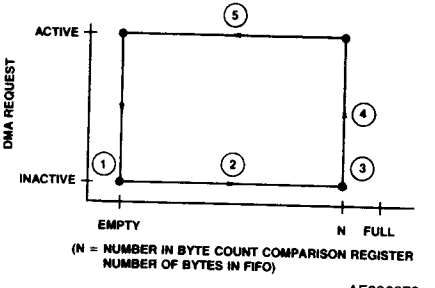


Figure 14. Non-Z-BUS Memory to FIO Data Transaction



Notes: 1. FIFO empty.
2. REQUEST enabled, FIO request DMA transfer.
3. DMA transfers data into the FIO.
4. FIFO full, REQUEST inactive.
5. The FIFO empties from the opposite port until the number of bytes in the FIFO buffer is the same as the number programmed in the Byte Count Comparison register.

Figure 15. Byte Count Control: Write to FIO



Notes: 1. FIFO empty.
2. CPU/DMA fills FIFO buffer from the opposite port.
3. Number of bytes in FIFO buffer is the same as the number of bytes programmed in the Byte Count Comparison register.
4. REQUEST goes active.
5. DMA transfers data out of FIFO until it is empty.

Figure 16. Byte Count Control: Read from FIO

Message Registers

Two CPUs can communicate through a dedicated "mailbox" register without involving the 128 x 8 bit FIFO buffer (Figure 19). This mailbox approach is useful for transferring control parameters between the interfacing devices on either side of the FIO without using the FIFO buffer. For example, when Port 1's CPU writes to the Message Out register, Port 2's message IP is set. If interrupts are enabled, Port 2's CPU is interrupted. Port 2's message status is readable from the Port 1 side via Control register 2. When Port 2's CPU reads the data from its Message In register, the Port 2 IP is cleared. Thus, Port 1's CPU can tell that the message has been read and can now send another message or follow whatever protocol that is set up between the two CPU's. The same transfer can also be made from Port 2's CPU to Port 1's CPU.

CLEAR (Empty) FIFO Operation

The $\overline{\text{CLEAR}}$ FIFO bit (active LOW) clears the FIFO buffer of data. Writing a 0 to this bit empties the FIFO buffer, inactivates the $\overline{\text{REQUEST}}$ line, and disables the handshake (if programmed). The $\overline{\text{CLEAR}}$ bit does not affect any control or data register. To remove the $\overline{\text{CLEAR}}$ state, write a 1 to the $\overline{\text{CLEAR}}$ bit.

In CPU/CPU mode, under program control, only one of the ports can empty the FIFO by writing to its Control register 3, bit 6. The Port 1 CPU must program bit 7 in Control register 3 to determine which port controls the CLEAR FIFO operation (0 = Port 1 control; 1 = Port 2 control).

Direction of Data Transfer Operation

The Data Direction bit controls the direction of data transfer in the FIFO buffer. The Data Direction bit is defined as 0 = output from CPU and 1 = input to CPU. This bit reads correctly when read by either port's CPU. For example, if Port 1's CPU reads a 0 (CPU output) in its Data Direction bit, then Port 2's CPU reads a 1 (input to CPU) in its Data Direction bit.

In CPU/CPU mode, under program control, only one of the ports can control the direction of data transfer. The Port 1 CPU must program bit 5 in Control register 3 to determine which port controls the data direction (0 = Port 1 control; 1 = Port 2 control). Figure 18 shows FIO data transfer options.

CPU TO I/O OPERATION

When Port 2 is programmed in the Interlocked 2-Wire Handshake mode or the 3-Wire Handshake mode, and Port A is programmed in Z-BUS or non-Z-BUS Microprocessor mode, the FIO interfaces a CPU and a peripheral device. In the interlocked 2-Wire Handshake mode, RFD/$\overline{\text{DAV}}$ and $\overline{\text{ACKIN}}$ strobe data to and from Port 2. In the 3-Wire Handshake mode, RFD/$\overline{\text{DAV}}$, $\overline{\text{DAV}}$/DAC, and DAC/RFD signal control data flow.

Interlocked 2-Wire Handshake

In the Interlocked Handshake, the action of the FIO must be acknowledged by the other half of the handshake before the next action can take place. In output mode, Port 2 does not indicate that new data is available until the external device indicates it is ready for the data. Similarly, in input mode, Port 2 does not indicate that it is ready for new data until the data source indicates that the previous byte of the data is no longer available, thereby acknowledging Port 2's acceptance of the last byte. This allows the FIO to directly interface to a Z8's port, a CIO's port, a UPC's port, another FIO port, or another FIFO Z8060, with no external logic (Figures 19 and 20).

3-Wire Handshake

The 3-Wire Handshake is designed for applications in which one output port is communicating with many input ports simultaneously. It is essentially the same as the Interlocked Handshake, except that two signals are used to indicate that an input port is ready for new data or that it has accepted the present data. In the 3-Wire Handshake, the rising edge of the RFD status line indicates that the port is ready for data, and the rising edge of the DAC status line indicates that the data has been accepted. With 3-Wire Handshake, the lines of many input ports can be bussed together with open-drain drivers, and the output port knows when all of the ports are ready and have accepted the data. This handshake is the same handshake used in the IEEE-488 Instruments. Since the port's direction can be changed under software control, bidirectional IEEE-488 type transfers can be performed. Figures 21 and 22 show the timings associated with 3-Wire Handshake communications.

CLEAR FIFO Operation

In CPU-to-I/O operation, the CLEAR FIFO operation can be performed by the CPU side (Port 1) under software control as previously explained. The CLEAR FIFO operation can also be performed under hardware control by defining the $\overline{\text{CLEAR}}$ pin of Port 2 as an input (Control register 3, bit 7 = 1).

For cascading purposes, the $\overline{\text{CLEAR}}$ pin can also be defined as an output (Control register 3, bit 7 = 0), which reflects the current state of the $\overline{\text{CLEAR}}$ FIFO bit. It can then empty other FIOs or initialize other devices in the system.

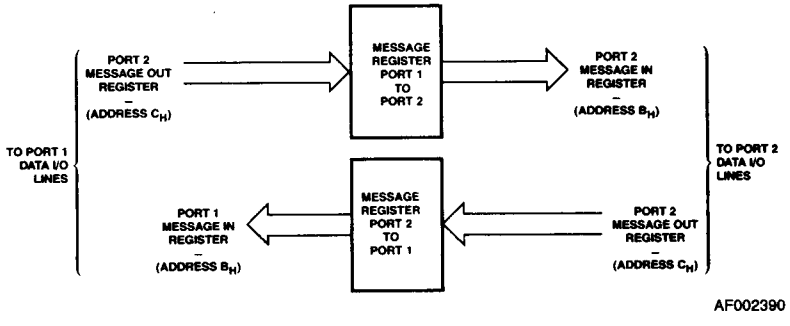


Figure 17. Message Register Operation

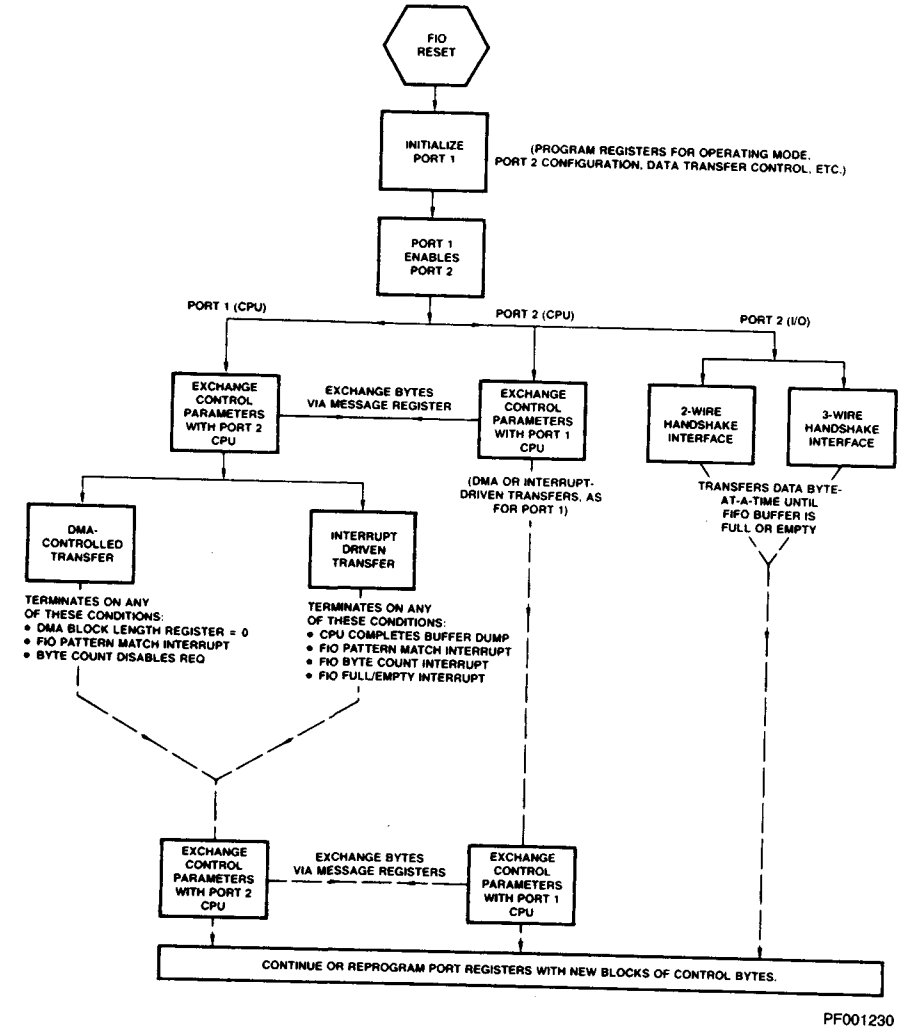


Figure 18. FIO Data Transfer Options

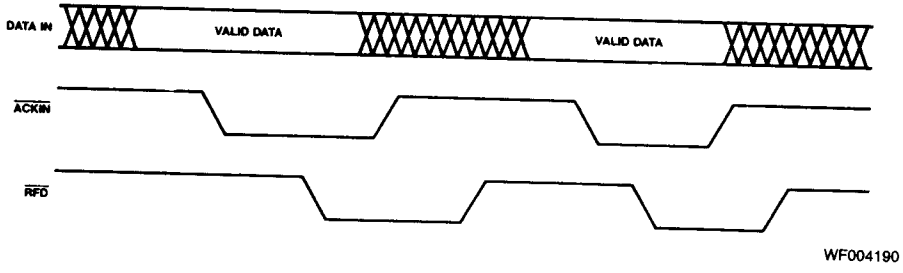


Figure 19. Input Timing for Interlocked Handshake Timing (Port 2 Side Only)

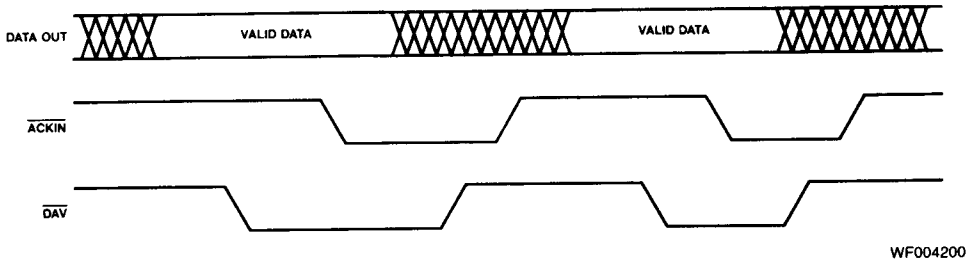


Figure 20. Output Timing for Interlocked Handshake Timing (Port 2 Side Only)

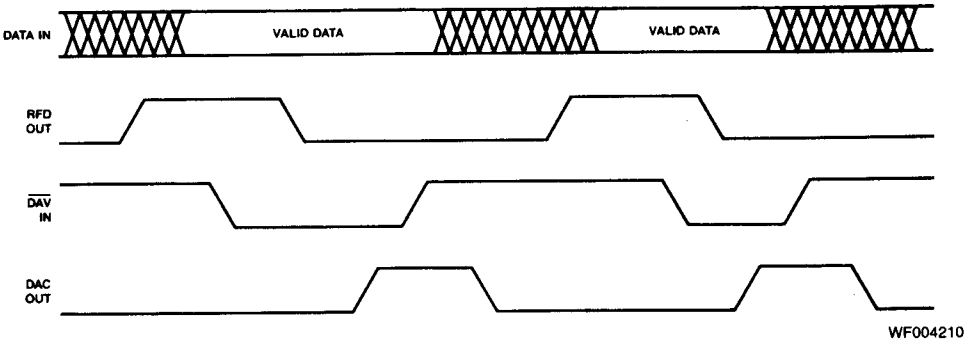


Figure 21. Input (Acceptor) Timing IEEE-488 HS (Port 2 Side Only)

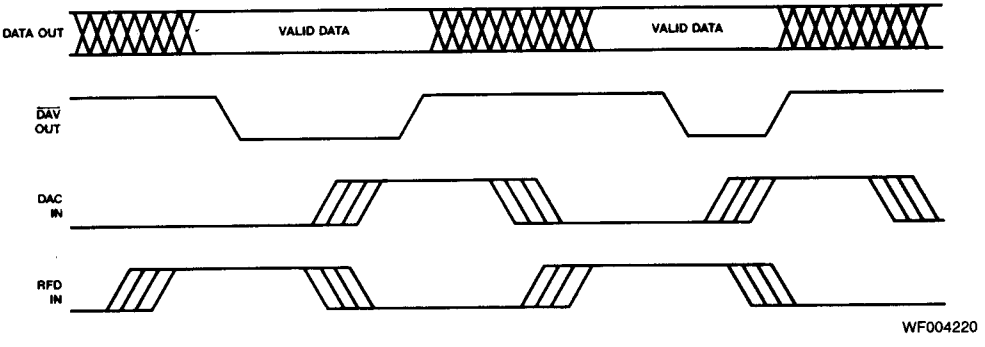


Figure 22. Output (Source) Timing IEEE-488 HS Port (Port 2 Side Only)

Data Direction Control

In CPU-to-I/O mode, the direction of data transfer can be controlled by the CPU side (Port 1) under software control as previously explained. The data direction can also be determined by hardware control by defining the Data Direction pin of Port 2 as an input (Control register 3, bit 5 = 1).

For cascading purposes, the Data Direction pin can also be defined as an output (Control register 3, bit 5 = 0) pin which reflects the current state of the Data Direction bit. It can then be used to control the direction of data transfer for other FIOs or for external logic.

On the Port 2 side, when data direction is 0, Port 2 is in Output Handshake mode. When data direction is 1, Port 2 is in Input Handshake mode.

PROGRAMMING INFORMATION

The Programming of the FIO is greatly simplified by the efficient grouping of the various operation modes in the control registers. Since all of the control registers are read/write, the need for maintaining their image in system memory is eliminated. Also, the read/write feature of the registers aids in system debugging.

Each side of the FIO has 16 registers. All 16 registers are used by the Port 1 side; Control register 2 is not used on the Port 2 side. All registers are addressable O_H through F_H.

In the Z-BUS Low Byte mode, the FIO allows two methods for register addressing under control of the Right Justify Address (RJA) bit in Control register 0. When RJA = 0, address bus bits 1 – 4 are used for register addressing and bits 0, 5, 6 and 7 are ignored (Table 3). When RJA = 1, bits 0 – 3 are used for the register addresses and bits 4 – 7 are ignored.

Control Registers

These four registers specify FIO operation. The Port 2 side control registers operate only if the Port 2 device is a CPU. The Port 2 CPU can control interface operations, including data direction, only when enabled by the setting of bit 0 in the Port 1 side of Control register 2. A 1 in bit 1 of the same register enables the handshake logic.

Interrupt Status Registers

These four registers control and monitor the priority interrupt functions for the FIO.

Interrupt Vector Register

This register stores the interrupt service routine address. This vector is placed on $D_0 - D_7$ when IUS is set by the Interrupt Acknowledge signal from the CPU. When bit 4 (Vector Includes Status) is set in Control register 0, the reason for the Interrupt is encoded within the vector address in bits 1, 2 and 3. If bit 5 is set in Control register 0, no vector is output by the FIO during an Interrupt Acknowledge cycle. However, IUS is set as usual.

Byte Count Compare Register

This register contains a value compared with the byte count in the Byte Count register. If the Byte Count Compare interrupt is enabled, an interrupt will occur upon compare.

Message Out Register

Either CPU can place a message in its Message Out register. If the opposite side Message register interrupt is enabled, the receiving side CPU will receive an interrupt request, advising that a message is present in its Message In register. Bit 5 in Control register 1 on the initiating side is set when a message is written. It is cleared when the Byte Count register read is completed.

TABLE 3. FIO REGISTER ADDRESS SUMMARY

Non-Z-Bus		D_7-D_4	D_3	D_2	D_1	D_0	
Z-BUS High Byte			A_3	A_2	A_1	A_0	
Z-BUS Low Byte	RJA = 0	AD_7-AD_5	AD_4	AD_3	AD_2	AD_1	AD_0
	RJA = 1	AD_7-AD_4	AD_3	AD_2	AD_1	AD_0	
Description							
Control Register 0		X	0	0	0	0	X
Control Register 1		X	0	0	0	1	X
Interrupt Status Register 0		X	0	0	1	0	X
Interrupt Status Register 1		X	0	0	1	1	X
Interrupt Status Register 2		X	0	1	0	0	X
Interrupt Status Register 3		X	0	1	0	1	X
Interrupt Vector Register		X	0	1	1	0	X
Byte Count Register		X	0	1	1	1	X
Byte Count Comparison Register		X	1	0	0	0	X
Control Register 2*		X	1	0	0	1	X
Control Register 3		X	1	0	1	0	X
Message Out Register		X	1	0	1	1	X
Message In Register		X	1	1	0	0	X
Pattern Match Register		X	1	1	0	1	X
Pattern Mask Register		X	1	1	1	0	X
Data Buffer Register		X	1	1	1	1	X

X = Don't Care
*Register is only on Port 1 side

Refer to page 7-1 for Essential Information on Military Devices

Message in Register

This register receives a message placed in the Message Out register by the opposite side CPU.

Pattern Match Register

This register contains a bit pattern matched against the byte in the Data Buffer register. When these patterns match, a Pattern Match interrupt will be generated, if previously enabled.

Pattern Mask Register

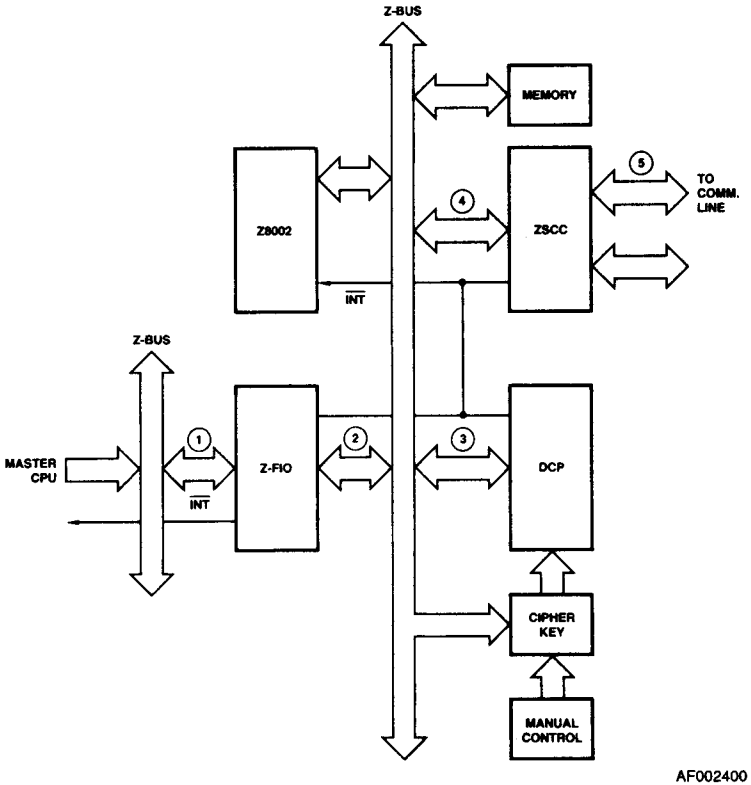
The Pattern Mask register may be programmed with a bit pattern mask that limits comparable bits in the Pattern Match register to non-masked bits (1 = mask).

Data Buffer Register

This register contains the data to be read from or written to the FIFO buffer.

Byte Count Register

This is a read-only register, containing the byte count for the FIFO buffer. The byte count is derived by subtracting the number of bytes read from the buffer from the number of bytes written into the buffer. The count is copied into a holding register for an accurate reading by setting bit 6 (Freeze Status register) in Control register 1. This bit is cleared when the Byte Count register is completed.



DATA FLOW: 1. Data from master CPU → Z-FIO Port 2.
2. Z-FIO Port 1 → DCP.
3. DCP → RAM.
4. RAM → Z-SCC.
5. Z-SCC → data comm. line loop.

Figure 23. Typical Application: Node Controller

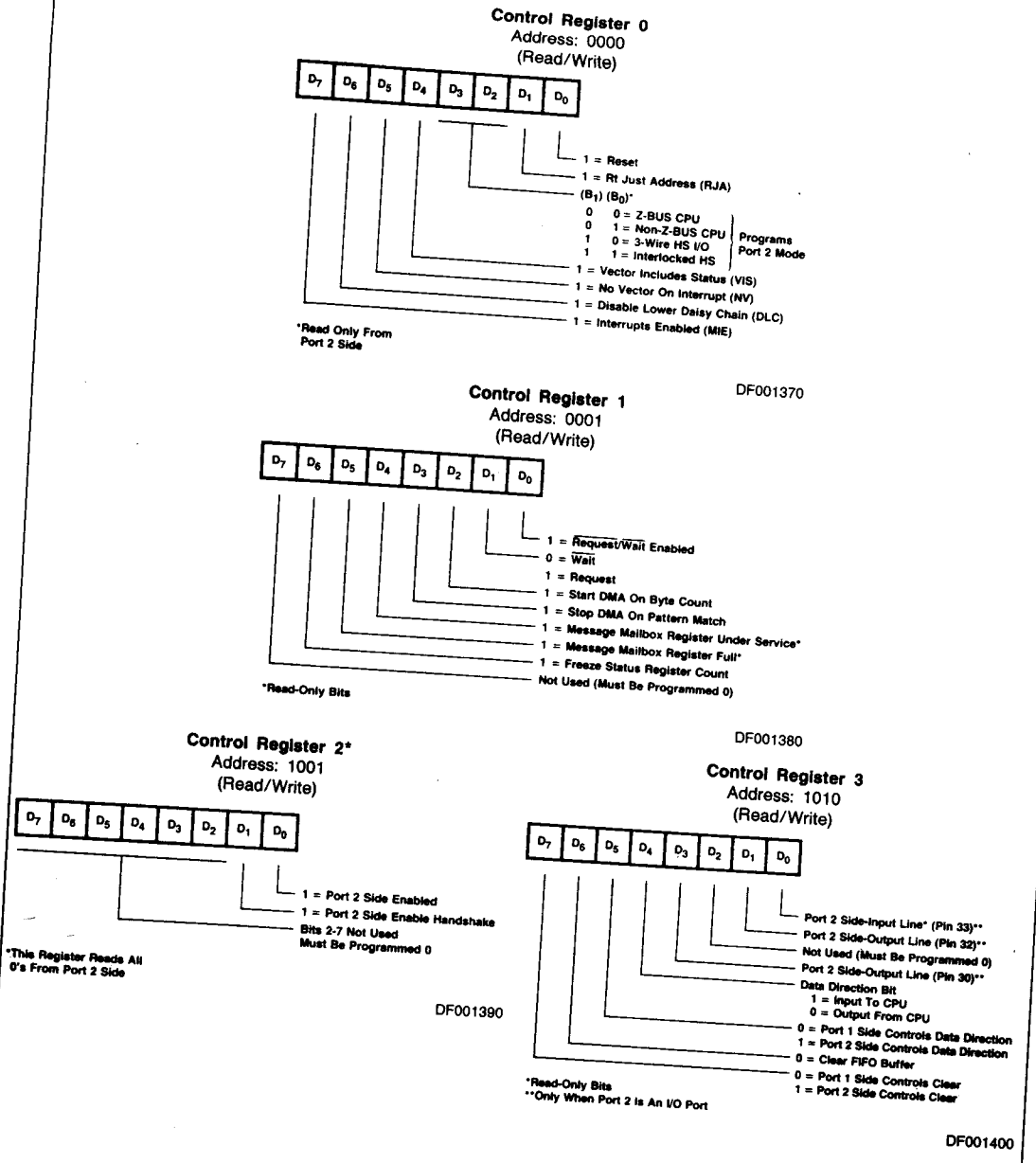
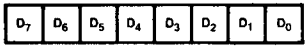


Figure 24. Control Registers

REGISTERS (Cont.)

Interrupt Status Register 0

Address: 0010
(Read/Write)



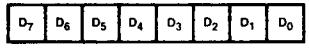
Not Used
(Must Be Programmed 0)
Message Interrupt Pending (IP)
Message Interrupt Enable (IE)
Message Interrupt Under Service (IUS)

Messages IUS, IE, and IP are Written Using The Following Commands: ($D_4 - D_0 = 0$)

D_7	D_6	D_5	
0	0	0	Null Code (No Change)
0	0	1	Clear IP & IUS
0	1	0	Set IUS
0	1	1	Clear IUS
1	0	0	Set IP
1	0	1	Clear IP
1	1	0	Set IE
1	1	1	Clear IE

DF001411

Interrupt Status Register 1
Address: 0011
(Read/Write)



Data Direction Change Interrupt Under Service (IUS)
Data Direction Change Interrupt Enable (IE)
Data Direction Change Interrupt Pending (IP)
1 = Pattern Match Flag*
Pattern Match Interrupt Pending (IP)
Pattern Match interrupt Enabled (IE)
Pattern Match Interrupt Under Service (IUS)
Not Used
(Must Be Programmed 0)

Directions IUS, IE, and IP are Written Using The Following Commands: (D_0 and $D_4 = 0$)

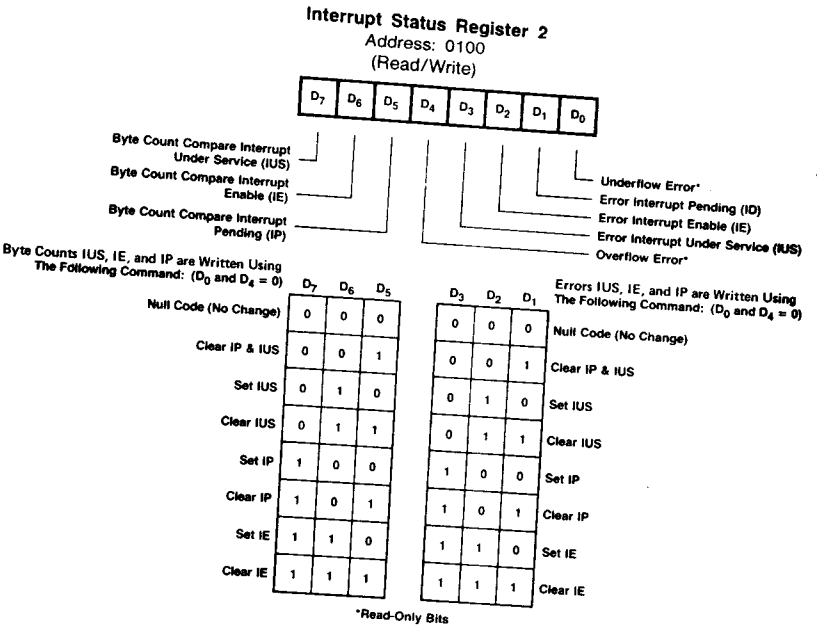
Pattern Matches IUS, IE, and IP are Written Using The Following Commands: (D_0 and $D_4 = 0$)

D_7	D_6	D_5	D_3	D_2	D_1	
0	0	0	0	0	0	Null Code (No Change)
0	0	1	0	0	1	Clear IP & IUS
0	1	0	0	1	0	Set IUS
0	1	1	0	1	1	Clear IUS
1	0	0	1	0	0	Set IP
1	0	1	1	0	1	Clear IP
1	1	0	1	1	0	Set IE
1	1	1	1	1	1	Clear IE

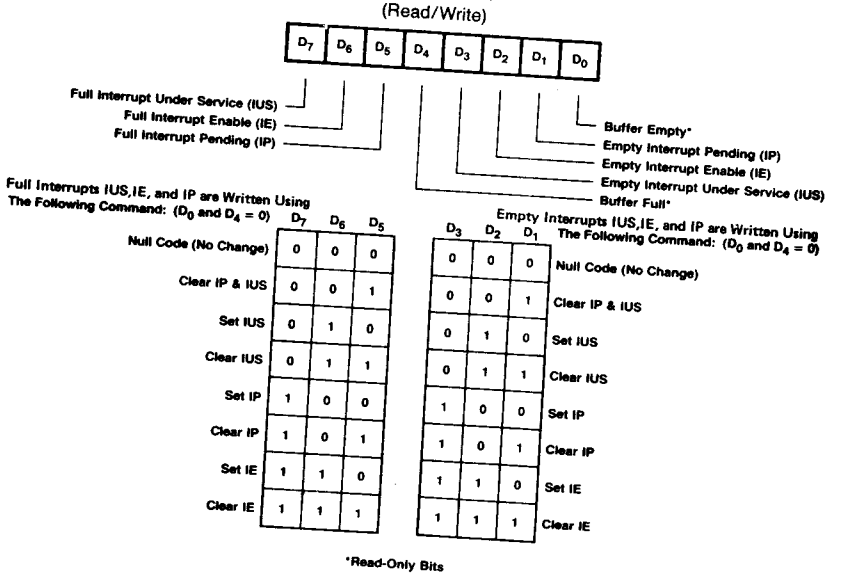
*Read only bits

DF001421

Figure 25. Interrupt Status Registers



DF001431



DF001441

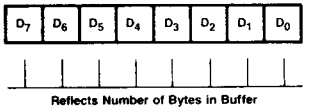
Figure 25. Interrupt Status Registers (Cont.)

Refer to page 7-1 for Essential Information on Military Devices

REGISTERS (Cont.)

Byte Count Register

Address: 0111



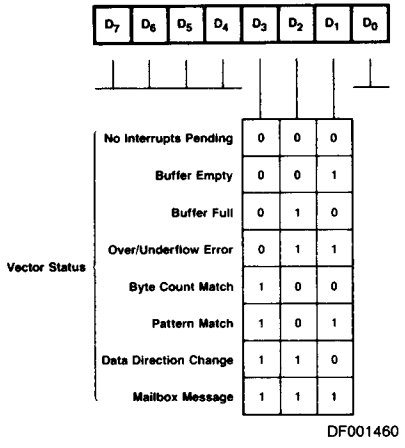
(Copied from actual Byte Counter by setting bit 6 of CR1.)

DF001450

Figure 26. Byte Count Register

Interrupt Vector Register

Address: 0110
(Read/Write)

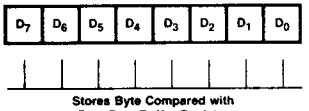


DF001460

Figure 27. Interrupt Vector Register

Pattern Match Register

Address: 1101
(Read/Write)

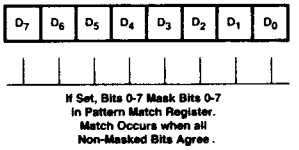


DF001470

Figure 28. Pattern Match Register

Pattern Mask Register

Address: 1110
(Read/Write)

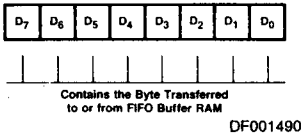


DF001481

Figure 29. Pattern Mask Register

Data Buffer Register

Address: 1111
(Read/Write)

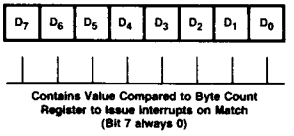


DF001490

Figure 30. Data Buffer Register

Byte Count Comparison Register

Address: 1000
(Read/Write)

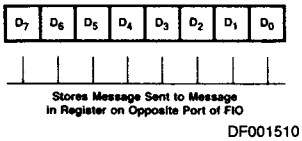


DF001500

Figure 31. Byte Count Comparison Register

Message Out Register

Address: 1011
(Read/Write)

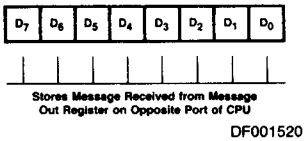


DF001510

Figure 32. Message Out Register

Message In Register

Address: 1100
(Read Only)



DF001520

Figure 33. Message In Register

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage at any Pin Relative to V_{SS} ..... −0.5V to +7.0V
Power Dissipation 1.75W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

	4MHz	6MHz
	Z8038	Z8038A
Commercial Operating Range T_A = 0 to +70°C V_{CC} = 5V ±5% V_{SS} = 0V	Z8038DC Z8038PC	Z8038ADC Z8038APC
Industrial Operating Range T_A = −40 to +85°C V_{CC} = 5V ±10% V_{SS} = 0V	Z8038DI	

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Note 1)

Parameters	Description	Test Conditions		Min	Typ	Max	Units
V_{IL}	Input LOW Voltage			−0.5		+.8	Volts
V_{IH}	Input HIGH Voltage	Standard Temp		2.0		V_{CC}	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 3.2mA				0.5	Volts
V_{OH}	Output HIGH Voltage	I_{OL} = 2.0mA				0.4	Volts
I_{OZL}	Output Leakage Current	I_{OH} = −250µA		2.4			Volts
I_{OZH}	Output Leakage Current	V_{OUT} = 0.4V				10	µA
I_I	Input Leakage Current	V_{OUT} = V_{CC}				10	µA
C_{IN}	Input Capacitance	Unmeasured pins returned to ground. f = 1MHz over specified temperature range.				±10	µA
$C_{I/O}$	I/O Capacitance					10	pF
C_{OUT}	Output Capacitance					20	pF
I_{CC}	Power Supply Current	V_{CC} = MAX	T_A = 0°C			15	pF
			T_A = −55°C			200	mA
						250	

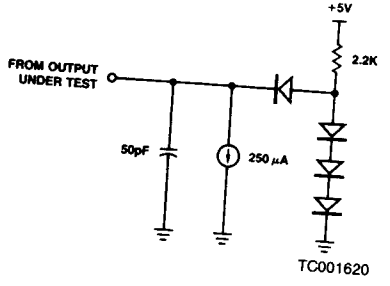
Note: 1. See table for operating range. Typical conditions apply at T_A = 25°C, V_{CC} = 5.0V.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

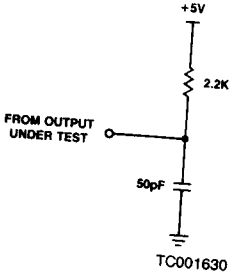
+4.75V ≤ V_{CC} ≤ +5.25V
GND = 0V
0°C ≤ T_A ≤ +70°C

Standard Test Load



TC001620

Open-Drain Test Load



TC001630

00867B

Refer to page 7-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Z-BUS CPU INTERFACE TIMING

Number	Parameters	Description	4MHz		6MHz		Units	Notes*
			Min	Max	Min	Max		
1	TwAS	$\overline{AS}$ Low Width	70		50		ns	
2	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time	30		10		ns	1
3	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time	50		30		ns	1
4	TsCSO(AS)	$\overline{CS}$ to $\overline{AS}$ ↑ Setup Time	0		0		ns	1
5	ThCSO(AS)	$\overline{CS}$ to $\overline{AS}$ ↑ Hold Time	60		40		ns	1
6	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↑ Delay	60		40		ns	1
7	TsA(DS)	Address to $\overline{DS}$ ↓	120		100		ns	
8	TsRWR(DS)	R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Setup Time	100		80		ns	
9	TsRWW(DS)	R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Setup Time	0		0		ns	
10	TwDS	$\overline{DS}$ Low Width	390		250		ns	
11	TsDW(DSf)	Write Data to $\overline{DS}$ ↓ Setup Time	30		20		ns	
12	TdDS(DRV)	$\overline{DS}$ (Read) ↓ to Address Data Bus Driven	0		0		ns	
13	TdDSf(DR)	$\overline{DS}$ ↓ to Read Data Valid Delay		250		180	ns	
14	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	30		20		ns	
15	TdDSr(DR)	$\overline{DS}$ ↑ to Read Data Not Valid Delay	0		0		ns	
16	TdDS(DRz)	$\overline{DS}$ ↑ to Read Data Float Delay		70		45	ns	2
17	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time	55		40		ns	
18	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	50		25		ns	
19	Trc	Valid Access Recovery Time	1000		650		ns	3

Notes:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is measured up to the time when the output has changed 0.5V from steady state with minimum AC load and maximum DC load.
3. This is the delay from $\overline{DS}$ of one CIO access to $\overline{DS}$ of another FIO access (either read or write).

*All timings are preliminary and subject to change. All timing references assume 2.0V for a logic "1" and 0.8V for a logic "0."

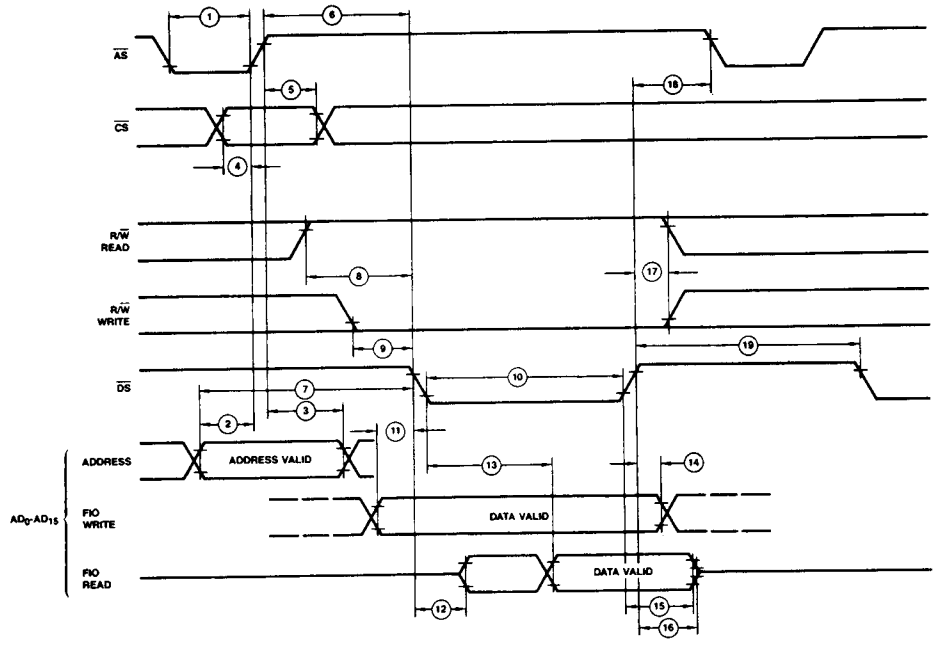


Figure 34. Z-BUS CPU Interface Timing

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Refer to page 7-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Z-BUS CPU INTERRUPT ACKNOWLEDGE TIMING

Number	Parameters	Description	4MHz		6MHz		Units	Notes
			Min	Max	Min	Max		
20	TslA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	0		0		ns	
21	ThlA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250		250		ns	
22	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Data Valid Delay		250		180	ns	
23	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	390		250		ns	
24	TdAS(IEO)	$\overline{AS}$ ↑ to IEO ↓ Delay ($\overline{INTACK}$ Cycle)		350		250	ns	
25	TdIEI(IEO)	IEI to IEO Delay		150		100	ns	4
26	TsIEI(DSA)	IEI to $\overline{DS}$ (Acknowledge) ↓ Setup Time	100		70		ns	4
27	ThIEI(DSA)	IEI to $\overline{DS}$ (Acknowledge) ↑ Hold Time	50		30		ns	
28	TdDS(INT)	$\overline{DS}$ ($\overline{INTACK}$ Cycle) to $\overline{INT}$ Delay		800		800	ns	4
29	TdDCST	Interrupt Daisy Chain Settle Time					ns	4

Note: 4. The parameters for the devices in any particular daisy chain must meet the following constraints: the delay from $\overline{AS}$ to $\overline{DS}$ must be greater than the sum of TdAS(IEO) for the highest priority peripheral, TsIEI(DSA) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.

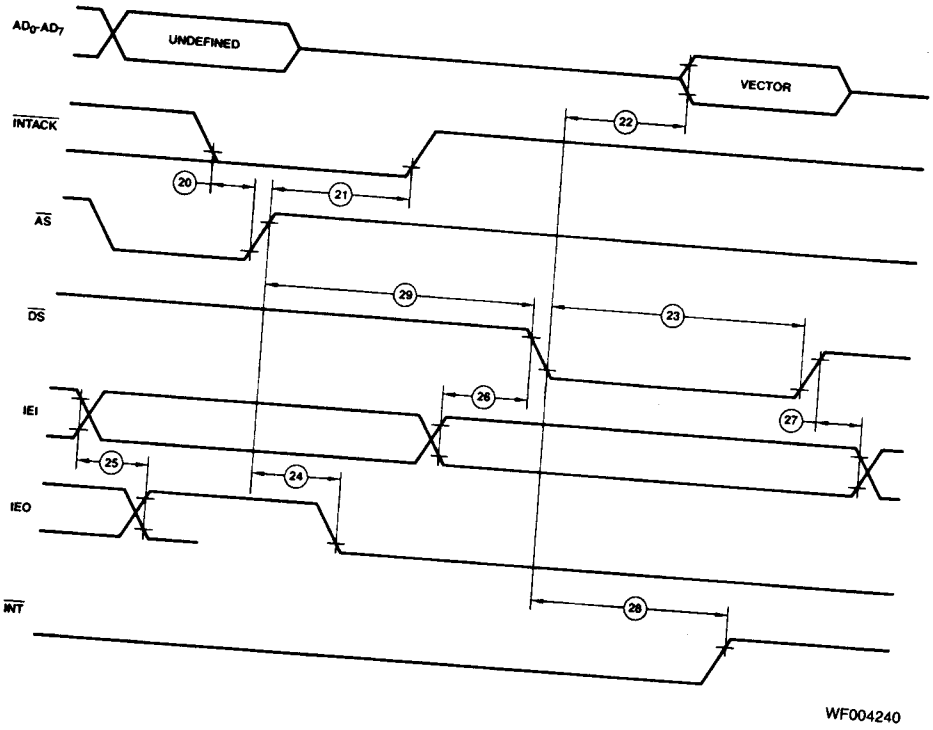

Figure 35. Z-Bus CPU Interrupt Acknowledge Timing

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Z-BUS INTERRUPT TIMING

Number	Parameters	Description	4MHz Min	4MHz Max	6MHz Min	6MHz Max	Units	Notes
30	TdMW(INT)	Message Write to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles + ns	5
31	TdDC(INT)	Data Direction Change to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles + ns	6
32	TdPMW(INT)	Pattern Match to $\overline{INT}$ Delay (Write Case)		1		1	$\overline{AS}$ Cycles + ns	
33	TdPMR(INT)	Pattern Match (Read Case) to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles + ns	
34	TdSC(INT)	Status Compare to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles + ns	6
35	TdER(INT)	Error to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles + ns	
36	TdEM(INT)	Empty to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles + ns	6
37	TdFL(INT)	Full to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles + ns	6
38	TdAS(INT)	$\overline{AS}$ to $\overline{INT}$ Delay					$\overline{AS}$ Cycles + ns	

Notes: 5. Write is from the other side of FIO.
6. Write can be from either side, depending on programming of FIO.

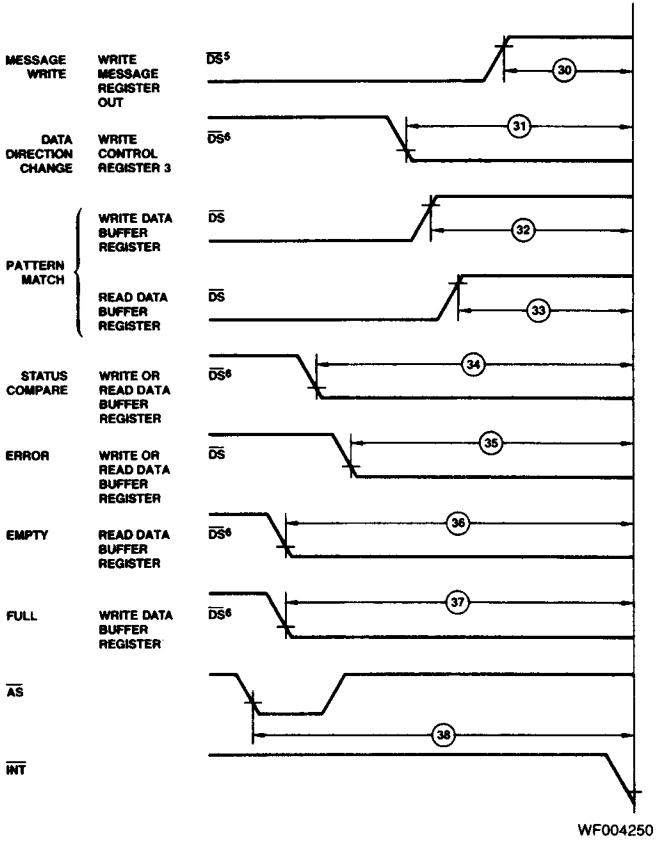

Figure 36. Z-Bus Interrupt Timing

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Z-BUS REQUEST/WAIT TIMING

Number	Parameters	Description	4MHz		6MHz		Units	Notes
			Min	Max	Min	Max		
1	TdDS(WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay		190		160	ns	
2	TdDS1(WAIT)	$\overline{DS1}$ ↑ to $\overline{WAIT}$ ↑ Delay		1000		1000	ns	
3	TdACK(WAIT)	$\overline{ACKIN}$ ↓ to $\overline{WAIT}$ ↑ Delay		1000		1000	ns	
4	TdDS(REQ)	$\overline{DS}$ ↓ to $\overline{REQ}$ ↑ Delay		350		300	ns	1
5	TdDMA(REQ)	$\overline{DMASTB}$ ↓ to $\overline{REQ}$ ↑ Delay		350		300	ns	
6	TdDS1(REQ)	$\overline{DS1}$ ↑ to $\overline{REQ}$ ↓ Delay		1000		1000	ns	
7	TdACK(REQ)	$\overline{ACKIN}$ ↓ to $\overline{REQ}$ ↓ Delay		1000		1000	ns	
8	TdSU(DMA)	Data Setup Time to $\overline{DMASTB}$	200		150		ns	
9	TdH(DMA)	Data Hold Time to $\overline{DMASTB}$	30		20		ns	
10	TdDMA(DR)	$\overline{DMASTB}$ ↓ Data Valid		150		100	ns	
11	TdDMA(DRH)	$\overline{DMASTB}$ ↑ to Data Not Valid	0		0		ns	
12	TdDMA(DR2)	$\overline{DMASTB}$ ↑ to Data Bus Float		70		45	ns	

Note: 1. The Delay is from $\overline{DAV}$ ↓ for 3-Wire Input Handshake. The delay is from DAC ↑ for 3-Wire Output Handshake.

SWITCHING WAVEFORMS

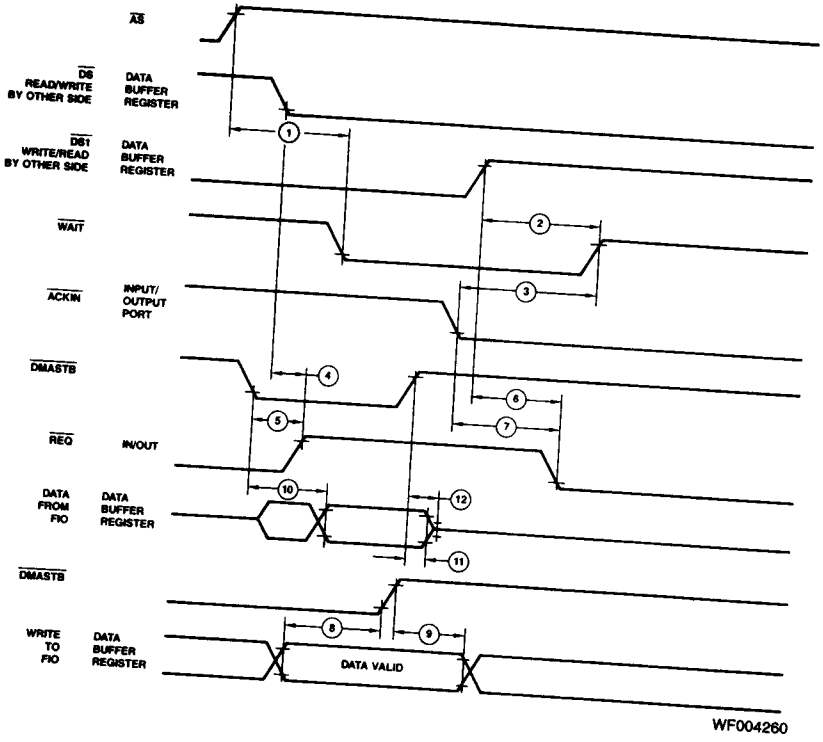

Figure 37.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Z-BUS RESET TIMING

Number	Parameters	Description	4MHz		6MHz		Units	Notes
			Min	Max	Min	Max		
1	TdDSQ(AS)	Delay from $\overline{DS}$ ↑ to $\overline{AS}$ ↓ for No. Reset	40		20		ns	
2	TdASQ(DS)	Delay for $\overline{AS}$ ↑ to $\overline{DS}$ ↓ for No. Reset	50		30		ns	
3	Tw(AS + DS)	Minimum Width of $\overline{AS}$ and $\overline{DS}$ both Low for Reset	500		350		ns	1

Note: 1. Internal circuitry allows for the reset provided by the Z8 ($\overline{DS}$ held Low while $\overline{AS}$ pulses) to be sufficient.

SWITCHING WAVEFORMS

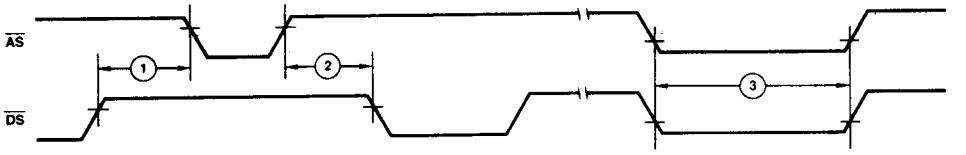

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Figure 38.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

NON-Z-BUS CPU INTERFACE TIMING

Number	Parameters	Description	4MHz		6MHz		Units	Notes
			Min	Max	Min	Max		
1	TsA(RD)	Address Setup to $\overline{RD}$ ↓	80		80		ns	1
2	TsA(WR)	Address Setup to $\overline{WR}$ ↓	80		80		ns	
3	ThA(RD)	Address Hold Time to $\overline{RD}$ ↑	0		0		ns	1
4	ThA(WR)	Address Hold Time to $\overline{WR}$ ↑	0		0		ns	
5	TsCEI(RD)	$\overline{CE}$ Low Setup Time to $\overline{RD}$	0		0		ns	1
6	TsCEI(WR)	$\overline{CE}$ Low Setup Time to $\overline{WR}$	0		0		ns	
7	ThCEI(RD)	$\overline{CE}$ Low Hold Time to $\overline{RD}$	0		0		ns	1
8	ThCEI(WR)	$\overline{CE}$ Low Hold Time to $\overline{WR}$	0		0		ns	
9	TsCEh(RD)	$\overline{CE}$ High Setup Time to $\overline{RD}$	0		0		ns	1
10	TsCEh(WR)	$\overline{CE}$ High Setup Time to $\overline{WR}$	100		70		ns	
11	TwRD1	$\overline{RD}$ Low Width	100		70		ns	1
12	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	390		250		ns	
13	TdRDf(DR)	$\overline{RD}$ ↓ to Valid Data Delay	0		0		ns	
14	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay		250		180	ns	
15	TdRD(DRz)	$\overline{RD}$ ↑ to Data Bus Float	0		0		ns	
16	TwWR1	$\overline{WR}$ Low Width		70		45	ns	2
17	TsDW(WR)	Data Setup Time to $\overline{WR}$	390		250		ns	
18	ThDW(WR)	Data Hold Time to $\overline{WR}$	0		0		ns	
19	Trc	Valid Access Recovery Time	30		20		ns	
			1000		650		ns	3

Notes: 1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is measured to the time the output has changed 0.5V from steady state with minimum AC load and maximum DC load.
3. This is the delay from $\overline{RD}$ ↑ or $\overline{WR}$ ↑ of one FIO access to $\overline{RD}$ ↓ or $\overline{WR}$ ↓ of another FIO access.

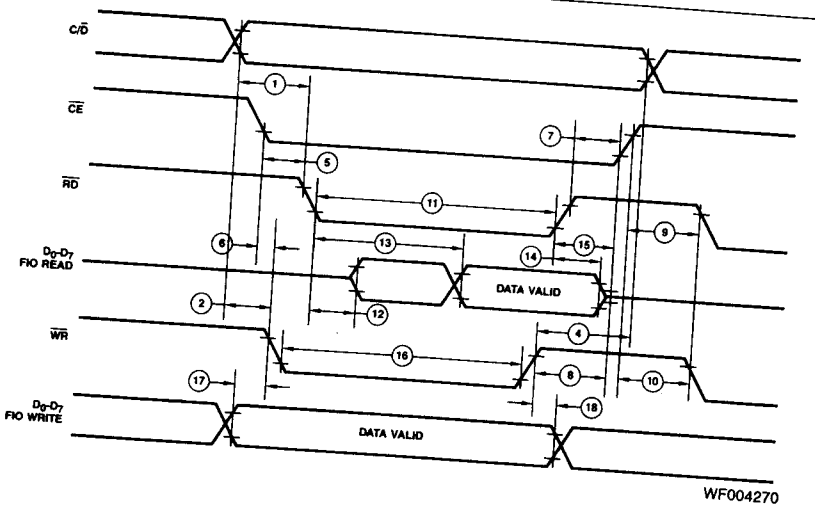

Figure 39a. Non-Z-Bus CPU Interface Timing

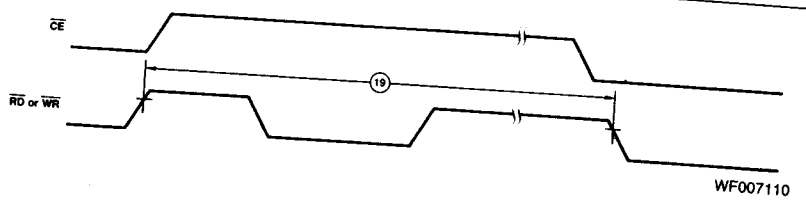

Figure 39b. Non-Z-Bus Interface Timing

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

NON-Z-BUS INTERRUPT ACKNOWLEDGE TIMING

Number	Parameters	Description	4MHz		6MHz		Units	Notes
			Min	Max	Min	Max		
20	TdIEI(IEO)	IEI to IEO Delay		150		100	ns	4
21	TdI(IEO)	$\overline{INTACK}$ ↓ to IEO ↓ Delay		350		250	ns	4
22	TsIEI(RDA)	IEI Setup Time to $\overline{RD}$ (Acknowledge)	100		70		ns	4
23	TdRD(DR)	$\overline{RD}$ ↓ to Vector Valid Daly		250		180	ns	
24	TwRD1(IA)	Read Low Width (Interrupt Acknowledge)	390		250		ns	
25	ThIA(RD)	$\overline{INTACK}$ ↑ to $\overline{RD}$ ↑ Hold Time	30		20		ns	
26	ThIEI(RD)	IEI Hold Time to $\overline{RD}$ ↑	20		10		ns	
27	TdRD(INT)	$\overline{RD}$ ↑ to $\overline{INT}$ ↑ Delay		800		800	ns	
28	TdDCST	Interrupt Daisy Chain Settle Time		350		250	ns	4

Notes: 4. The parameter for the devices in any particular daisy chain must meet the following constraints: the delay from $\overline{INTACK}$↓ to $\overline{RD}$↓ must be greater than the sum of TdINA(IEO) for the highest priority peripheral, TsIEI(RD) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.

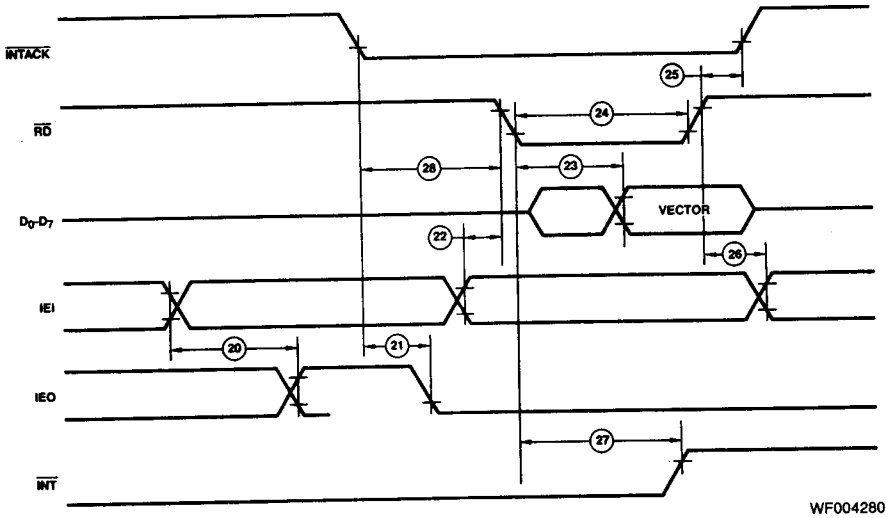

Figure 40. Non-Z-Bus Interrupt Acknowledge Timing

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

NON-Z-BUS REQUEST/WAIT TIMING

Number	Parameters	Description	4MHz		6MHz		Units	Notes
			Min	Max	Min	Max		
1	TdRD(WT)	$\overline{CE}$ ↓ to $\overline{WAIT}$ Active		200		170	ns	
2	TdRD1(WT)	$\overline{RD1}$ ↓ to $\overline{WAIT}$ Inactive		1000		1000	ns	
3	TdACK(WT)	$\overline{ACKIN}$ ↓ to $\overline{WAIT}$ Inactive		1000		1000	ns	
4	TdRD(REQ)	$\overline{RD}$ ↓ to $\overline{REQ}$ Inactive		350		300	ns	1
5	TdRD1(REQ)	$\overline{RD1}$ ↑ to $\overline{REQ}$ Active		1000		1000	ns	
6	TdACK(REQ)	$\overline{ACKIN}$ ↓ to $\overline{REQ}$ Active		1000		1000	ns	
7	TdDAC(RD)	$\overline{DACK}$ ↓ to $\overline{RD}$ ↓ or $\overline{WR}$ ↓	100		80		ns	
8	TSU(WR)	Data Setup Time to $\overline{WR}$	200				ns	
9	Th(WR)	Data Hold Time to $\overline{WR}$	30		20		ns	
10	TdDMA	$\overline{RD}$ ↓ to Valid Data		150		100	ns	
11	TdDMA(DRH)	$\overline{RD}$ ↑ to Data Not Valid	0		0		ns	2
12	TdDMA(DRZ)	$\overline{RD}$ ↑ to Data Bus Float		70		45	ns	2

Notes: 1. The delay is from $\overline{DAV}$↓ for 3-Wire Input Handshake. The delay is from DAC↑ for 3-Wire Input Handshake.
2. Only when $\overline{DACK}$ is active.

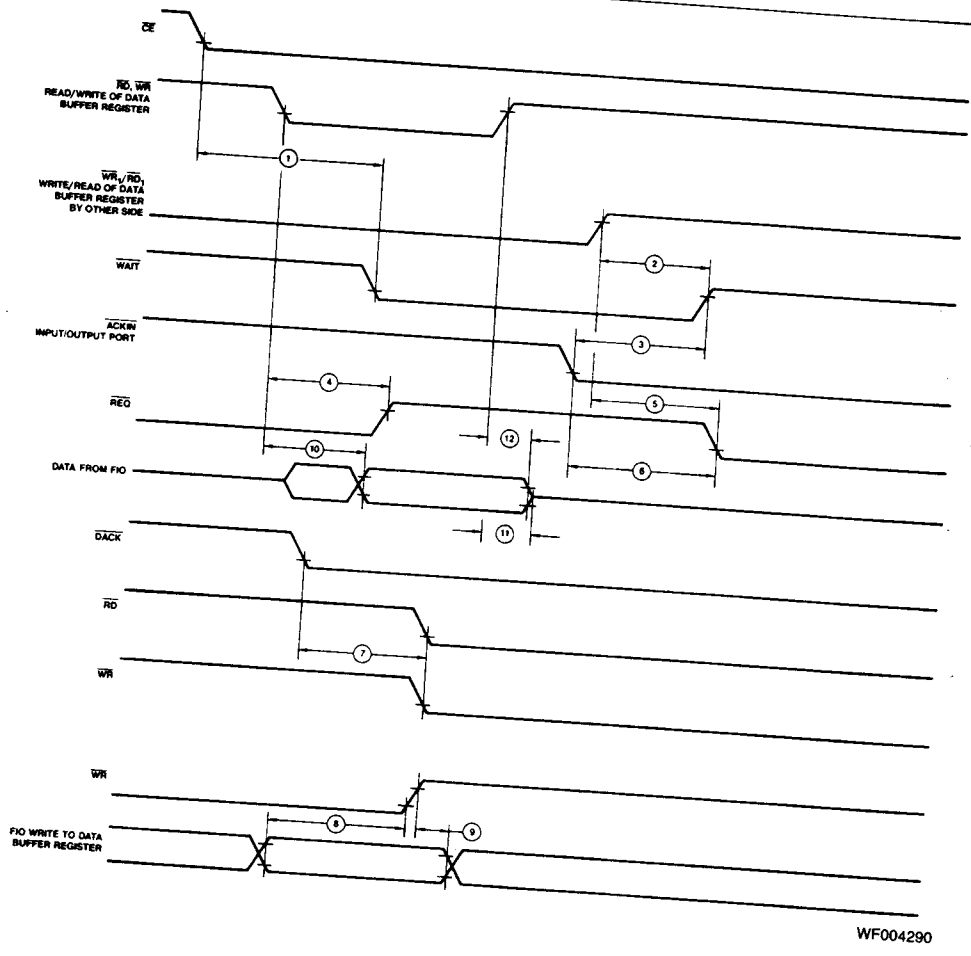

Figure 41. Non-Z-Bus Request/Wait Timing

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
NON-Z-BUS RESET TIMING

Number	Parameters	Description	4MHz		6MHz		Units	Notes
			Min	Max	Min	Max		
1	TdWR(RD)	Delay from $\overline{WR}$ ↑ to $\overline{RD}$ ↓	100		70		ns	
2	TdRD(WR)	Delay from $\overline{RD}$ ↑ to $\overline{WR}$ ↓	100		70		ns	
3	TwRD + WR	Width of $\overline{RD}$ and $\overline{WR}$, both Low for Reset	500		350		ns	

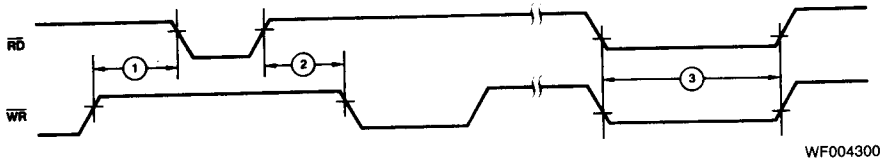

Figure 42. Non-Z-Bus Reset Timing

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
PORT 2 SIDE OPERATION

Number	Parameters	Description	4MHz		6MHz		Units	Notes
			Min	Max	Min	Max		
1	TwCLR	Width of Clear to Reset FIFO	700		700		ns	
2	TdOE(DO)	$\overline{OE}$ ↓ to Data Bus Driven	0	150	0	150	ns	
3	TdOE(DRZ)	$\overline{OE}$ ↑ to Data Bus Float		100		100	ns	

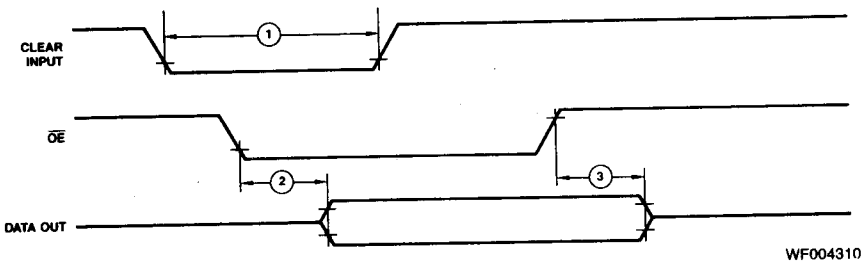

Figure 43. Port 2 Side Operation

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

FIO 2-WIRE HANDSHAKE TIMING

Number	Parameters	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TsDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ to Setup Time	50		50		ns
2	TdACKf(RFD)	$\overline{ACKIN}$ ↓ to RFD↓ Delay	0	500	0	500	ns
3	TdRFDr(ACK)	RFD ↑ to $\overline{ACKIN}$ ↓ Delay	0		0		ns
4	TsDO(DAV)	Data Out to $\overline{DAV}$ ↓ Setup Time	25		25		ns
5	TdDAVf(ACK)	$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ Delay	0		0		ns
6	ThDO(ACK)	Data Out to $\overline{ACKIN}$ Hold Time	50		50		ns
7	TdACK(DAV)	$\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ Delay	0	500	0	500	ns
8	ThDI(RFD)	Data Input to RFD ↓ Hold Time	0		0		ns
9	TdRFDf(ACK)	RFD ↓ to $\overline{ACKIN}$ ↑ Delay	0		0		ns
10	TdACKr(RFD)	$\overline{ACKIN}$ ↑ ($\overline{DAV}$ ↑) to RFD ↑ Delay – Interlocked and 3-Wire Handshake	0	400	0	400	ns
11	TdDAVr(ACK)	$\overline{DAV}$ ↑ to $\overline{ACKIN}$ ↑ (RFD ↑)	0		0		ns
12	TdACKr(DAV)	$\overline{ACKIN}$ ↑ to $\overline{DAV}$ ↓	0	800	0	800	ns
13	TdACK(Empty)	$\overline{ACKIN}$ to Empty		600		600	ns
14	TdACK (Full)	$\overline{ACKIN}$ to Full		600		600	ns
15	$\overline{ACKIN}$ Clock Rate		1.0				μs

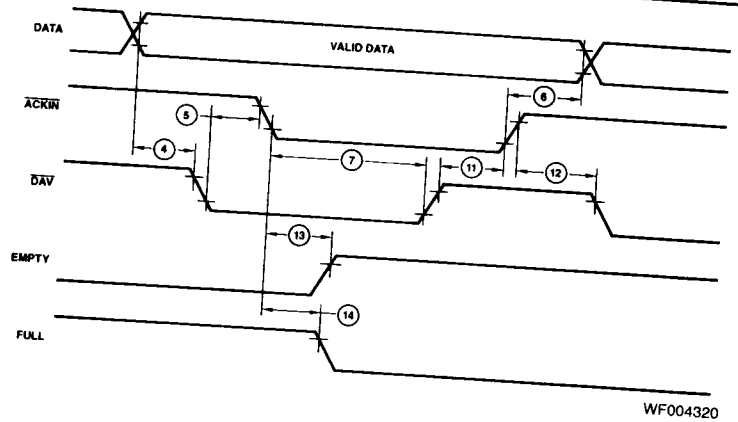

Figure 44a. 2-Wire Handshake (Port 2 Side Only) Output

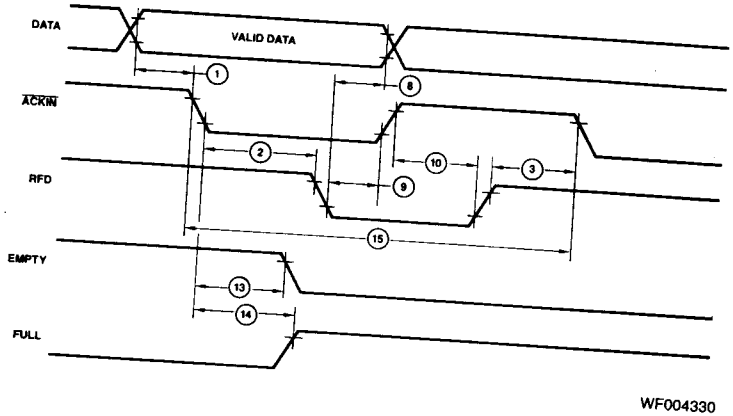

Figure 44b. 2-Wire Handshake (Port 2 Side Only) Input

Refer to page 7-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

3-WIRE HANDSHAKE

Number	Parameters	Description	4MHz		6MHz		Units
			Min	Max	Min	Max	
1	TsDI(DAV)	Data Input to $\overline{DAV}$ ↓ Setup Time	50		50		ns
2	TdDAVIf(RFD)	$\overline{DAV}$ ↓ to RFD ↓ Delay	0	500	0	500	ns
3	TdDAVf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay	0	500	0	500	ns
4	ThDI(DAC)	Data In to DAC ↑ Hold Time	0		0		ns
5	TdDAClr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ Delay	0		0		ns
6	TdDAVIr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay	0	500	0	500	ns
7	TdDAVIr(RFD)	$\overline{DAV}$ ↑ to RFD ↑ Delay	0	500	0	500	ns
8	TdRFDI(DAV)	RFD ↑ to $\overline{DAV}$ ↓ Delay	0		0		ns
9	TsDO(DAC)	Data Out to $\overline{DAV}$ ↓					ns
10	TdDAVOf(RFD)	$\overline{DAV}$ ↓ to RFD ↓ Delay	0		0		ns
11	TdDAVOf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay	0		0		ns
12	ThDO(DAC)	Data Out to DAC ↑ Hold Time					ns
13	TdDACOr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ Delay		400		400	ns
14	TdDAVOr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay	0		0		ns
15	TdDAVOR(RFD)	$\overline{DAV}$ ↑ to RFD ↑ Delay	0		0		ns
16	TdRFDO(DAV)	RFD ↑ to $\overline{DAV}$ ↓ Delay	0	800	0	800	ns

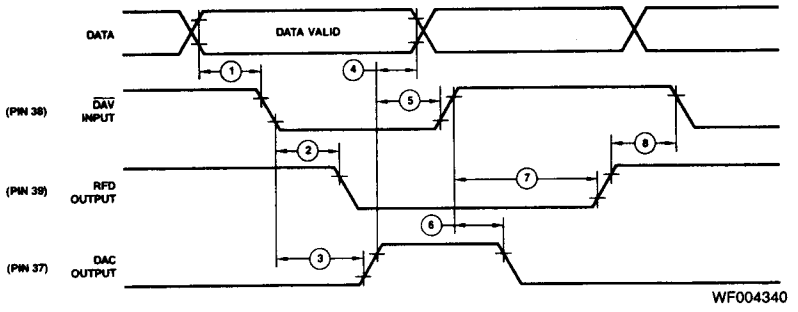

Figure 45a. 3-Wire Handshake Input

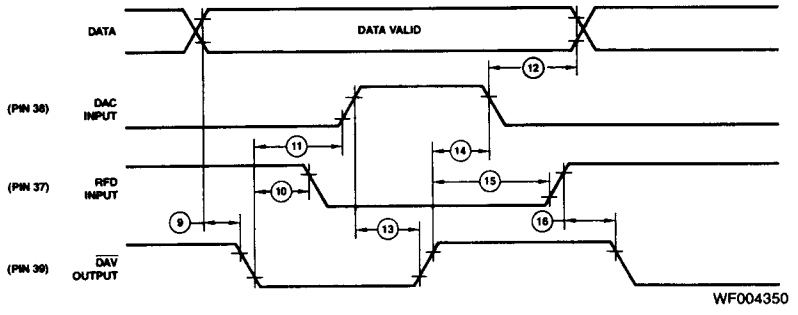

Figure 45b. 3-Wire Handshake Output