Low Skew, 1-to-5 Differential-to-LVDS, LVPECL Fanout Buffer

ICS854S015-01

PRELIMINARY DATA SHEET

General Description

The ICS854S015-01 is a low skew, high performance 1-to-5, 2.5V, 3.3V Differential-to-LVPECL/LVDS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS854S015-01 has two selectable differential clock inputs.

Guaranteed output and part-to-part skew characteristics make the ICS854S015-01 ideal for those applications demanding well defined performance and repeatability.

SEL_OUT Function Table

Input	Outputs
SEL_OUT	Q0:Q4/nQ0:nQ4
0	LVDS
1	LVPECL

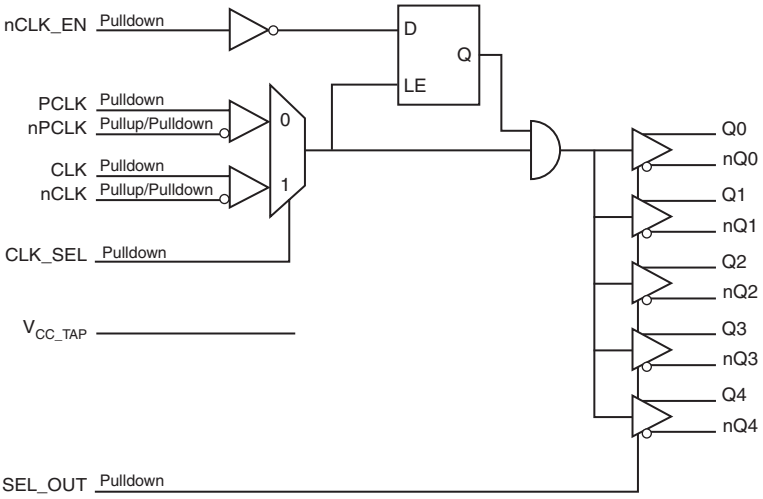
V_{CC_TAP} Function Table

Outputs		
Q0:Q4/nQ0:nQ4	Output Level Supply	V_{CC_TAP}
LVPECL	2.5V	2.5V
LVPECL	3.3V	3.3V
LVDS	2.5V	2.5V
LVDS	3.3V	Float

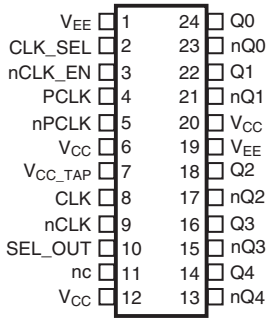
Features

- Five differential LVDS or LVPECL outputs
- Two differential clock input pairs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, CML, SSTL
- Either CLK or PCLK inputs can be configured to accept single-ended inputs
- Maximum output frequency: >2GHz
- Output skew: 25ps (typical)
- Propagation delay: 575ps (typical)
- Full 3.3V or 2.5V power supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS854S015-01
24-Lead, 173-MIL TSSOP
4.4mm x 7.8mm x 0.92mm body package
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 19	V_{EE}	Power		Negative supply pins.
2	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK, nCLK inputs. When LOW, selects PCLK, nPCLK inputs. LVTTL / LVCMOS interface levels.
3	nCLK_EN	Input	Pulldown	Synchronizing clock enable. When LOW, clock outputs follow clock input. When HIGH, Q outputs are forced low, nQ outputs are forced high. LVTTL / LVCMOS interface levels.
4	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
5	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
6, 12, 20	V_{CC}	Power		Positive supply pins.
7	V_{CC_TAP}	Power		Power supply pin. Tie to V_{CC} for 2.5V operation with LVDS outputs. Tie to V_{CC} for 2.5V or 3.3V operation with LVPECL outputs. Leave floating for 3.3V LVDS operation.
8	CLK	Input	Pulldown	Non-inverting differential clock input.
9	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input.
10	SEL_OUT	Input	Pulldown	Output select pin. When LOW, selects LVDS output levels. When HIGH, selects LVPECL output levels. See Table 3. LVCMOS/LVTTL interface levels.
11	nc	Unused		No connect.
13, 14	nQ4, Q4	Output		Differential output pair. LVPECL or LVDS interface levels.
15, 16	nQ3, Q3	Output		Differential output pair. LVPECL or LVDS interface levels.
17, 18	nQ2, Q2	Output		Differential output pair. LVPECL or LVDS interface levels.
21, 22	nQ1, Q1	Output		Differential output pair. LVPECL or LVDS interface levels.
23, 24	nQ0, Q0	Output		Differential output pair. LVPECL or LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ
$R_{VCC/2}$	Pullup/Pulldown Resistors			50		kΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs	
nCLK_EN	**CLK_SEL**	**Selected Source**	**Q0:Q4**	**nQ0:nQ4**
0	0	PCLK, nPCLK	Enabled	Enabled
0	1	CLK, nCLK	Enabled	Enabled
1	0	PCLK, nPCLK	Disabled; LOW	Disabled; HIGH
1	1	CLK, nCLK	Disabled; LOW	Disabled; HIGH

After nCLK_EN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1.*

In the active mode, the state of the outputs are a function of the PCLK, nPCLK and CLK, nCLK inputs as described in *Table 3B.*

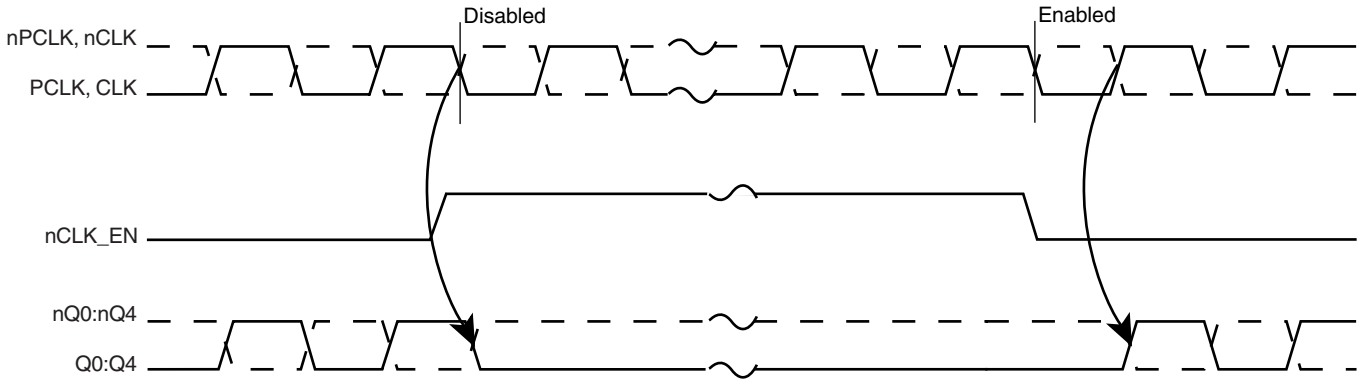


FIGURE 1. nCLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
PCLK or CLK	**nPCLK or nCLK**	**Q0:Q4**	**nQ0:nQ4**		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	82.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. LVDS Power Supply DC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				165	mA

Table 4B. LVDS Power Supply DC Characteristics, V_{CC} = V_{CC_TAP} = 2.5V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
V_{CC_TAP}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				155	mA
I_{TAP}	Power Supply Current				5	mA

Table 4C. LVPECL Power Supply DC Characteristics, V_{CC} = V_{CC_TAP} = 3.3V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
V_{CC_TAP}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				90	mA
I_{TAP}	Power Supply Current				5	mA

Table 4D. LVPECL Power Supply DC Characteristics, V_{CC} = V_{CC_TAP} = 2.5V±5%, V_{EE} = 0V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
V_{CC_TAP}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				85	mA
I_{TAP}	Power Supply Current				5	mA

TABLE 4E. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR $V_{CC} = V_{TAP}$ = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2.2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	SEL_OUT, CLK_SEL, nCLK_EN	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	SEL_OUT, CLK_SEL, nCLK_EN	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

TABLE 4F. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR $V_{CC} = V_{CC\_TAP}$ = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			150	µA
		nCLK	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V			10	µA
I_{IL}	Input Low Current	CLK	$V_{CC} = V_{IN}$ = 3.465V or 2.625V	-10			µA
		nCLK	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4G. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CC\_TAP}$ = 3.3V±5%, V_{EE} = 0V, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		nPCLK	$V_{CC} = V_{IN}$ = 3.465V			10	µA
I_{IL}	Input Low Current	PCLK	V_{CC} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLK	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.3		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 1.5		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 3		SEL_OUT = 1	V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 3		SEL_OUT = 1	V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		SEL_OUT = 1	0.6		1.0	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4H. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CC\_TAP} = 2.5V±5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	$V_{CC} = V_{IN} = 2.625V$			150	µA
		nPCLK	$V_{CC} = V_{IN} = 2.625V$			10	µA
I_{IL}	Input Low Current	PCLK	$V_{CC} = 2.625V$, $V_{IN} = 0V$	-10			µA
		nPCLK	$V_{CC} = 2.625V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.3		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 1.5		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 3		SEL_OUT = 1	V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 3		SEL_OUT = 1	V_{CC} - 2.0		V_{CC} - 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		SEL_OUT = 1	0.4		1.0	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4I. LVDS DC CHARACTERISTICS, $V_{CC} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	SEL_OUT = 0		400		mV
ΔV_{OD}	V_{OD} Magnitude Change	SEL_OUT = 0		40		mV
V_{OS}	Offset Voltage	SEL_OUT = 0		1.27		V
ΔV_{OS}	V_{OS} Magnitude Change	SEL_OUT = 0		50		mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 4J. LVDS DC CHARACTERISTICS, $V_{CC} = V_{CC\_TAP} = 2.5V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	SEL_OUT = 0		370		mV
ΔV_{OD}	V_{OD} Magnitude Change	SEL_OUT = 0		40		mV
V_{OS}	Offset Voltage	SEL_OUT = 0		1.23		V
ΔV_{OS}	V_{OS} Magnitude Change	SEL_OUT = 0		50		mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 5A. LVDS AC CHARACTERISTICS, V_{CC} = 3.3V ± 5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>2	GHz
t_{PD}	Propagation Delay; NOTE 1			570		ps
*t*sk(o)	Output Skew; NOTE 2, 3			25		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range: 12kHz - 20MHz		0.25		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		150		ps
odc	Output Duty Cycle			50		%
$MUX_{ISOLATION}$	MUX Isolation	@ 550MHz		55		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. LVDS AC CHARACTERISTICS, $V_{CC} = V_{CC\_TAP}$ = 2.5V ± 5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>2	GHz
t_{PD}	Propagation Delay; NOTE 1			575		ps
*t*sk(o)	Output Skew; NOTE 2, 3			25		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range: 12kHz - 20MHz		0.13		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		150		ps
odc	Output Duty Cycle			50		%
$MUX_{ISOLATION}$	MUX Isolation	@ 550MHz		55		dB

All parameters measured at 500MHz unless noted otherwise.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
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NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. LVPECL AC CHARACTERISTICS, $V_{CC} = V_{CC\_TAP} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>2	GHz
t_{PD}	Propagation Delay; NOTE 1			575		ps
*t*sk(o)	Output Skew; NOTE 2, 3			25		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range: 12kHz - 20MHz		0.12		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		150		ps
odc	Output Duty Cycle			50		%
$MUX_{ISOLATION}$	MUX Isolation	@ 550MHz		55		dB

All parameters measured at 500MHz unless noted otherwise.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

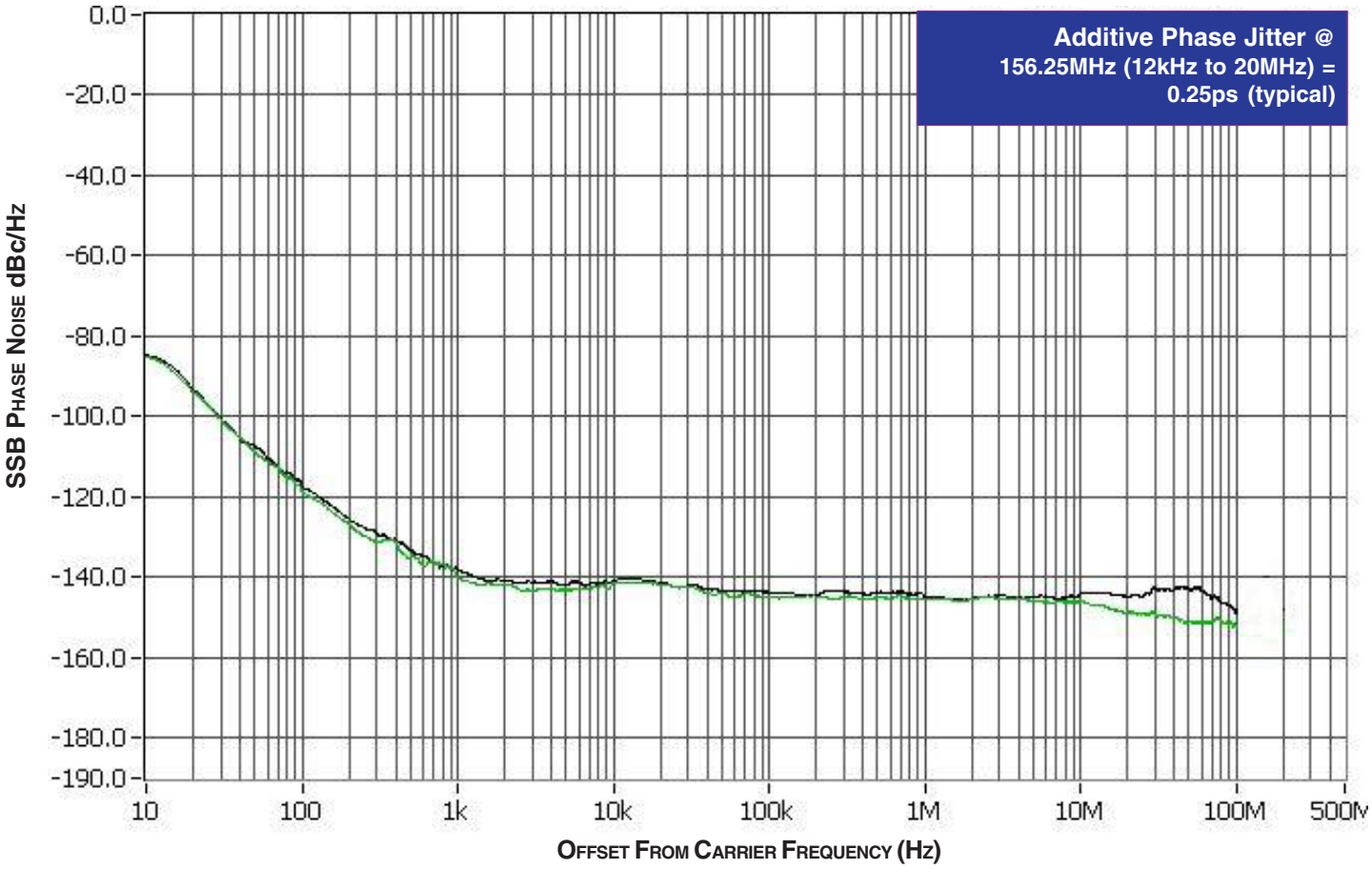
TABLE 5D. LVPECL AC CHARACTERISTICS, $V_{CC} = V_{CC\_TAP} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>2	GHz
t_{PD}	Propagation Delay; NOTE 1			580		ps
*t*sk(o)	Output Skew; NOTE 2, 3			25		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range: 12kHz - 20MHz		0.07		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		150		ps
odc	Output Duty Cycle			50		%
$MUX_{ISOLATION}$	MUX Isolation	@ 550MHz		55		dB

All parameters measured at 500MHz unless noted otherwise.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

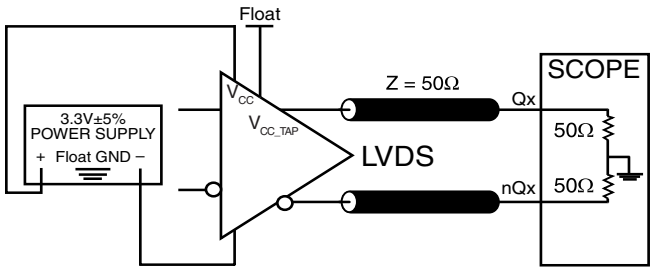
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

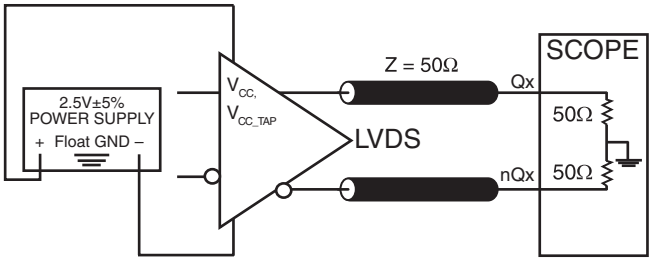


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

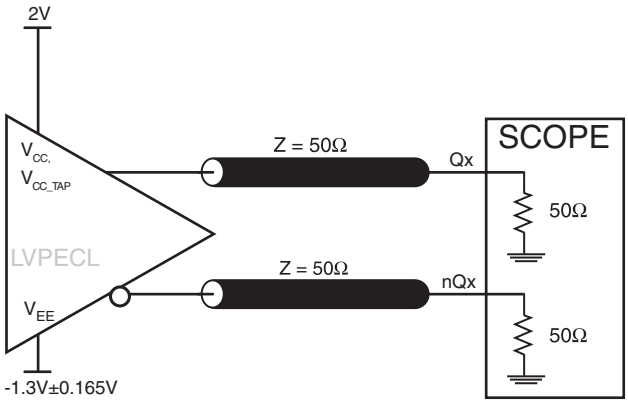
PARAMETER MEASUREMENT INFORMATION



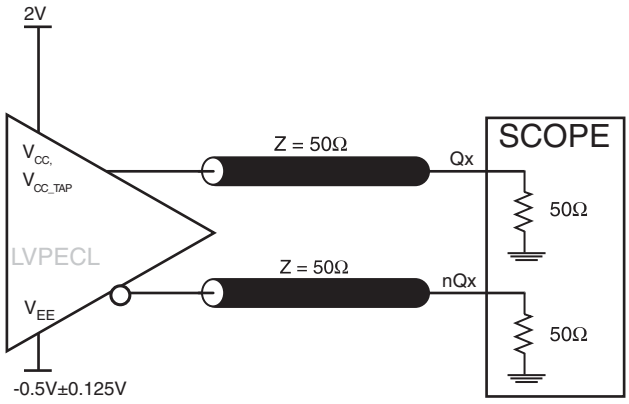
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



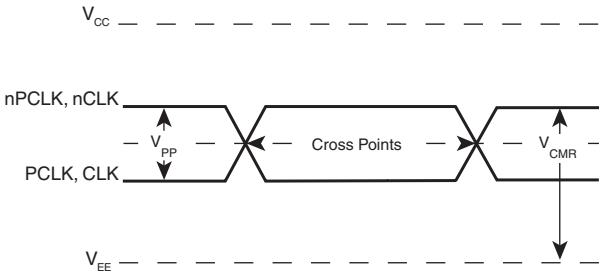
2.5V LVDS OUTPUT LOAD AC TEST CIRCUIT



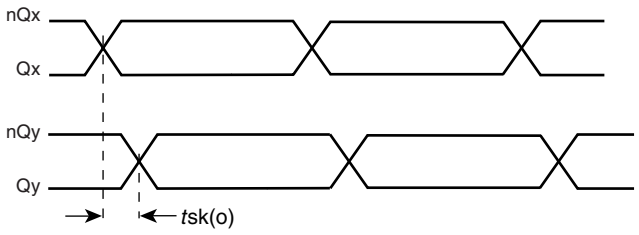
3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT



2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT

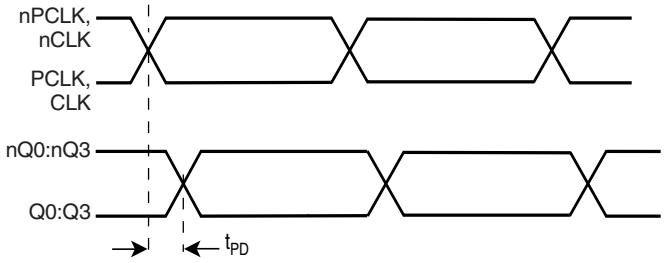


DIFFERENTIAL INPUT LEVEL

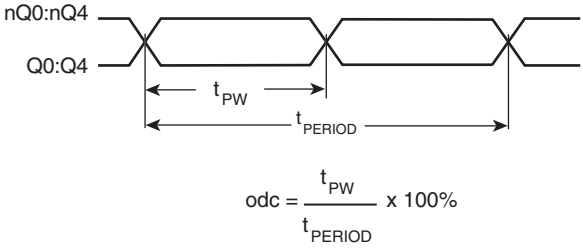


OUTPUT SKEW

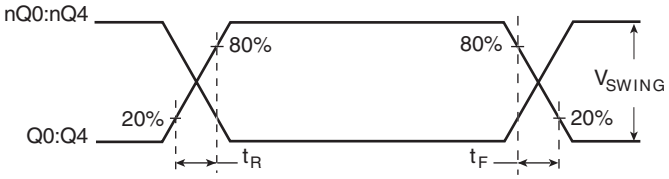
PARAMETER MEASUREMENT INFORMATION, CONTINUED



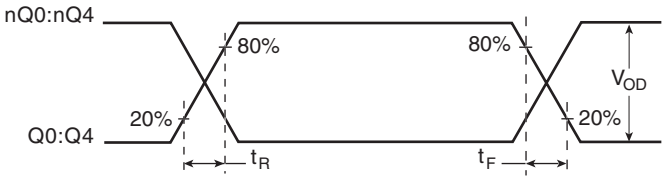
PROPAGATION DELAY



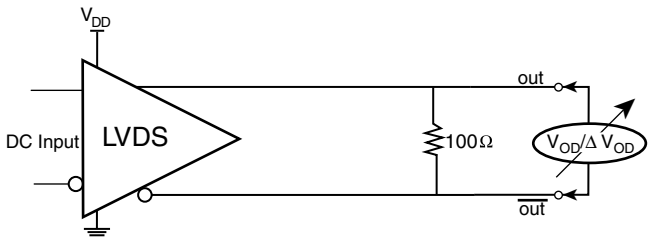
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



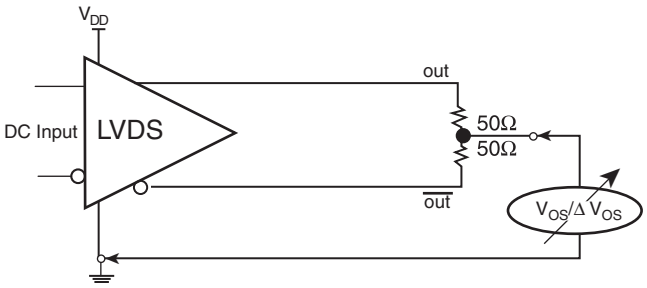
LVPECL OUTPUT RISE/FALL TIME



LVDS OUTPUT RISE/FALL TIME



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

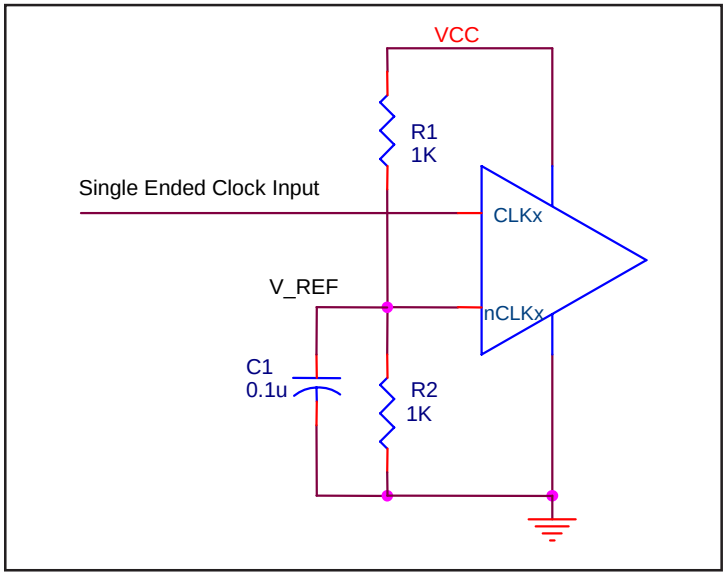


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUTS

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

PCLK/nPCLK INPUTS

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVCMOS CONTROL PINS

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVDS OUTPUTS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

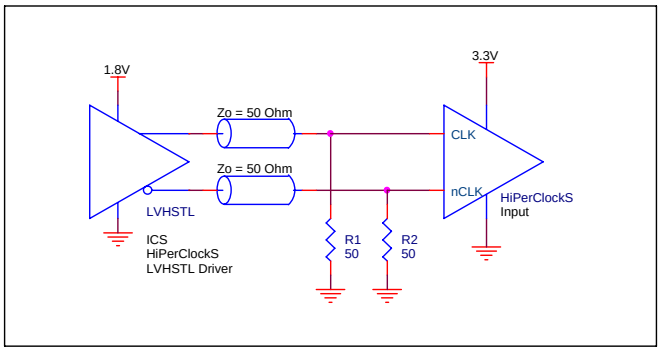


Figure 3A. HiPerClockS CLK/nCLK Input Driven by IDT HiPerClockS LVHSTL Driver

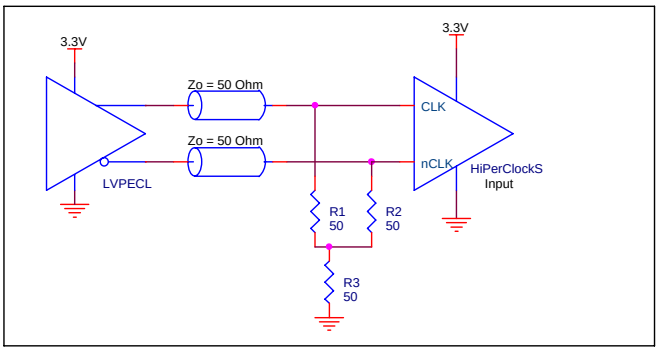


Figure 3B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

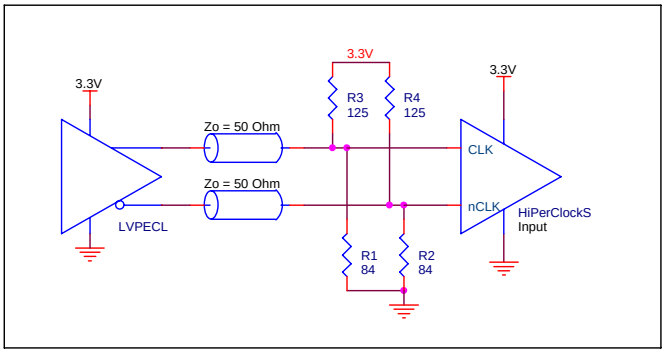


Figure3C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

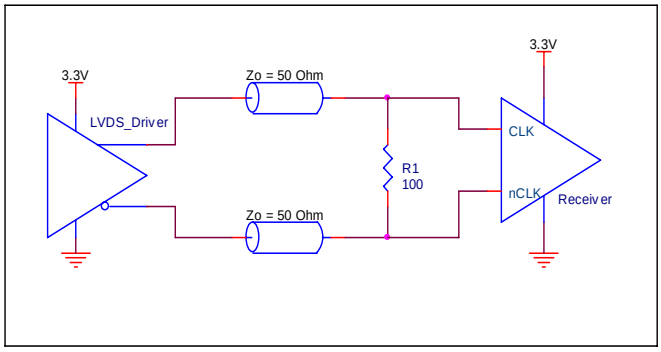


Figure 3D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

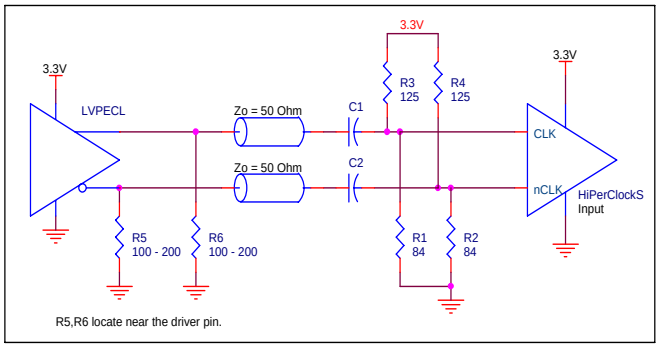


Figure 3E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

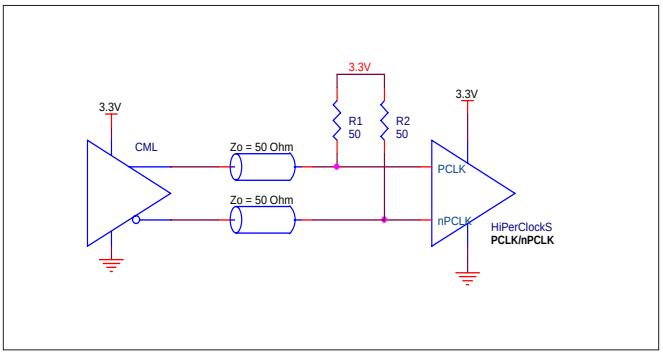


Figure 4A. HiPerClockS PCLK/nPCLK Input Driven by an Open Collector CML Driver

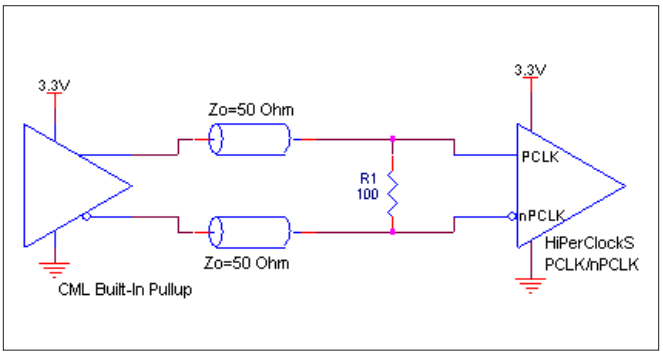


Figure 4B. HiPerClockS PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

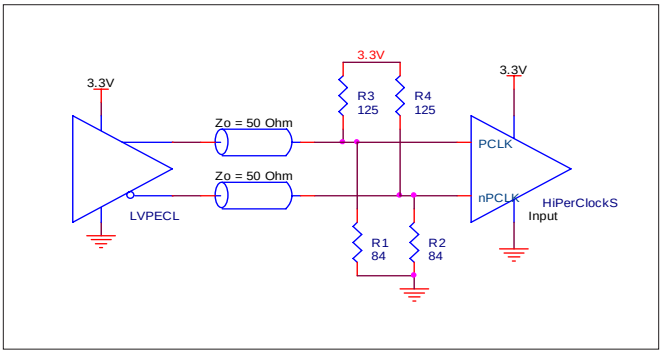


Figure 4C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

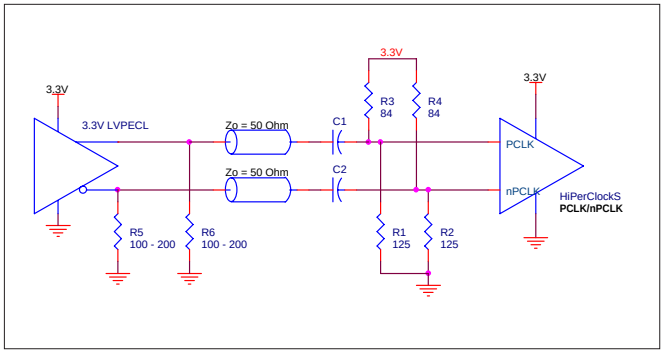


Figure 4D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

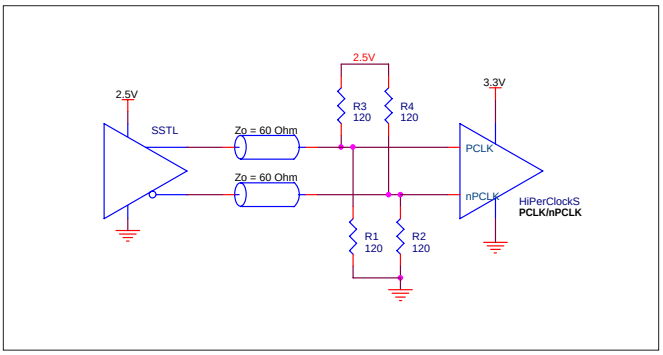


Figure 4E. HiPerClockS PCLK/nPCLK Input Driven by an SSTL Driver

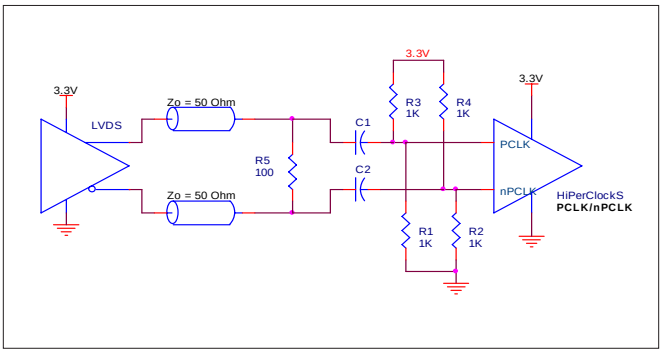


Figure 4F. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 5.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

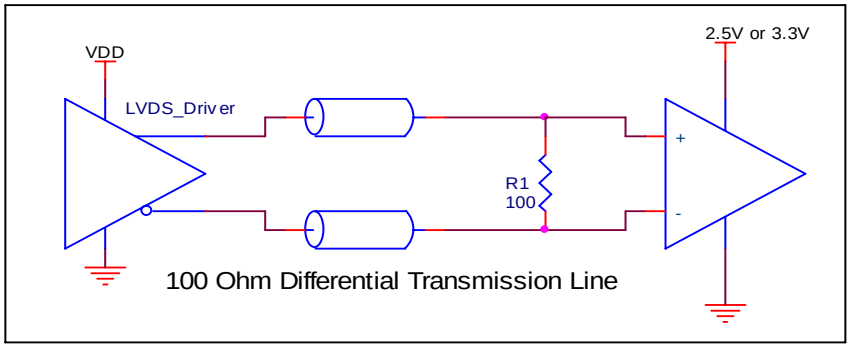


Figure 5. Typical LVDS Driver Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

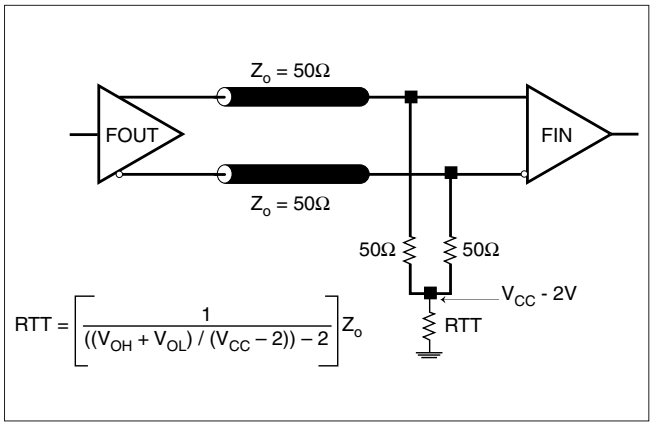


Figure 6A. LVPECL Output Termination

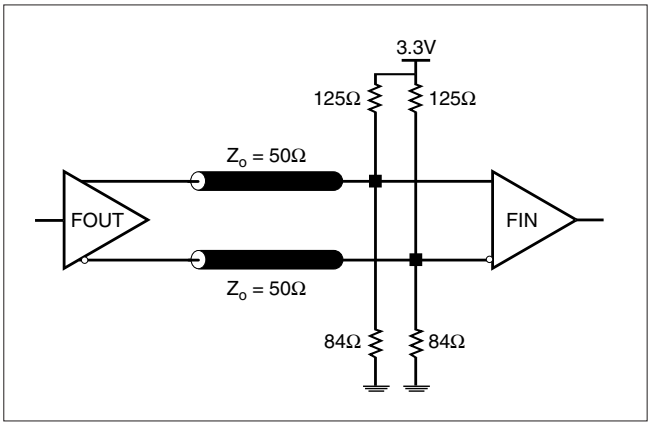


Figure 6B. LVPECL Output Termination

TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 7A and *Figure 7B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{cc} - 2V. For V_{cc} = 2.5V, the V_{cc} - 2V is very close to ground level. The R3 in Figure 7B can be eliminated and the termination is shown in *Figure 7C.*

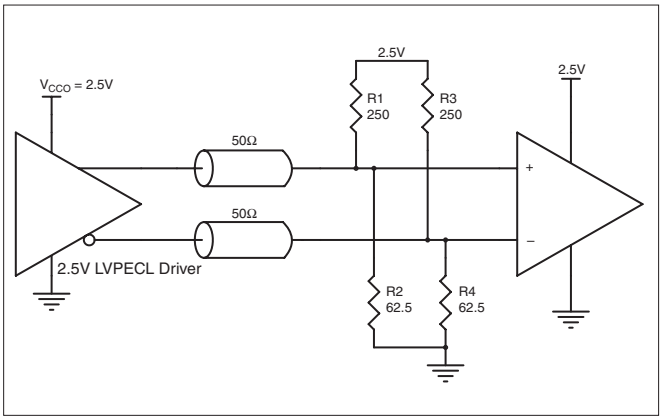


FIGURE 7A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

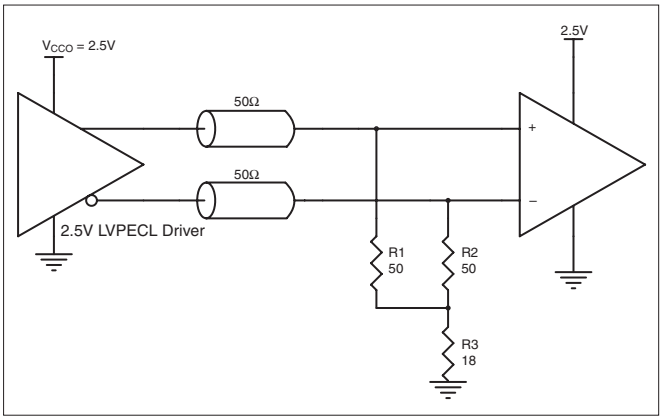


FIGURE 7B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

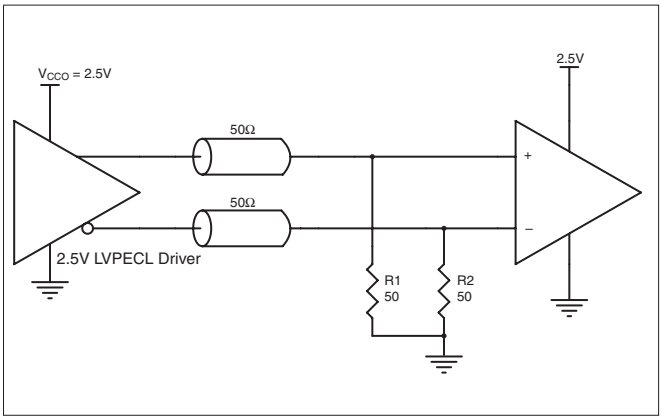


FIGURE 7C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS (LVDS)

This section provides information on power dissipation and junction temperature for the ICS854S015-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS854S015-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worse case results.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{CC_MAX} = 3.465V * 165mA = **571.725mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

q_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 82.8°C/W per Table 6A below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.572W * 82.8°C/W = 117.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 6A. THERMAL RESISTANCE θ_{JA} FOR 24-LEAD TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.8°C/W	78.5°C/W	76.3°C/W

POWER CONSIDERATIONS (LVPECL)

This section provides information on power dissipation and junction temperature for the ICS854S015-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS854S015-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worse case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- The maximum current at 85°C is as follows:
  I_{CC_MAX} = 85mA
- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 90mA = **311.85mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 5 * 30mW = **150mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 311.85mW + 150mW = **461.85mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 82.8°C/W per Table 6B below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.462W * 82.8°C/W = 108.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 6B. THERMAL RESISTANCE θ_{JA} FOR 24 LEAD TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.8°C/W	78.5°C/W	76.3°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 8.*

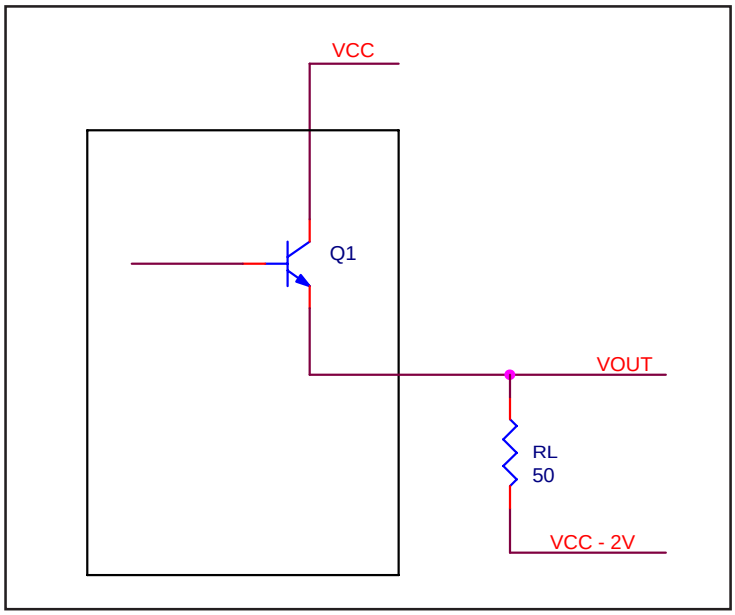


FIGURE 8. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} – 0.9V$

  $(V_{CC\_MAX} – V_{OH\_MAX}) =$ **0.9V**

- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} – 1.7V$

  $(V_{CCO\_MAX} – V_{OL\_MAX}) =$ **1.7V**

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$

$[(2V – 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$

$[(2V – 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 24 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.8°C/W	78.5°C/W	76.3°C/W

Transistor Count

The transistor count for ICS854S015-01 is: 521

Package Outline and Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

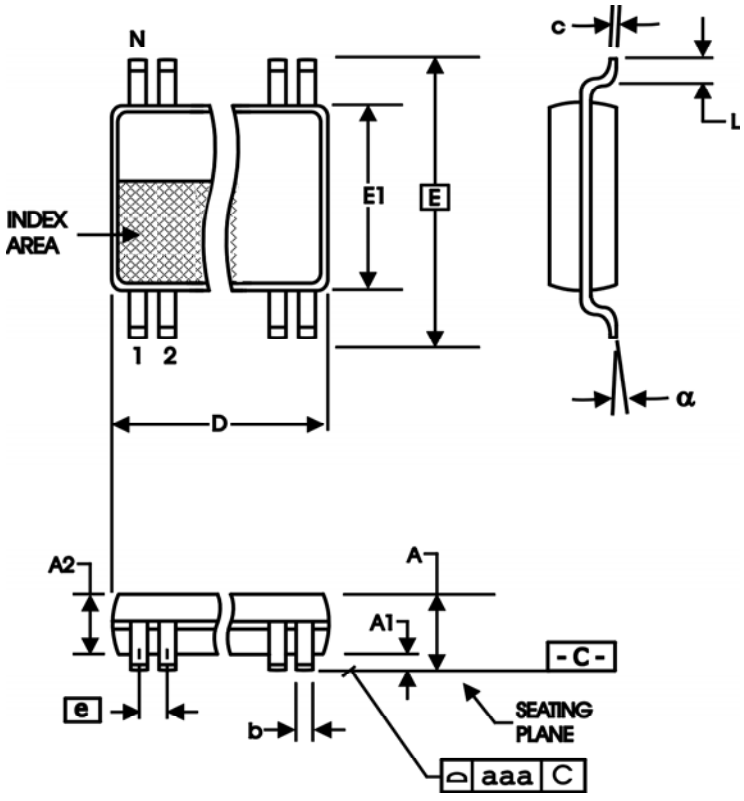


Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S015CG-01LF	ICS54S015C01L	24 lead "Lead-Free" TSSOP	tube	0°C to 70°C
854S015CG-01LFT	ICS54S015C01L	24 lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

www.IDT.com

6024 Silver Creek Valley Road
San Jose, CA 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Techical Support
netcom@idt.com
+480-763-2056