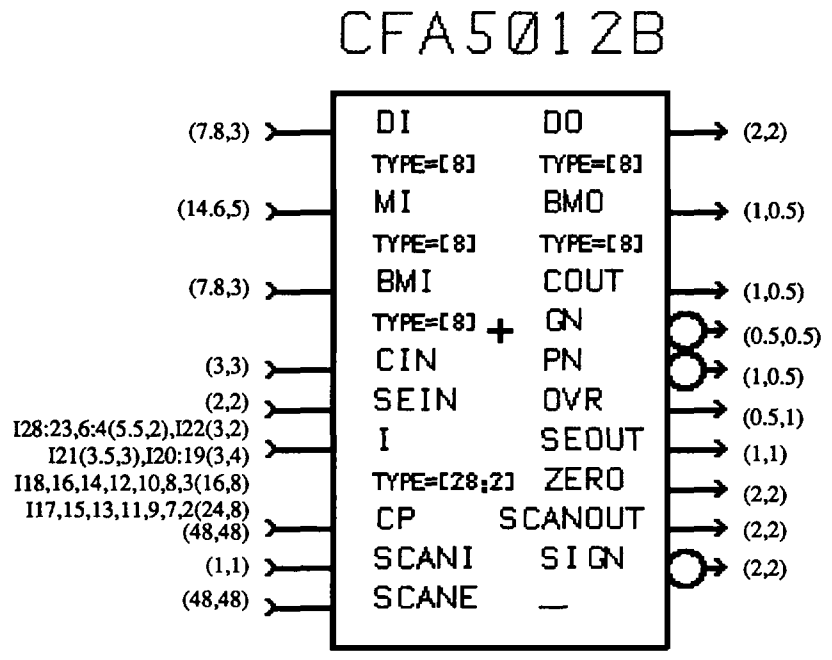
**GENERAL DESCRIPTION:** MULTIPORT, PIPELINED PROCESSOR, BYTE SLICE WITH SCAN PATH

CFA5012B is designed to be fully compatible with AM29501 byte-slice, multi-port, pipelined processor with the exception that all bidirectional pins are separated into input and output signals. To convert the CFA5012B to AM29501 I/O format, the user can easily tie DI7:0 and DO7:0, and BMI7:0 and BMO7:0 together and use I0 and I1 as the bidirect-select signals. CFA5012B is completely microprogrammable. No instruction decoding is required, and all operation combinations are available. Six 8-bit registers in the CFA5012B have multiple data input selections and are arranged in a pipelined fashion. The 8-bit ALU can operate four arithmetic operations with three carry modes and four logic operations. It can operate on all data from all the six registers and MI7:0, BMI7:0, and SEIN direct inputs.

**PIN CONNECTION DIAGRAM:**




**FEATURES:**

- Internal registers can be loaded in and read out through the SCAN circuit. SCANI is the SCAN input; SCANE is SCAN enable. When SCANE is HIGH, it enables data to flow from SCANI to A1, A2, A3, B1, B2, B3, and SCANOUT. Inside the registers, signals are from LSB to MSB
- Sign is the MSB of ALU

**EQUIVALENT USED GATES:** 1530 GATES
(for rough area estimates)

**THIS MEGAFUNCTION CONSISTS OF :**
1530 soft-coded gates.

**POWER:** NOT AVAILABLE.

**FAULT COVERAGE(%):** 99.5%

This megafunction was designed to be 100% functionally compatible as specified in the vendor's data book. However, LSI LOGIC makes no warranty that this megafunction behaves identically to the standard part. It is the user's responsibility to assure that the megafunction operates correctly in his/her ASIC design and meets desired system requirements.

INPUTS

| Name | Description |
|---|---|
| DI7:0 | General purpose data inputs |
| MI7:0 | General purpose data inputs |
| BMI7:0 | General purpose data inputs |
| CIN | ALU carry input |
| SEIN | Sign extension bit for two's complement operations |
| I28:23 | Instruction inputs to select ALU inputs |
| I22 | Instruction input to select ALU operations |
| I21 | Instruction input to select ALU operations |
| I20:19 | Instruction inputs to select ALU operations |
| I18 | Instruction input to select B3 register inputs |
| I17 | Instruction input to select B3 register inputs |
| I16 | Instruction input to select B2 register inputs |
| I15 | Instruction input to select B2 register inputs |
| I14 | Instruction input to select B1 register inputs |
| I13 | Instruction input to select B1 register inputs |
| I12 | Instruction input to select A3 register inputs |
| I11 | Instruction input to select A3 register inputs |
| I10 | Instruction input to select A2 register inputs |
| I9 | Instruction input to select A2 register inputs |
| I8 | Instruction input to select A1 register inputs |
| I7 | Instruction input to select A1 register inputs |
| I6:4 | Instruction inputs to select BMO7:0 outputs |
| I3 | Instruction input to select DO7:0 outputs |
| I2 | Instruction input to select DO7:0 outputs |
| CP | Clock input |
| SCANI | SCAN input |
| SCANE | SCAN enable |

OUTPUTS

| Name | Description |
|---|---|
| DO7:0 | Data outputs |
| BMO7:0 | Data outputs |
| COUT | ALU carry output |
| GN | ALU GN output for carry look ahead |
| PN | ALU PN output for carry look ahead |
| OVR | ALU overflow output |
| SEOUT | The most significant bit of S-operand |
| ZERO | HIGH when ALU outputs are zeroes |
| SCANOUT | SCAN output |
| SIGN | AUL MSB output |

SWITCHING CHARACTERISTICS

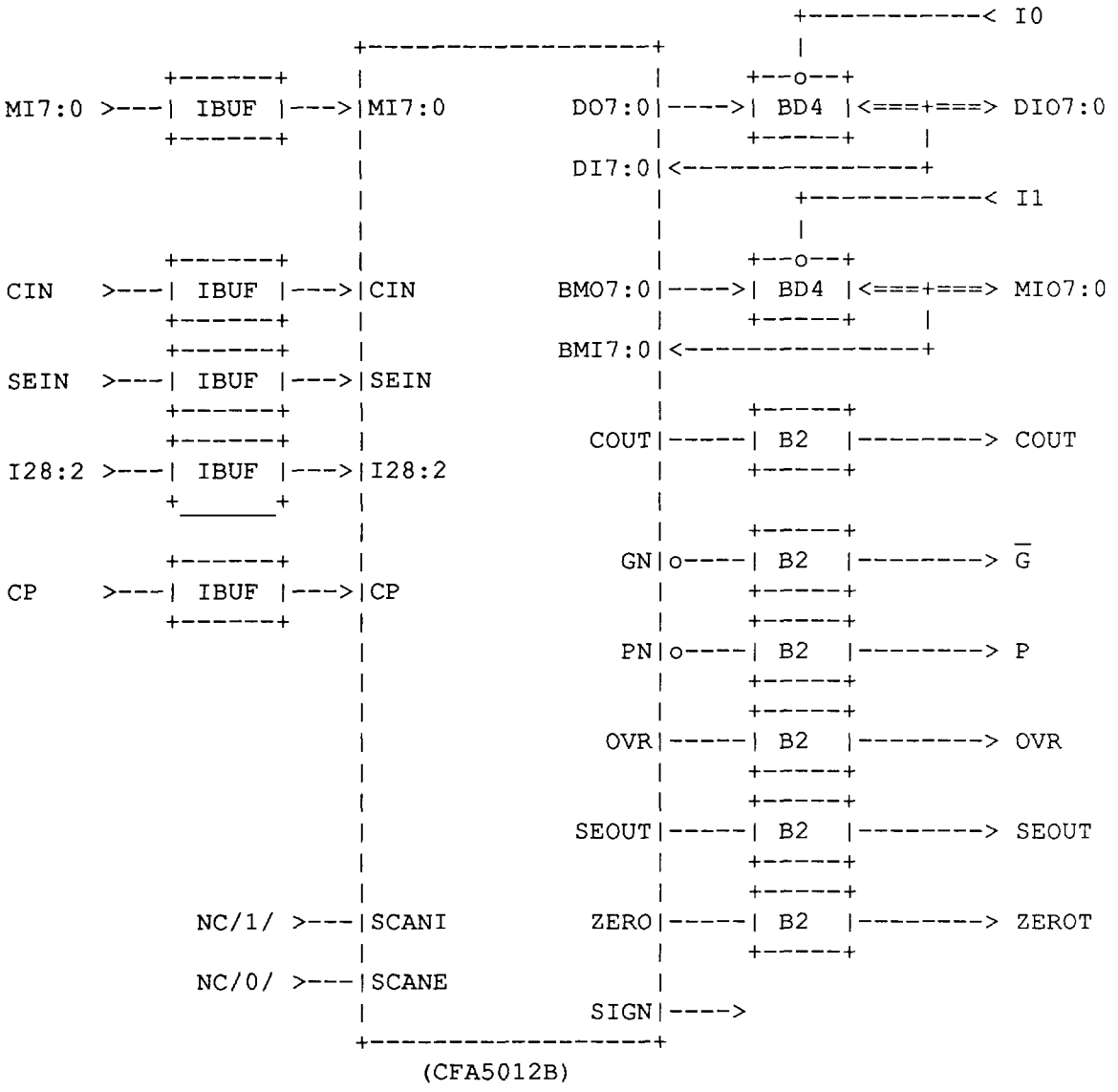
| From input | To output, propagation delays in ns | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | BMO | BMO via ALU | DO | COUT | GN | PN | Z | OVR | SEOUT |
| CP | 7.3 | 19 | 5.1 | 16.5 | 14.8 | 11.4 | 18.4 | 18.1 | 6.7 |
| DI | 3.6 | - | - | - | - | - | - | - | - |
| BMI | - | 17 | - | 14.1 | 12.4 | 9 | 17.5 | 15.7 | 4.6 |
| MI | - | 18 | - | 15.5 | 13.8 | 10.4 | 18.9 | 16.8 | 5.7 |
| CIN | - | 12.1 | - | 4 | - | - | 13 | 7.8 | - |
| SEIN | - | 16.3 | - | 13.8 | 12.1 | 8.7 | 17.2 | 15.4 | - |
| I3:2,DO | - | - | 2.0 | - | - | - | - | - | - |
| I6:4,BMO | 6.8 | - | - | - | - | - | - | - | - |
| I22:19,ALU OP | - | 18.9 | - | 16.4 | 14.7 | 11.3 | 19.8 | 18 | - |
| I28:23,ALU SEL | - | 19.3 | - | 17.5 | 15.8 | 12.4 | 20.9 | 19.1 | 7.7 |

| From input | Set-up,tS/Hold,tH in ns | |
|---|---|---|
| | Register Input | Register via ALU |
| DI | 2.6/0 | - |
| BMI | 2.7/0 | 17.7/0 |
| MI | 2.8/0 | 18.7/0 |
| CIN | - | 12.8/0 |
| SEIN | - | 17.0/0 |
| I18:7,REG | 3.2/0 | - |
| I22:19,ALU OP | - | 19.6/0 |
| I28:23,ALU SEL | - | 20.7/0 |

*Minimun CLOCK cycle time: 42ns

*All timings are based on 10K, nominal conditions with 2 output loadings.

MACRO TO STANDARD PART I/O CONVERSION




(CFA5012B)