



NMC6552 1024-Bit (256 × 4) Static RAM

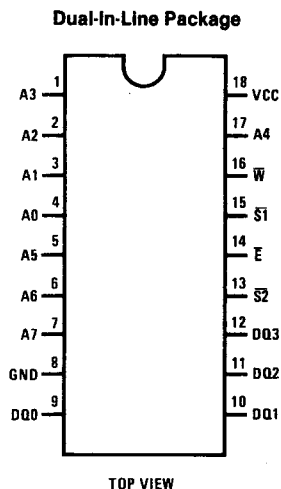
General Description

The NMC6552 is a static CMOS random access read/write memory organized as 256 words of 4 bits each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible with the TTL environment. Synchronous operation is provided by the on-chip address input and data output registers. The ENABLE input serves as the device strobe controlling the latching functions. The data I/O terminals, when not output data enabled, represent a high impedance for easy memory expansion.

Features

- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- Common I/O — high density packaging
- Output data latches
- Select latch for microprocessor interface

Connection Diagram



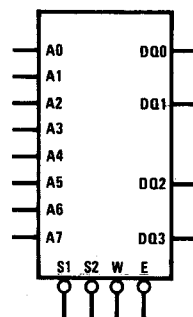
Order Number NMC6552J-2, NMC6552J-9
or NMC6552J-5
See NS Package J18A

Order Number NMC6552N-5
See NS Package N18A

Pin Names

A0-A7	Address Inputs
$\bar{E}$	Chip Enable
$\bar{W}$	Write Enable
DQ0-DQ3	Data In/Out
$\bar{S}1, \bar{S}2$	Chip Selects

Logic Symbol



Functional Description

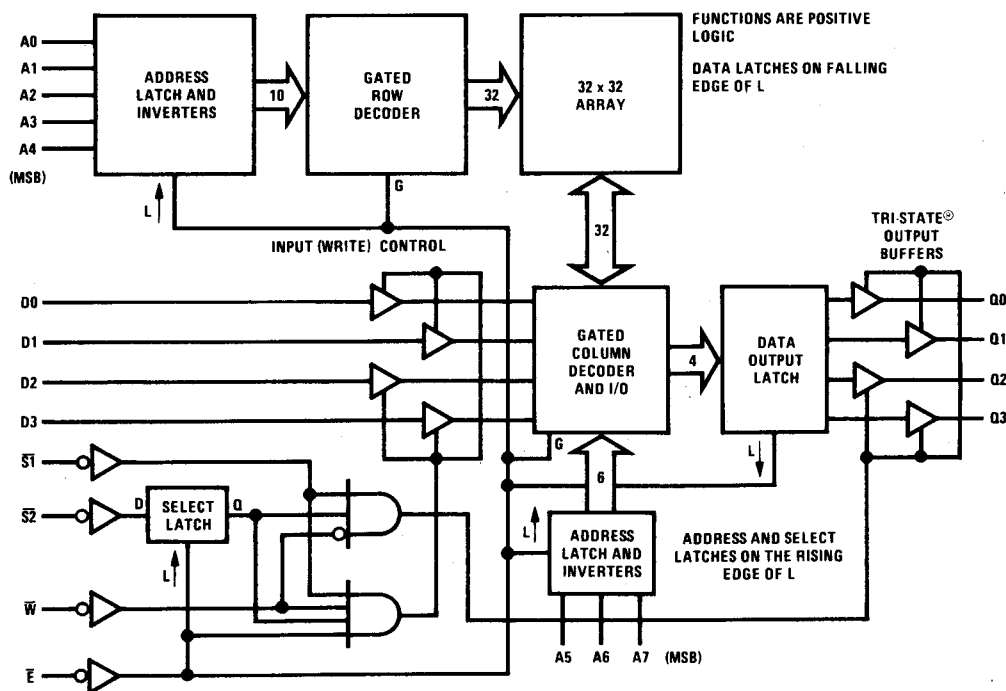
An NMC6552 memory cycle is initiated by the falling edge of the ENABLE ($\bar{E}$) input, which latches the ADDRESS and SELECT 2 ($\bar{S}_2$) information into the on-chip registers. The output data latches are transparent when the ENABLE input is LOW, allowing the state of the memory to be presented to the output buffers. The output buffers are enabled when the WRITE ($\bar{W}$) input is HIGH, and the SELECT 1 ($\bar{S}_1$) input is LOW.

When performing a read cycle, a minimum ENABLE LOW time is required to assure valid data at the device outputs. This minimum LOW time is defined as the enable access time. A minimum ENABLE HIGH time is required

to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next cycle. The data is latched with the rising edge of the ENABLE input, allowing maintenance of output data until the SELECT 1 input goes HIGH.

When performing a write cycle, a minimum ENABLE LOW time is required for new data entry. The write pulse timing is defined by the coincident LOW of the WRITE, ENABLE and SELECT 1 inputs. The input data set-up and hold times are referenced to the rising edge of the WRITE, ENABLE, or SELECT 1 inputs, whichever occurs first.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	-0.3V to VCC + 0.3V
Storage Temperature Range	-65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6552B-9	4.5V	5.5V
NMC6552B-2	4.5V	5.5V
NMC6552-9	4.5V	5.5V
NMC6552-2	4.5V	5.5V
NMC6552-5	4.75V	5.25V
Temperature		
NMC6552B-9	-40°C	85°C
NMC6552B-2	-55°C	125°C
NMC6552-9	-40°C	85°C
NMC6552-2	-55°C	125°C
NMC6552-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

Symbol	Parameter	Conditions	NMC6552B-9, NMC6552B-2 NMC6552-9, NMC6552-2		NMC6552-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			10 1(+25°C)		100	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		4		4	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		10		100	μA
II	Input Leakage Current	VI = VCC, GND	-1.0	+1.0	-1.0	+1.0	μA
VIL	Input Low Voltage		-0.3	0.8	-0.3	0.8	V
VIH	Input High Voltage		VCC - 2.0	VCC + 0.3	VCC - 2	VCC + 0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	-1.0	+1.0	-1.0	+1.0	μA
VOL	Output Low Voltage	IOL = 3.2 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = -0.4 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		6		6	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

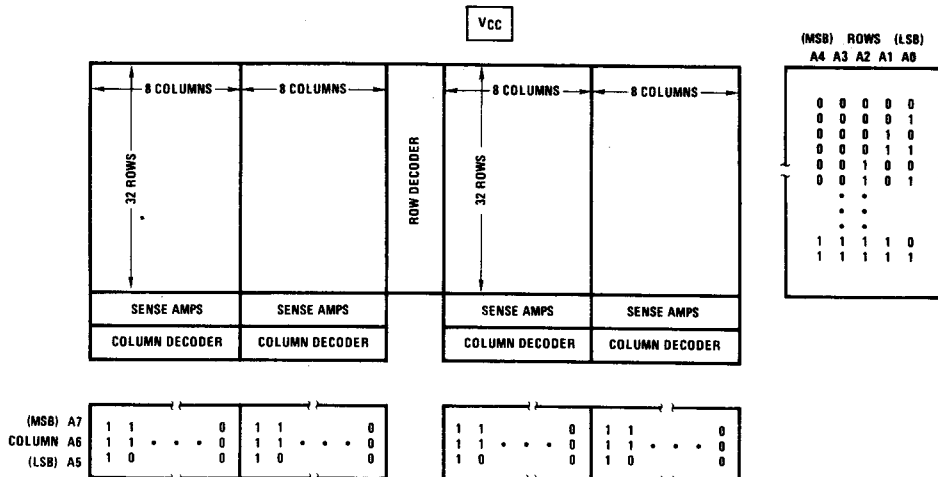
AC Test Conditions

Input Rise and Fall Times: ≤ 20 ns

All Timing Reference Levels: 1/2 VCC

Output Load: 1 TTL Load, 50 pF

NMC6552 Bit Map and Address Decoding

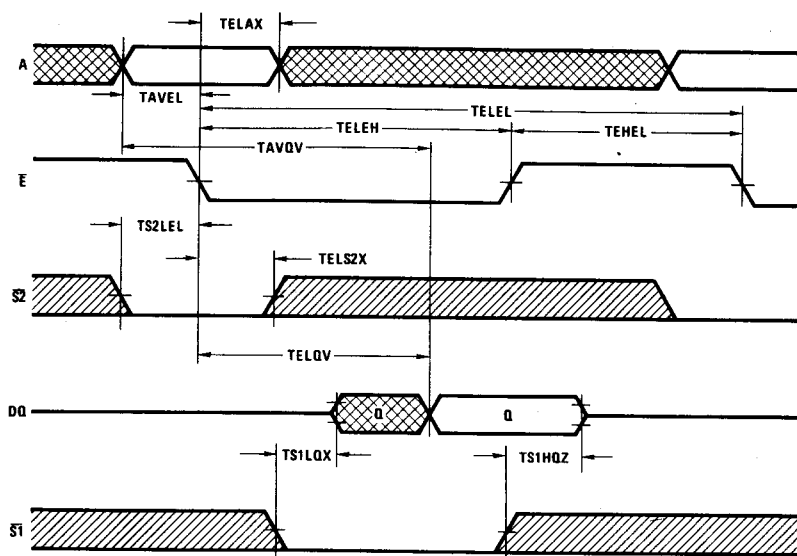


Read Cycle AC Electrical Characteristics over the operating range

NMC6552

Symbol	Parameter	NMC6552B-9 NMC6552B-2		NMC6552-9 NMC6552-2		NMC6552-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		220		300		350	ns
TAVQV	Address Access Time		220		300		360	ns
TELEH	Enable ($\bar{E}$) Minimum Low Time	220		300		350		ns
TELS2X	Chip Select 2 Hold Time	40		50		70		ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	100		100		150		ns
TELEL	Read or Write Cycle Time	320		400		500		ns
TS1LQX	Chip Select 1 Output Enable Time		130		150		180	ns
TS1HQZ	Chip Select 1 Output Disable Time		130		150		180	ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns

Read Cycle Waveforms

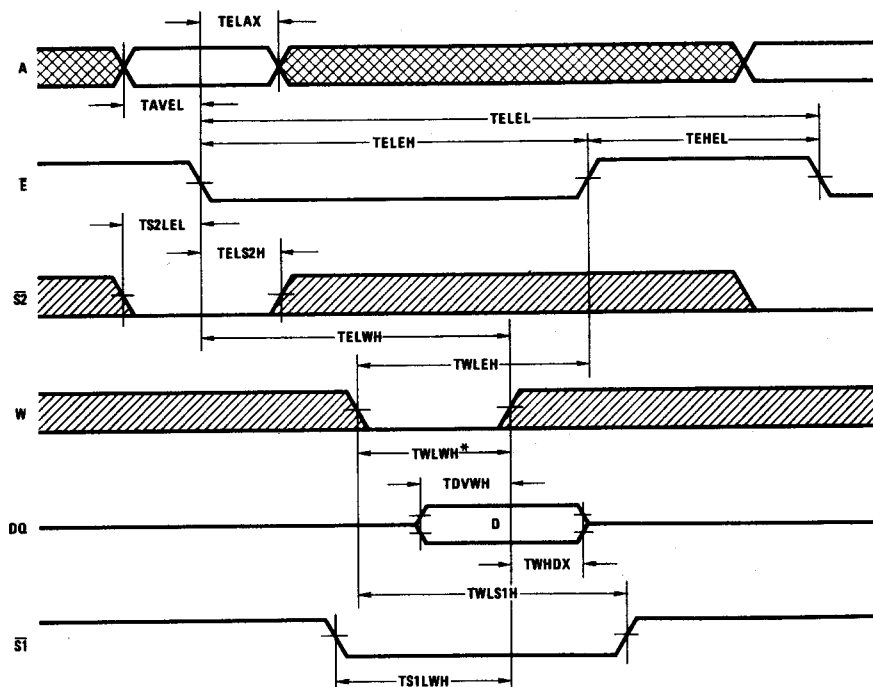


4

Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6552B-9 NMC6552B-2		NMC6552-9 NMC6552-2		NMC6552-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns
TWHDX	Data Hold Time	0		0		0		ns
TELEH	Enable ($\bar{E}$) Minimum Low Time	220		300		350		ns
TWLWH	Write Pulse Width ($\bar{W}$ Low)	120		180		210		ns
TELEL	Read or Write Cycle Time	320		400		500		ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	100		100		150		ns
TDVWH	Data Set-up Time	100		150		170		ns
TELWH	Write Pulse Width ($\bar{E}$ and $\bar{W}$ Low)	120		180		210		ns
TWLEH	Write Pulse Width ($\bar{W}$ and $\bar{E}$ Low)	120		180		210		ns
TELS2H	Chip Select 2 Hold Time	40		50		70		ns
TWLS1H	Chip Select 1 Write Pulse Set-up Time	120		180		210		ns
TS1LWL	Chip Select 1 Write Pulse Hold Time	120		180		210		ns

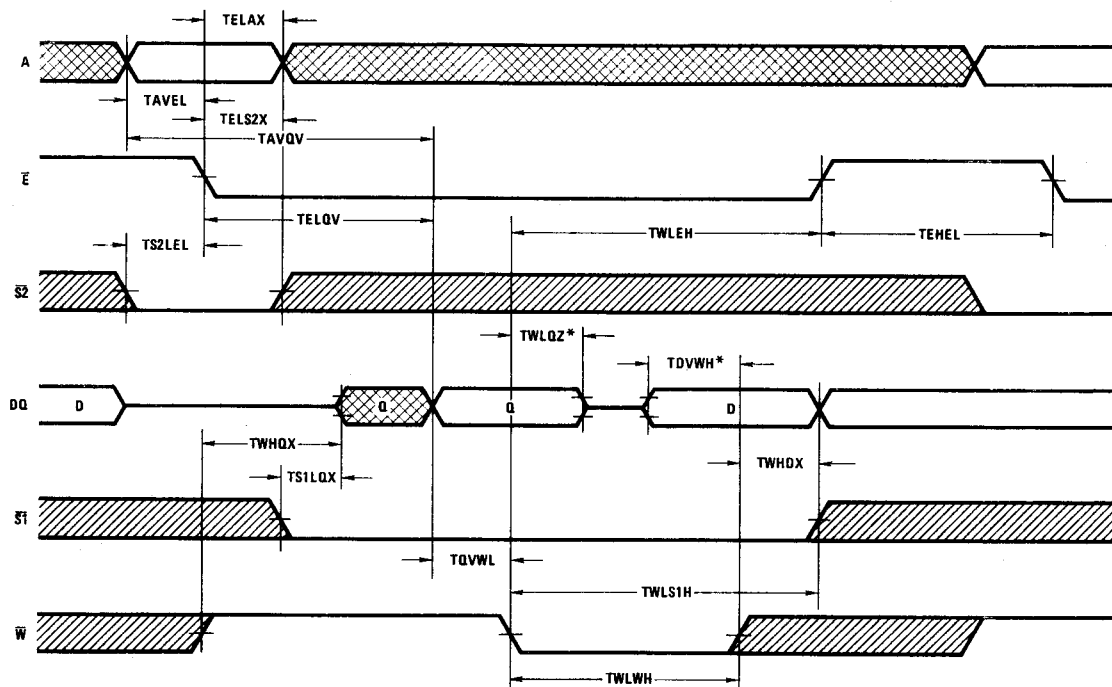
Write Cycle Waveforms



* TWLWH, the write pulse, is the coincidence low of $\bar{E}$, $\bar{W}$, and $\bar{S}_1$ inputs

Read-Modify-Write Cycle Waveforms

Symbol	Parameter	NMC6552B-9 NMC6552B-2		NMC6552-9 NMC6552-2		NMC6552-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		220		300		350	ns
TAVQV	Address Access Time		220		300		360	ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns
TWHDX	Data Hold Time	0		0		0		ns
TELS2X	Chip Select 2 Hold Time	40		50		70		ns
TWLS1H	Chip Select 1 Write Pulse Set-up Time	120		180		210		ns
TS1LQX	Chip Select 1 Output Enable Time		130		150		180	ns
TDVWH	Data Set-up Time	100		150		170		ns
TWLEH	Write Pulse Width ($\overline{W}$ and $\overline{E}$ Low)	120		180		210		ns
TQVWL	Data Valid to Write Time	0		0		0		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	120		180		210		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TQVWL	Data Valid to Write Time	0		0		0		ns
TWHQX	Output Enable from Write ($\overline{W}$)		130		150		180	ns
TWLQZ	Output Disable from Write ($\overline{W}$)		130		150		180	ns



* Avoid bus contention