M5M482257J,TP,RT-7,-8,-10

HYPER PAGE MODE 2097152-BIT DUAL-PORT DYNAMIC RAM

DESCRIPTION

M5M482257J, TP, RT is a high speed 2097152-bit Dual-Port Dynamic Memory equipped with a 256K × 8 Dynamic RAM Port and a 512 × 8 Serial Read Port.

High performance CMOS process using 4-layer polysilicon and silicide technology provide both high circuit density and low power dissipation.

The Serial Read Ports are connected to an internal 4096 bit Data Register through a 512 × 8 Serial Output control circuit and can be serially read out with a clock rate of up to 33MHz.

All Serial Reads are done relative to the RAM array, thus data transfer from the RAM array to the Data Register is referred to as a Read Transfer Cycle.

FEATURES

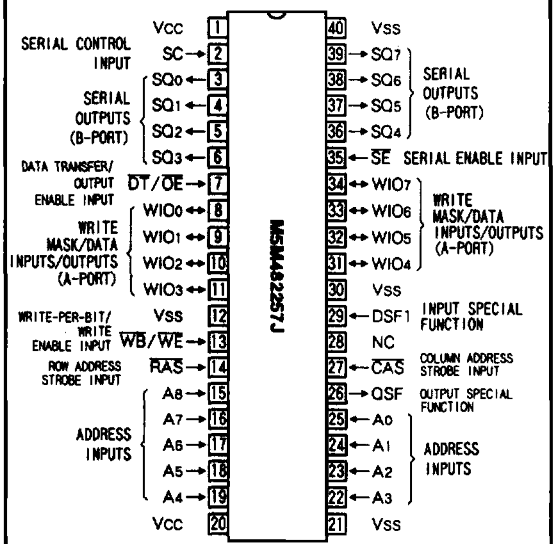
Type name	$\overline{RAS}$ Access Time (ns)	Random Read/Write cycle time (ns)	Serial Read cycle time (ns)	Random Read/Write Vcc supply current (mA)	Serial Read Vcc supply current (mA)
M5M482257 J,TP,RT-7	70	130	25	90	55
M5M482257 J,TP,RT-8	80	150	30	80	55
M5M482257 J,TP,RT-10	100	180	30	70	55

- Dual-Port Architecture
  RAM Port : 256K word × 8-bit
  SAM Port : 512 word × 8-bit
- One-way Data Transfer function from the RAM Array to the Data Register
- Fully Asynchronous Dual-Port Accessability.(Split SAM)
- Addressable Start Pointer of Serial Read (Point Control Function)
- Programmable stop of the Data Register.(Stop Register)
- Write Per Bit Function
- Real Time Data Transfer from the RAM Array to the Data Register
- Hyper Page Mode
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden Refresh
- 512 cycle/8ms Refresh
- Flash write, Block write operation
- Write Mask Select (New Mask/Old Mask)

APPLICATION

Display equipment for personal computer/work station, Frame memory for digital TV/VCR, Video printer

PIN CONFIGURATION (TOP VIEW)

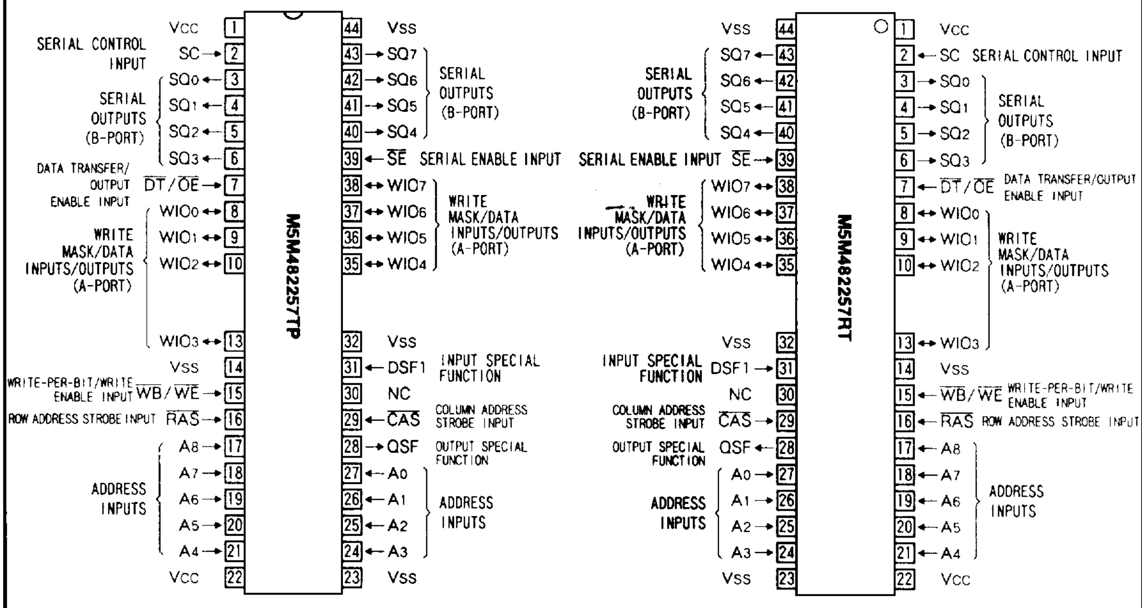


Outline 40P0K(400mil 40pin SOJ)

NC : NO CONNECTION

MITSUBISHI ELECTRIC

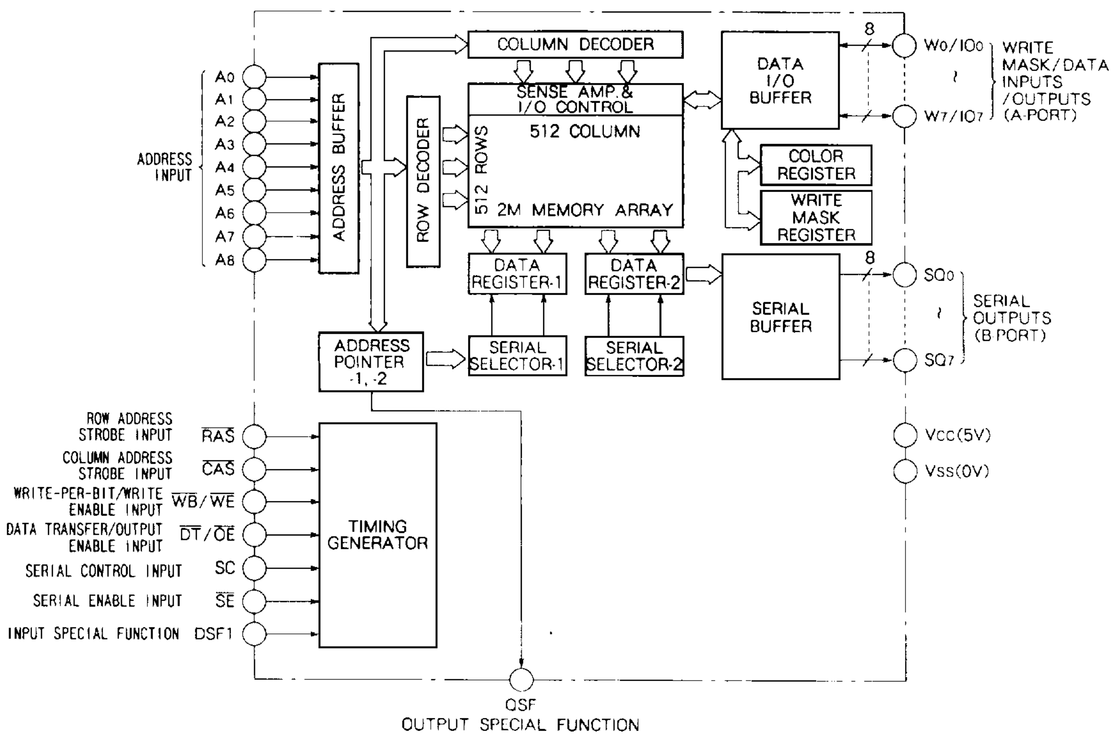
PIN CONFIGURATION (TOP VIEW)



Outline 44P3W-L (400mil 44(40)pin TSOP II) Outline 44P3W-M (400mil 44(40)pin TSOP II)

NC : NO CONNECTION

BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
$\overline{RAS}$	ROW ADDRESS STROBE INPUT	It is used a clock which latches the row address (A_0~A_8) to select the word line. It also latches the mask data for Write-per-bit and Flash write functions when the $\overline{WB}$ level is low. $\overline{CAS}$ before $\overline{RAS}$ refresh mode is activated when preceeded by $\overline{CAS}$ falling edge.
$\overline{CAS}$	COLUMN ADDRESS STROBE INPUT	It is used as a clock which latches the column address (A_9~A_{17}) and initiates the reading or writing of the selected words. In the data transfer cycle, this latches the SAM Top address point.(TAP)
A_0~A_8	ADDRESS INPUT	The M5M482257 utilizes an address multiplex method for selecting one word among the 256K-word memory cells. 9 row address and 9 column address are latched by $\overline{RAS}$ and $\overline{CAS}$ falling edge. In the data transfer cycle this column address input is also combined with the serial access start address.(TAP)
$\overline{WB}/\overline{WE}$	WRITE-PER-BIT/WRITE ENABLE INPUT	When the $\overline{WB}/\overline{WE}$ level is low at $\overline{RAS}$ falling edge, Write-per-bit (RAM write with Mask) or Flash write or load stop cycle is selected. When it is high, normal read/write or Read transfer or Load color register cycle is selected. This clock also controls early/delayed write mode at the $\overline{CAS}$ falling edge.
$\overline{DT}/\overline{OE}$	DATA TRANSFER/OUTPUT ENABLE INPUT	During RAM read cycle, It enables the data output (RAM port). Also when the $\overline{DT}/\overline{OE}$ level is low at the $\overline{RAS}$ falling edge, the data transfer cycle is selected and when it is high, RAM read /write cycle or Load color register or Load mask or Load stop or Flash write or Block write cycle is activated to the $\overline{WB}/\overline{WE}$, DSF1 condition.
WIOn *	WRITE MASK/DATA INPUT/OUTPUT	These are the data Input/output pins to the RAM. During RAM write-per-bit, flash write, block write cycle, the high data pin at the $\overline{RAS}$ falling edge enables the selected bit write operation.
SC	SERIAL CONTROL INPUT	The serial access is initiated from the SC clock rising edge. In the serial read cycle. The output data is held until the next clock rise.
SQn *	SERIAL OUTPUT	512-bit × 8 word serial output.
$\overline{SE}$	SERIAL ENABLE INPUT	This enables the serial output.
DSF1	INPUT SPECIAL FUNCTION-1	This input defines special functions such as Split transfer, flash write, block wirte and Load color, Load mask register. When it is low grounded, the device works as a basic dual-port memory.
QSF	OUTPUT SPECIAL FUNCTION	Output indicating the serial data selector status.

Note * : n = 0~7

TRUTH TABLE

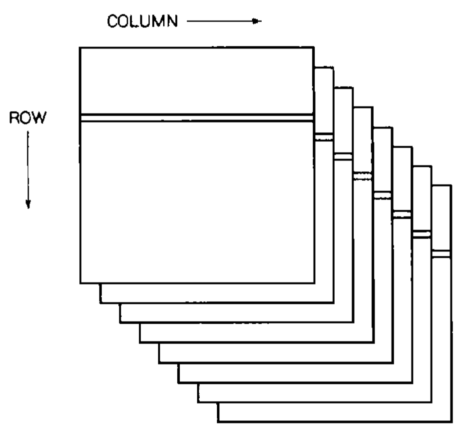
Menu code	$\overline{RAS}$				$\overline{CAS}$	Address		MD input			Write mask	Register		Function
	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF1	DSF1	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{CAS}$,$\overline{W}$		WM	color	
CBRS	0	*	0	1	–	STOP	–	*	–	*	*	*	*	CBR refresh/Stop Register Set(No Reset)
CBRN	0	*	1	1	–	*	–	*	–	*	*	*	*	CBR refresh/ (No Reset)
CBR	0	*	*	0	–	*	–	*	–	*	*	*	*	CBR refresh (Option Reset)
RT	1	0	1	0	*	ROW	TAP	*	*	*	*	*	*	Read x-fer
SRT	1	0	1	1	*	ROW	TAP	*	*	*	*	*	*	Split read x-fer with programmable stop
RWM	1	1	0	0	0	ROW	COL	new WM	–	Data input	Yes	Load use	*	Read/Write (New/Old mask)
BWM	1	1	0	0	1	ROW	Col Y2-Y8	new WM	Col select	–	Yes	Load use	USE	Block write (New/Old mask)
FWM	1	1	0	1	–	ROW	*	new WM	–	–	Yes	Load use	USE	Flash write (New/Old mask)
RW	1	1	1	0	0	ROW	COL	*	*	Data input	*	*	*	Read/Write no mask
BW	1	1	1	0	1	ROW	Col Y2-Y8	*	Col select	–	*	*	USE	Block write no mask
LMR	1	1	1	1	0	ROW	*	*	*	Load mask	*	*	*	Load mask register
LCR	1	1	1	1	1	ROW	*	*	*	Load color	*	*	*	Load color register

Option means Stop Register and Old mask mode. CBR resets both Stop Register and Old mask mode.(= Stop Register is reset to defaut value and New mask mode is active when CBR operation is executed.)

FUNCTION

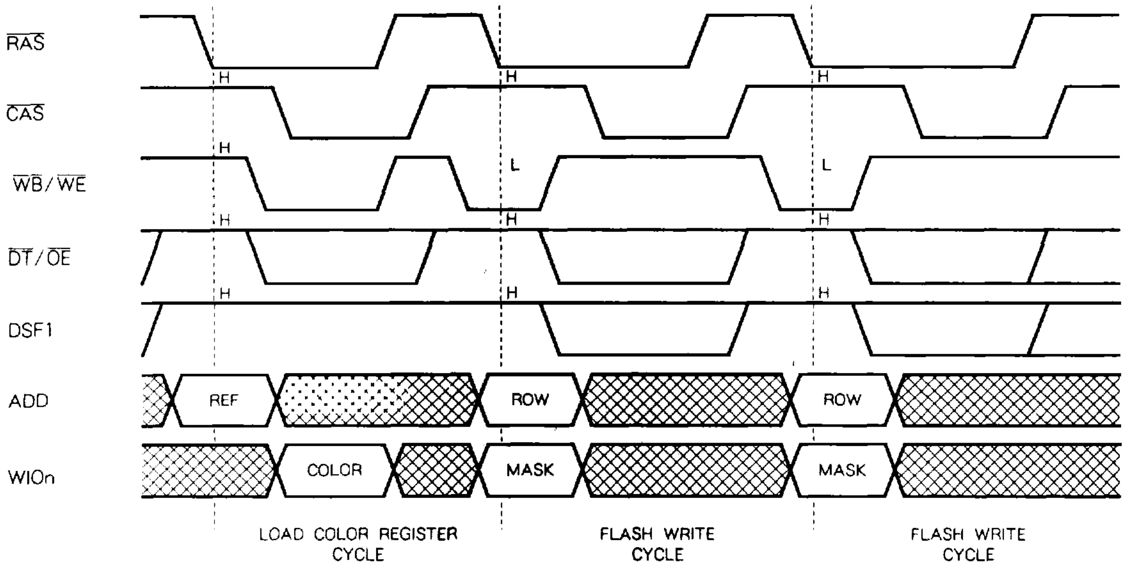
1. Flash Write

Utility : A high speed clear can be performed with flash write cycle.



* Write a color (0 or 1) to an entire row in one RAM cycle.
* Before flash write cycle, the color data must be set into an internal color register at least once.

Flash Write Timing Description



2. Split Register with Programmable Stop function

Utility

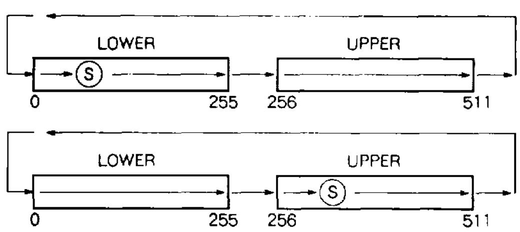
a. To simplify real time transfer timing.(fully asynchronous serial access)

b. To split serial register into two halves and optimize the memory size to CRT.

Pointer path

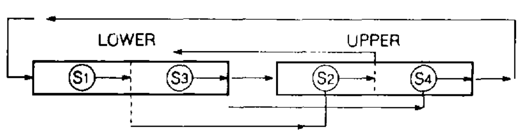
At Normal Read Transfer Cycle

1. Transfer the data from RAM to SAM, and set the SAM start address among 0 to 511.
2. Start the serial read cycle.
3. Serial read from lower to upper/upper to lower.(the pointer of the lower/upper SAM will be automatically cleared to address 0/256 after over carried)



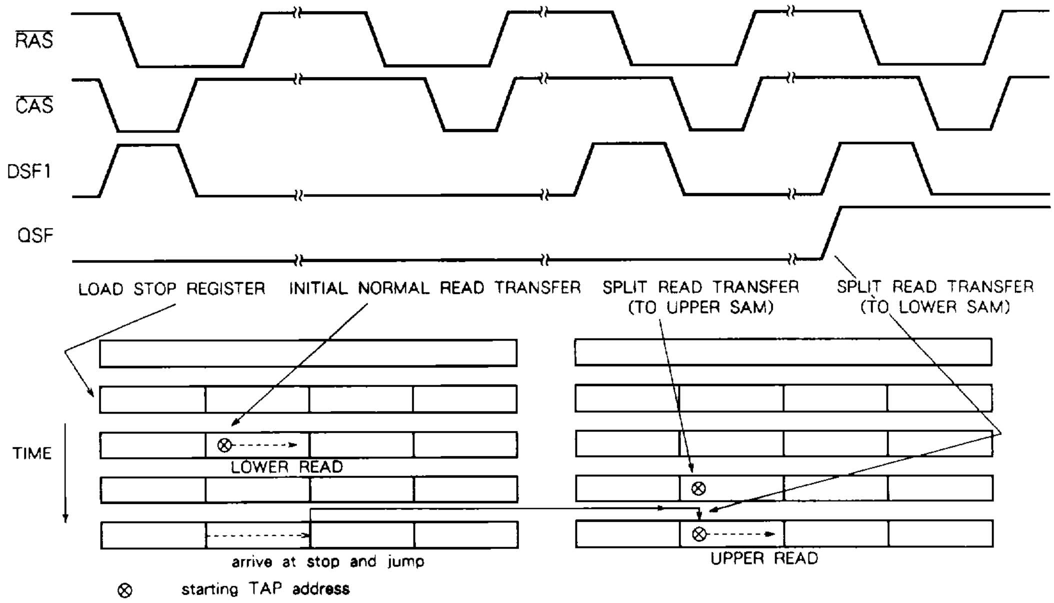
At Split Transfer Cycle

1. Load stop register cycle and define SAM division.
2. Normal read transfer cycle must be performed prior to the split transfer cycle.
   1 →2 or 2 →1 is permitted.
3. At the split transfer mode, data are transferred to the idle half of the SAM automatically.(column address A_8 is ignored)
4. QSF indicates the busy SAM.
   lower half SAM is busy : 0
   upper half SAM is busy : 1
5. Serial read can be performed asynchronously during RAM cycle and Split transfer cycle.

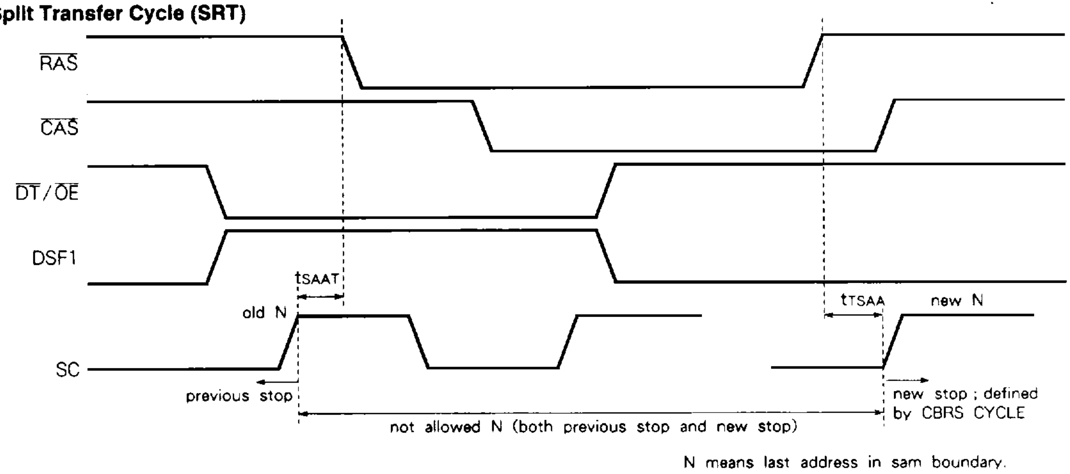


S_1, S_2, S_3 or S_4 is tap address, that is defined during split transfer cycle.
SAM is devided into 4 subsections in this example.

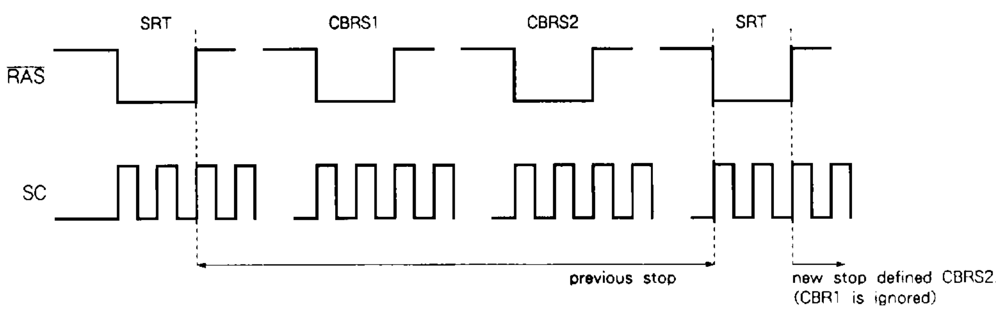
EXAMPLE



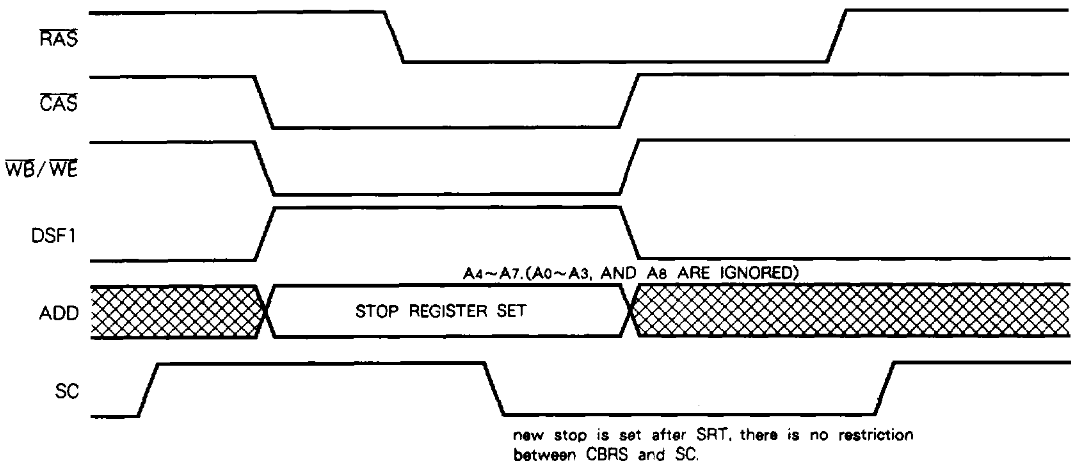
Split Transfer Cycle (SRT)



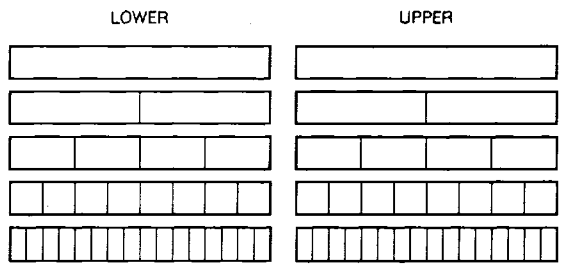
Previous stop is cleard by SRT cycle at $\overline{RAS}$ low edge and New stop is started after SRT cycle $\overline{RAS}$ high edge.



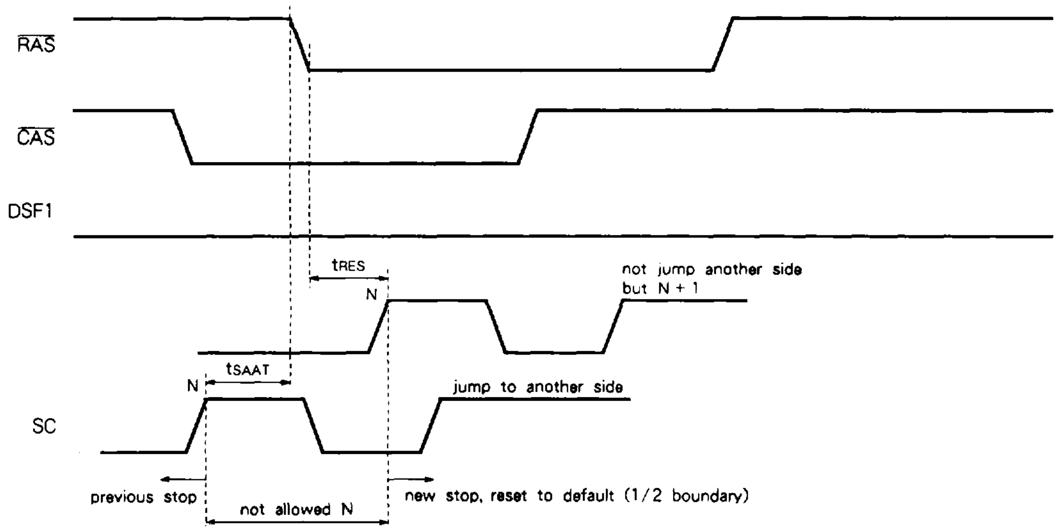
CBR with Load Stop Register Cycle (CBRS)



A7	A6	A5	A4	DIVISION	BIT WIDTH
1	1	1	1	1/2	256
0	1	1	1	1/4	128
0	0	1	1	1/8	64
0	0	0	1	1/16	32
0	0	0	0	1/32	16



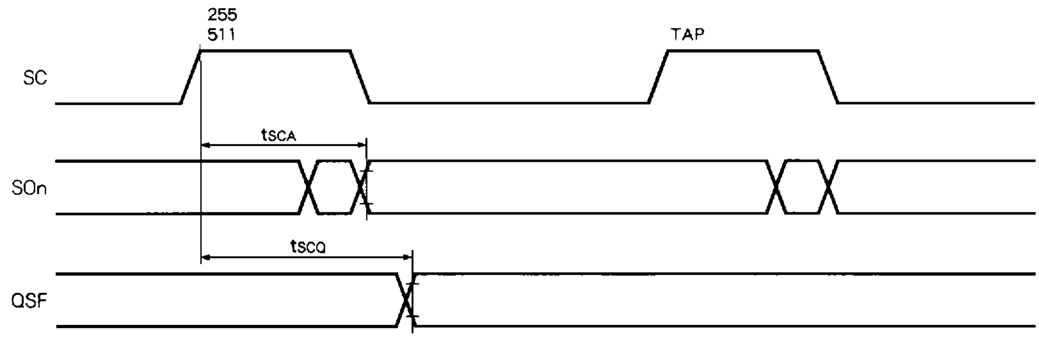
CBR Option Reset Cycle (CBR)



N means last address in SAM boundary.

Previous stop is cleard by CBR cycle $\overline{RAS}$ low edge and new boundary (1/2 boundary) is started.

QSF Timing Description



3. Block Write

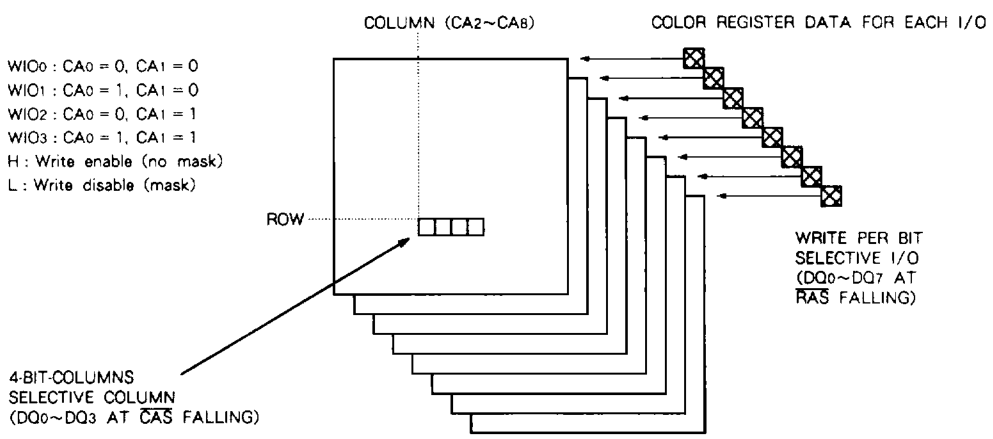
In the Block Write cycle, data stored in color register can be written into 4-bit-columns (block is selected with column address $CA_2 \sim CA_8$) at one time. The $DQ_0 \sim DQ_3$ inputs at $\overline{CAS}$ falling edge enable a selective column write operation of the selected 4-bit-columns.

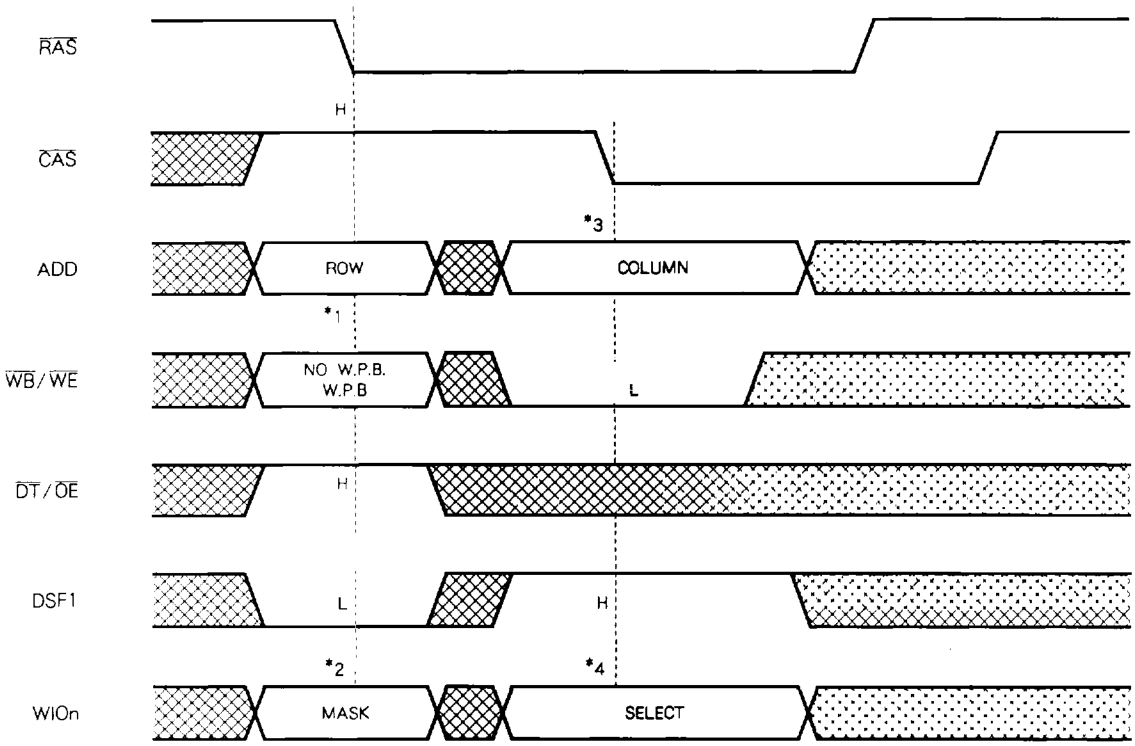
When $\overline{WB}/\overline{WE}$ is low at $\overline{RAS}$ falling edge, Write-Per-Bit operation applies to writing of color register data.

The color register must be loaded prior to the block write cycle.

Application

Block write operation is available for the partial-cleaning or partial-painting of bit-map display with same color data. With the selective-column writing of data, any of the 4-bit-columns can be masked, allowing the boundary treatment in the same cycle.



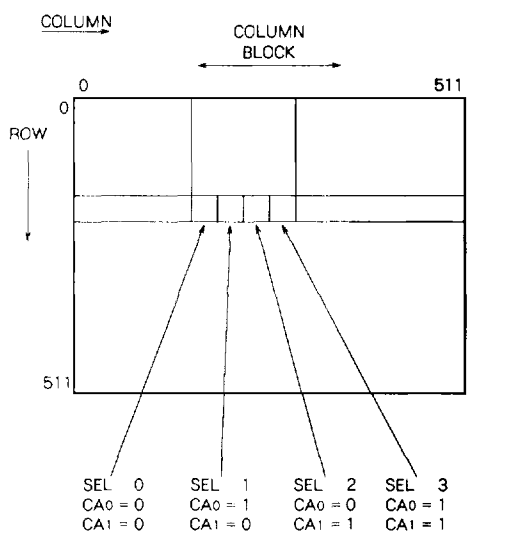


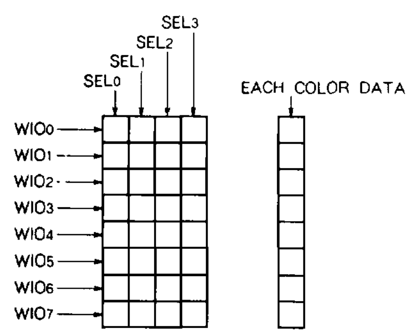
*1 H : No mask
L : Write per bit

*2 H : Write enable
L : Write disable

*3 column address CA2~CA8, CA0~CA1 = Don't care.

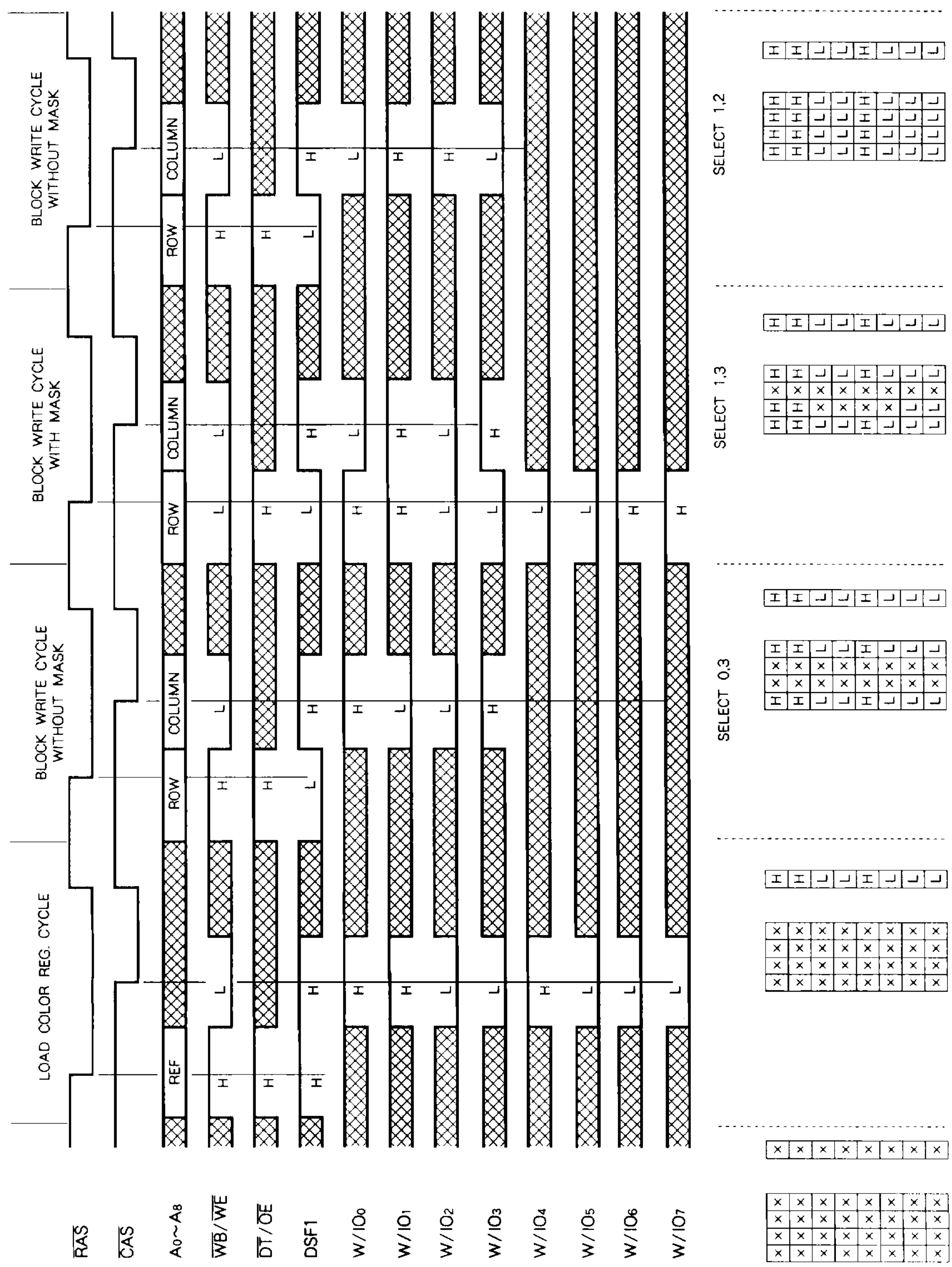
*4 Select WIO0 : CA0 = 0, CA1 = 0
WIO1 : CA0 = 1, CA1 = 0
WIO2 : CA0 = 0, CA1 = 1
WIO3 : CA0 = 1, CA1 = 1
H : Write enable
L : Write disable





A0, A1 and WIO4~7 at CAS falling edge, are "don't care."
but must be set H or L state.

Example


LOAD COLOR REG. CYCLE
BLOCK WRITE CYCLE WITHOUT MASK
BLOCK WRITE CYCLE WITH MASK
BLOCK WRITE CYCLE WITHOUT MASK
RAS
CAS
A0~A8
WB/WE
DT/OE
DSF1
W/IO0
W/IO1
W/IO2
W/IO3
W/IO4
W/IO5
W/IO6
W/IO7
REF
ROW
COLUMN
SELECT 0,3
SELECT 1,3
SELECT 1,2

NEW MASK/OLD MASK

Mask data can be selected, in write per bit cycle, flash write cycle and block write cycle. New mask is defined and only available during each set cycle.

Old mask is set by Load Mask cycle and it is continuously used in all masked cycle. Old mask mode is cleared by CBR reset cycle and New mask mode is active. New mask mode is active after CBR reset cycle which clears old mask mode.

example1

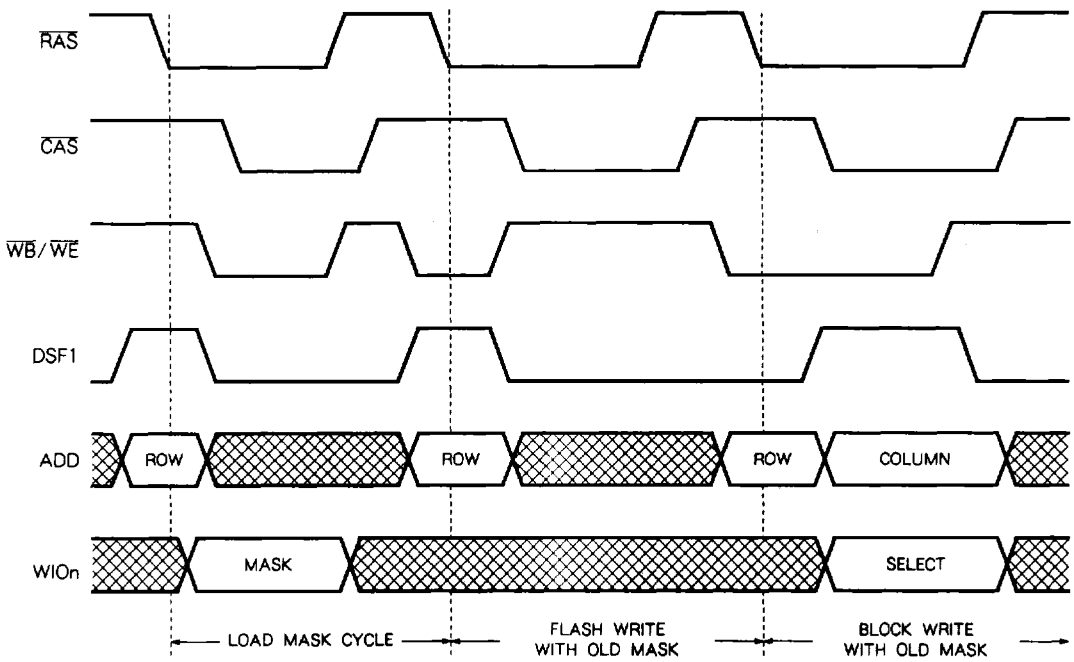
Load Mask Register cycle → Flash Write cycle → Block Write cycle → CBR Reset cycle → Block Write cycle →

Load Mask Register cycle	Flash Write cycle	Block Write cycle	CBR Reset cycle	Block Write cycle
	< old mask >	< old mask > *		< new mask > *

* 4-bit masks apply only if mask mode is enabled.

example 2

Timing Description



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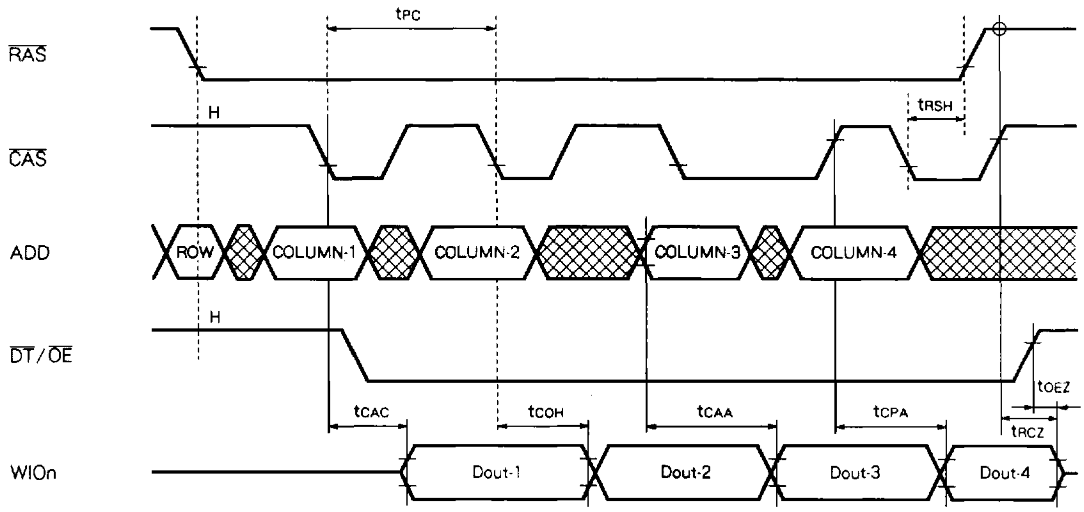
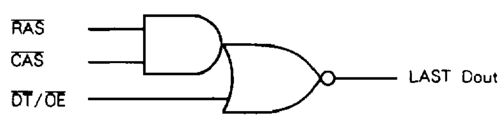
Hyper Page mode cycle with extended data out

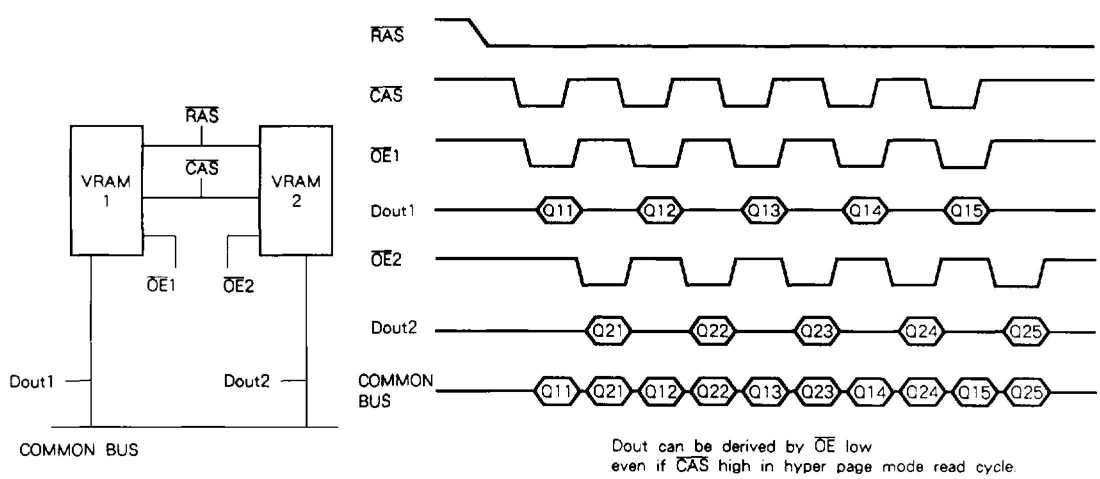


In Hyper page mode read cycle, $\overline{CAS}$ is treated as a low edge triger.
Data output enable/disable is controlled by only $\overline{DT}/\overline{OE}$.
Last Dout (in this case Dout-4) is disabled $\overline{OE}$ high edge or $\overline{RAS}$, $\overline{CAS}$ high.

Access time from $\overline{CAS}$ is determined by t_{CAC}, t_{CAA} and t_{CPA}.
Previous Dout will be sustained until next Dout. (extended data out)



$\overline{OE}$ interleave is possible in hyper page mode



Dout can be derived by $\overline{OE}$ low
even if $\overline{CAS}$ high in hyper page mode read cycle.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	$T_a = 25$℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Norm	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input	2.4		6.5	V
V_{IL}	Low-level input	−1.0		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{OH(R)}$	High-level output (RAM port)	$I_{OH(R)} = -1$mA	2.4		Vcc	V
$V_{OL(R)}$	Low-level output (RAM port)	$I_{OL(R)} = 2.1$mA	0		0.4	V
$V_{OH(S)}$	High-level output (Serial Io port)	$I_{OH(S)} = -1$mA	2.4		Vcc	V
$V_{OL(S)}$	Low-level output (Serial Io port)	$I_{OL(S)} = 2.1$mA	0		0.4	V
I_{OZ}	Off-state output current	Q Floating $0 < V_{OUT} < V_{CC}$	−10		10	μA
I_I	Input current	$0 < V_{in} < V_{CC}$	−10		10	μA

Note 2 : Current flowing into an IC is positive, out is negative.

CAPACITANCE (Ta = 25℃, f = 1MHz, Vi = 25mVmrs)

Symbol	Pin name	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN0}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, SC, $\overline{SE}$, $\overline{DT}/\overline{OE}$, DSF	$V_I = V_{SS}$, f = 1MHz, $V_i = 25$mVrms			7	pF
C_{IN1}	A_0~A_8				7	pF
C_O	WIO_0~WIO_7, SIO_0~SIO_7, QSF				9	pF

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted)

Symbol	Parameter: RAM port	Parameter: SAM port	Limits M5M482257-7 Max	Limits M5M482257-8 Max	Limits M5M482257-10 Max	Unit
I_{CC1}	Random R/W cycle, $\overline{RAS}/\overline{CAS}$ cycling, t_{RC}=min (Note 3, 4)	Stand-by ($SC=V_{IL}$)	90	80	70	mA
I_{CC2}	Stand-by, $\overline{RAS}=V_{IH}$, $\overline{CAS}=V_{IH}$, D_{OUT}=Hi-Z		5	5	5	mA
I_{CC3}	$\overline{RAS}$ only refresh cycle, $\overline{RAS}$=cycling, $\overline{CAS}=V_{IH}$, t_{RC}=min (Note 3, 4)		90	80	70	mA
I_{CC4}	Page mode cycle, $\overline{RAS}=V_{IL}$, $\overline{CAS}$=cycling, t_{PC}=min (Note 3, 4)		90	80	70	mA
I_{CC5}	$\overline{CAS}$ before $\overline{RAS}$ refresh, t_{RC}=min (Note 3, 4)		90	80	70	mA
I_{CC6}	Data transfer cycle, t_{RC}=min (Note 3, 4)		110	100	90	mA
I_{CC7}	Random R/W cycle, $\overline{RAS}/\overline{CAS}$ cycling, t_{RC}=min (Note 3, 4)	Active (t_{SCC}=min)	140	130	120	mA
I_{CC8}	Stand-by, $\overline{RAS}=V_{IH}$, $\overline{CAS}=V_{IH}$, D_{OUT}=Hi-Z (Note 3, 4)		55	55	55	mA
I_{CC9}	$\overline{RAS}$ only refresh cycle, $\overline{RAS}$=cycling, $\overline{CAS}=V_{IH}$, t_{RC}=min (Note 3, 4)		140	130	120	mA
I_{CC10}	Page mode cycle, $\overline{RAS}=V_{IL}$, $\overline{CAS}$=cycling, t_{PC}=min (Note 3, 4)		140	130	120	mA
I_{CC11}	$\overline{CAS}$ before $\overline{RAS}$ refresh, t_{RC}=min (Note 3, 4)		140	130	120	mA
I_{CC12}	Data transfer cycle, t_{RC}=min (Note 3, 4)		160	150	140	mA

Note 3: I_{CC1}, I_{CC3}~I_{CC12} are dependent on output loading. Specific values are obtained with the output open.
4: I_{CC1}, I_{CC3}~I_{CC12} are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

SWITCH CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 5)

Symbol	Parameter		M5M482257-7 Min	M5M482257-7 Max	M5M482257-8 Min	M5M482257-8 Max	M5M482257-10 Min	M5M482257-10 Max	Unit
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 8)		20		20		25	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 9)		70		80		100	ns
t_{CAA}	Column address access time	(Note 6, 10)		35		40		50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 11)		40		45		55	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		20		20		25	ns
t_{CLZ}	Output low impedance from $\overline{CAS}$ low		5		5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	20	0	20	ns
t_{RCZ}	Output disable time after $\overline{RAS}$, $\overline{CAS}$ high		0	15	0	20	0	20	ns
t_{COH}	Output hole time after $\overline{CAS}$ low		5		5		5		ns
t_{SCA}	Access time from SC high	(Note 7)		20		25		25	ns
t_{SOA}	Access time from $\overline{SE}$ low	(Note 7)	0	20	0	20	0	25	ns
t_{SOZ}	Output disable time after $\overline{SE}$ high	(Note 12)	0	15	0	20	0	20	ns
t_{SOH}	Serial output hold time after SC high		5		5		5		ns

Note 5: An initial pause of 500μs is required after power up followed by eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock, such as $\overline{RAS}$ only refresh)
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{RAS}$ inacitivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 1TTL loads and 50pF.
7: Measured with a load circuit equivalent to 1TTL loads and 30pF.
8: Assume that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
9: Assume that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
10: Assume that t_{RCD}-$t_{RAD} \leq t_{CAA}(max)$-$t_{CAC}(min)$ and $t_{RCD} \geq t_{RCD}(max)$.
11: Assume that $t_{CP} \leq t_{CP}(max)$ and $t_{ASC} \geq t_{ASC}(max)$.
12: $t_{OFF}(max)$, $t_{SOZ}(max)$ and $t_{OEZ}(max)$ define the time at which output achieves high impedance state.

TIMING REQUIREMENTS (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 13, 14)

(1) Read, Write, Refresh, Load Color Register, Load Mask Register, Block Write, Flash Write, Read Transfer and Page Mode Cycles

Symbol	Parameter	Limits						Unit
		M5M482257-7		M5M482257-8		M5M482257-10		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read, write cycle time	130		150		180		ns
t_{RAS}	$\overline{\text{RAS}}$ low pulse width	70	10000	80	10000	100	10000	ns
t_{CAS}	$\overline{\text{CAS}}$ low pulse width	20	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$	70		80		100		ns
t_{RSH}	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$	20		25		30		ns
t_{REF}	Refresh cycle time		8		8		8	ms
t_{RP}	$\overline{\text{RAS}}$ high pulse width	50		60		70		ns
t_{RCD}	Delay time $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note 15)	20	50	25	60	25	75	ns
t_{CRP}	Delay time $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low (Note 16)	10		10		10		ns
t_{CPN}	$\overline{\text{CAS}}$ high pulse width	10		10		10		ns
t_{ASR}	Row address setup time before $\overline{\text{RAS}}$	0		0		0		ns
t_{RAH}	Row address hold time after $\overline{\text{RAS}}$	10		15		15		ns
t_{RAD}	Column address delay time from $\overline{\text{RAS}}$ (Note 17)	15	35	20	40	20	50	ns
t_{ASC}	Column address setup time before $\overline{\text{CAS}}$	0		0		0		ns
t_{CAH}	Column address hold time after $\overline{\text{CAS}}$	15		15		20		ns
t_{WSR}	$\overline{\text{WB}}/\overline{\text{WE}}$ setup time before $\overline{\text{RAS}}$	0		0		0		ns
t_{RWH}	$\overline{\text{WB}}/\overline{\text{WE}}$ hold time after $\overline{\text{RAS}}$	10		15		15		ns
t_{DTRS}	$\overline{\text{DT}}/\overline{\text{OE}}$ high setup time before $\overline{\text{RAS}}$	0		0		0		ns
t_{DTRH}	$\overline{\text{DT}}/\overline{\text{OE}}$ high hold time after $\overline{\text{RAS}}$	10		15		15		ns
t_{FSR}	DSF1 setup time before $\overline{\text{RAS}}$	0		0		0		ns
t_{RFH}	DSF1 hold time after $\overline{\text{RAS}}$	10		15		15		ns
t_{FSC}	DSF1 setup time before $\overline{\text{CAS}}$	0		0		0		ns
t_{CFH}	DSF1 hold time after $\overline{\text{CAS}}$	15		15		20		ns
t_{WS}	Write mask setup time before $\overline{\text{RAS}}$	0		0		0		ns
t_{WH}	Write mask hold time after $\overline{\text{RAS}}$	10		15		15		ns
t_T	Transition time (Note 18)	3	35	3	35	3	35	ns

Note 13: Timing requirements are assumed t_T = 5ns.
14: $V_{IH}(min)$ and $V_{IL}(max)$ are raference levels for measuring timing of input signals.
15: $t_{RCD}(max)$ limit ensures that $t_{RAC}(max)$ can be met. $t_{RCD}(max)$ is specified as a reference point only. If t_{RCD} is greater than t_{RCD} (max), access time is controlled by t_{CAC} or t_{CAA} as shown in notes 7 or 9.
16: t_{CRP} requirement is applicable for all $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.
17: $t_{RAD}(max)$ limit ensures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a refrence point only. If t_{RAD} is greater than t_{RAD} (max), access time is controlled by t_{CAC} or t_{CAA} as shown in notes 7 or 9.
18: t_T is measured between $V_{IH}(min)$ and $V_{IL}(max)$.

(2) Read and Refresh Cycles

Symbol	Parameter	M5M482257-7 Min	M5M482257-7 Max	M5M482257-8 Min	M5M482257-8 Max	M5M482257-10 Min	M5M482257-10 Max	Unit
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 19)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 19)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time	35		40		50		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	20		25		25		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	70		80		100		ns
t_{DOEL}	Delay time data to $\overline{OE}$ low	0		0		0		ns
t_{OEHD}	Delay time $\overline{OE}$ high to Data	15		15		20		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low	20		20		25		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low	20		20		20		ns

Note 19: Either t_{RCH} or t_{RRH} must be satisfied.

(3) Write Cycle (Eary Write and Delayed Write)

Symbol	Parameter	M5M482257-7 Min	M5M482257-7 Max	M5M482257-8 Min	M5M482257-8 Max	M5M482257-10 Min	M5M482257-10 Max	Unit
t_{WCS}	Write setup time before $\overline{CAS}$ (Note 20)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$	15		15		15		ns
t_{CWL}	$\overline{CAS}$ hold time after write	20		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after write	20		20		25		ns
t_{WP}	Write pulse width	15		15		15		ns
t_{DSC}	Data setup time before $\overline{CAS}$	0		0		0		ns
t_{DHC}	Data hold time after $\overline{CAS}$	15		15		20		ns
t_{DSW}	Data setup time before write	0		0		0		ns
t_{DHW}	Data hold time after write	15		15		20		ns
t_{OEHD}	Delay time $\overline{OE}$ high to data	15		15		20		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write	15		15		20		ns

Note 20: t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} do not define the limits of operation, but are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$, early write cycle is performed with data outputs keeping high impedance state. If $t_{RWD} \geq t_{RWD(min)}$, $t_{CWD} \geq t_{CWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, read-write cycle is performed with the data of the selected address being out from the data output. If neither of the above condition is satisfied, the condition of data out (at access time and untill $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminated.

(4) Read-Write and Read-Modify-Write Cycle

Symbol	Parameter	Limits						Unit
		M5M482257-7		M5M482257-8		M5M482257-10		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read-Write, read-modify-write cycle time	185		205		245		ns
t_{RAS}	$\overline{RAS}$ low pulse width	115	10000	125	10000	155	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	70	10000	70	10000	85	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$	115		125		155		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$	70		70		85		ns
t_{RCS}	Read setup time before $\overline{CAS}$	0		0		0		ns
t_{CWD}	Delay time $\overline{CAS}$ to write (Note 20)	40		40		50		ns
t_{RWD}	Delay time $\overline{RAS}$ to write (Note 20)	90		100		125		ns
t_{CWL}	$\overline{CAS}$ hold time after write	20		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after write	20		20		25		ns
t_{WP}	Write pulse width	15		15		20		ns
t_{DSW}	Data setup time before write	0		0		0		ns
t_{DHW}	Data hold time after write	15		15		20		ns
t_{AWD}	Delay time address to write (Note 20)	55		60		75		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$	20		20		25		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$	70		80		100		ns
t_{DOEL}	Delay time data to $\overline{OE}$ low	0		0		0		ns
t_{OEHD}	Delay time $\overline{OE}$ high to data	15		15		20		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write	15		15		20		ns

(5) Hyper Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter	Limits						Unit
		M5M482257-7		M5M482257-8		M5M482257-10		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Read, write cycle time	40		45		55		ns
t_{RWPC}	Read-write, read modify write cycle time	95		100		115		ns
t_{RASP}	$\overline{RAS}$ low pulse width	115	100000	135	100000	160	100000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	20	10000	25	10000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 21)	10	15	10	20	10	25	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$	20		25		30		ns
$t_{d(RAND)}$	$\overline{OE}$ high hold time after $\overline{CAS}$ high	10		10		10		ns
$t_{w(RAND)}$	$\overline{OE}$ high pulse width	10		10		10		ns

Note 21 : $t_{CP(max)}$ is specified as a reference point only. If $t_{CP(max)} \leq t_{CP}$, access time is determined by t_{CAC}.

(6) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Load stop Register, Option Reset, Non Reset Cycle) (Note 22)

Symbol	Parameter	Limits						Unit
		M5M482257-7		M5M482257-8		M5M482257-10		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$	15		15		20		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns
t_{FSR}	DSF1 setup time before $\overline{RAS}$	0		0		0		ns
t_{RFH}	DSF1 hold time after $\overline{RAS}$	10		15		15		ns
t_{SAAT}	Delay time last SC to $\overline{RAS}$	30		30		30		ns
t_{RES}	Delay time $\overline{RAS}$ to last SC	60		60		60		ns

Note 22 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

(7) Normal-Read Transfer Cycle

Symbol	Parameter	Limits						Unit
		M5M482257-7		M5M482257-8		M5M482257-10		
		Min	Max	Min	Max	Min	Max	
t_{DLS}	$\overline{DT}/\overline{OE}$ low setup time before $\overline{RAS}$	0		0		0		ns
t_{RDH}	$\overline{DT}/\overline{OE}$ low hold time after $\overline{RAS}$	10	10000	15	10000	15	10000	ns
t_{RSD}	Delay time $\overline{RAS}$ to SC	80		80		100		ns
t_{ASD}	Delay time address to SC	40		40		50		ns
t_{CSD}	Delay time $\overline{CAS}$ to SC	30		30		30		ns
t_{SDH}	SC hold time after $\overline{DT}$	15		15		15		ns
t_{RQ}	Delay time $\overline{RAS}$ to QSF		85		85		85	ns
t_{AQ}	Delay time address to QSF		40		40		40	ns
t_{CQ}	Delay time $\overline{CAS}$ to QSF		35		35		35	ns
t_{DTQ}	Delay time $\overline{DT}$ to QSF		25		25		25	ns
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	50		60		70		ns
t_{DTW}	$\overline{DT}$ Precharge Time	15		15		15		ns

(8) Real Time Read Transfer Cycle

Symbol	Parameter	Limits						Unit
		M5M482257-7		M5M482257-8		M5M482257-10		
		Min	Max	Min	Max	Min	Max	
t_{DLS}	$\overline{DT}$ setup time before $\overline{RAS}$	0		0		0		ns
t_{RDH}	$\overline{DT}$ hold time after $\overline{RAS}$	55	10000	65	10000	80	10000	ns
t_{CDH}	$\overline{DT}$ hold time after $\overline{CAS}$	30		30		30		ns
t_{ADH}	$\overline{DT}$ hold time after address	30		30		30		ns
t_{SDD}	Delay time SC to $\overline{DT}$	5		5		5		ns
t_{SDH}	SC hold time after $\overline{DT}$	15		15		15		ns
t_{DTQ}	Delay time $\overline{DT}$ to QSF		25		25		25	ns

(9) Split Read Transfer Cycle

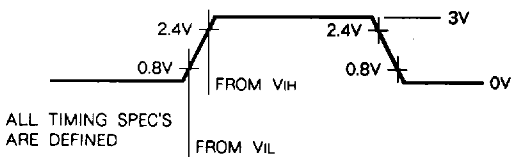
Symbol	Parameter	Limits						Unit
		M5M482257-7		M5M482257-8		M5M482257-10		
		Min	Max	Min	Max	Min	Max	
t_{SAAT}	Delay time last SC to $\overline{RAS}$	30		30		30		ns
t_{TSAA}	Delay time $\overline{RAS}$ to last SC	0		0		0		ns

(10) Serial Read Cycle

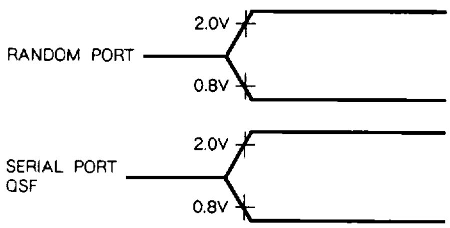
Symbol	Parameter	Limits						Unit
		M5M482257-7		M5M482257-8		M5M482257-10		
		Min	Max	Min	Max	Min	Max	
t_{SCC}	SC clock cycle time	25		30		30		ns
t_{SCH}	SC high pulse width	10		10		10		ns
t_{SCL}	SC low pulse width	10		10		10		ns
t_{SOP}	$\overline{SE}$ high pulse width	25		25		25		ns
t_{SOE}	$\overline{SE}$ low pulse width	25		25		25		ns
t_{SCQ}	Delay time SC to QSF		30		30		30	ns

Switching Measurement Condition

1. Input reference point

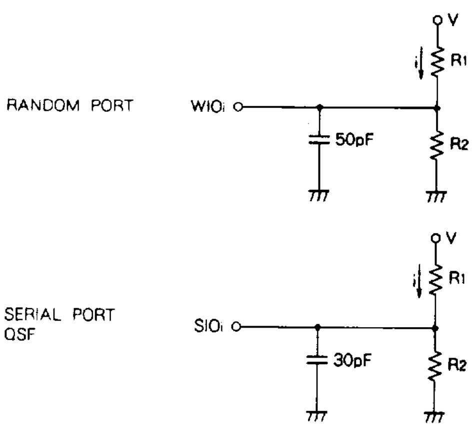


2. Output reference point



DC LEVEL OF OUTPUT IS $V_{OH} = 2.4V$, $V_{OL} = 0.4V$

3. Load condition



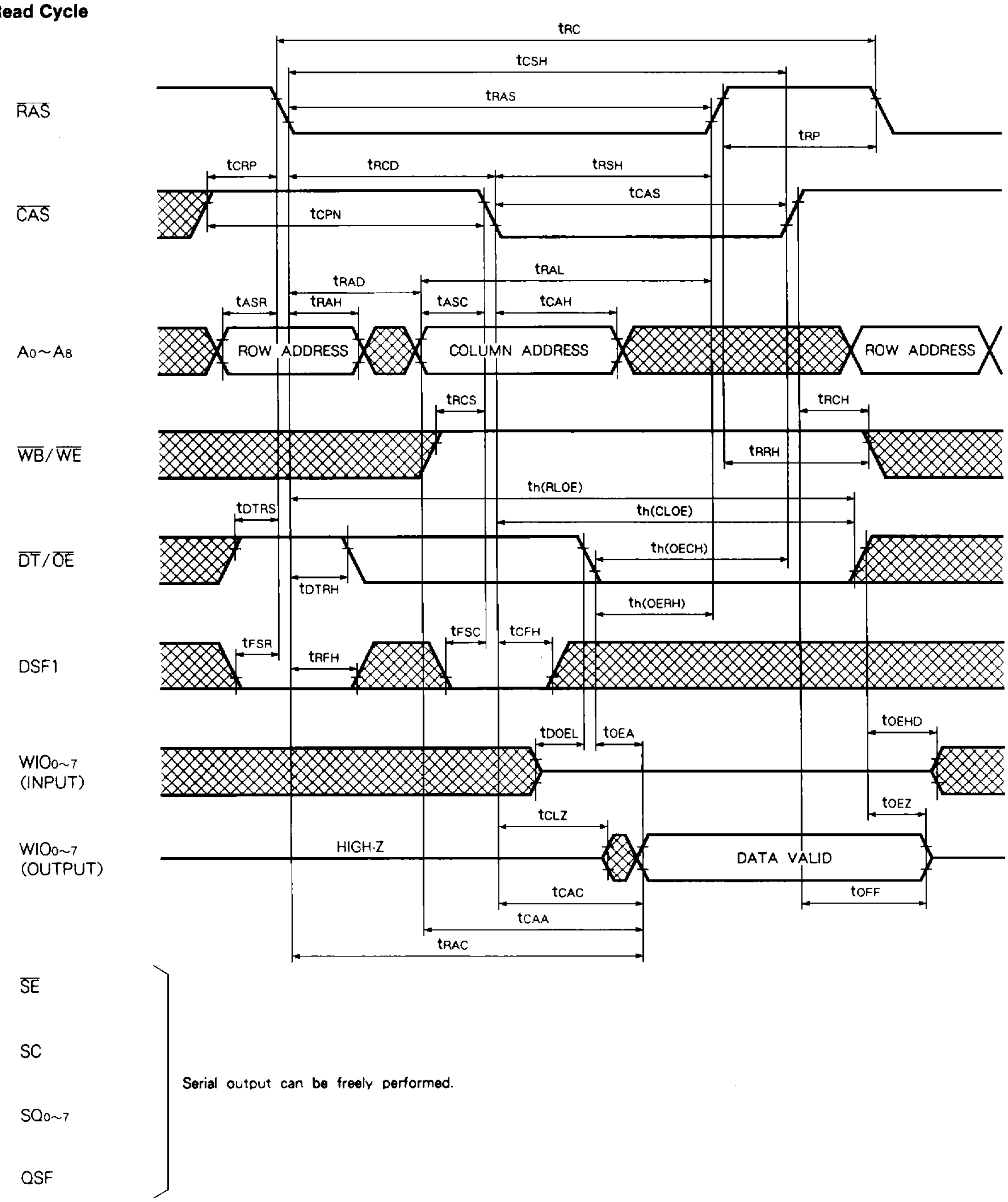
$$\left(\begin{array}{ll} V = V_{OH} + R_1 \cdot i_H & V = V_{OL} + R_1 \cdot i_L \\ V_{OH} = (i_H - I_{OH}) \cdot R_2 & V_{OL} = (i_L - I_{OL}) \cdot R_2 \\ \text{When } V = 5V,\ R_1 = 1838\,\Omega,\ R_2 = 994\,\Omega & \end{array}\right)$$

$$R_1 = \frac{V_{OH}\ (V - V_{OL})\ - V_{OL}\ (V - V_{OH})}{V_{OH} \cdot I_{OL} - V_{OL} \cdot I_{OH}}$$

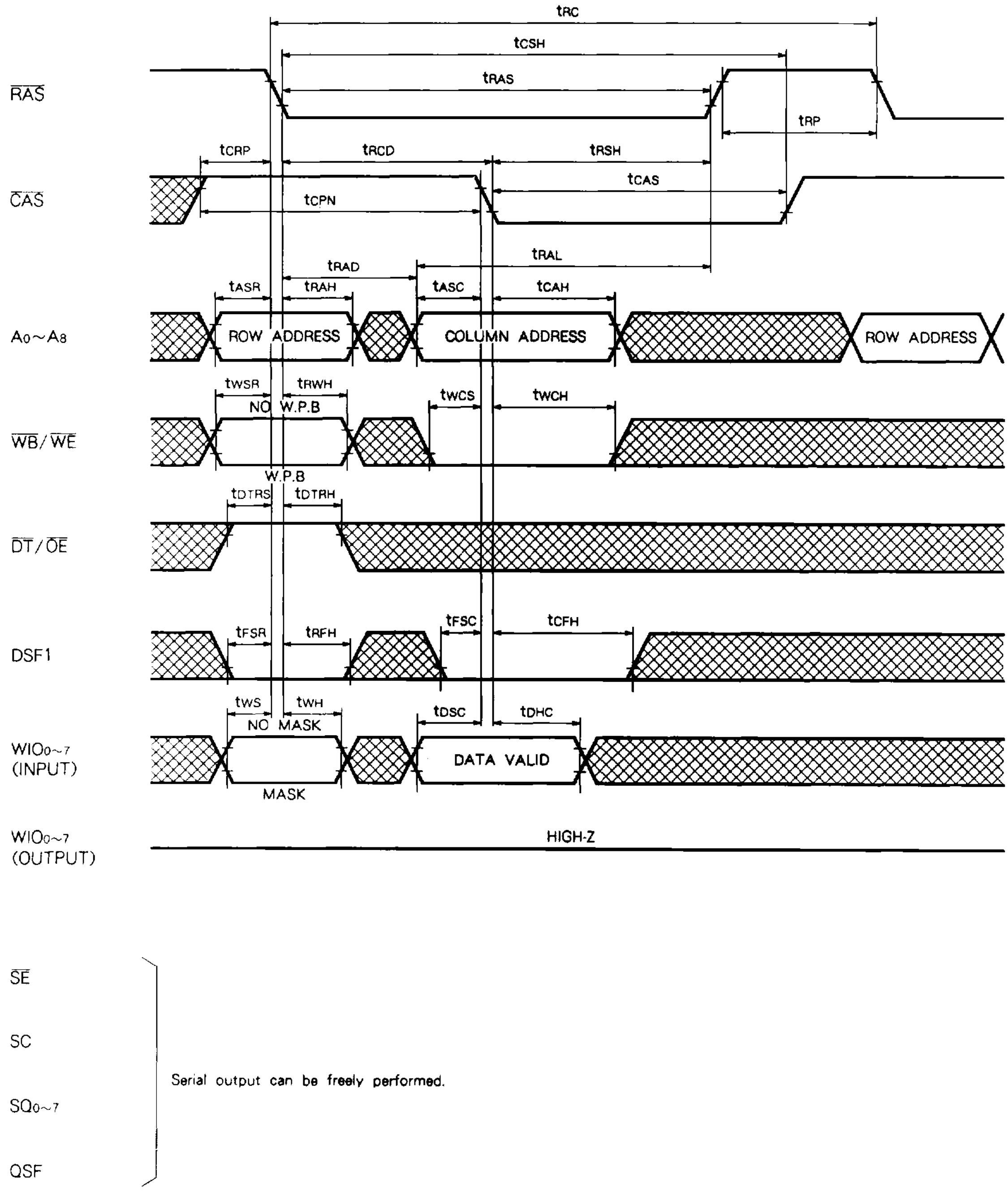
$$R_2 = \frac{V_{OH} \cdot R_1}{(V - V_{OH})\ - I_{OH} \cdot R_1}$$

TIMING DIAGRAMS

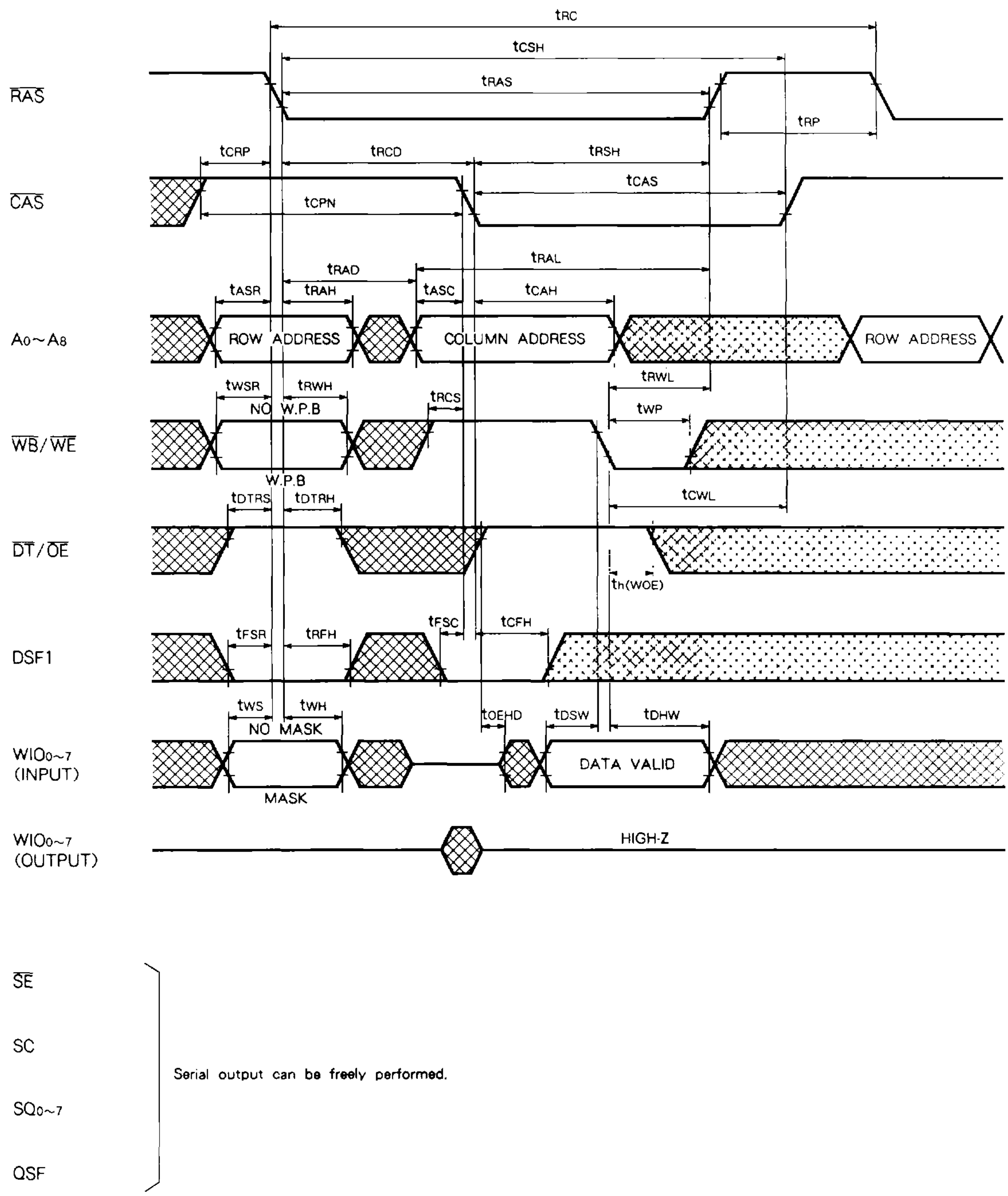
Read Cycle



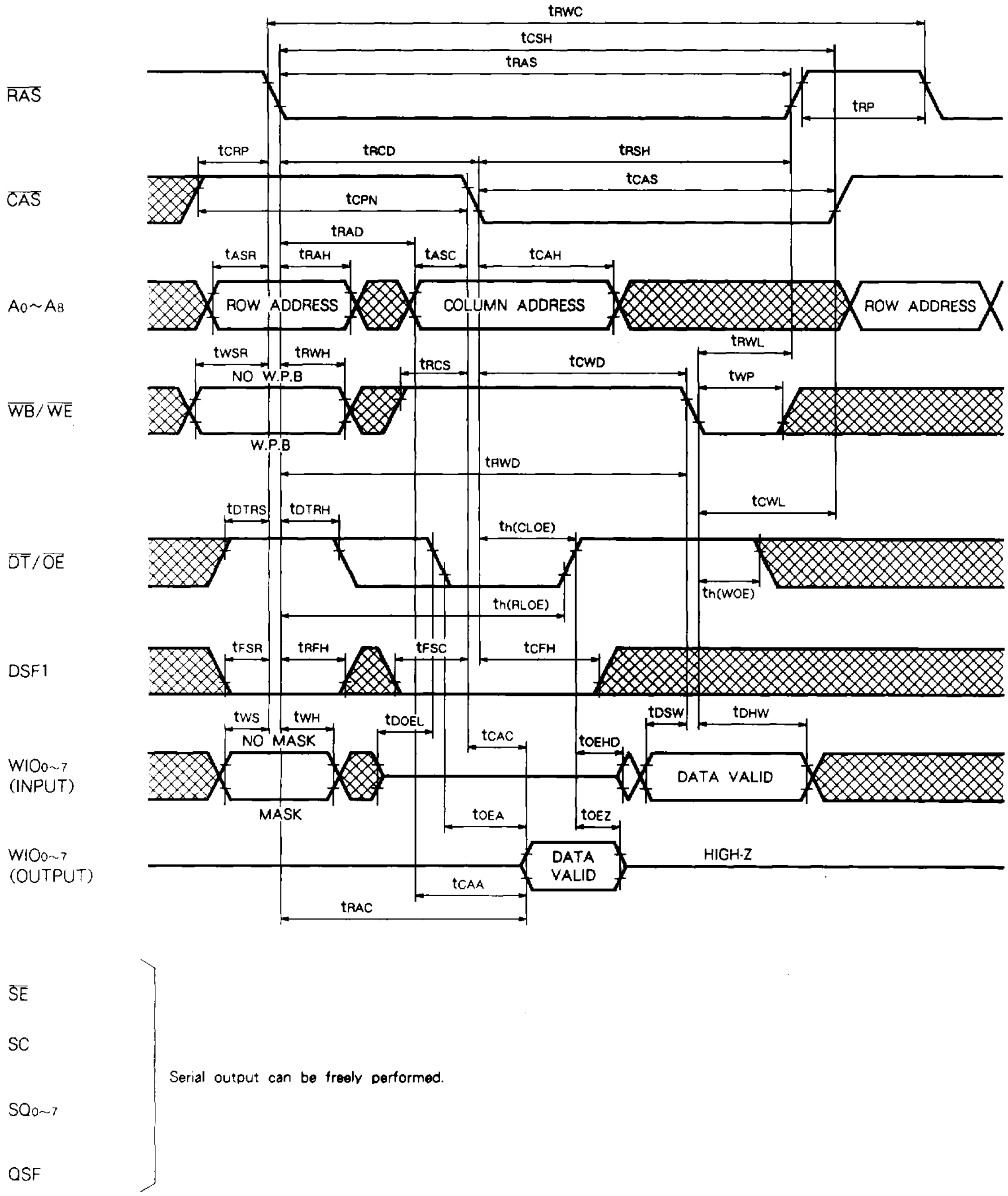
Write Cycle (Early Write)



Write Cycle (Late Write)

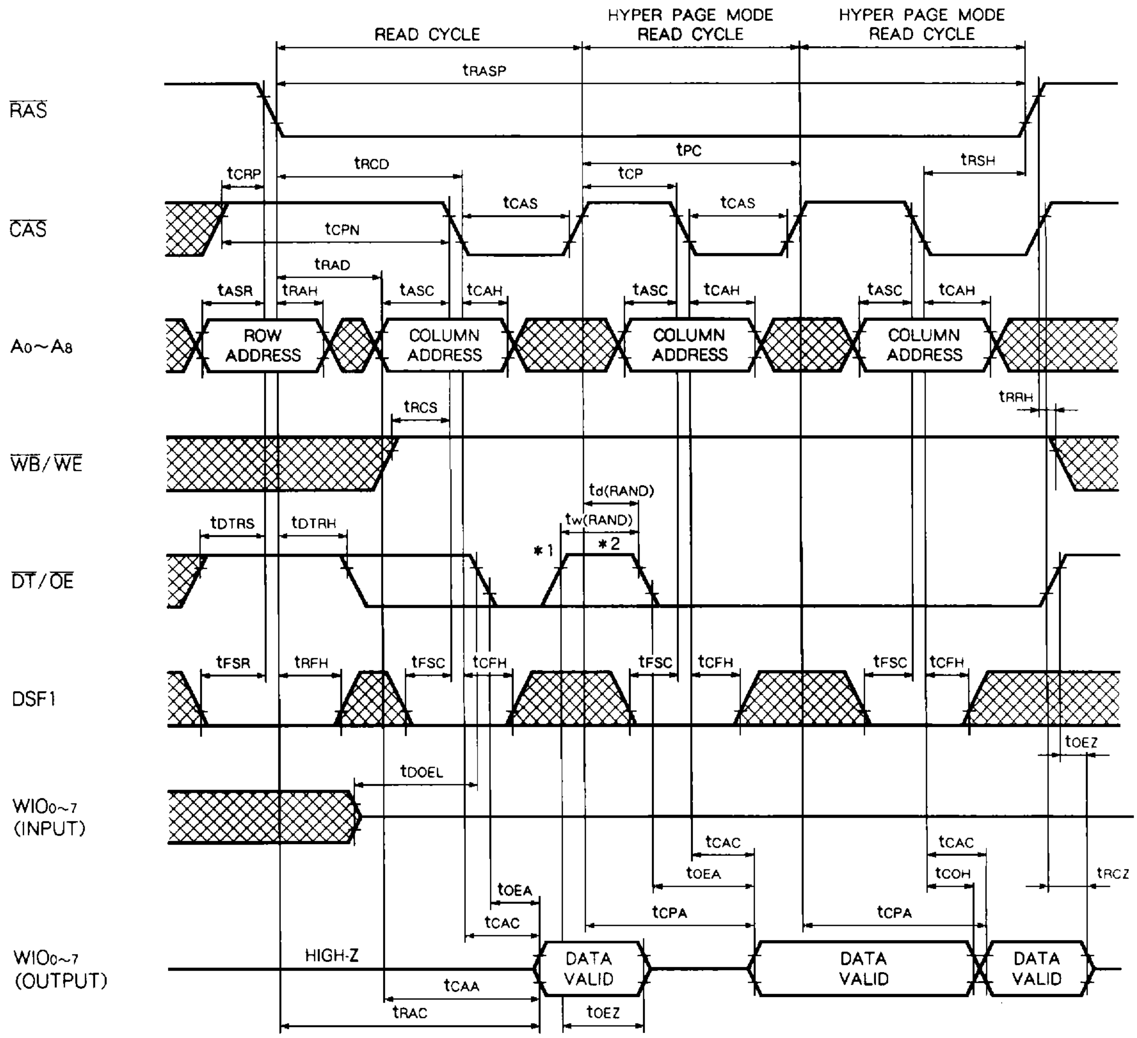


Read Modify Write Cycle



MITSUBISHI ELECTRIC

Hyper Page Mode Read Cycle

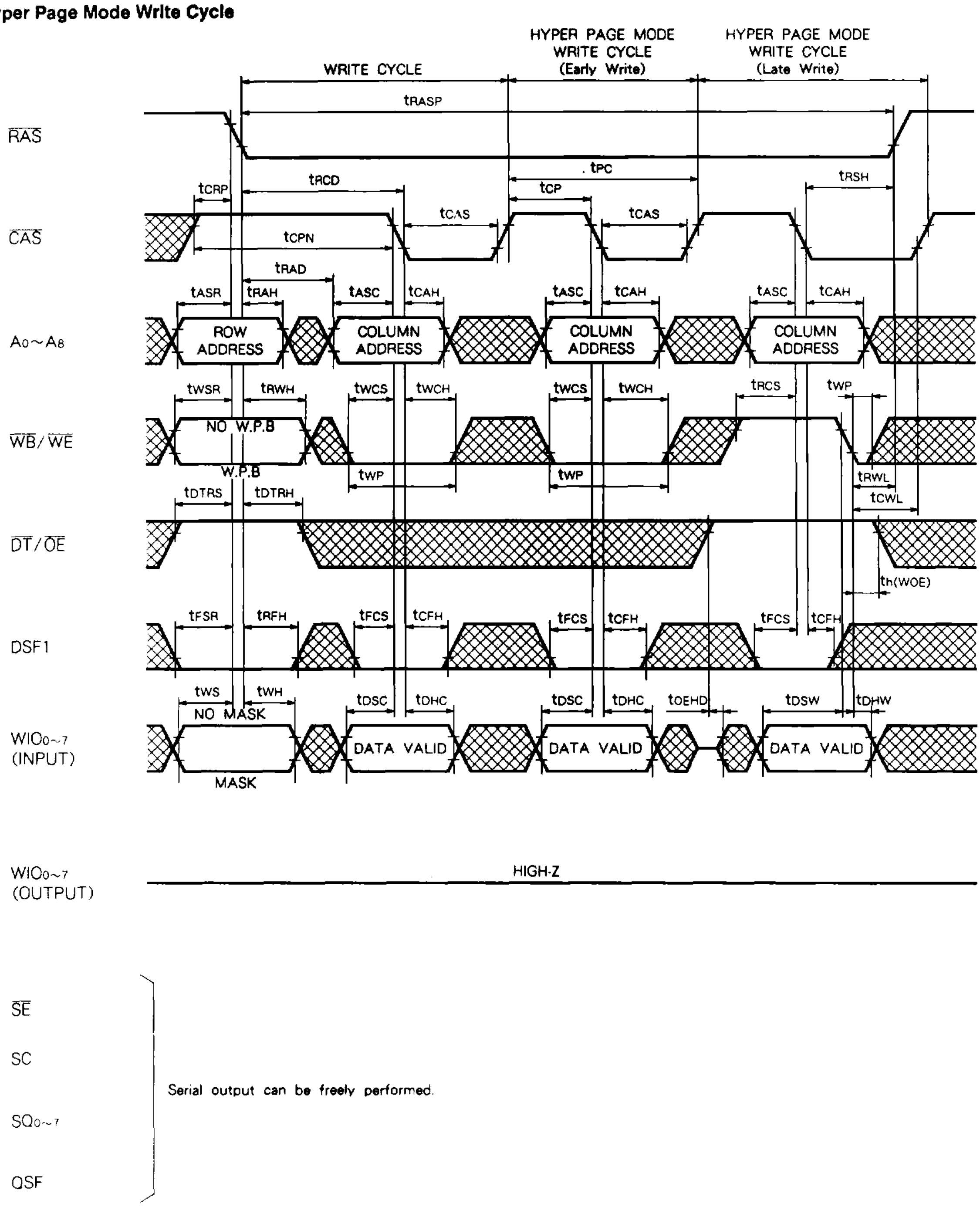


* 1 WHEN $\overline{OE}$ = high, DATA OUTPUT will be Hi-Z immediately.
  In that case Access time of next Data is determined by tCAC (tCAC ≥ tOEA) or tOEA (tOEA ≥ tCAC).
* 2 td(RAND), tw(RAND) = 10NS (min) is necesarry to remain Hi-Z however $\overline{CAS}$ = High and $\overline{OE}$ = Low.

  Next DATA OUTPUT is determined after $\overline{CAS}$ Low edge.

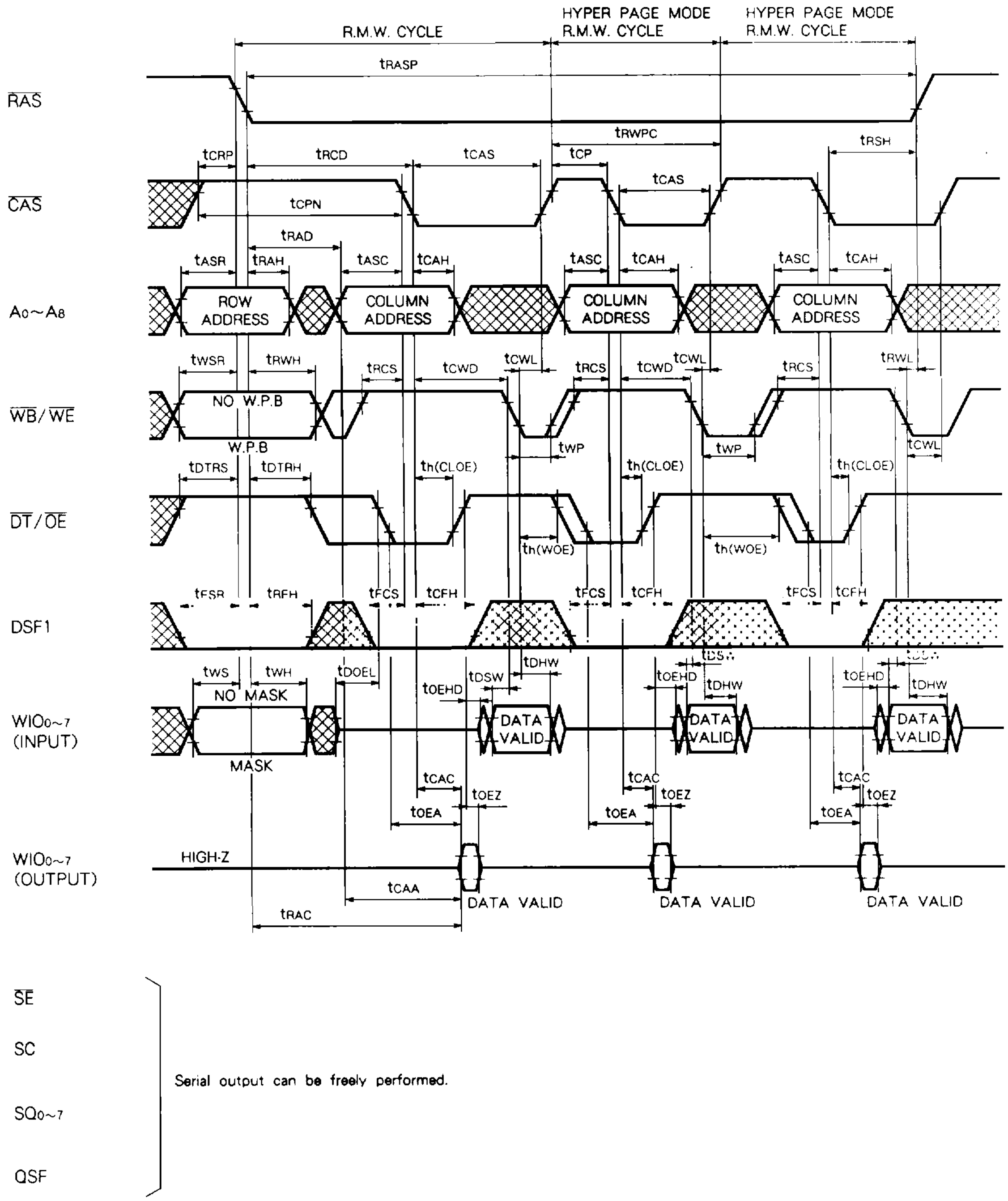
$\overline{SE}$, SC, SQ0~7, QSF	Serial output can be freely performed.

Hyper Page Mode Write Cycle

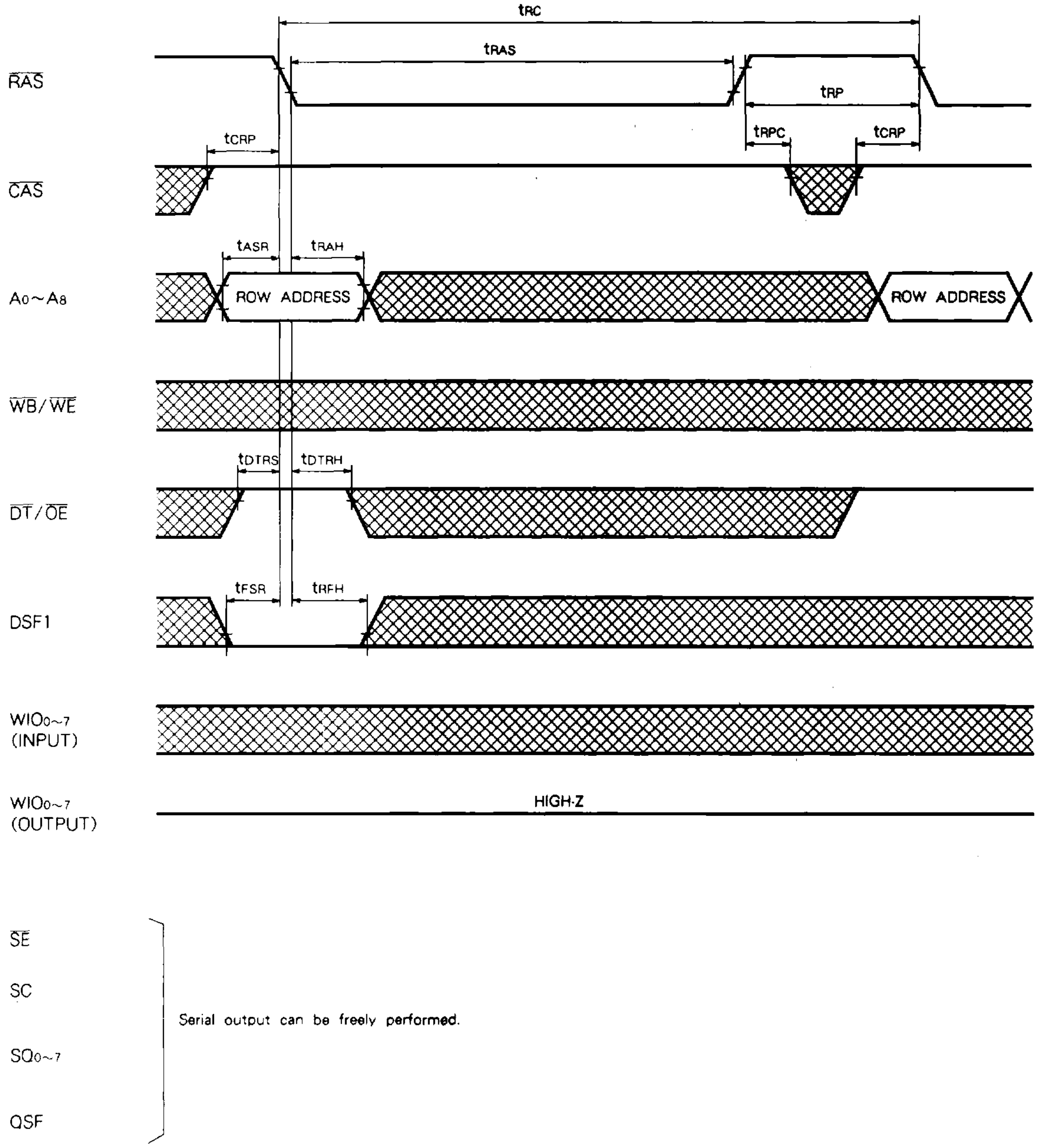


MITSUBISHI ELECTRIC

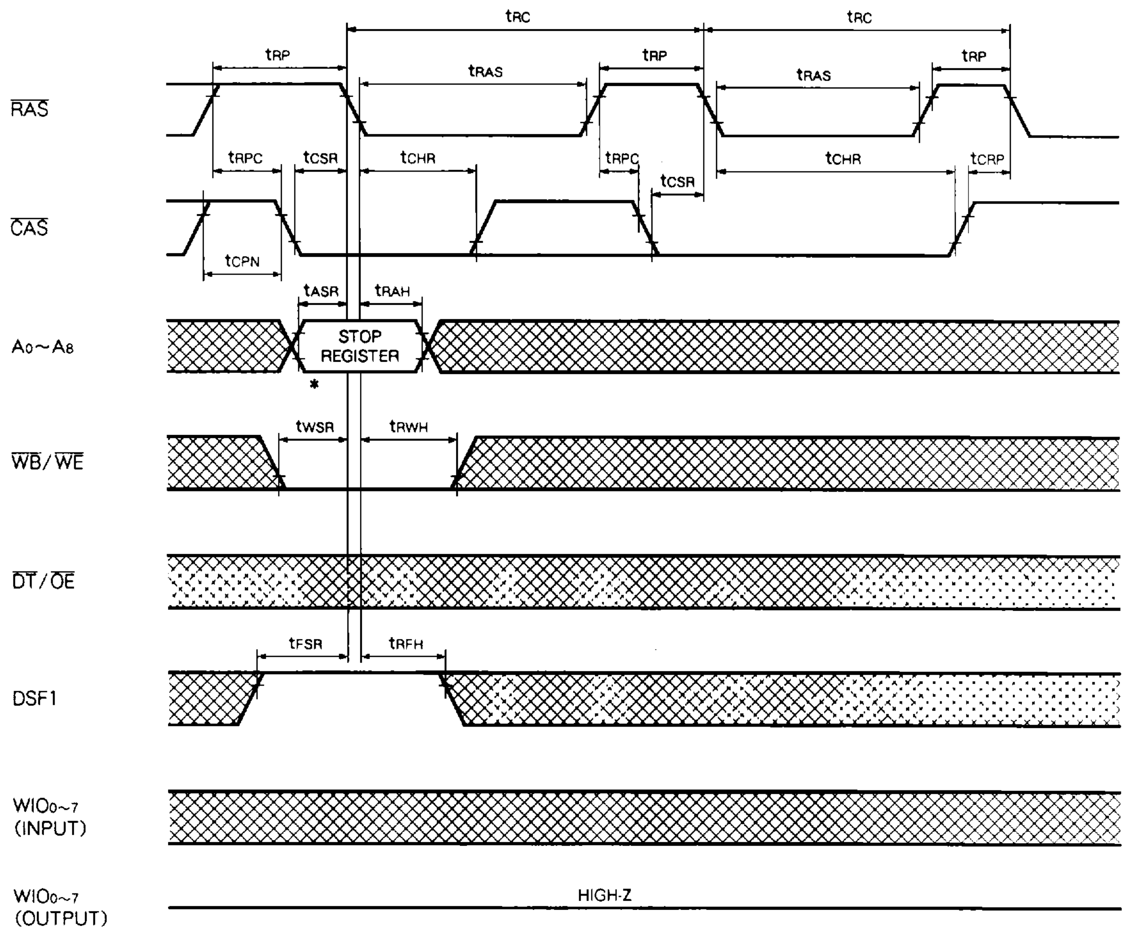
Hyper Page Mode Write Cycle (Read-Modify-Write)



$\overline{RAS}$ Only Refresh Cycle



CAS before RAS Refresh Cycle / Stop Register Set (No Reset)

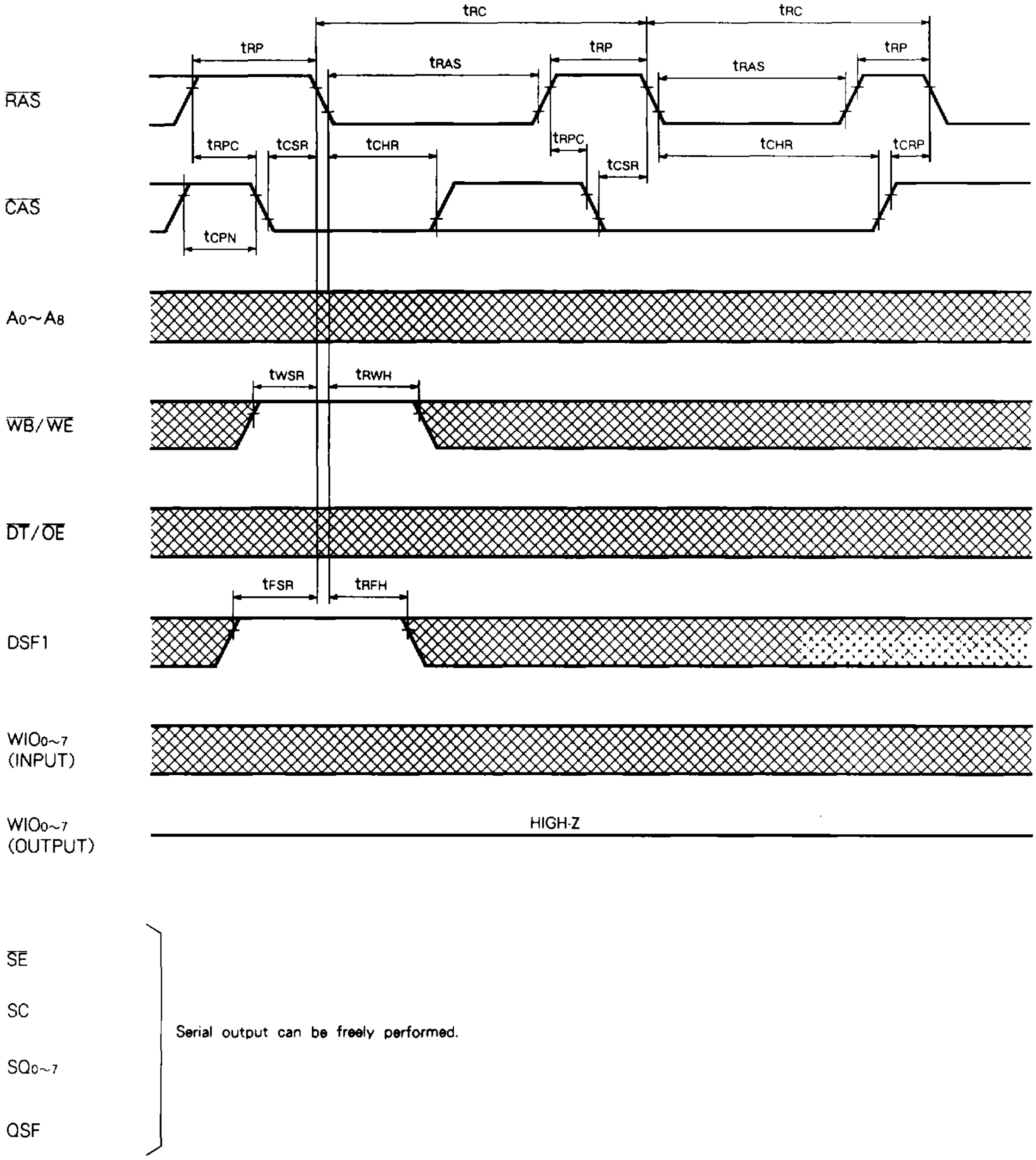


SE
SC
SQ0~7
QSF

Serial output can be freely performed.

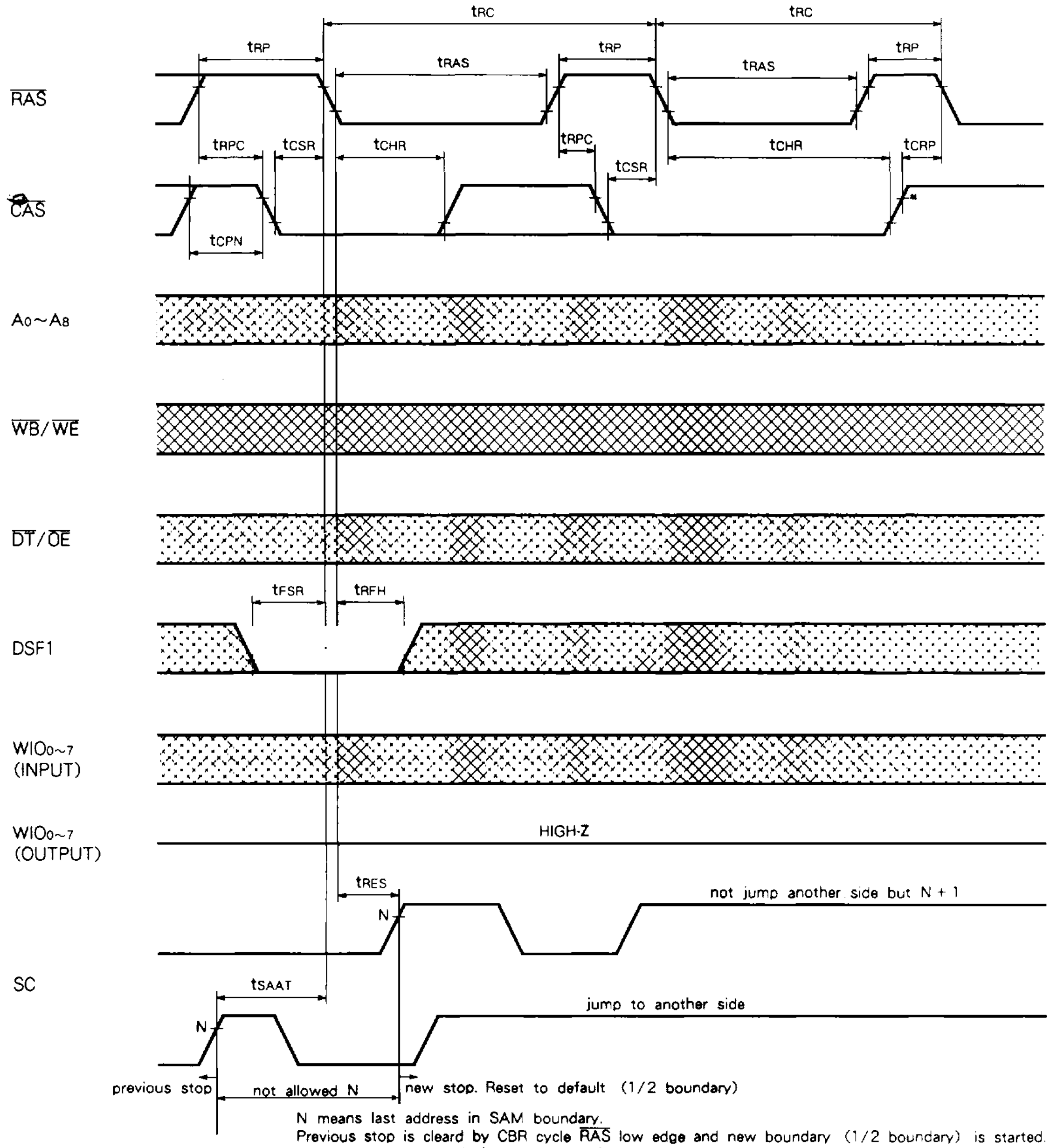
*A7	A6	A5	A4	divison	lower	upper
1	1	1	1	1/2		
0	1	1	1	1/4		
0	0	1	1	1/8		
0	0	0	1	1/16		
0	0	0	0	1/32		

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle / (No Reset)



MITSUBISHI ELECTRIC

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle / (Option Reset)



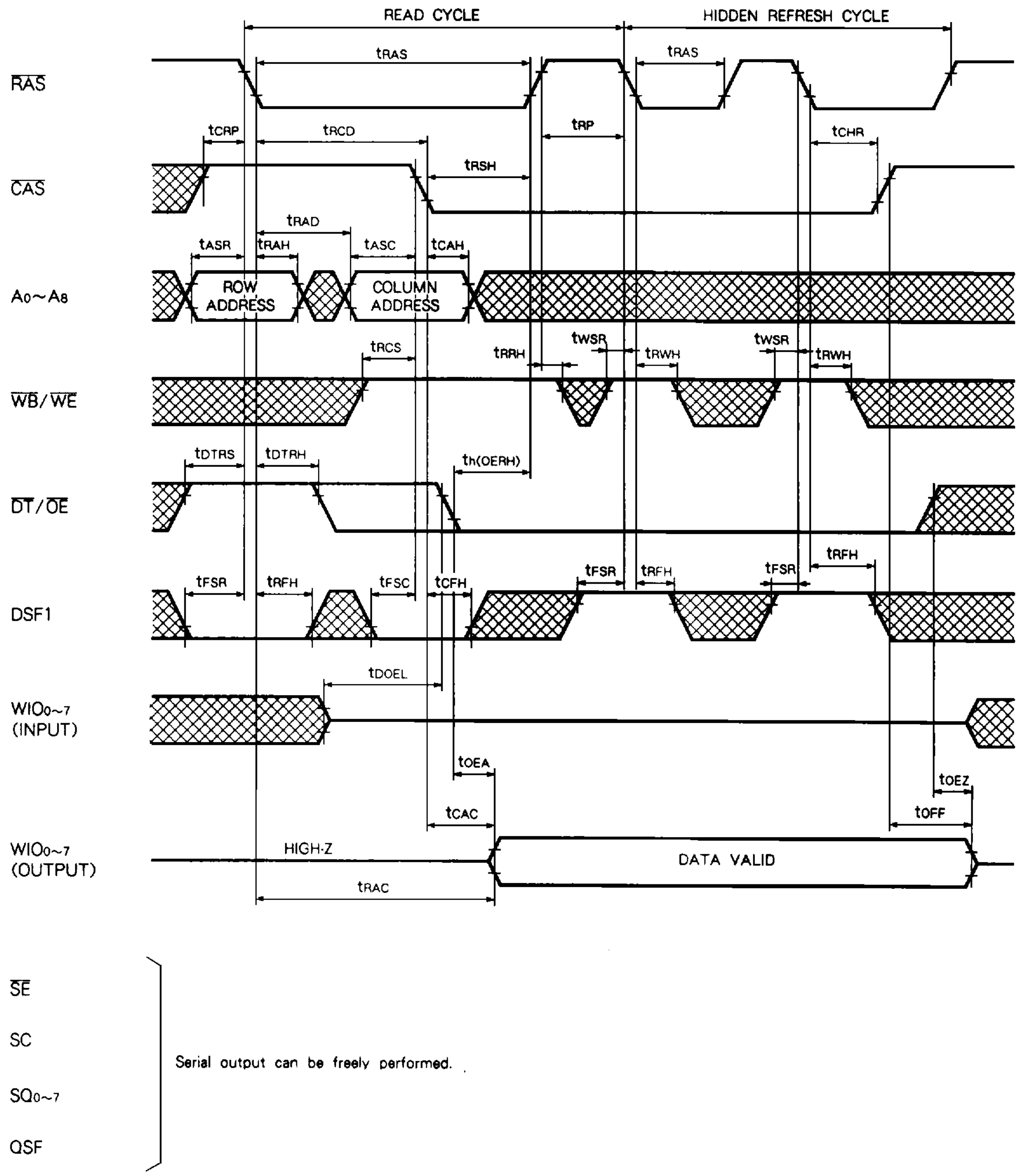
N means last address in SAM boundary.
Previous stop is cleard by CBR cycle $\overline{RAS}$ low edge and new boundary (1/2 boundary) is started.
If stop register value isn't changed by CBR cycle, Hidden Refresh cycle, tSAAT, tRES don't care for those cycles.

$\overline{SE}$

SQ0~7

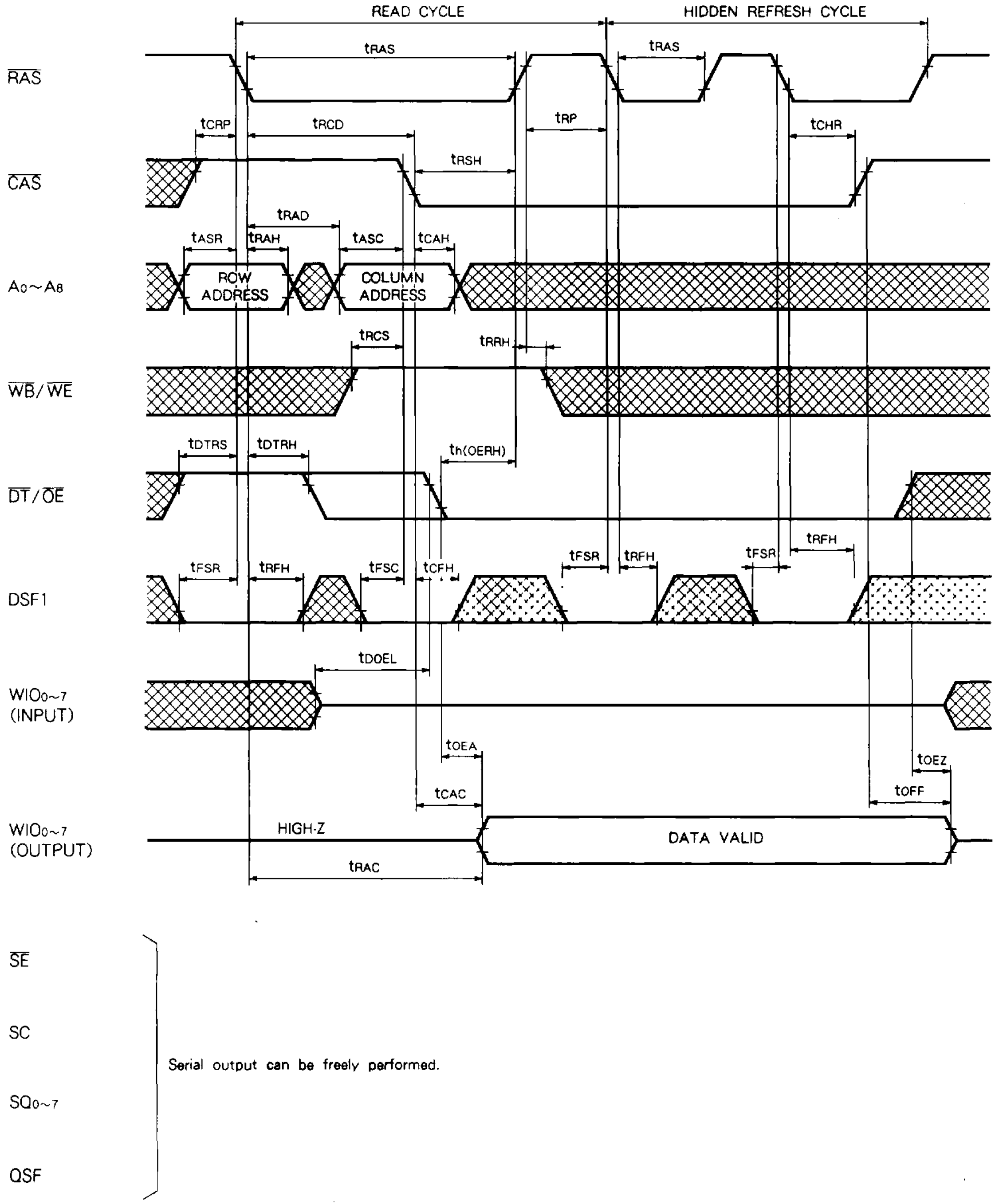
Serial output can be freely performed.

Hidden CBR Refresh Cycle / (No Reset)

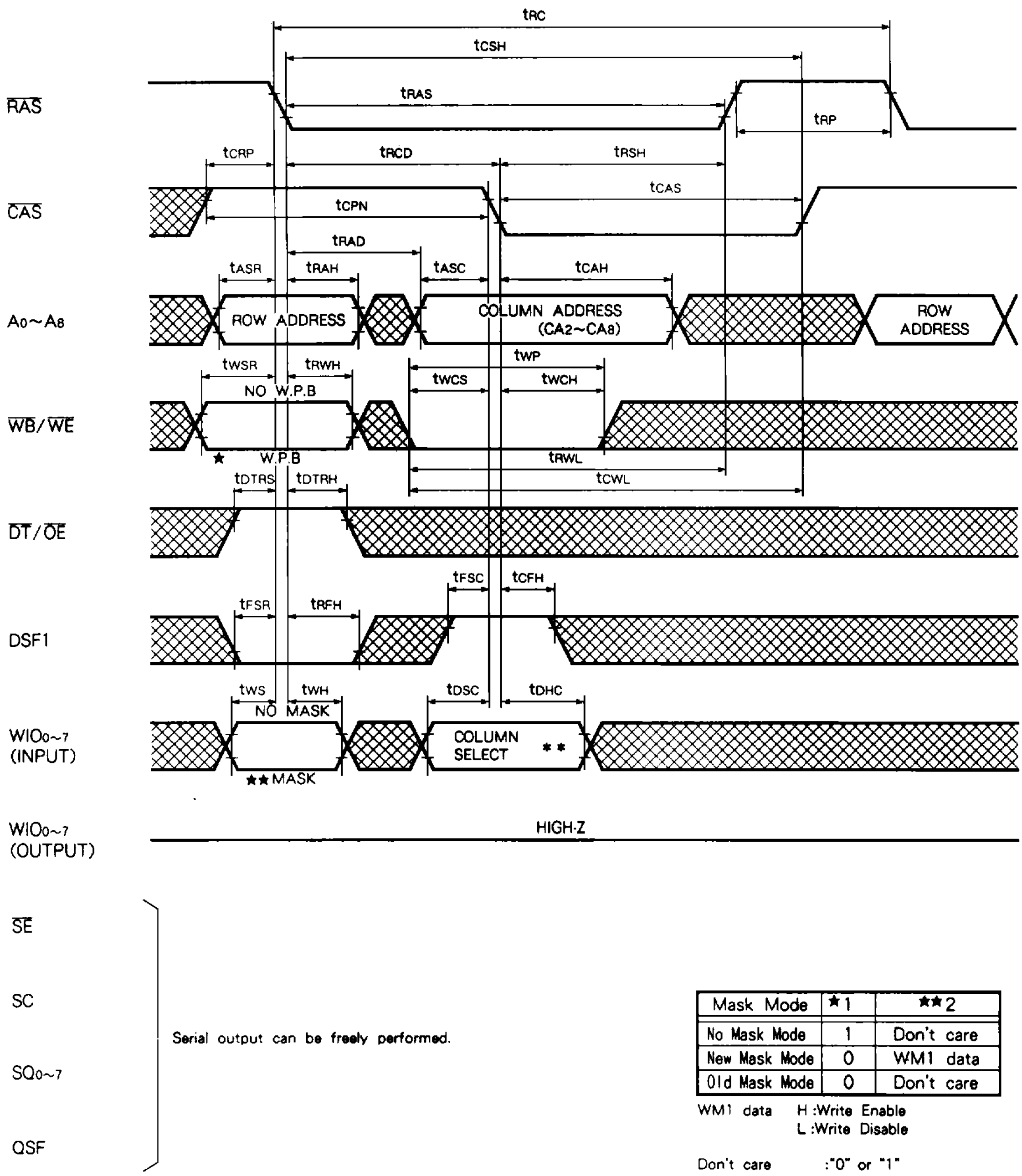


MITSUBISHI ELECTRIC

Hidden CBR Refresh Cycle / (Reset)



Block Write Cycle (Early write)



Mask Mode	★1	★★2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

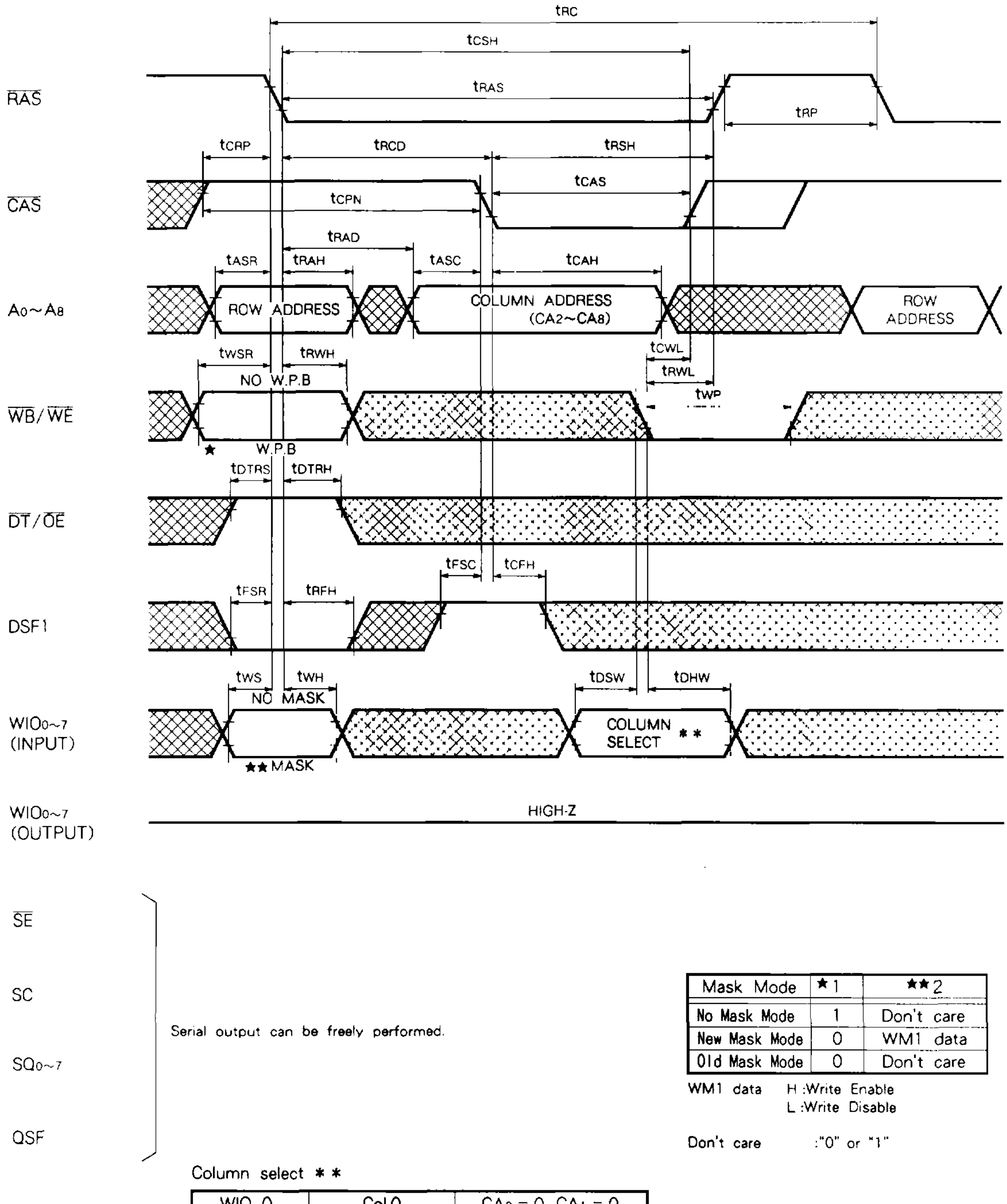
WM1 data H :Write Enable
L :Write Disable

Don't care :"0" or "1"

Column select ＊＊

WIO 0	Col-0	$CA_0 = 0$, $CA_1 = 0$
WIO 1	Col-1	$CA_0 = 1$, $CA_1 = 0$
WIO 2	Col-2	$CA_0 = 0$, $CA_1 = 1$
WIO 3	Col-3	$CA_0 = 1$, $CA_1 = 1$

Block Write Cycle (Late Write)



Mask Mode	★1	★★2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

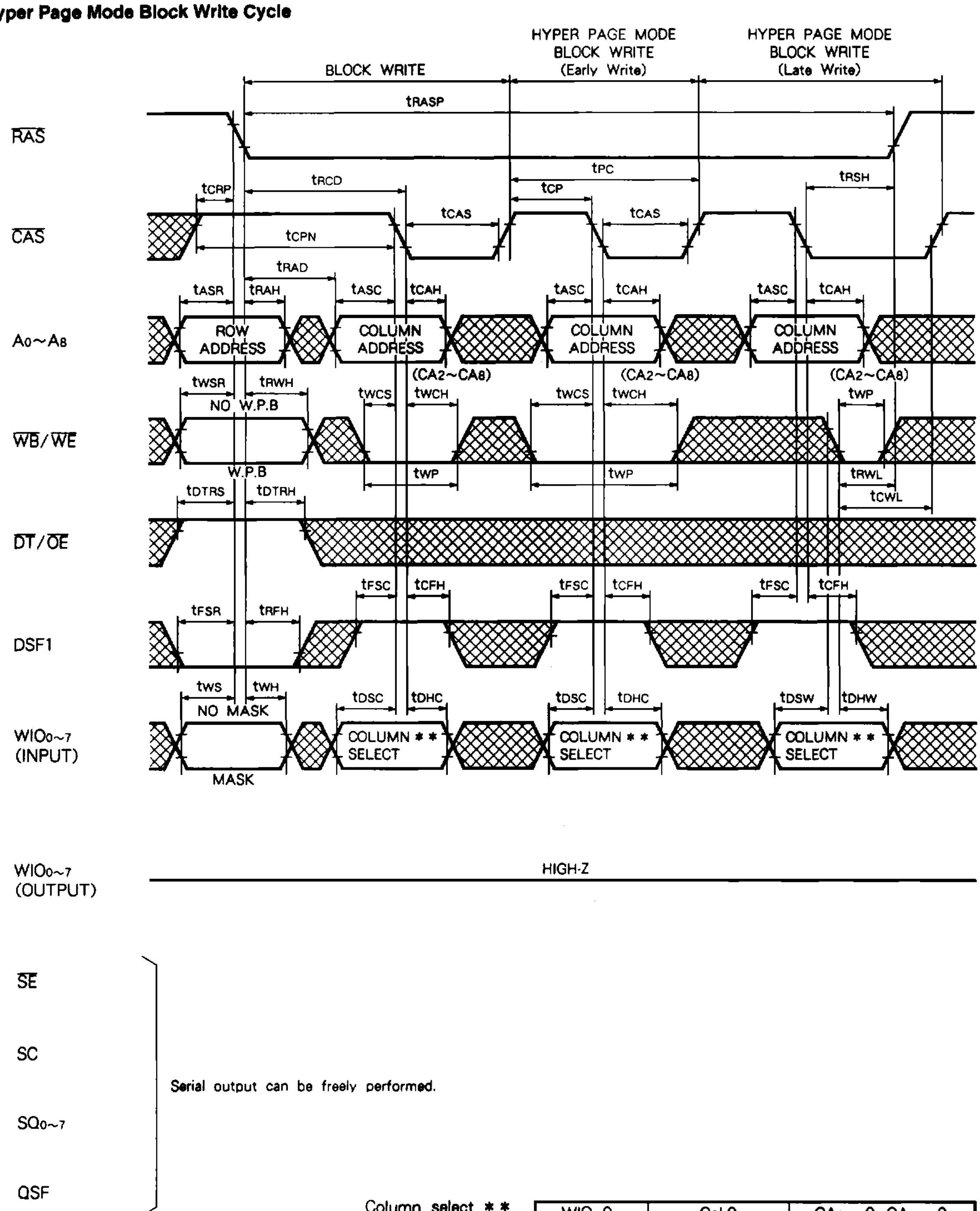
WM1 data H :Write Enable
L :Write Disable

Don't care :"0" or "1"

Column select ★★

WIO 0	Col-0	$CA_0 = 0, CA_1 = 0$
WIO 1	Col-1	$CA_0 = 1, CA_1 = 0$
WIO 2	Col-2	$CA_0 = 0, CA_1 = 1$
WIO 3	Col-3	$CA_0 = 1, CA_1 = 1$

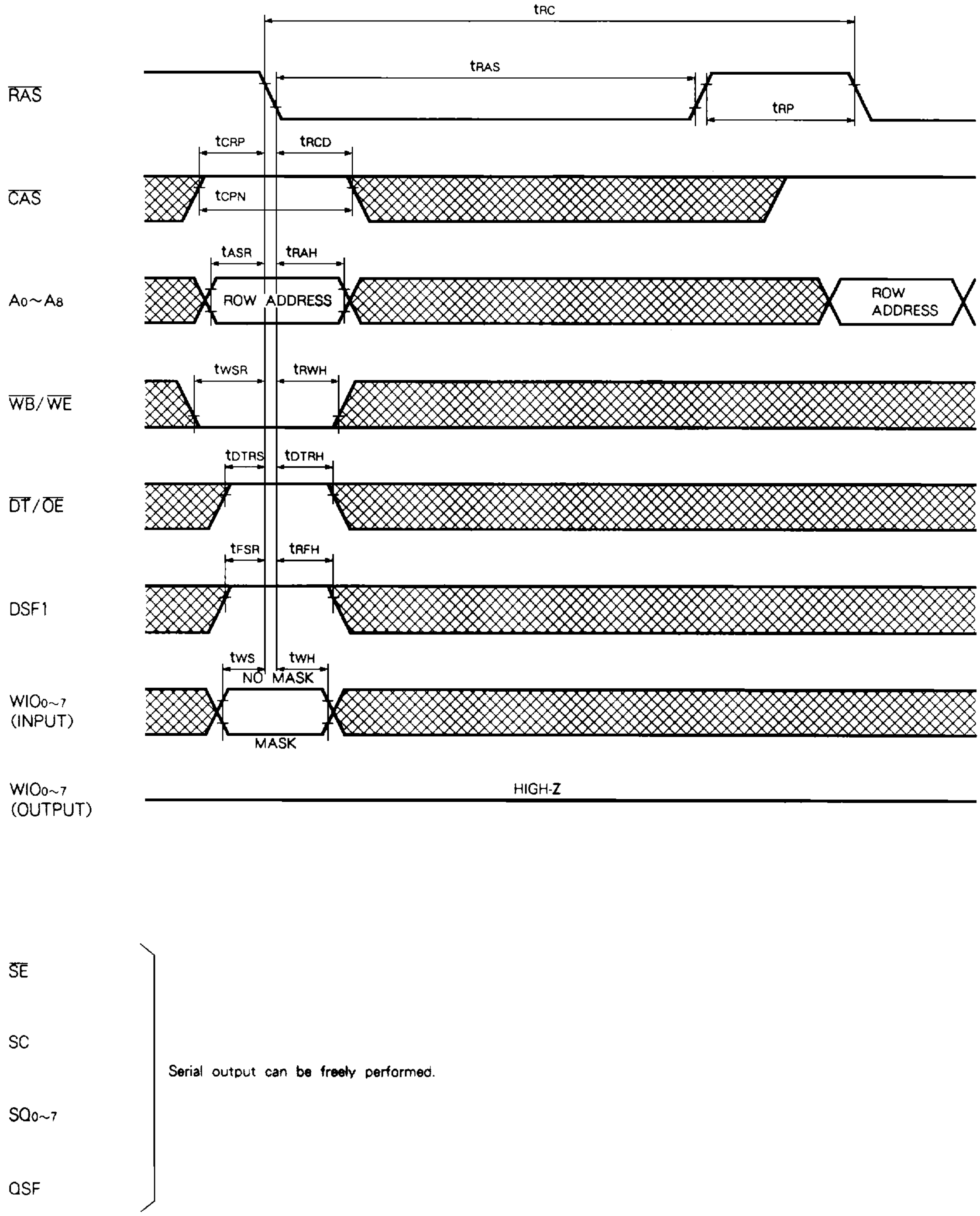
Hyper Page Mode Block Write Cycle



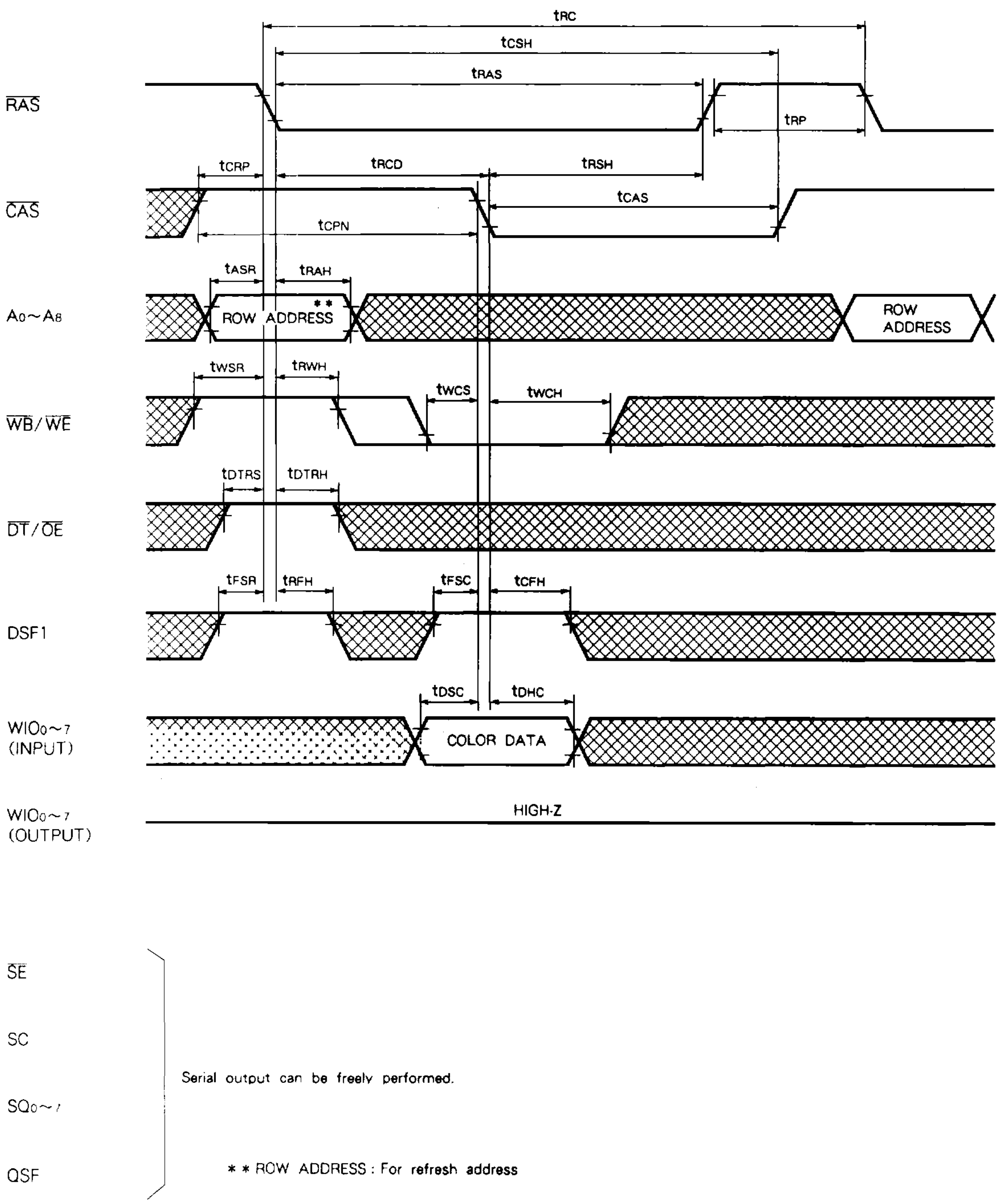
Column select * *

WIO 0	Col-0	$CA_0 = 0,\ CA_1 = 0$
WIO 1	Col-1	$CA_0 = 1,\ CA_1 = 0$
WIO 2	Col-2	$CA_0 = 0,\ CA_1 = 1$
WIO 3	Col-3	$CA_0 = 1,\ CA_1 = 1$

Flash Write Cycle

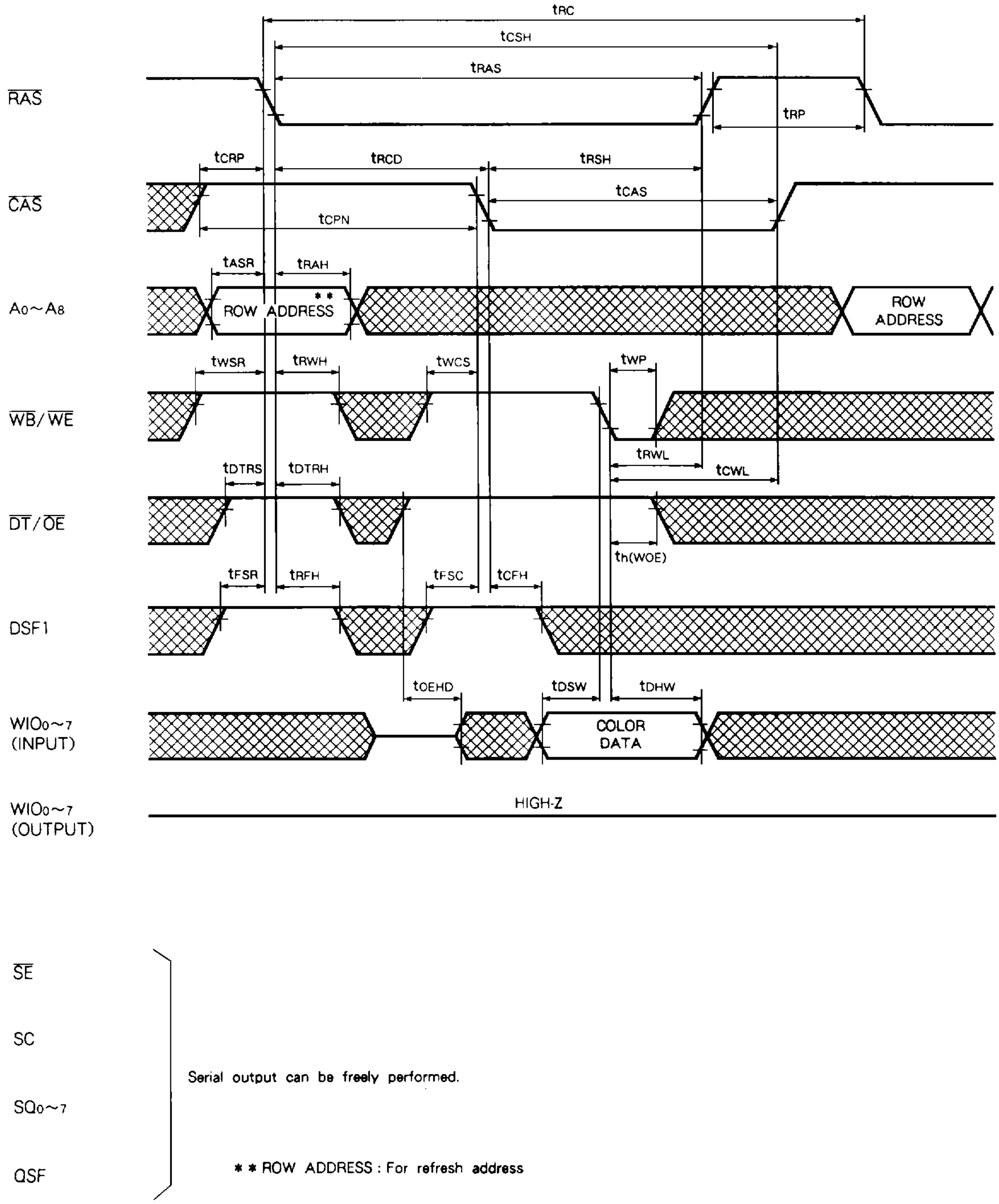


Load Color Register Cycle (Early Write)

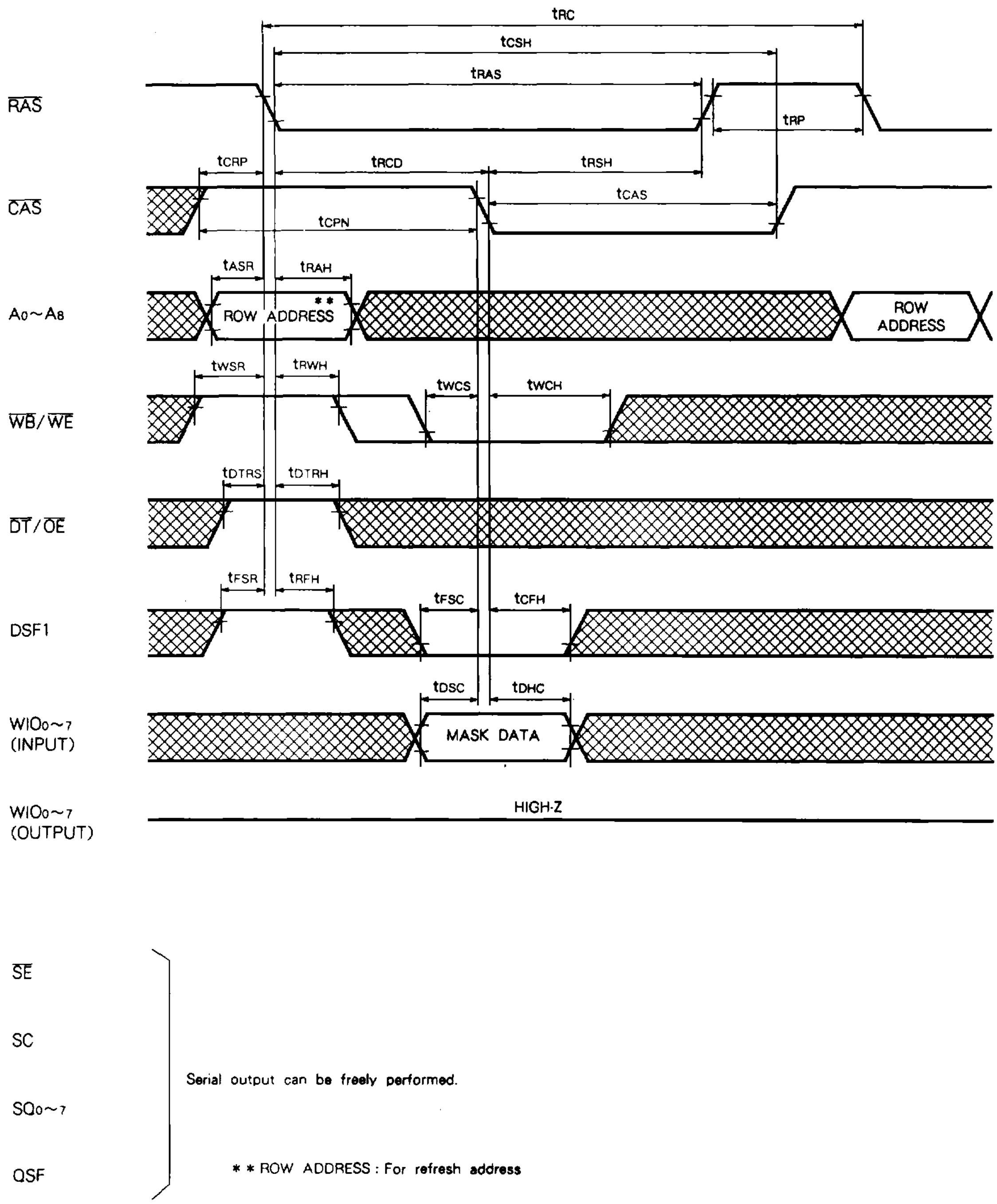


** ROW ADDRESS : For refresh address

Load Color Register Cycle (Late Write)

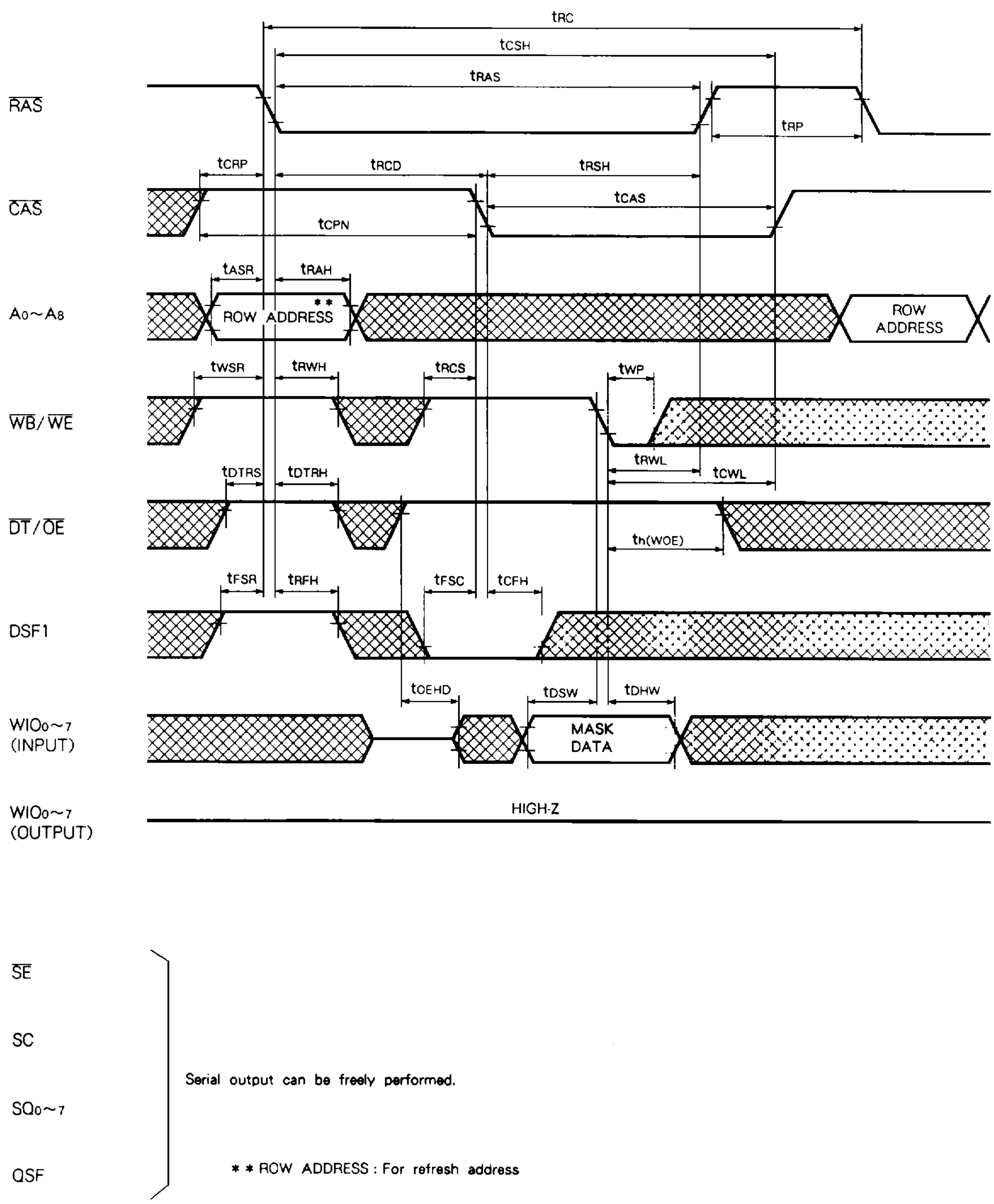


Load Mask Register Cycle (Early Write)



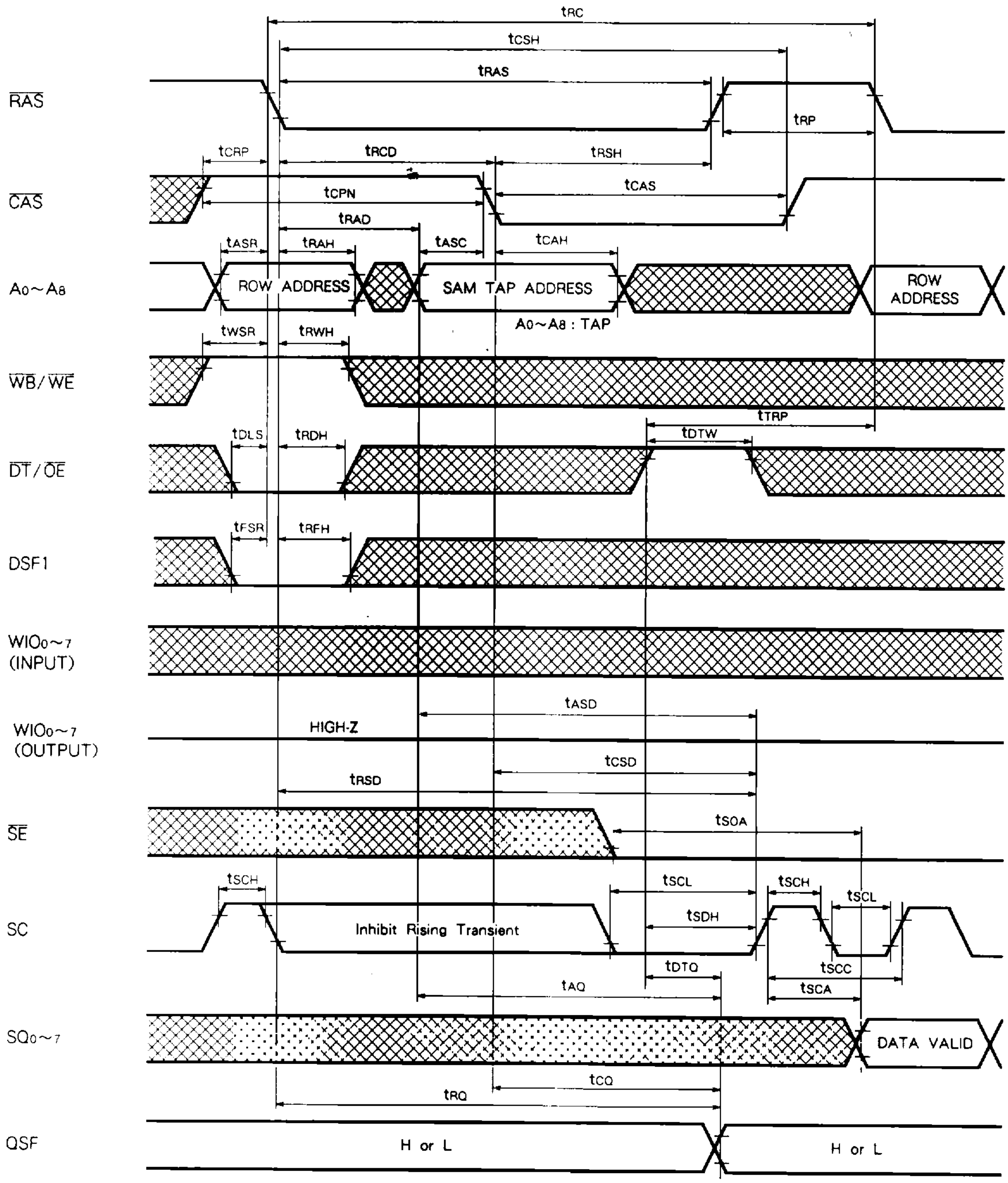
* * ROW ADDRESS : For refresh address

Load Mask Register Cycle (Late Write)

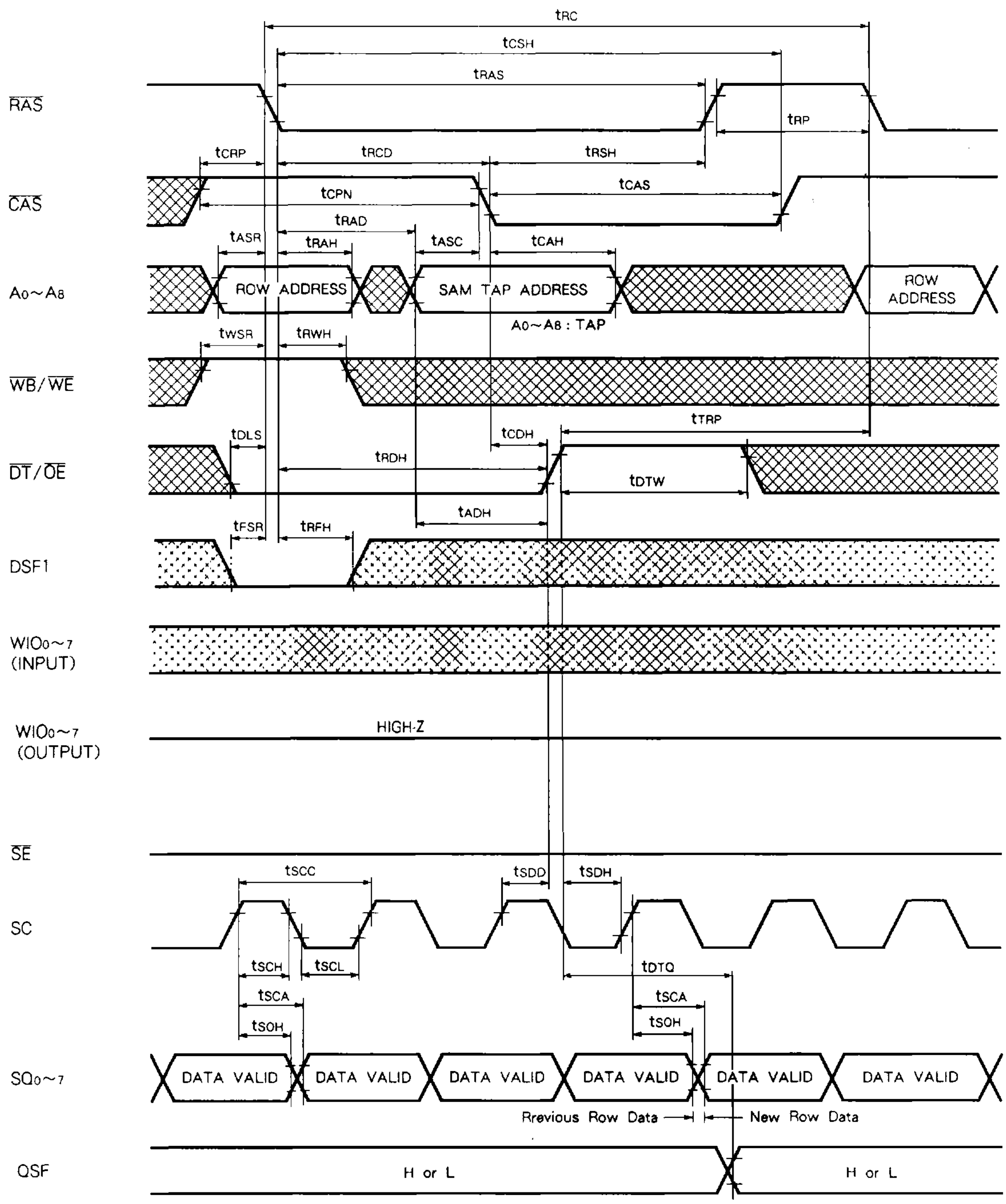


* * ROW ADDRESS : For refresh address

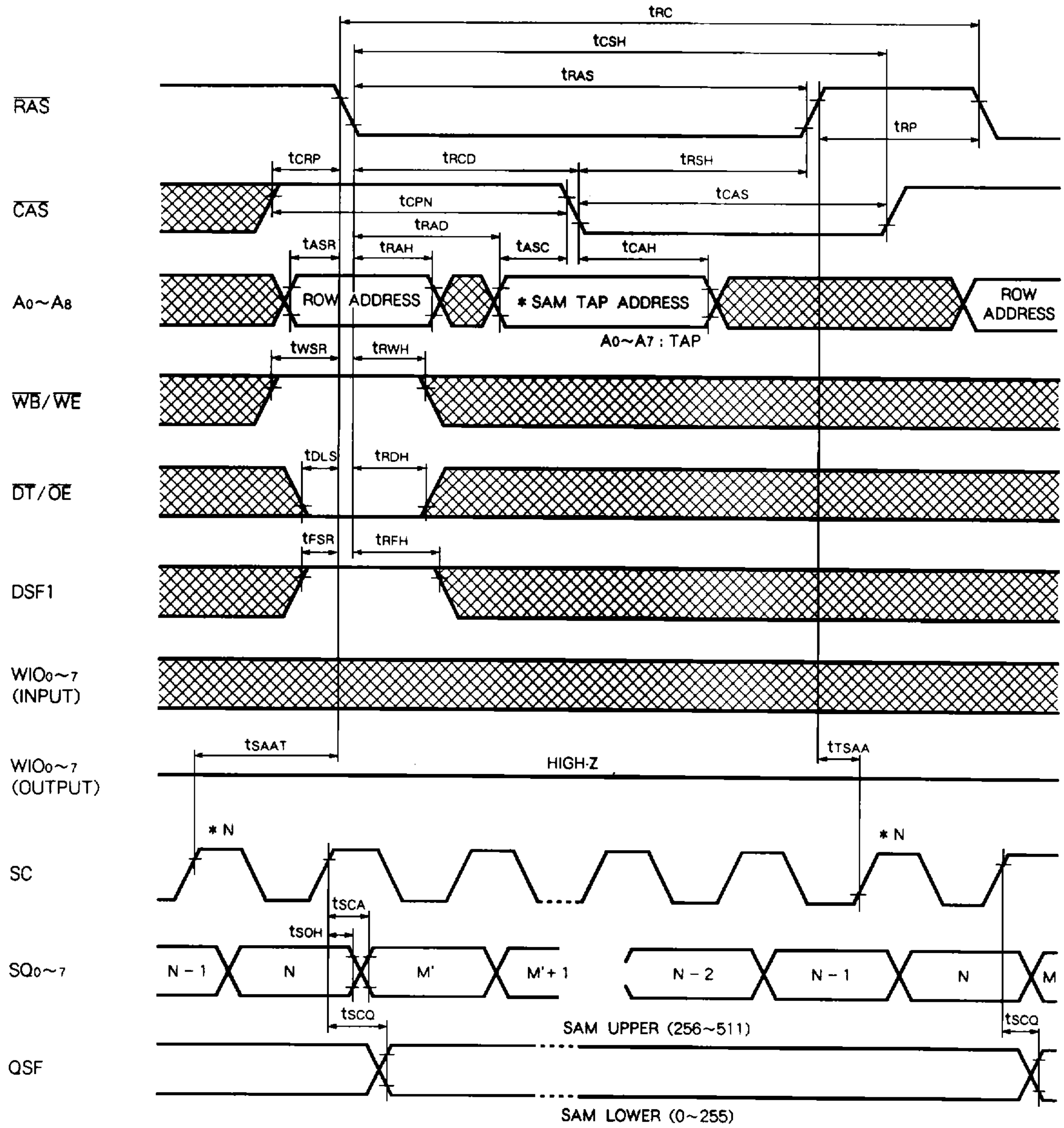
Read Transfer Cycle



Real Time Read Transfer

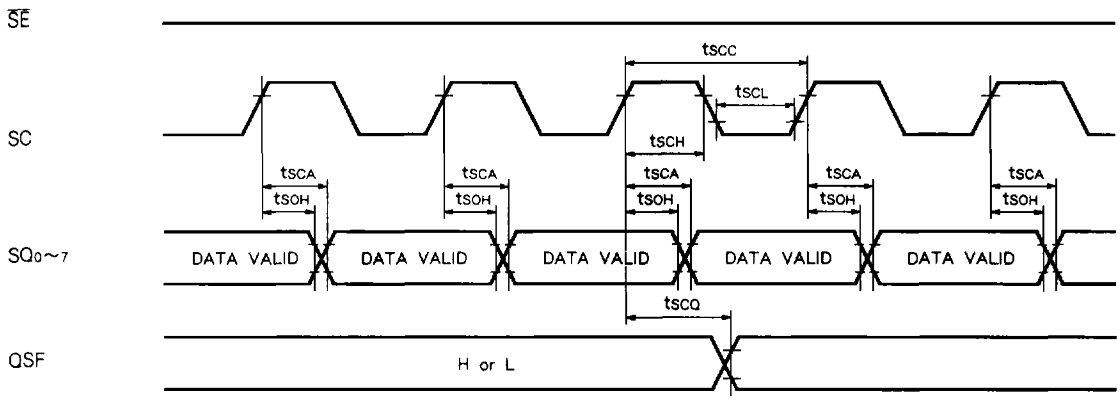


Split Read Transfer Cycle



* SAM TAP ADDRESS can not be set N
N means last address of boundary.
M means SAM TAP ADDRESS.

Serial Read Cycle ($\overline{SE}$=L)



Serial Read Cycle ($\overline{SE}$ Control)