HARRIS

HI-562A

12-Bit High Speed Monolithic Digital-to-Analog Converter

Features

- Output Current ..... 2mA, F.S.
- Monolithic Construction
- Extremely Fast Settling ..... 300ns To 0.01% (Typ)
- Low Gain Drift ..... ±10ppm/°C (Max)
- Linearity Guaranteed Over Temperature ... ±1/2 LSB (Max)
- Designed for Minimum Glitches
- Monotonic Over Temperature

Applications

- CRT Display Generation
- High Speed A/D Converters
- Video Signal Reconstruction
- Waveform Synthesizers
- High Speed Data Acquisition
- High-Rel Applications
- Precision Instruments

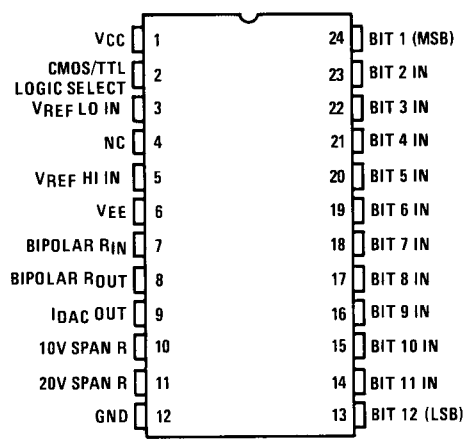
Description

The Harris HI-562A is the first monolithic digital-to-analog converter to combine both high speed performance and 12-bit accuracy on the same chip. The HI-562A's fast output current settling of 300ns to 0.01% is achieved using Dielectric Isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562A by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562A with guaranteed 12-bit linearity to within ±1/2LSB maximum at +25°C for -4 and -5 parts and to within ±1/4LSB maximum at +25°C for -2 and -8 parts. The HI-562A is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 3.3MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562A is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-562A is offered in commercial, industrial and military grades. The HI-562A is available in a 24 pin Ceramic Sidebraze DIP. For MIL-STD-883 compliant parts, request the HI-562A/883 data sheet.

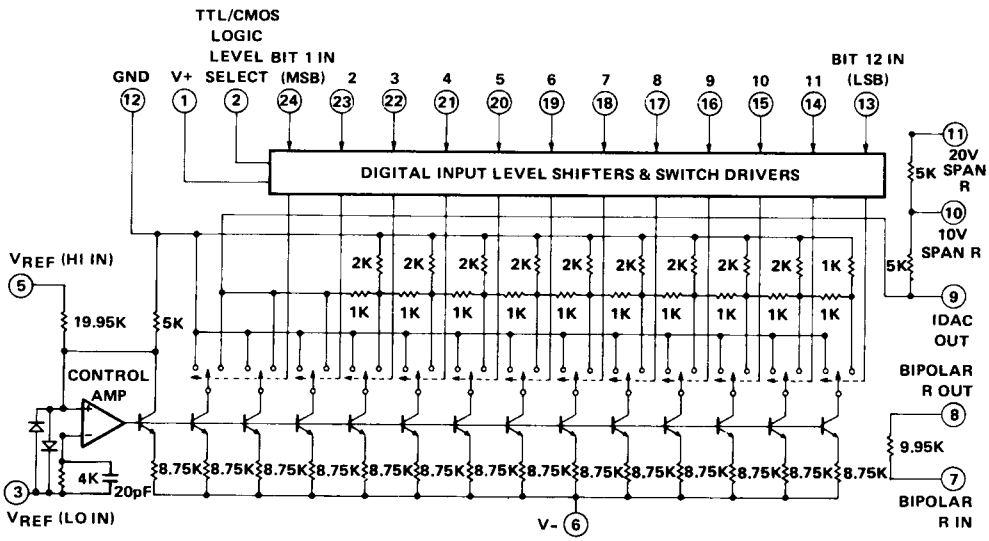
Pinouts

HI1-562A (CERAMIC SIDEBRAZE DIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC handling procedures.

Functional Diagram



NOTE: Pin Numbers Refer to DIP Package Only.

Specifications HI-562A

Absolute Maximum Ratings (Referred to GND, Note 1)

Power Supply Inputs
- V_{ps+} ..... +20V
- V_{ps-} ..... -20V

Reference Inputs
- V_{REF} (High) ..... ±16.5V

Digital Inputs
- Bits 1-12 (TTL) ..... -1V, +7.5V
- Bits 1-12 (CMOS) ..... -1V, V_{ps+}
- CMOS/TTL Logic Select ..... -1V, +16.5V

Outputs
- Pins 7, 8, 10, 11 ..... $\pm V_{ps}$
- Pin 9 ..... $+V_{ps}$, -5V

Junction Temperature ..... +175°C

Operating Temperature Range

HI-562A-2 ..... -55°C to +125°C
HI-562A-4 ..... -25°C to +85°C
HI-562A-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

(@ +25°C, V_{ps+} = +5V, V_{ps-} = -15V, V_{REF} = +10V, CMOS/TTL Logic Select = GND, Unless Otherwise Specified.)

PARAMETER	CONDITION	HI-562A-2 MIN	HI-562A-2 TYP	HI-562A-2 MAX	HI-562A-4/HI-562A-5 MIN	HI-562A-4/HI-562A-5 TYP	HI-562A-4/HI-562A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (Note 3)	Bit ON "Logic 1"							
TTL/CMOS Input Voltage (Note 2)	Bit OFF "Logic 0"							
Logic "1"		2.0			2.0			V
Logic "0"	(V_{ps+} <9.5V)			0.8			0.8	V
TTL/CMOS Input Current (Note 2)	Pin 2 Tied to Pin 12							
Logic "1"	Over Full Temperature Range		20	±500		20	±500	nA
Logic "0"			-50	-100		-50	-100	µA
CMOS Input Voltage								
Logic "1"		0.7V_{ps+}			0.7V_{ps+}			V
Logic "0"	Pin 2 Tied to Pin 1			0.3V_{ps+}			0.3V_{ps+}	V
CMOS Input Current	($V_{ps+} \geq$ +9.5V)							
Logic "1"	Over Full Temperature Range		20	±500		20	±500	nA
Logic "0"			-50	-100		50	-100	µA
Reference Input								
Input Resistance	(±20%)		19.95K			19.95K		Ω
Input Voltage			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Over Full Temperature Range			12			12	Bits
Nonlinearity (Note 3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over Full Temperature Range		±1/2	±1			±1	LSB
Differential Nonlinearity (Note 3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over Full Temperature Range		MONOTONICITY GUARANTEED					
Relative Accuracy (Note 6)	With 50Ω (1%) Resistors							
Gain Error	All Bits ON		±0.024	±0.25		±0.024	±0.25	%FSR
Bipolar Offset Error	All Bits OFF		±0.024	±0.25		±0.024	±0.25	%FSR
Unipolar Offset Error	All Bits OFF		±0.012	±0.05		±0.012	±0.05	%FSR
								(Note 4)
Adjustment Range	See Operating Instructions							
Gain	With 100Ω Trim		±0.3			±0.3		%FSR
Bipolar Offset	Potentiometers		±0.6			±0.6		%FSR
Temperature Stability	Drift Specified With Internal Span Resistors For Volt. Output							
Gain Drift (Note 3)	Over Full Temperature Range		±6	±10			±10	ppm of FSR/°C
Offset Drift (Note 3)	Over Full Temperature Range							
Unipolar Offset	All Bits OFF			±2			±2	ppm of FSR/°C
Bipolar Offset	All Bits OFF			±4			±4	
Differential Nonlin.	Over Full Temperature Range		±1	±2		±1	±2	ppm of FSR/°C
Settling Time (Note 3) to ±1/2LSB	All Bits ON-to-OFF or OFF-to-ON		300	400		300	400	ns

Electrical Specifications (Continued)

PARAMETER	CONDITIONS	HI-562A-2			HI-562A-4/HI-562A-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Major Carry Transient								
Peak Amplitude Settling	From 011...1 to 100...0		0.7			0.7		mA
Time to 90% Complete	or 100...0 to 011...1		35			35		ns
Power Supply Sensitivity (Note 3)								
Unipolar Offset								
V_{ps+} @ +5V or +15V	All Bits OFF		±0.5			±0.5		ppm of
V_{ps-} @ -15V	"		±0.5			±0.5		FSR/
Bipolar Offset								%V_{ps}
V_{ps+} @ +5V or +15V	All Bits OFF, Bipolar Mode		±1.5			±1.5		ppm of
V_{ps-} @ -15V	"		±1.5			±1.5		FSR/
Gain								%V_{ps}
V_{ps+} @ +5V or +15V	All Bits ON			±3.5			±3.5	ppm of
V_{ps-} @ -15V				±7.5			±7.5	FSR/
								%V_{ps}
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar		-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar		±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance			2K			2K		Ω
Capacitance			20			20		pF
Output Voltage Ranges								
Unipolar	Using External Op Amp		0 to +5			0 to +5		V
	and Internal Scaling Resistors.		0 to +10			0 to +10		V
Bipolar	See Figure 1 and Table 1		±2.5			±2.5		V
	For Connections		±5			±5		V
			±10			±10		V
Compliance Limit (Note 3)		-3		+10	-3		+10	V
Compliance Voltage (Note 3)	Over Full Temperature Range		±1.0			±1.0		V
Output Noise	0.1 to 10Hz (All Bits ON)		30			30		μV_{p-p}
	0.1 to 5MHz (All Bits ON)		100			100		μV_{p-p}
POWER REQUIREMENTS								
V_{ps+} (Note 7)	Over Full Temperature Range	4.5	5	16.5	4.75	5	16.5	V
V_{ps-}	Over Full Temperature Range	-13.5	-15	-16.5	-13.5	-15	-16.5	V
I_{ps+} (Note 5)	All Bits ON or OFF in Either		8	15		8	15	mA
I_{ps-} (Note 5)	TTL or CMOS Mode (25°C)		16	23		16	23	mA
I_{ps+} (Note 5)	Same as Above Except		11	20		11	20	mA
I_{ps-} (Note 5)	Over Full Temperature Range		20	30		20	30	mA
Power Dissipation (25°C)	V_{ps+} = +5V, V_{ps-} = -15V		280	420		280	420	mW

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{ps+} tolerance is ±10% for HI-562A-2, and ±5% for HI-562A-4, -5.
3. See Definitions.
4. FSR is "Full Scale Range" and is 20V for ±10V ranges, 10V for ±5V ranges, etc., or 2mA (±20%) for current output.
5. After 30 seconds warm-up.
6. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R1 and R2. Errors are adjustable to zero using R1 and R2 potentiometers. (See Operating Instructions Figure 2.)
7. The HI-562A is designed for V_{ps+} = 5V, but +4.5V ≤ V_{ps+} ≤ 16.5V may be connected if convenient (For V_{ps+} above +5V, there is an increase in power dissipation but little change in performance.)

Die Characteristics

Transistor Count	150	
Die Dimensions	103 x 209 mils	
Thermal Impedance (°C/W)	θ_{ja}	θ_{jc}
Sidebraze DIP	50	15
Ceramic LCC	81	40
Tie Substrate to	V_{REF} Low (Analog Ground)	
Process	Bipolar-DI	

Definitions of Specifications

Digital Inputs

The HI-562A accepts digital input codes in binary format and may be user connected for any one of three binary codes: Straight Binary, Two's Complement, or Offset Binary (see Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	1/2 FS	Zero	-FS
111...111	+FS - 1 LSB	+FS - 1 LSB	1/2 FS - 1 LSB
011...111	1/2 FS - 1 LSB	Zero - 1 LSB	+FS - 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

Accuracy

INTEGRAL NONLINEARITY — The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY — The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY — The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

Drift

GAIN DRIFT — The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Gain error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25^{o}C) and low (+25^{o}C - T_L) ranges by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT — The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Offset error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25^{o}C) and low (+25^{o}C - T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%Vps).

Compliance

Compliance Voltage is the maximum output range for which specified accuracy limits are guaranteed. Compliance Limit implies functional operation only and makes no claims to accuracy.

Glitch

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Operating Instructions

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-562A (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

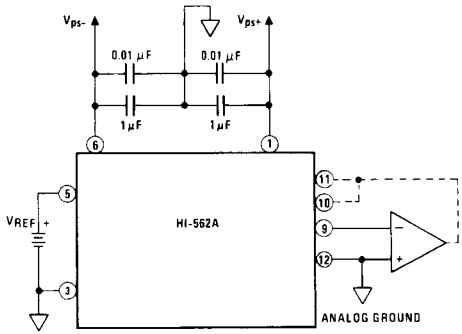
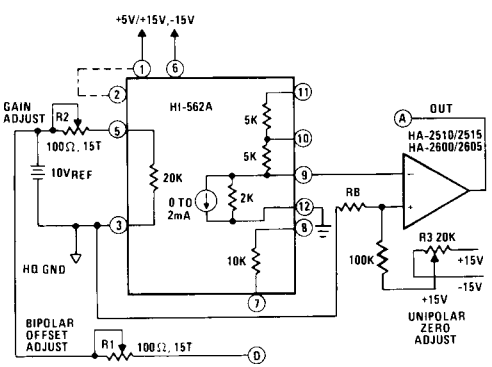


FIGURE 1.

Unipolar and Bipolar Voltage Output Connections

CONNECTIONS — Using an external resistive load, the output compliance should not exceed ±1V to maintain specified accuracy. For higher output voltages, accuracy can be maintained by using an external op amp and the internal span resistors as shown in Figure 2 and defined in Table 1 for unipolar and bipolar modes.



*For TTL and DTL compatibility, connect +5V to pin 1 and tie pin 2 to pin 12. For CMOS compatibility, connect digital power supply (9.5V ≤ VDD ≤ +12V) to pin 1 and short pin 2 to pin 1.

**Bias resistor, RB, should be chosen to equalize op amp offset voltage due to bias current. Its value is calculated from the parallel combination of the current source output resistance (2K) and the op amp feedback resistor. See Table 1 for values of RB.

FIGURE 2.

TABLE 1.

	CONNECTIONS					
	OUTPUT RANGE	PIN 7 TO	PIN 8 TO	PIN 10 TO	PIN 11 TO	BIAS (RB) RESISTOR
Unipolar Mode	0 to +10V	NC	NC	A	NC	1.43K
	0 to +5V	NC	NC	A	9	1.11K
Bipolar Mode	±10V	D	9	NC	A	760Ω
	±5V	D	9	A	NC	840Ω
	±2.5V	D	9	A	9	766Ω

External Gain and Zero Calibration (See Figure 2)

The input reference resistor (20K nominal) and bipolar offset resistors shown in Figure 2 are both intentionally set low by 50Ω to allow the user to externally trim-out initial errors to a very high degree of precision. The adjustments are made in the voltage output mode using an external op amp as current-to-voltage converter and the HI-562A internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. For best accuracy over temperature, select an op amp that has good front-end temperature coefficients such as the HA-2600/2605 with offset voltage and offset current tempco's of 5µV/°C in 1nA/°C, respectively. For high speed voltage mode applications where fast settling is required, the HA-2510/2515 is recommended for better than 1.5µs settling to 0.01%. Using either one, potentiometer R3 conveniently nulls unipolar offset plus op amp offset in one operation (for HA-2510/2515 and HA-2600/2605 use R3 = 20K and 100K, respectively). For bipolar mode operation, R3 should be used to null op amp offset to optimize its tempco (i.e., short 9 to A and adjust R3 for zero before calibrating in bipolar mode). The gain and bipolar offset adjustment range using 100Ω potentiometers is ±12 LSB and ±25 LSB, respectively. If desired, the potentiometers can be replaced with fixed 50Ω (1%) resistors resulting in an initial gain and bipolar offset accuracy of typically ±1/2 LSB.

UNIPOLAR CALIBRATION

Step 1: Unipolar Offset
- Turn all bits OFF
- Adjust R3 for zero volts output

Step 2: Gain
- Turn all bits ON
- Adjust R2 for an output of FS - 1 LSB
  That is, adjust for:
  9.9976V for 0V to +10V range
  4.9988V for 0V to +5V range

BIPOLAR CALIBRATION

Step 1: Bipolar Offset
- Turn all bits OFF
- Adjust R1 for an output of:
  -10V for ±10V range
  -5V for ±5V range
  -2.5V for ±2.5V range

Step 2: Gain
- Turn bit 1 (MSB) ON; all other bits OFF
- Adjust R2 for zero volts output