D2744, MARCH 1983 – REVISED DECEMBER 1989

- **Each Device Drives 32 Electrodes**
- **60-V Output Voltage Swing Capability**
- **15-mA Output Source and Sink Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **Totem-Pole Outputs**
- **Latches on All Driver Outputs**

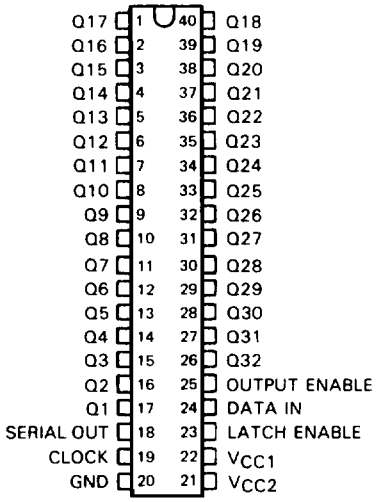
description

The SN65553, SN65554, SN75553, and SN75554 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN65554 and SN75554 output sequence is reversed from the SN65553 and SN75553 for ease in printed circuit board layout.

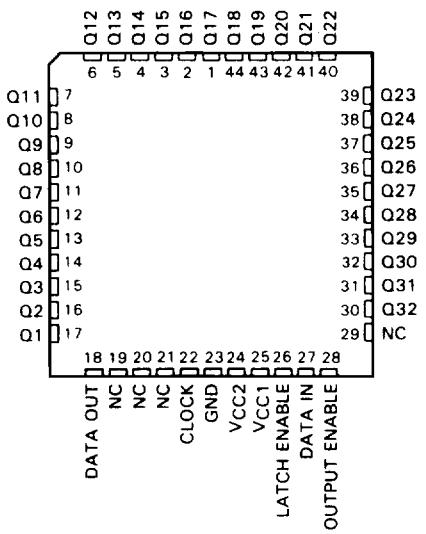
The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 32 latches. When OUTPUT ENABLE is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or OUTPUT ENABLE.

The SN65553 and SN65554 are characterized for operation from −40°C to 85°C. The SN75553 and SN75554 are characterized for operation from 0°C to 70°C.

N PACKAGE
(TOP VIEW)
SN65553, SN75553



FN PACKAGE
(TOP VIEW)
SN65553, SN75553



NC – No internal connection

†BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip – patented process.

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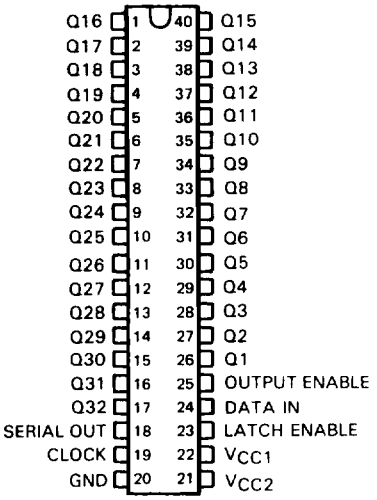
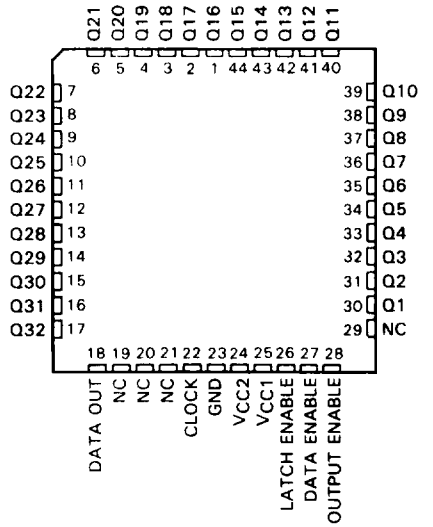
N PACKAGE
(TOP VIEW)
SN65554, SN75554



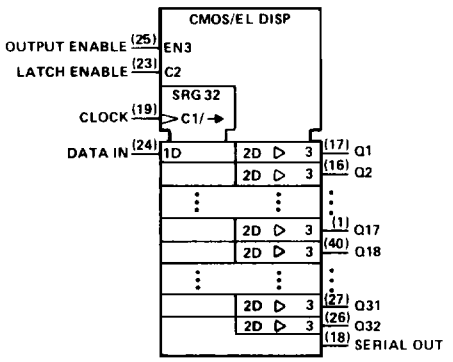
FN PACKAGE
(TOP VIEW)
SN65554, SN75554



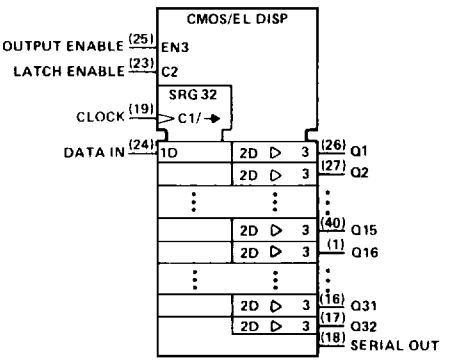
NC--No internal connection

logic symbols†

SN65553, SN75553

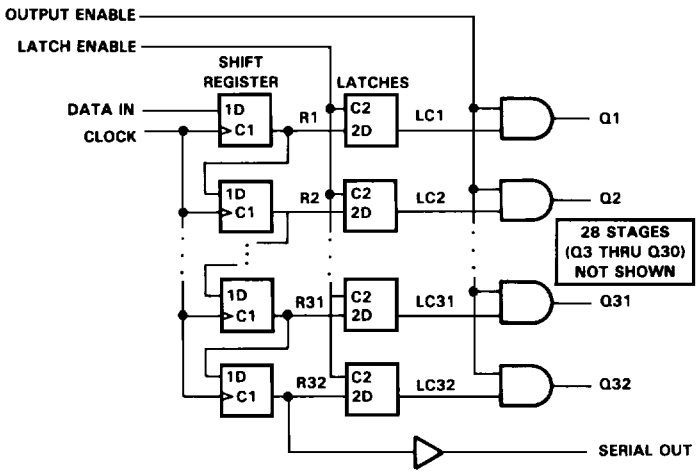


SN65554, SN75554



†These symbols are in accordance with ANSI/IEEE Std 91 1984 and IEC Publication 617-12.
Pin numbers shown are for N packages.

logic diagram (positive logic)

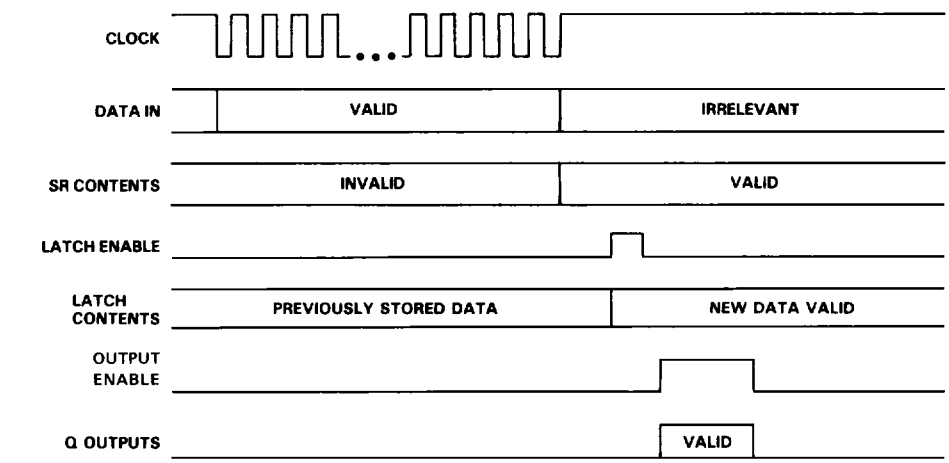


FUNCTION TABLE

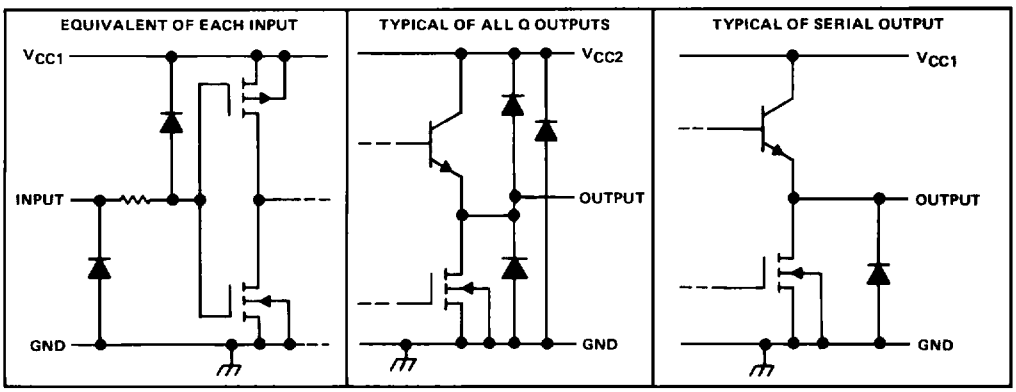
FUNCTION	CONTROL INPUTS			SHIFT REGISTER	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE	R1 THRU R32	LC1 THRU LC32	SERIAL	Q1 THRU Q22
LOAD	↑	X	X	Load and shift†	Determined by	R32	Determined by
	Not↑	X	X	No change	LATCH ENABLE‡	R32	OUTPUT ENABLE
LATCH	X	L	X	As determined	Stored data	R32	Determined by
	X	H	X	above	New data	R32	OUTPUT ENABLE
OUTPUT	X	X	L	As determined	Determined by	R32	All L
ENABLE	X	X	H	above	LATCH ENABLE‡	R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . .R2 takes on the state of R1, and R1 takes on the state of the data input.
‡New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1} + 0.3 V
Ground current . . . . . 700 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65553, SN65554 . . . . . −40°C to 85°C
SN75553, SN75554 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	15	V
Supply voltage, V_{CC2}		0		60	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC1} = 10.8 V	8.1		11.1	V
	V_{CC1} = 15 V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)	V_{CC1} = 10.8 V	−0.3		2.7	V
	V_{CC1} = 15 V	−0.3		3.75	
High-level output current, I_{OH}		−15			mA
Low-level output current, I_{OL}		15			mA
Output clamp current, I_{OK}				20	mA
Clock frequency, f_{clock}		0		6.25	MHz
Pulse duration, CLOCK high or low, $t_{w(CLK)}$ (see Figure 2)		80			ns
Pulse duration, LATCH ENABLE, $t_{w(LE)}$ (see Figure 4)		80			ns
Data setup time before CLOCK ↑, t_{su} (see Figure 2)		20			ns
Data hold time after CLOCK ↑, t_h (see Figure 2)		80			ns
Operating free-air temperature, T_A	SN65553, SN65554	−40		85	°C
	SN75553, SN75554	0		70	

electrical characteristics over recommended ranges of V_{CC1} and operating free-air temperature, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	57		V
		SERIAL OUT	I_O = −100 μA	V_{CC1} − 1.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 15 mA		8	V
		SERIAL OUT	I_{OL} = 100 μA		1	
I_{IH}	High-level input current		$V_I = V_{CC1}$		1	μA
I_{IL}	Low-level input current		V_I = 0		−1	μA
I_{CC1}	Supply current from V_{CC1}				5	mA
I_{CC2}	Supply current from V_{CC2}	SN65553, SN65554			12	mA
		SN75553, SN75554			10	

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level SERIAL OUT from CLOCK	C_L = 20 pF to ground, See Figure 3		140	ns
t_{PLH}	Propagation delay time, low-to-high-level SERIAL OUT from CLOCK			140	ns
t_{DHL}	Delay time, high-to-low-level Q output from LATCH ENABLE	C_L = 20 pF to ground, See Figure 4		500	ns
t_{DLH}	Delay time, low-to-high-level Q output from LATCH ENABLE	C_L = 20 pF to ground, See Figure 4		1	μs

RECOMMENDED OPERATION CONDITIONS

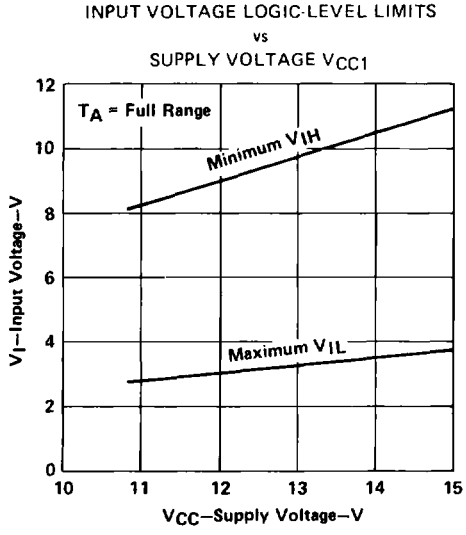

FIGURE 1

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PARAMETER MEASUREMENT INFORMATION

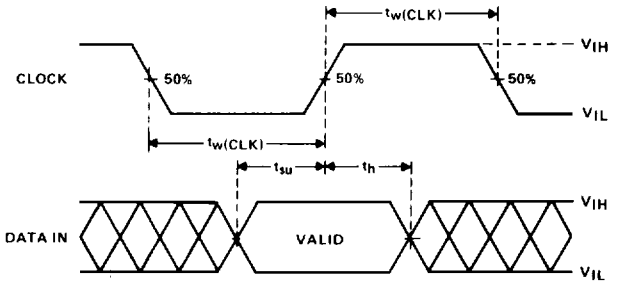

FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

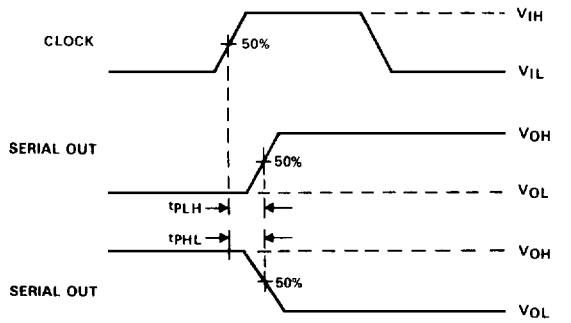

FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY CLOCK TO SERIAL OUTPUT

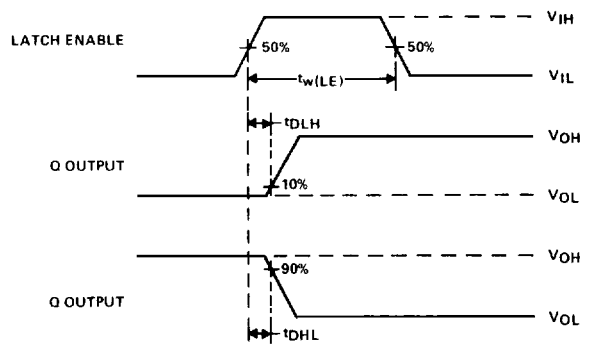

FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES, LATCH ENABLE TO Q OUTPUTS