Features

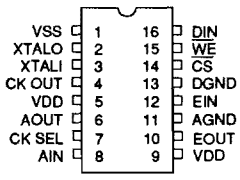
- High Accuracy Programmable Gain Amplifiers
  - ± 0.02 dB Accuracy (Typical)
  - 31.5 dB Range in 0.5 dB Steps
- Software Programmable Group Delay Equalizer For Leased and Dial-Up Lines
- High Dynamic Range - over 90 dB
- On-Chip Anti-Aliasing Filters
- On-Chip E^2PROM Configuration Code Memory
- Microcomputer Interface with Serial Data Port
- Three Convenient Clock Options
  - 11.0592 MHz
  - 3.6864 MHz
  - 2.4576 MHz (or 2.56 MHz)
- Operates from ± 5 V Supplies
- Low Power Standby Mode - 100 µA (Typical)
- TTL and CMOS Compatible Digital Interface
- Economical 16-Lead Package
- Full Military, Commercial and Industrial Temperature Ranges

CMOS E^2PROM Programmable Amplifier Delay Equalizer

Description

The AT76C10E integrates two Programmable Gain Amplifiers and a Programmable Telephone Line Group Delay Equalizer on a monolithic substrate. It is fabricated in a state-of-the-art, low power CMOS process. The Gain and Group Delay steps are controlled by a seven-bit configuration code which can be programmed in real time and can also be stored permanently in on-chip E^2PROMS. The AT76C10E is implemented in an advanced switched-capacitor technology and is designed to provide precise Gain and Group Delay compensation for low bit-error-rate data transmission over dial-up and leased lines. Anti-alias and clock filters are included on-chip as the AT76C10E employs sampled-data techniques, and external filters are not required for most applications.

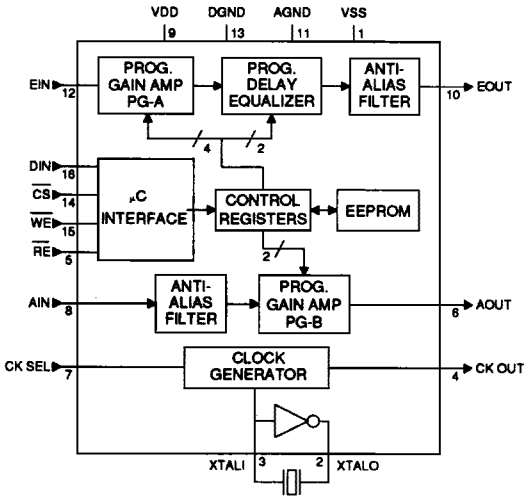
Pin Configuration



Pin Definitions

No.	Pin Name	Function
1	VSS	Negative Power Supply. Nominal -5 Volts.
2	XTALO	Crystal Oscillator Output.
3	XTALI	Crystal Oscillator Input.
4	CK OUT	Sampling Clock Output. (Open Drain)
5	$\overline{RE}$	Recall Enable Input. Loads Configuration into Control Registers from On-Chip E^2PROM.
6	AOUT	PG-B Analog Signal Output.
7	CK SEL	Clock Select. Selects one of the 3 recommended Clock frequencies.
8	AIN	PG-B Analog Signal Input.
9	VDD	Positive Power Supply. Nominal +5 Volts.
10	EOUT	Delay Equalizer Analog Signal Output.
11	AGND	Analog Ground.
12	EIN	Delay Equalizer Analog Signal Input.
13	DGND	Digital Ground.
14	$\overline{CS}$	Chip Select Control Input.
15	$\overline{WE}$	Write Enable Control Input.
16	DIN	Serial Data Input.

Block Diagram



Device Operation

The AT76C10E is designed for use in the signal paths of a modem or voice/data phone to minimize the bit-error-rate over dial-up and leased lines. Gain and Group Delay response of the AT76C10E are controlled by a serial seven-bit configuration code. D1 and D0 of the configuration code are the address bits which select one of the three control registers. Bits D2 to D5 set the gain and delay equalizer steps. D6 is an option bit which determines whether the configuration code will update one of the control registers only, or also be stored in on-chip non-volatile memory (E^2PROM) of the AT76C10E. All the functions associated with the configuration code are summarized in Tables 1 to 4.

Configuration Code Format

D6	D5	D4	D3	D2	D1	D0
Option Select	Control Code				Address	

This chip can be used as part of an adaptive equalizer for medium to high speed modems (1200 bps to greater than 19.2K bps). The configuration code is loaded into the chip at a serial data input port and updated in real time. It can also be stored permanently in on-chip E^2PROMS and updated periodically. The high performance Atmel E^2PROM process together with redundancy circuits allows over 10E6 write cycles. The amplitude response of the equalizer is nominally at 0 dB with negligible ripple. The AT76C10E can also be used as a fixed compromise delay equalizer.

PROGRAMMABLE GAIN AMPLIFIER: The AT76C10E provides two high dynamic range amplifiers for maximizing signal-to-noise ratio. Amplifier PG-A offers 16 programmable gain steps from 0 dB to 7.5 dB in 0.5 dB steps. Amplifier PG-B provides -8 to 16 dB of gain in 8 dB steps. The two amplifiers can be cascaded to provide 31.5 dB range of programmable gain in 0.5 dB steps. The Programmable Amplifiers can be used as an Automatic Gain Control Circuit or as a fixed gain adjustment.

PROGRAMMABLE GROUP DELAY EQUALIZER: The Group Delay Equalizer is designed to provide programmable compromise group delay compensation to achieve low bit-error-rate data transmission. Four group delay responses are provided to accommodate the majority of conditioned as well as unconditioned lines. The first three responses are recommended for line types C2 and C1, while the fourth response can be used for 3002-type lines. Two or more AT76C10Es can be cascaded to obtain additional group delay compensation.

CONTROL REGISTERS: Four control registers are used to store the configuration codes for the gain steps of PG-A and PG-B, the delay steps of the Delay Equalizer, and the control bit for the power-down mode. All the control bits, except the power down-bit, can also be programmed into on-chip non-volatile memories of the AT76C10E.

MICROCOMPUTER INTERFACE: Control inputs $\overline{CS}$, $\overline{WE}$, $\overline{RE}$ and serial data input DIN allow the AT76C10E to be easily interfaced with most popular microcontrollers. All digital I/Os are TTL as well as CMOS compatible. For stand alone operation, $\overline{CS}$ should be tied to VDD while $\overline{WE}$, $\overline{RE}$ and DIN should be tied to ground.

WRITE OPERATION: To program a configuration code into a particular control register, the voltage at $\overline{CS}$ has to be brought low while the data bits appearing at DIN are strobed in at the rising edge of $\overline{WE}$. At the rising edge of $\overline{CS}$, the last 7 input data bits are latched into the control registers. Therefore, if the first bit of an update byte is a "start bit," it will be ignored. If a "0" was inserted at D6 of the input code, the configuration code will also be immediately written into on-chip E^2PROM of the AT76C10E. As all timing signals and programming voltages are generated internally, writing the E^2PROM is transparent to the user. However, while the E^2PROM is being programmed, which takes 1.5 mS, any further attempt to initiate programming will be ignored until the first operation is completed.

RECALL OPERATION: A RECALL operation can be initiated any time during operation by bringing both $\overline{CS}$ and $\overline{RE}$ low simultaneously. The configuration codes which have been preprogrammed in the E^2PROM of the AT76C10E are loaded into the control registers.

POWER-DOWN MODE: To minimize power consumption for battery powered applications and in certain linecard applications, the AT76C10E provides a low power standby mode of operation. In the power-down mode, the analog outputs go into a high impedance state. The power-down mode is initiated by writing a "0" into the power-down register. Once in the power-down mode, the AT76C10E can be reactivated by writing a "1" into the power-down register or performing a RECALL operation. It should be noted that upon powering up the AT76C10E for the first time, it automatically goes into the normal active mode of operation.

CRYSTAL OSCILLATOR: Internal timing of the chip is generated either by connecting a crystal across pins XTALI and XTALO of the on-chip oscillator, or by applying an external clock at pin XTALI. In the latter case, pin XTALO should be left unconnected. To accommodate different applications, three clock options: 2.4576 MHz, 3.6864 MHz and 11.0592 MHz, can be selected via control pin CK SEL. For applications in a linecard environment, a 2.56 MHz clock can be used instead of the 2.4576 MHz clock. The 153.6 kHz (160 kHz with 2.56 MHz clock) sampling clock is available as an open drain output at CK OUT for synchronization or driving other circuits, e.g. the transmit or receive filters, or A/D and D/A converters.

CK SEL	Recommended XTAL Frequency	CK OUT
VDD	11.0592 MHz	153.6 kHz
DGND	3.6864 MHz	153.6 kHz
VSS	2.4576 MHz	153.6 kHz
VSS	2.56 MHz	160.0 kHz

Group Delay Characteristics (Microseconds)

Fs = 153.6 kHz

Frequency (Hz)	Step #1	Step #2	Step #3	Step #4
300	158	278	416	284
600	188	336	502	386
900	237	463	681	680
1200	325	671	985	1360
1500	431	890	1330	1791
1700	462	938	1382	1838
1900	435	897	1305	1810
2100	372	777	1144	1510
2400	266	542	808	683
2700	181	361	534	342
3000	136	250	368	213
3300	102	182	267	148

Table 1. Option Selection

Address D1	Address D0	Option Bit D6	Function
0	0	0	Writes Control Code into E^2PROM and updates Control Registers
0	1	0	
1	0	0	
0	0	1	Updates Control Registers Only
0	1	1	
1	0	1	
1	1	0	Power Down Mode
1	1	1	Active Mode

Table 2. Equalizer Selection

Address D1	Address D0	Control Code D5	D4	D3	D2	Equalizer Step No.	Recommened Line Condition
0	0	X	X	0	0	1	C2
0	0	X	X	0	1	2	C1
0	0	X	X	1	0	3	C1
0	0	X	X	1	1	4	3002

Table 3. Programmable Gain Amplifier, PG-A

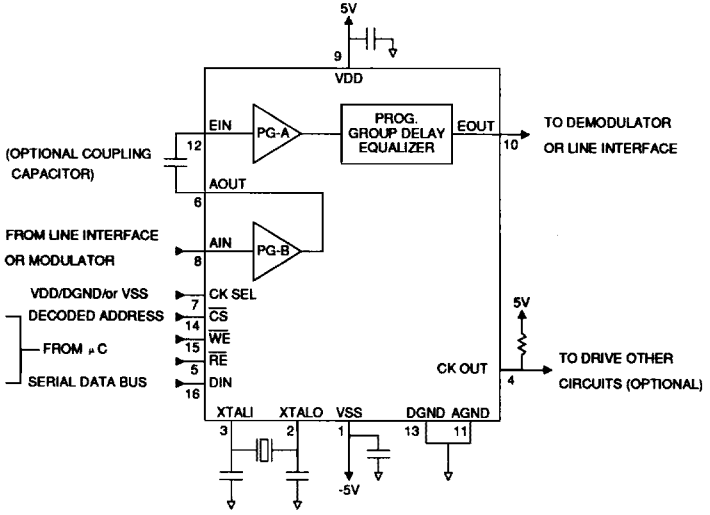
Address D1	Address D0	Control Code D5	D4	D3	D2	PG-A Step No.	PG-A Gain (dB)
0	1	0	0	0	0	1	0.0
0	1	0	0	0	1	2	0.5
0	1	0	0	1	0	3	1.0
0	1	0	0	1	1	4	1.5
0	1	0	1	0	0	5	2.0
0	1	0	1	0	1	6	2.5
0	1	0	1	1	0	7	3.0
0	1	0	1	1	1	8	3.5
0	1	1	0	0	0	9	4.0
0	1	1	0	0	1	10	4.5
0	1	1	0	1	0	11	5.0
0	1	1	0	1	1	12	5.5
0	1	1	1	0	0	13	6.0
0	1	1	1	0	1	14	6.5
0	1	1	1	1	0	15	7.0
0	1	1	1	1	1	16	7.5

Table 4. Programmable Gain Amplifier, PG-B

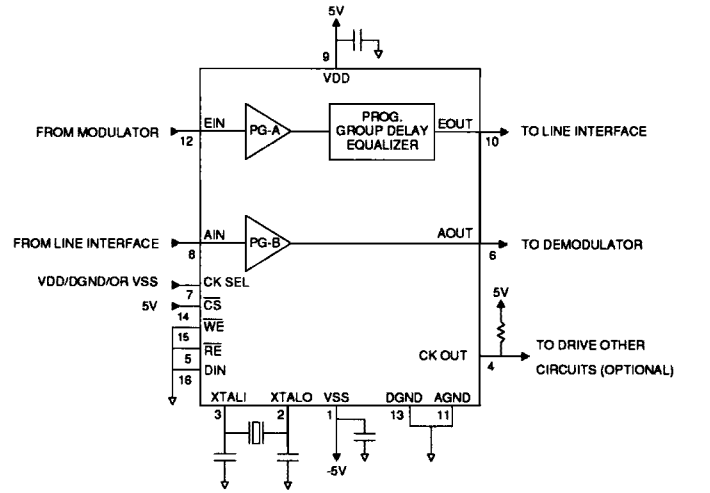
Address D1	Address D0	Control Code D5	D4	D3	D2	PG-B Step No.	PG-B Gain (dB)
1	0	X	X	0	0	1	0.0
1	0	X	X	0	1	2	8.0
1	0	X	X	1	0	3	16.0
1	0	X	X	1	1	4	-8.0

X = Don't Care

Sample Connection for Typical Application



Stand Alone Operation Example



Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 125° C
Storage Temperature	-65° C to 150° C
Voltage on Pins AGND and DGND with Respect to VSS	-0.6 V to 6.25 V
All Voltages with Respect to VSS	-0.6 V to VDD + 0.6 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

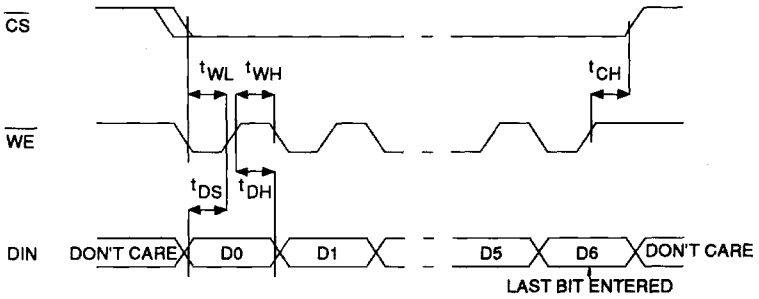
D.C. and A.C. Operating Range

	Operating Temperature (Case)	VDD / VSS Power Supplies
Commercial	0° C - 70° C	5 V / -5V ± 10%
Industrial	-40° C - 85° C	5 V / -5 V ± 10%
Military	-55° C - 125° C	5 V / -5 V ± 5%

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DDO}	VDD Quiescent Current (active mode)			3	6	mA
I_{SSO}	VSS Quiescent Current (active mode)			3	6	mA
I_{DDP}	VDD Quiescent Current (power-down mode)			100	500	µA
I_{SSP}	VSS Quiescent Current (power-down mode)			100	500	µA
R_{IA}	Input Resistance at AIN		100			kohm
R_{IE}	Input Resistance at EOUT	F_S=153.6 KHz	1			Mohm
C_I	Input Capacitance				20	pF
ROA	Ouput Resistance at AOUT				1	kohm
ROE	Ouput Resistance at EOUT				200	ohm
F_O	Center Frequency			1700		Hz
DT	Group Delay Tolerance		-1.5		+1.5	%
GT	Gain Tolerance		-0.05		0.05	dB
G_O	Insertion Loss		-0.15		0.15	dB
V_O	Output Voltage	RL = 20 kohm	VSS		VDD	V
V_N	Output Noise	BW = F_S/2			200	µVrms
THD	Total Harmonic Distortion	RL = 20 kohm V_O = 8 Vpp		0.1	0.5	%
F_S	Sampling Frequency			153.6		kHz
V_{FT}	Clock Feedthrough				5	mVpp

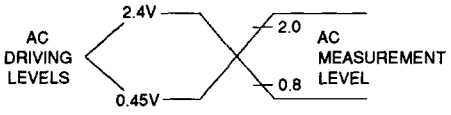
Configuration Code Write Waveform



Digital Timing Parameters

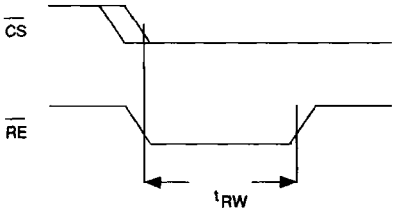
Symbol	Parameter	Min	Max	Units
t_{WL}	Write Enable Low	50		ns
t_{WH}	Write Enable High	50		ns
t_{CH}	$\overline{CS}$ Hold Time	100		ns
t_{DS}	Data Setup Time	40		ns
t_{DH}	Data Hold Time	40		ns

Input Test Waveform

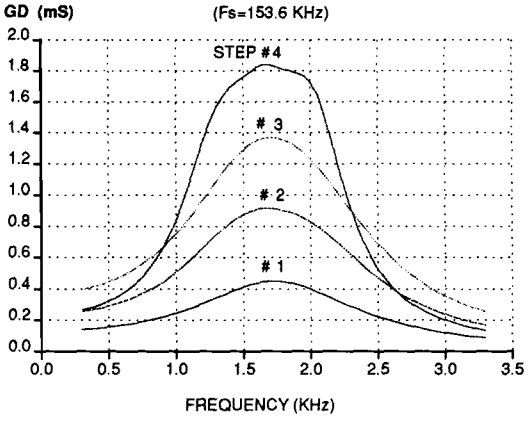


t_R, t_F < 20 ns (10% to 90%)

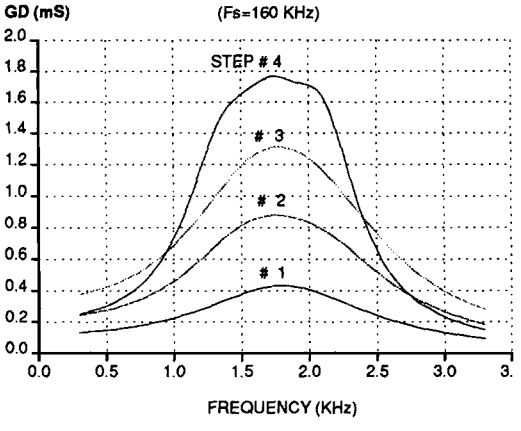
Configuration Code Recall Waveform



Typical Group Delay Response



Typical Group Delay Response



Ordering Information

Delay (ms)	Gain (dB)	Power Supply	Bandwidth (KHz)	Ordering Code	Package	Operation Range
1.8	31.5	±10%	4	AT76C10E-PC AT76C10E-SC	16P3 16S	Commercial (0°C to 70°C)
				AT76C10E-PI AT76C10E-SI	16P3 16S	Industrial (-40°C to 85°C)
1.8	31.5	±5%	4	AT76C10E-DM	16D3	Military (-55°C to 125°C)

Package Type	
16D3	16 Lead, 0.300" Wide Non-Windowed, Ceramic Dual Inline Package (Cerdip)
16P3	16 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
16S	16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)