HJ93D2010
User's Manual
(Preliminary)

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Contents

1. Overview

1.1. HJ93D2010 Outline

This component is a MCM (Multi Chip Module) containing SH3-DSP (SH7729) and two 64-MbitSDRAM (HM5264165F) (Memory capacity 16Mbytes). It is suitable for handheld communication equipment, graphic controller, network appliances etc, which require compactness, high-speed interface in one package.
The characteristics are described as follows.

- It enables high-speed operation in one package containing CPU and SDRAM. SH3-DSP internally operates 133.34[MHz] at maximum, and internal SH3-DSP-SDRAM I/F operates 66.67[MHz] at maximum.
  (1) SH3-DSP internal operating frequency: 133.34MHz
  (2) Internal SH3-DSP - SDRAM I/F operating frequency: 66.67MHz
- Package dimension is 13mm X 19mm, thickness is 1.7(+/-0.2) mm, suitable for applications such as handheld appliances to require compactness.

1.2. Usage Notes

HJ93D2010 contains SH3-DSP (SH7729) and two 64-MbitSDRAMs (HM5264165F) (Memory capacity 16Mbytes). Because the SDRAMs are connected with area 3 of SH3-DSP, HJ93D2010 has some limitations as shown in Table 1.1.

Table 1.1 the limitations of HJ93D2010

Item	Limitations
Bus State Controller (BSC)	DRAM can not be connected with HJ93D2010.
I/O Ports	Port A, Port B, PTJ2, 0 of Port J and PTK7-5, 1 of Port K can not be used.

1.3. Block Diagram

Figure 1.1 shows an internal Block diagram of the HJ93D2010.

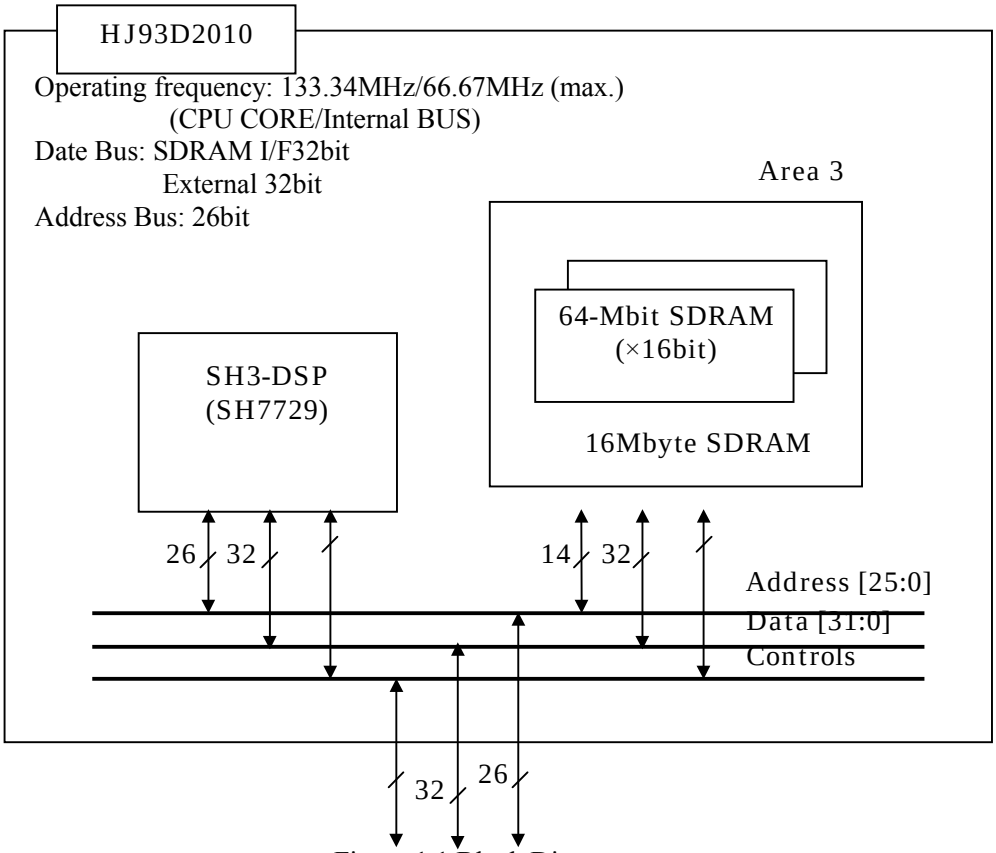

Figure 1.1 Block Diagram

1.4. HJ93D2010 Features

The features of the HJ93D2010 are listed in table 1.2.

Table 1.2 HJ93D2010 Features

Item		Features
MCM		System Structure :SH3-DSP (SH7729) X 1 + 64M SDRAM(HM5264165F) X 2 Operating Voltage :1.9V(internal), 3.3V(I/O) Package :13mm X 19mm, BGA273
CPU	Outline	Include HD6417729 (SH7729) See "SH7729 Hardware Manual, Section 1" for details of architecture.
	Operation Frequency	CPU internal frequency :133.34MHz at maximum Internal SH3-DSP-SDRAM I/F :66.67MHz at maximum MCM external :66.67MHz
	Access	CPU-SDRAM :32-bit data buses and 14-bit address buses MCM external : 32-bit data buses and 26-bit address buses
	Instruction Set	See "SH7729 Hardware Manual, Section 2" or "SH-3, SH-3E, SH-3-DSP Programming Manual, Section 7".
	Internal register structure	See "SH7729 Hardware Manual, Section 2" or "SH-3, SH-3E, SH-3-DSP Programming Manual, Section 2".
	Clock Generator	See "SH7729 Hardware Manual, Section 10".
	MMU	See "SH7729 Hardware Manual, Section 3".
	Caches	See "SH7729 Hardware Manual, Section 5".
	X/Y Memory	See "SH7729 Hardware Manual, Section 6".
	Interrupt Controller	See "SH7729 Hardware Manual, Section 7".
	UBC	See "SH7729 Hardware Manual, Section 8".
	BSC	16-Mbyte SDRAMs are connected with the SH3-DSP in the lower 32-Mbytes in area 3. Therefore, DRAM can not be connected with this MCM. See "SH7729 Hardware Manual, Section 11".
	DMAC	See "SH7729 Hardware Manual, Section 12".
	H-UDI	See "SH7729 Hardware Manual, Section 23".
	TMU	See "SH7729 Hardware Manual, Section 13".
	RTC	See "SH7729 Hardware Manual, Section 14".
	SCI0, 1, 2	See "SH7729 Hardware Manual, Section 15 - 18".
	I/O Ports	16-Mbyte SDRAMs are connected with the SH3-DSP by D31-0. Therefore, Port A, Port B, PTJ2,0 of Port J and PTK7-5,1 of Port K can not be used. See "SH7729 Hardware Manual, Section 20".
	A/D Converter	See "SH7729 Hardware Manual, Section 21".
	D/A Converter	See "SH7729 Hardware Manual, Section 22".
SDRAM	Capacity	HM5264165F X 2 (16Mbyte)
	Address	In the lower 32-Mbyte in area 3 of the SH7729 external memory space
	Operation Frequency	66.67MHz maximum (CL=2)
	CAS Latency	Burst read/single write mode, CAS latency = 2/3, burst sequence = sequence mode, burst length 1

Figure 1.2 shows the connection between SH7729 and 64-Mbit SDRAMs.

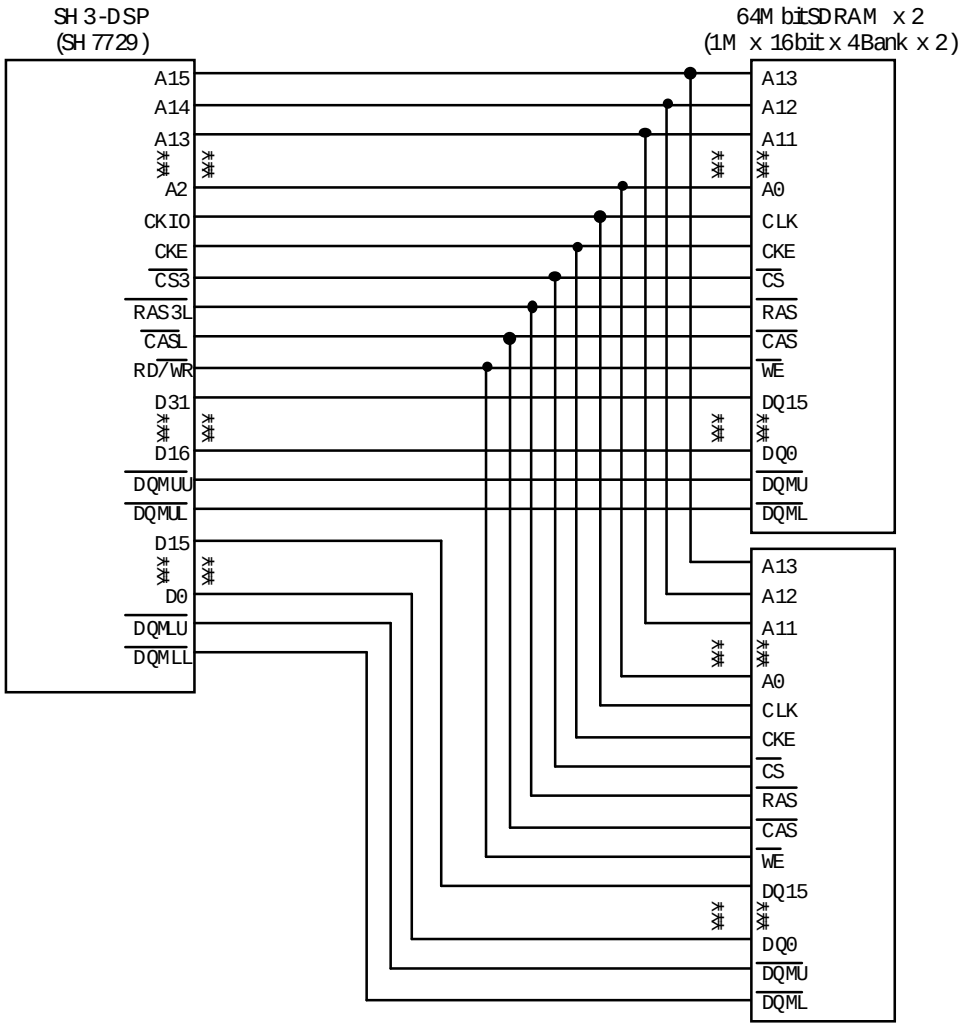

Figure 1.2 Connection between SH7729 and 64-Mbit SDRAMs

1.5. External Memory Space

Table 1.3 shows the external memory space of the HJ93D2010.

Table 1.3 External Memory Space Map

Area	Connectable Memory	External Addresses	Size	Access size
0	Ordinary Memory*1 Burst ROM	H'00000000 - H'03FFFFFF	64MB	8,16,32*2
		H'00000000 - H'03FFFFFF +H'20000000×n +H'20000000×n	Shadow	(n:1-6)
1	Internal I/O registers*8	H'04000000 - H'07FFFFFF	64MB	8,16,32*3
		H'04000000 - H'07FFFFFF +H'20000000×n +H'20000000×n	Shadow	(n:1-6)
2	Ordinary Memory *1 Synchronous DRAM	H'08000000 - H'0BFFFFFF	64MB	8,16,32*3, *4
		H'08000000 - H'0BFFFFFF +H'20000000×n +H'20000000×n	Shadow	(n:1-6)
3	Internal Synchronous DRAM	H'0C000000 - H'0FFFFFFF	64MB	32*5
		H'0C000000 - H'0FFFFFFF +H'20000000×n +H'20000000×n	Shadow	(n:1-6)
4	Ordinary Memory	H'10000000 - H'13FFFFFF	64MB	8,16,32*3
		H'10000000 - H'13FFFFFF +H'20000000×n +H'20000000×n	Shadow	(n:1-6)
5	Ordinary Memory PCMCIA Burst ROM	H'14000000 - H'15FFFFFF	32MB	8,16,32*3, *6
		H'16000000 - H'17FFFFFF	32MB	
		H'14000000 - H'17FFFFFF +H'20000000×n +H'20000000×n	Shadow	(n:1-6)
6	Ordinary Memory PCMCIA Burst ROM	H'18000000 - H'19FFFFFF	32MB	8,16,32*3, *6
		H'1A000000 - H'1BFFFFFF	32MB	
		H'18000000 - H'1BFFFFFF +H'20000000×n +H'20000000×n	Shadow	(n:1-6)
7*7	Reserved Area	H'1C000000 - H'1FFFFFFF +H'20000000×n +H'20000000×n		(n:0-7)

[Notes] *1 Memory with interface such as SRAM or ROM.
*2 Use external pin to specify memory bus width.
*3 Use register to specify memory bus width.
*4 With synchronous DRAM interfaces, bus width must be 16 or 32 bits.
*5 Bus width must be 32 bits for internal synchronous DRAM interface.
*6 With PCMCIA interface, bus width must be 8 or 16 bits.
*7 Do not access the reserved area. If the reserved area is accessed, correct operation cannot be guaranteed.
*8 When the control register in area 1 is not used for address translation by the MMU, set the first three bits of the logical address to 101 for allocation to the P2 space.

1.6. Pin Arrangement

Figure 1.3 shows the pin arrangement of the HJ93D2010.

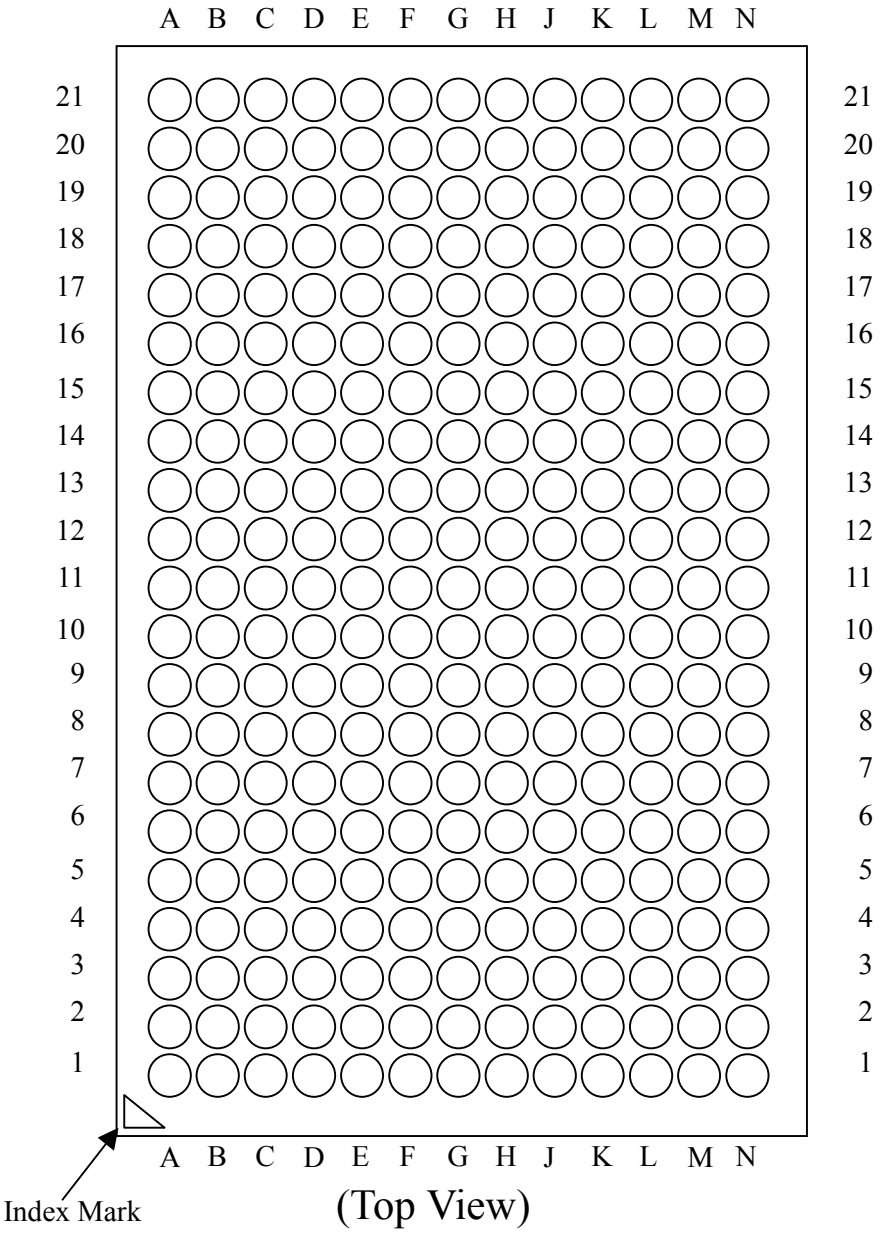

Figure 1.3 Pin Arrangement

Table 1.4 shows the pin functions of the HJ93D2010.

Table 1.4 Pin Function

Pin No.	Pin Name	I/O	Description
A01	NC	-	No connection
A02	NC	-	No connection
A03	CS5/CE1A/PTK[3]	O / I/O	Chip select 5/CE1 (area 5 PCMCIA) / input / output port K
A04	CS6/CE1B	O	Chip select 6/CE1 (area 6 PCMCIA)
A05	CE2A/PTE[4]	O / I/O	Area 5 PCMCIA card enable / input / output port E
A06	CE2B/PTE[5]	O / I/O	Area 6 PCMCIA card enable / input / output port E
A07	BREQ	I	Bus request
A08	RESETM	I	Manual reset request
A09	ASEMD0/PTG[6]	I	ASE mode / input port G
A10	AUDATA[3]/PTG[3]	O / I	AUD data / input port G
A11	TRST/PTF[7]/PINT[15]	I	Test reset / input port F / port interrupt
A12	TCK/PTF[4]/PINT[12]	I	Test clock / input port F / port interrupt
A13	MCS[3]/PTC[3]/PINT[3]	O / I/O / I	Mask ROM chip select / input / output port C / port interrupt
A14	MCS[6]/PTC[6]/PINT[6]	O / I/O / I	Mask ROM chip select / input / output port C / port interrupt
A15	STATUS0/PTJ[6]	O / I/O	Processor status / input / output port J
A16	STATUS1/PTJ[7]	O / I/O	Processor status / input / output port J
A17	Vss-PLL1*2	-	PLL1 power supply (0 V)
A18	Vss-PLL2*2	-	PLL2 power supply (0 V)
A19	XTAL	O	Clock oscillator pin
A20	NC	-	No connection
A21	NC	-	No connection
B01	NC	-	No connection
B02	CS3/PTK[1]	O / I/O	Chip select 3 / input / output port K
B03	CS4/PTK[2]	O / I/O	Chip select 4 / input / output port K
B04	RAS3L/PTJ[0]	O / I/O	Lower 32 MB address (area 3 DRAM, SDRAM) RAS / input / output port J
B05	CASHL/PTJ[4]	O / I/O	D23–D16 (DRAM) CAS / input / output port J
B06	DACK1/PTD[7]	O / I/O	DMA acknowledge 1 / input / output port D
B07	WAIT	I	Hardware wait request
B08	ADTRG/PTH[5]	I	Analog trigger / input port H
B09	ASEBRKAK/PTG[5]	O / I	ASE break acknowledge / input port G
B10	AUDATA[2]/PTG[2]	O / I	AUD data / input port G

Table 1.4 Pin Function(Cont)

Pin No.	Pin Name	I/O	Description
B11	TMS/PTF[6]/PINT[14]	I	Test mode switch / input port F / port interrupt
B12	IRLS3/PTF[3]/PINT[11]	I	External interrupt request / input port F / port interrupt
B13	IRLS1/PTF[1]/PINT[9]	I	External interrupt request / input port F / port interrupt
B14	MCS[5]/PTC[5]/PINT[5]	O / I/O / I	Mask ROM chip select / input / output port C / port interrupt
B15	SCK0/SCPT[1]	I/O	Serial clock 0 / SCI input / output port
B16	TxD0/SCPT[0]	O	Transmit data 0 / SCI output port
B17	MD0	I	Clock mode setting
B18	CAP1	-	PLL1 external capacitance pin
B19	CAP2	-	PLL2 external capacitance pin
B20	EXTAL	I	External clock / crystal oscillator pin
B21	NC	-	No connection
C01	RD/WR	O	Read/write
C02	CS0/MCS[0]	O	Chip select 0/mask ROM chip select 0
C03	CS2/PTK[0]	O / I/O	Chip select 2 / input / output port K
C04	RAS2L/PTJ[1]	O / I/O	Lower 32 MB address (area 2 DRAM) RAS / input / output port J
C05	CASHH/PTJ[5]	O / I/O	D31–D24 (DRAM) CAS / input / output port J
C06	CASLH/CASU/PTJ[3]	O / I/O	D15–D8 (DRAM) CAS / Upper 32 MB address (SDRAM) CAS / input / output port J
C07	AUDSYNC/PTE[7]	O / I/O	AUD synchronous / input / output port E
C08	IOIS16/PTG[7]	I	area 6 16-bit input / output / input port G
C09	PTG[4]	I	Input port G
C10	AUDATA[1]/PTG[1]	O / I	AUD data / input port G
C11	TDI/PTF[5]/PINT[13]	I	Test data input / input port F / port interrupt
C12	IRLS2/PTF[2]/PINT[10]	I	External interrupt request / input port F / port interrupt
C13	IRLS0/PTF[0]/PINT[8]	I	External interrupt request / input port F / port interrupt
C14	MCS[4]/PTC[4]/PINT[4]	O / I/O / I	Mask ROM chip select / input / output port C / port interrupt
C15	RxD0/SCPT[0]	I	Transmit data 0 / SCI input port
C16	TxD1/SCPT[2]	O	Transmit data 1 / SCI output port
C17	MCS[7]/PTC[7]/PINT[7]	O / I/O / I	Mask ROM chip select / input / output port C / port interrupt
C18	Vcc-PLL1*2	-	PLL1 power supply (1.9/1.8 V*5)
C19	Vcc-PLL2*2	-	PLL2 power supply (1.9/1.8 V*5)

Table 1.4 Pin Function(Cont)

Pin No.	Pin Name	I/O	Description
C20	IRQOUT	O	Interrupt request notification
C21	CKIO	I/O	System clock input/output
D01	WE1/DQMLU/WE	O	D15–D8 select signal / DQM (SDRAM)
D02	WE2/DQMUL/ICIORD/PTK[6]	O / I/O	D23–D16 select signal / DQM (SDRAM) / PCMCIA input / output read / input / output port K
D03	WE3/DQMUU/ICIOWR/PTK[7]	O / I/O	D31–D24 select signal / DQM (SDRAM) / PCMCIA input / output write / input / output port K
D04	CASLL/CASL/PTJ[2]	O / I/O	D7–D0 (DRAM) CAS / Lower 32 MB address (SDRAM) CAS / input / output port J
D05	DACK0/PTD[5]	O / I/O	DMA acknowledge 0 / input / output port D
D06	BACK	O	Bus acknowledge
D07	VssQR	-	Input/output power supply (0 V)
D08	VccQR	-	Input/output power supply (3.3 V)
D09	VssQR	-	Input/output power supply (0 V)
D10	AUDATA[0]/PTG[0]	O / I	AUD data / input port G
D11	TDO/PTE[0]	O / I/O	Test data output / input / output port E
D12	VccQ	-	Input/output power supply (3.3 V)
D13	VssQ	-	Input/output power supply (0 V)
D14	VccQ	-	Input/output power supply (3.3 V)
D15	RxD1/SCPT[2]	I	Transmit data 1 / SCI input port
D16	SCK1/SCPT[3]	I/O	Serial clock 1 / SCI input / output port
D17	AUDCK/PTH[6]	I	AUD clock / input port H
D18	VssQ	-	Input/output power supply (0 V)
D19	RxD2/SCPT[4]	I	Transmit data 2 / SCI input port
D20	TCLK/PTH[7]	I/O	TMU or RTC clock input / output / input / output port H
D21	RTS2/SCPT[6]	O / I/O	Transmit request 2 / SCI input / output port
E01	RD	O	Read strobe
E02	WE0/DQMLL	O	D7–D0 select signal / DQM (SDRAM)
E03	CKE/PTK[5]	O / I/O	CK enable (SDRAM) / input / output port K
E04	Reserved	-	Connect to CKE(E03)
E05	VccQR	-	Input/output power supply (3.3 V)
E06	VssQR	-	Input/output power supply (0 V)
E07	VssQR	-	Input/output power supply (0 V)
E08	VccQR	-	Input/output power supply (3.3 V)
E09	VccQR	-	Input/output power supply (3.3 V)
E10	Vss	-	Power supply (0 V)

Table 1.4 Pin Function(Cont)

Pin No.	Pin Name	I/O	Description
E11	VssQ	-	Input/output power supply (0 V)
E12	VssQ	-	Input/output power supply (0 V)
E13	VccQ	-	Input/output power supply (3.3 V)
E14	Vcc	-	Power supply (1.9/1.8 V*5)
E15	Vss	-	Power supply (0 V)
E16	Vss	-	Power supply (0 V)
E17	Vcc	-	Power supply (1.9/1.8 V*5)
E18	Vcc	-	Power supply (1.9/1.8 V*5)
E19	TxD2/SCPT[4]	O	Transmit data 2 / SCI output port
E20	SCK2/SCPT[5]	I/O	Serial clock 2 / SCI input / output port
E21	CTS2/IRQ5/SCPT[7]	I	Transmit clear 2 / external interrupt request / SCI input port
F01	A25	O	Address bus
F02	A24	O	Address bus
F03	BS/PTK[4]	O / I/O	Bus cycle start signal / input / output port K
F04	CAS2L/PTE[6]	O / I/O	D7–D0 (area 2 DRAM) CAS / input / output port E
F05	VssQR	-	Input/output power supply (0 V)
F06	NC	-	No connection
F07	NC	-	No connection
F08	NC	-	No connection
F09	NC	-	No connection
F10	NC	-	No connection
F11	NC	-	No connection
F12	NC	-	No connection
F13	NC	-	No connection
F14	NC	-	No connection
F15	NC	-	No connection
F16	NC	-	No connection
F17	Vcc	-	Power supply (1.9/1.8 V*5)
F18	VccQ	-	Input/output power supply (3.3 V)
F19	WAKEUP/PTD[3]	O / I/O	Standby mode interrupt request notification / input / output port D
F20	RESETOUT/PTD[2]	O / I/O	Reset output / input / output port D
F21	RESETP	I	Power-on reset request
G01	A23	O	Address bus
G02	A22	O	Address bus
G03	A21	O	Address bus
G04	CAS2H/PTE[3]	O / I/O	D15–D8 (area 2 DRAM) CAS / input / output port E
G05	VccQR	-	Input/output power supply (3.3 V)

Table 1.4 Pin Function(Cont)

Pin No.	Pin Name	I/O	Description
G06	NC	-	No connection
G07	NC	-	No connection
G08	NC	-	No connection
G09	NC	-	No connection
G10	NC	-	No connection
G11	NC	-	No connection
G12	NC	-	No connection
G13	NC	-	No connection
G14	NC	-	No connection
G15	NC	-	No connection
G16	NC	-	No connection
G17	VccQ	-	Input/output power supply (3.3 V)
G18	Vss	-	Power supply (0 V)
G19	CA	I	Chip activate / hardware standby request
G20	MD3	I	Area 0 bus width setting
G21	MD4	I	Area 0 bus width setting
H01	A20	O	Address bus
H02	A19	O	Address bus
H03	A18	O	Address bus
H04	RAS2U/PTE[1]	O / I/O	Upper 32 MB address (area 2 DRAM) RAS / input / output port E
H05	VssQR	-	Input/output power supply (0 V)
H06	NC	-	No connection
H07	NC	-	No connection
H08	NC	-	No connection
H09	NC	-	No connection
H10	NC	-	No connection
H11	NC	-	No connection
H12	NC	-	No connection
H13	NC	-	No connection
H14	NC	-	No connection
H15	NC	-	No connection
H16	NC	-	No connection
H17	VccQ	-	Input/output power supply (3.3 V)
H18	VssQ	-	Input/output power supply (0 V)
H19	MD5	I	Endian setting
H20	AN[1]/PTL[1]	I	A/D converter input / input port L
H21	AN[0]/PTL[0]	I	A/D converter input / input port L
J01	A17	O	Address bus
J02	A16	O	Address bus
J03	A15	O	Address bus

Table 1.4 Pin Function(Cont)

Pin No.	Pin Name	I/O	Description
J04	RAS3U/PTE[2]	O / I/O	Upper 32 MB address (area 3 DRAM, SDRAM) RAS / input / output port E
J05	VccQR	-	Input/output power supply (3.3 V)
J06	VccQR	-	Input/output power supply (3.3 V)
J07	VccQR	-	Input/output power supply (3.3 V)
J08	VssQR	-	Input/output power supply (0 V)
J09	VccQR	-	Input/output power supply (3.3 V)
J10	VssQ	-	Input/output power supply (0 V)
J11	VssQ	-	Input/output power supply (0 V)
J12	VccQ	-	Input/output power supply (3.3 V)
J13	VccQ	-	Input/output power supply (3.3 V)
J14	VccQ	-	Input/output power supply (3.3 V)
J15	VccQ	-	Input/output power supply (3.3 V)
J16	Vcc	-	Power supply (1.9/1.8 V*5)
J17	VssQ	-	Input/output power supply (0 V)
J18	AN[5]/PTL[5]	I	A/D converter input / input port L
J19	AN[4]/PTL[4]	I	A/D converter input / input port L
J20	AN[3]/PTL[3]	I	A/D converter input / input port L
J21	AN[2]/PTL[2]	I	A/D converter input / input port L
K01	A14	O	Address bus
K02	A13	O	Address bus
K03	A12	O	Address bus
K04	A11	O	Address bus
K05	D0	I/O	Data bus
K06	D2	I/O	Data bus
K07	VssQR	-	Input/output power supply (0 V)
K08	VccQR	-	Input/output power supply (3.3 V)
K09	VssQR	-	Input/output power supply (0 V)
K10	VssQR	-	Input/output power supply (0 V)
K11	MCS[2]/PTC[2]/PINT[2]	O / I/O / I	Mask ROM chip select / input / output port C / port interrupt
K12	MCS[1]/PTC[1]/PINT[1]	O / I/O / I	Mask ROM chip select / input / output port C / port interrupt
K13	MCS[0]/PTC[0]/PINT[0]	O / I/O / I	Mask ROM chip select / input / output port C / port interrupt
K14	VssQ	-	Input/output power supply (0 V)
K15	VssQ	-	Input/output power supply (0 V)
K16	Vss	-	Power supply (0 V)
K17	AVss	-	Analog power supply (0 V)
K18	AVcc	-	Analog power supply (3.3 V)
K19	AN[6]/DA[1]/PTL[6]	I	A/D converter input / input port L
K20	AN[7]/DA[0]/PTL[7]	I	A/D converter input / input port L
K21	AVss	-	Analog power supply (0 V)

Table 1.4 Pin Function(Cont)

Pin No.	Pin Name	I/O	Description
L01	A10	O	Address bus
L02	A9	O	Address bus
L03	A8	O	Address bus
L04	A7	O	Address bus
L05	D1	I/O	Data bus
L06	D3	I/O	Data bus
L07	D6	I/O	Data bus
L08	D9	I/O	Data bus
L09	D12	I/O	Data bus
L10	D15	I/O	Data bus
L11	D18/PTA[2]	I/O	Data bus / input / output port A
L12	D21/PTA[5]	I/O	Data bus / input / output port A
L13	D24/PTB[0]	I/O	Data bus / input / output port B
L14	D27/PTB[3]	I/O	Data bus / input / output port B
L15	D30/PTB[6]	I/O	Data bus / input / output port B
L16	DRAK1/PTD[0]	O / I/O	DMA request acceptance / input / output port D
L17	IRQ4/PTH[4]	I	External interrupt request/input port H
L18	IRQ1/IRL1/PTH[1]	I	External interrupt request/input port H
L19	MD2	I	Clock mode setting
L20	MD1	I	Clock mode setting
L21	Vcc-RTC*1	-	RTC power supply (1.9/1.8 V*5)
M01	NC	-	No connection
M02	A6	O	Address bus
M03	A5	O	Address bus
M04	A4	O	Address bus
M05	A3	O	Address bus
M06	D4	I/O	Data bus
M07	D7	I/O	Data bus
M08	D10	I/O	Data bus
M09	D13	I/O	Data bus
M10	D16/PTA[0]	I/O	Data bus / input / output port A
M11	D19/PTA[3]	I/O	Data bus / input / output port A
M12	D22/PTA[6]	I/O	Data bus / input / output port A
M13	D25/PTB[1]	I/O	Data bus / input / output port B
M14	D28/PTB[4]	I/O	Data bus / input / output port B
M15	D31/PTB[7]	I/O	Data bus / input / output port B
M16	DREQ0/PTD[4]	I	DMA request / input port D
M17	IRQ3/IRL3/PTH[3]	I	External interrupt request/input port H
M18	IRQ0/IRL0/PTH[0]	I	External interrupt request/input port H
M19	EXTAL2	I	On-chip RTC crystal oscillator pin
M20	Vss-RTC*1	-	RTC power supply (0 V)
M21	NC	-	No connection

Table 1.4 Pin Function(Cont)

Pin No.	Pin Name	I/O	Description
N01	NC	-	No connection
N02	NC	-	No connection
N03	A2	O	Address bus
N04	A1	O	Address bus
N05	A0	O	Address bus
N06	D5	I/O	Data bus
N07	D8	I/O	Data bus
N08	D11	I/O	Data bus
N09	D14	I/O	Data bus
N10	D17/PTA[1]	I/O	Data bus / input / output port A
N11	D20/PTA[4]	I/O	Data bus / input / output port A
N12	D23/PTA[7]	I/O	Data bus / input / output port A
N13	D26/PTB[2]	I/O	Data bus / input / output port B
N14	D29/PTB[5]	I/O	Data bus / input / output port B
N15	DRAK0/PTD[1]	O / I/O	DMA request acceptance / input / output port D
N16	DREQ1/PTD[6]	I	DMA request / input port D
N17	IRQ2/IRL2/PTH[2]	I	External interrupt request/input port H
N18	NMI	I	Nonmaskable interrupt request
N19	XTAL2	O	On-chip RTC crystal oscillator pin
N20	NC	-	No connection
N21	NC	-	No connection

Note:
1. Must be connected to the power supply even when the RTC is not used.
2. Must be connected to the power supply even when the on-chip PLL circuits are not used (except in hardware standby mode).
3. Except in hardware standby mode, all VCC /VSS pins must be connected to the system power supply. (Supply power constantly.) In hardware standby mode, power must be supplied at least to VCC –RTC and VSS –RTC. If power is not supplied to VCC and VSS pins other than VCC –RTC and VSS –RTC, hold the CA pin low.
4. Do not make any connection to NC pins.
5. 1.9 V in 133 MHz models; 1.8 V in 100 MHz models.

1.7. Package Dimensions

Figure 1.4 shows the package dimensions of the HJ93D2010.

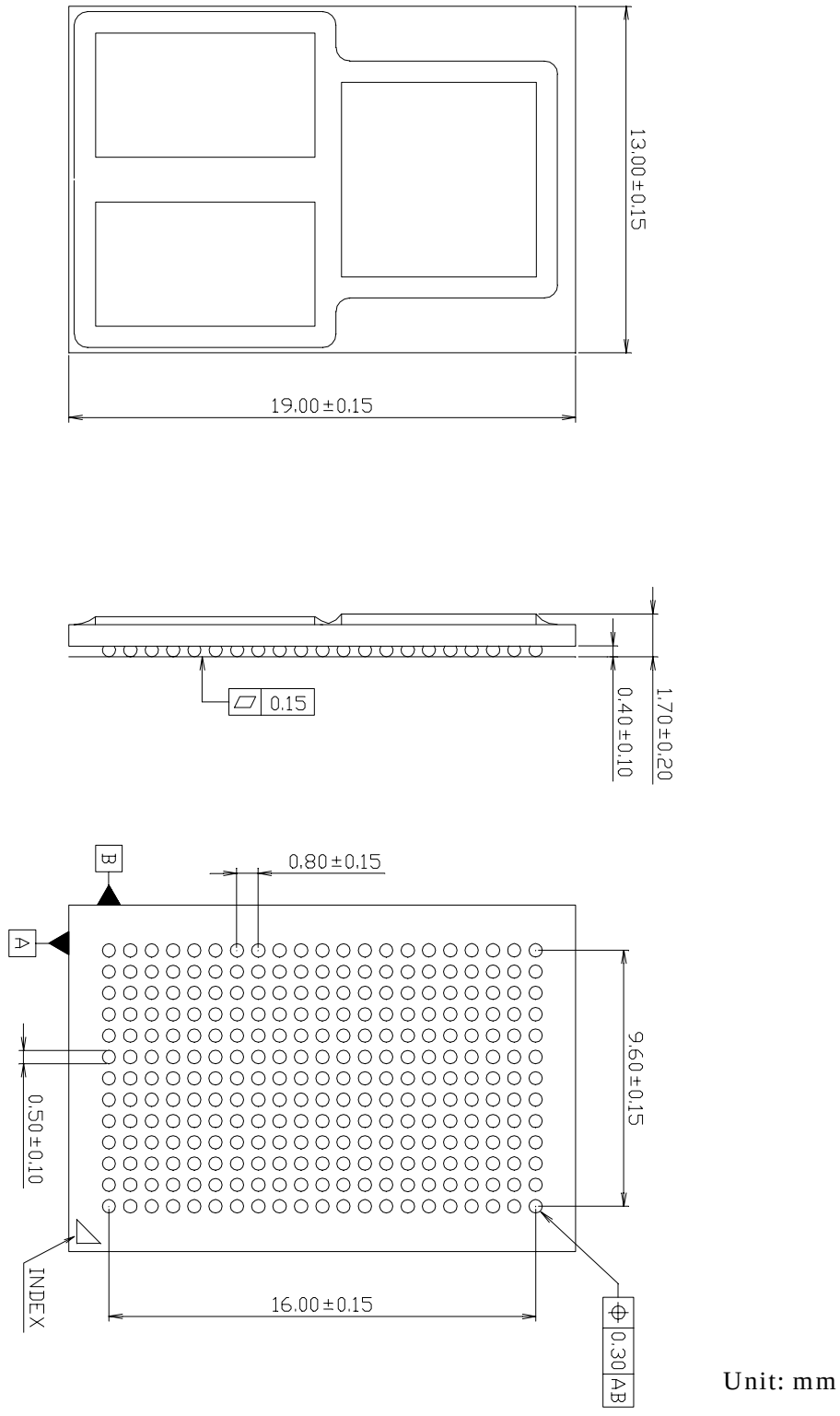

Figure 1.4 Package Dimensions