

74LCX112

Low Voltage Dual J-K Flip-Flops with Preset and Clear with 5V Tolerant Inputs

General Description

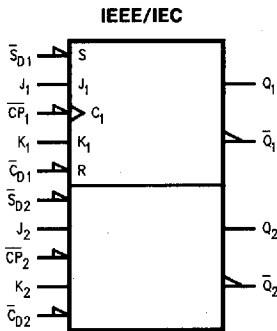
The 74LCX112 are dual J-K flip-flops. Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs Q, \bar{Q} outputs. These devices are edge sensitive and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input. LCX devices are designed for low voltage (3.3V) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX112 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

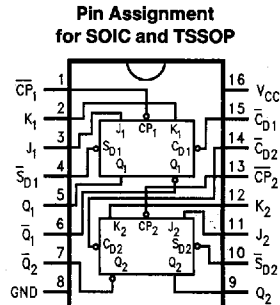
- 5V tolerant inputs
- 7.0 ns tpd max, 10 μ A I_{CCQ} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ± 24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 112
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

Logic Symbols

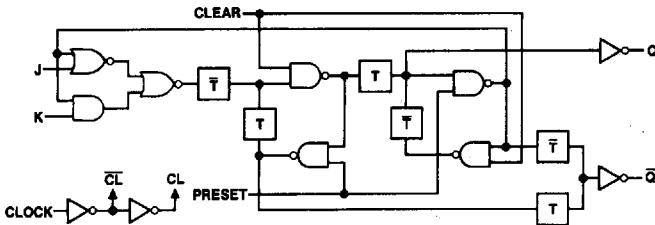


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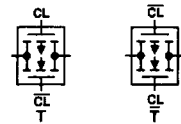
Connection Diagram



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TL/F/12424-2



TL/F/12424-3

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX112M 74LCX112MX	74LCX112SJ 74LCX112SJX	74LCX112MTC 74LCX112MTCX
See NS Package Number	M16A	M16D	MTC16