General Description

The ICS814253 is a PLL based synchronous clock generator that is optimized for Gigabit Ethernet and PCI Express™ clock jitter attenuation and frequency translation. The device contains two internal frequency multiplication stages that are cascaded in series. The first stage is a VCXO PLL that is optimized to provide reference clock jitter attenuation. The second stage is a FemtoClock® frequency multiplier that provides the low jitter, high frequency Gigabit Ethernet or PCI-Express output clock.

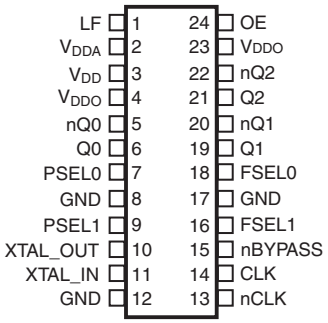
Pre-divider and output divider multiplication ratios are selected using device selection control pins. The multiplication ratios are optimized to support most common clock rates used in Gigabit Ethernet and PCI-Express applications. The VCXO requires the use of an external, inexpensive pullable crystal. The VCXO uses external passive loop filter components which allows configuration of the PLL loop bandwidth and damping characteristics.

Features

- Three differential LVDS output pairs
- One differential input supports the following input types: LVPECL, LVDS, LVHSTL, HCSL
- Accepts input frequencies from 19.6MHz to 136MHz, including: 25MHz, 62.5MHz, 100MHz and 125MHz input clocks
- Attenuates the phase jitter of the input clock by using a low-cost fundamental mode VCXO crystal
- Outputs common Gigabit Ethernet or PCI Express clock rates
- VCXO PLL bandwidth can be optimized for jitter attenuation and reference tracking using external loop filter connection
- Absolute pull range: ±50ppm
- FemtoClock frequency multiplier provides low jitter, high frequency output
- FemtoClock VCO range: 490MHz - 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.407ps (typical)
- Full 3.3V supply, or mixed 3.3V core/2.5V output supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment

ICS814253
24 Lead TSSOP
4.4mm x 7.85mm x 0.925mm
package body
G Package
Top View



Block Diagram

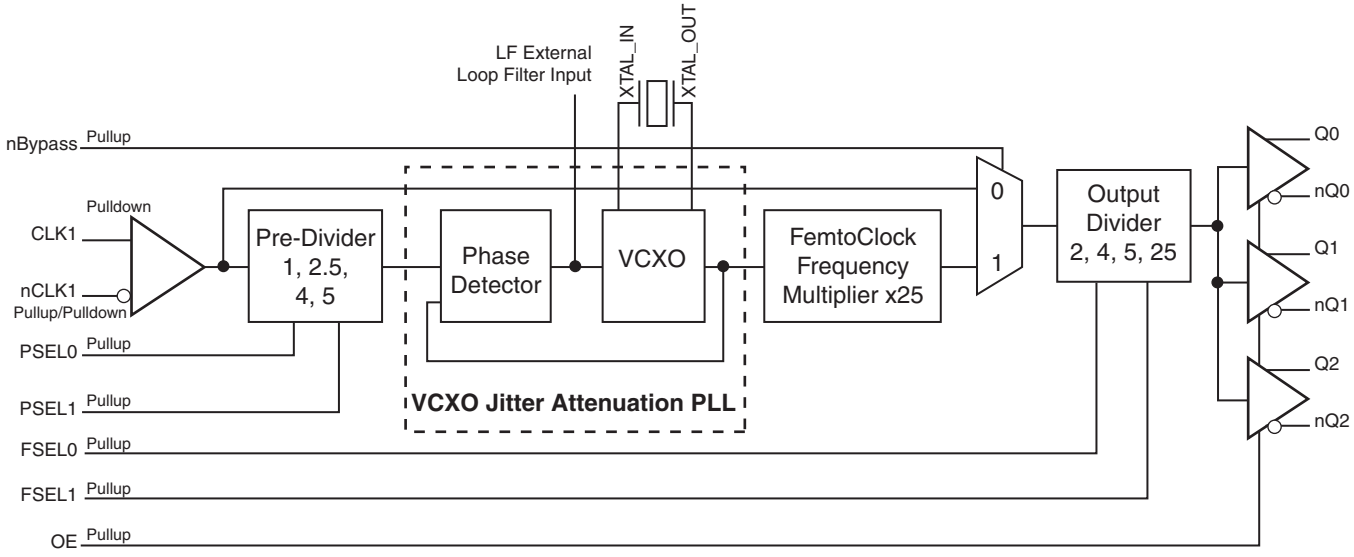


Table 1. Pin Descriptions

Number	Name	Type		Description
1	LF	Analog Input/Output		Loop filter connection node pin.
2	V_{DDA}	Power		Analog supply pin.
3	V_{DD}	Power		Core supply pin.
4, 23	V_{DDO}	Power		Output power supply pins.
5, 6	nQ0, Q0	Output		Differential clock outputs. LVDS interface levels.
7, 9	PSEL0, PSEL1	Input	Pullup	Pre-divider select pins. LVCMOS/LVTTL interface levels. See Table 3A.
8, 12, 17	GND	Power		Power supply ground.
10, 11	XTAL_OUT, XTAL_IN	Input		VCXO crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
13	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ bias voltage when left floating.
14	CLK	Input	Pulldown	Non-inverting differential clock input.
15	nBypass	Input	Pullup	PLL Bypass control pin. See Table 3D.
16, 18	FSEL1, FSEL0	Input	Pullup	Select pins. See Table 3B.
19, 20	Q1, nQ1	Output		Differential clock outputs. LVDS interface levels.
21, 22	Q2, nQ2	Output		Differential clock outputs. LVDS interface levels.
24	OE	Input	Pullup	Output enable. LVCMOS/LVTTL interface levels. See Table 3C.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Pre-divider Selection Function Table

Inputs		Pre-Divider Value
PSEL1	PSEL0	
0	0	÷1
0	1	÷2.5
1	0	÷4
1	1	÷5 (default)

Table 3B. FSEL Function Table

Inputs		Output Divider Value
FSEL1	FSEL0	
0	0	÷2
0	1	÷4
1	0	÷5
1	1	÷25 (default)

Table 3C. OE Function Table

Input	Clock Outputs	
OE	**Q[0:2]**	**nQ[0:2]**
0	LOW	HIGH
1	Enabled	Enabled (default)

Table 3D. Bypass Function Table

nBypass Input	Operation
0	VCXO jitter attenuation PLL and FemtoClock multiplier bypassed. Input passed directly to the output divider.
1 (default)	Normal operation mode.

Table 3E. Example Frequency Function Table

Input Frequency (MHz)	PSEL1	PSEL0	Input Divider	VCXO Crystal Frequency (MHz)	FemtoClock VCO Frequency (MHz)	FSEL1	FSEL0	Output Divider Value	Output Frequency (MHz)
25	0	0	÷1	25	625	0	0	÷2	312.5
25	0	0	÷1	25	625	0	1	÷4	156.25
25	0	0	÷1	25	625	1	0	÷5	125
25	0	0	÷1	25	625	1	1	÷25	25
62.5	0	1	÷2.5	25	625	0	0	÷2	312.5
62.5	0	1	÷2.5	25	625	0	1	÷4	156.25
62.5	0	1	÷2.5	25	625	1	0	÷5	125
62.5	0	1	÷2.5	25	625	1	1	÷25	25
100	1	0	÷4	25	625	0	0	÷2	312.5
100	1	0	÷4	25	625	0	1	÷4	156.25
100	1	0	÷4	25	625	1	0	÷5	125
100	1	0	÷4	25	625	1	1	÷25	25
100	1	1	÷5	20	500	0	0	÷2	250
100	1	1	÷5	20	500	0	1	÷4	125
100	1	1	÷5	20	500	1	0	÷5	100
100	1	1	÷5	20	500	1	1	÷25	20
125	1	1	÷5	25	625	0	0	÷2	312.5
125	1	1	÷5	25	625	0	1	÷4	156.25
125	1	1	÷5	25	625	1	0	÷5	125
125	1	1	÷5	25	625	1	1	÷25	25

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	82.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.13	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				113	mA
I_{DDA}	Analog Supply Current				13	mA
I_{DDO}	Output Supply Current				66	mA

Table 4B. LVDS Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.13	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				113	mA
I_{DDA}	Analog Supply Current				13	mA
I_{DDO}	Output Supply Current				64	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OE, PSEL[1:0], nBypass, FSEL[1:0]	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	OE, PSEL[1:0], nBypass, FSEL[1:0]	$V_{DD} = 3.465$, $V_{IN} = 0V$	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2. Common mode voltage is defined as V_{IH}.

Table 4D. DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 3.3V ± 5% or 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		525	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.25		1.55	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	Pre-divider = ÷1	19.6		27.2	MHz
		Pre-divider = ÷2.5	49		68	MHz
		Pre-divider = ÷4	78.4		108.8	MHz
		Pre-divider = ÷5	98		136	MHz
f_{OUT}	Output Frequency	Output Divider = ÷1	245		340	MHz
		Output Divider = ÷2.5	122.5		170	MHz
		Output Divider = ÷4	98		136	MHz
		Output Divider = ÷5	19.6		27.2	MHz
*t*jit(Ø)	RMS Phase Jitter, (Random), NOTE 1	156.25MHz f_{OUT}, 25MHz crystal, Integration Range: 1.875MHz – 20MHz		0.407		ps
*t*jit(per)	Period Jitter, RMS; NOTE 2			2.25	3.35	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3, 4				32	ps
*t*sk(o)	Output Skew; NOTE 3, 5				40	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		450	ps
odc	Output Duty Cycle		48		52	%
t_{LOCK}	VCXO & FemtoClock PLL Lock Time; NOTE 6	Reference Clock Input is ±50ppm from Nominal Frequency			205	ms

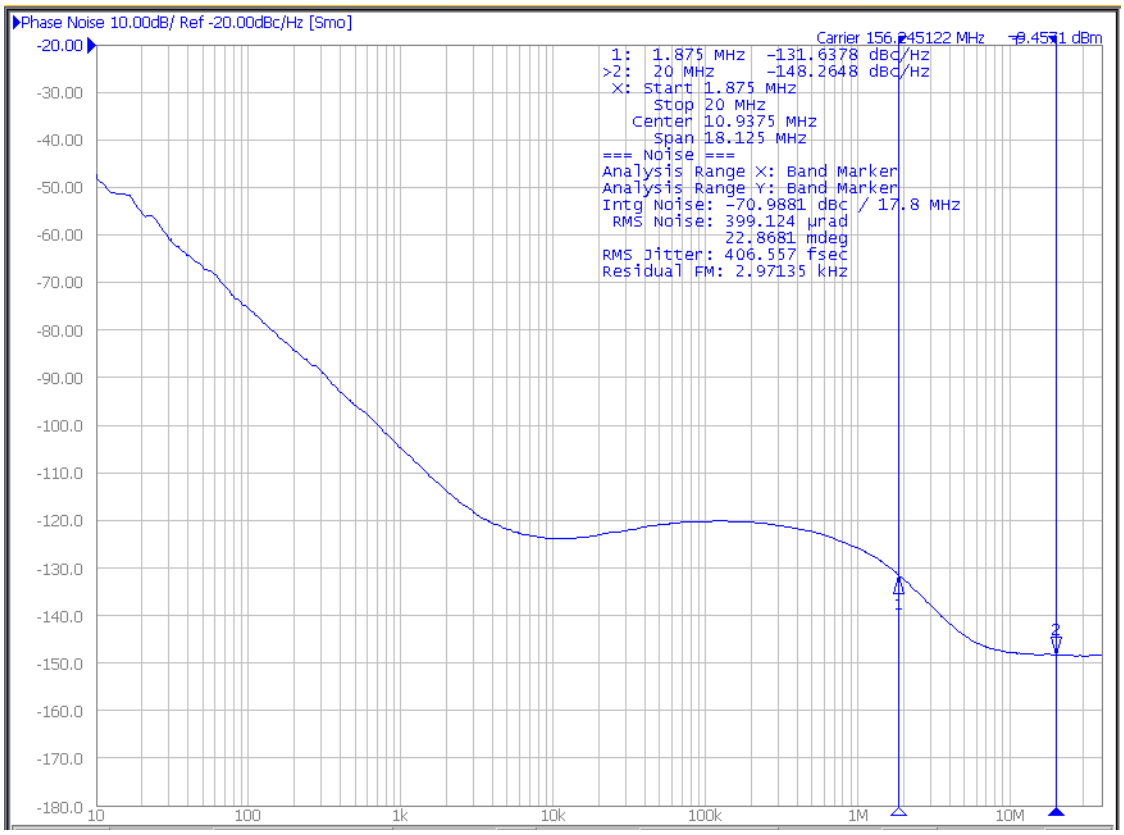
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized with outputs at the same frequency using the loop filter components for the mid loop badwidth. Refer to *VCXO-PLL Loop Bandwidth Selection Table.*
NOTE 1: Refer to the Phase Noise Plot.
NOTE 2: Characterized with outputs at the same frequency using the loop filter components for the mid loop bandwidth. Refer to the *VCXO-PLL Loop Bandwidth Selection Table.*
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Outputs terminated with 50Ω to $V_{DDO} – 2V$.
NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 6: Lock Time measured from power-up to stable output frequency.

Table 5B. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = 0°C to 70°C

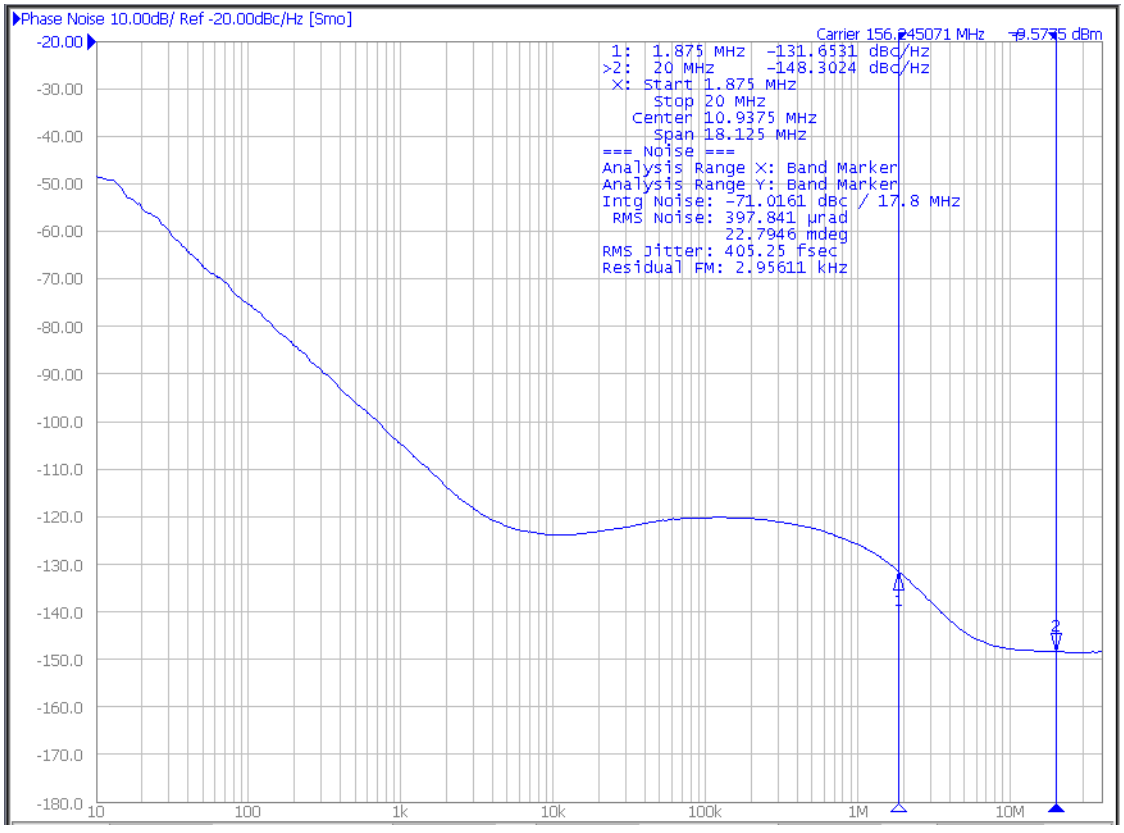
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	Pre-divider = ÷1	19.6		27.2	MHz
		Pre-divider = ÷2.5	49		68	MHz
		Pre-divider = ÷4	78.4		108.8	MHz
		Pre-divider = ÷5	98		136	MHz
f_{OUT}	Output Frequency	Output Divider = ÷1	245		340	MHz
		Output Divider = ÷2.5	122.5		170	MHz
		Output Divider = ÷4	98		136	MHz
		Output Divider = ÷5	19.6		27.2	MHz
*t*jit(Ø)	RMS Phase Jitter, (Random), NOTE 1	156.25MHz f_{OUT}, 25MHz crystal, Integration Range: 1.875MHz – 20MHz		0.405		ps
*t*jit(per)	Period Jitter, RMS; NOTE 2			2.30	3.55	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3, 4				32	ps
*t*sk(o)	Output Skew; NOTE 3, 5				40	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		450	ps
odc	Output Duty Cycle		48		52	%
t_{LOCK}	VCXO & FemtoClock PLL Lock Time; NOTE 6	Reference Clock Input is ±50ppm from Nominal Frequency			205	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized with outputs at the same frequency using the loop filter components for the mid loop badwidth. Refer to *VCXO-PLL Loop Bandwidth Selection Table.*
NOTE 1: Refer to the Phase Noise Plot.
NOTE 2: Characterized with outputs at the same frequency using the loop filter components for the mid loop bandwidth. Refer to the *VCXO-PLL Loop Bandwidth Selection Table.*
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Outputs terminated with 50Ω to V_{DDO} – 2V.
NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 6: Lock Time measured from power-up to stable output frequency.

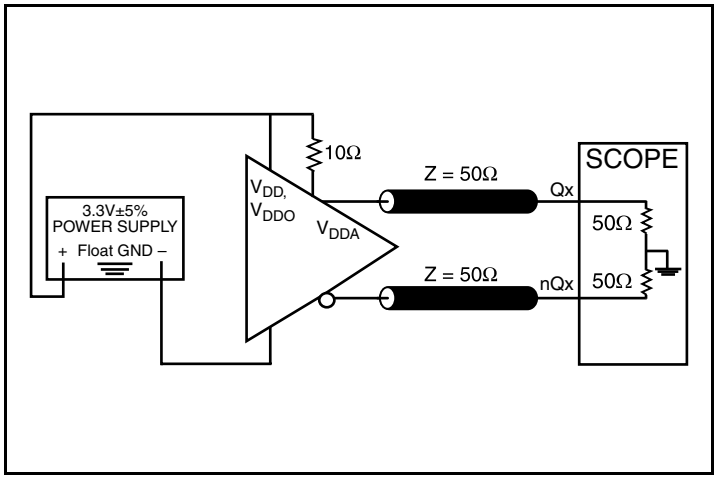
Typical Phase Noise at 156.25MHz (3.3V output)



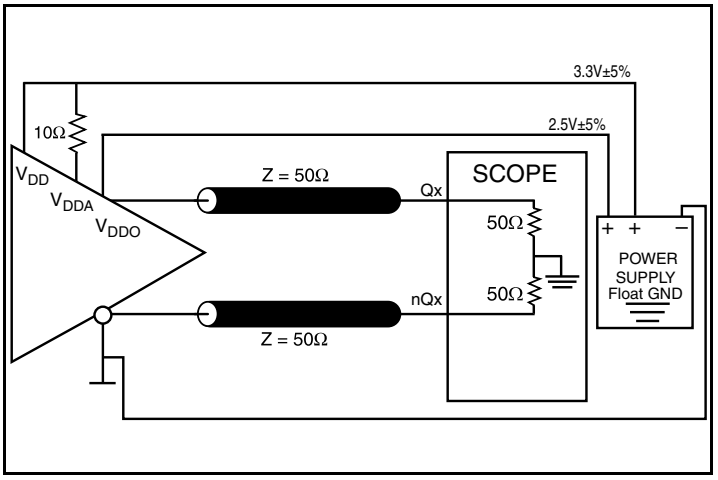
Typical Phase Noise at 156.25MHz (2.5V output)



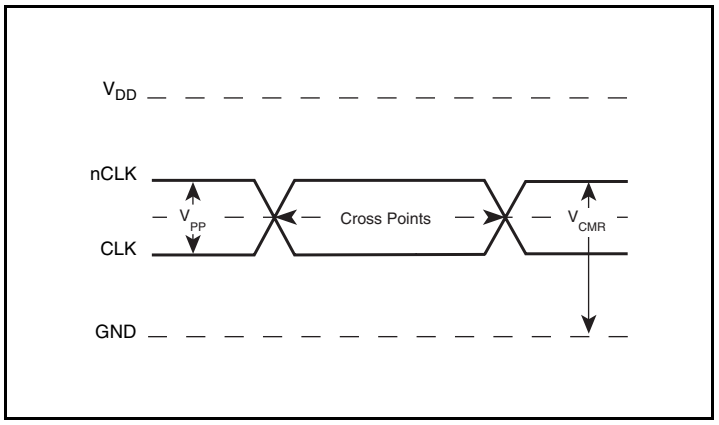
Parameter Measurement Information



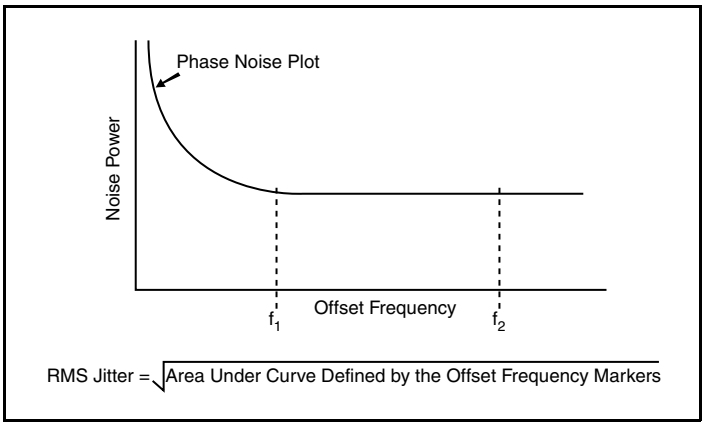
3.3V LVDS Output Load AC Test Circuit



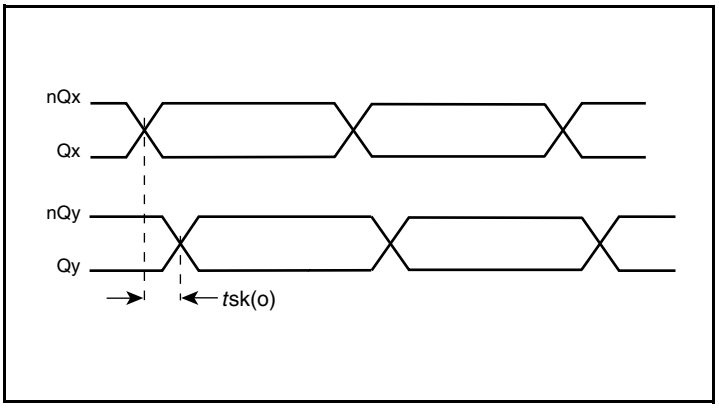
3.3V Core/2.5V LVDS Output Load AC Test Circuit



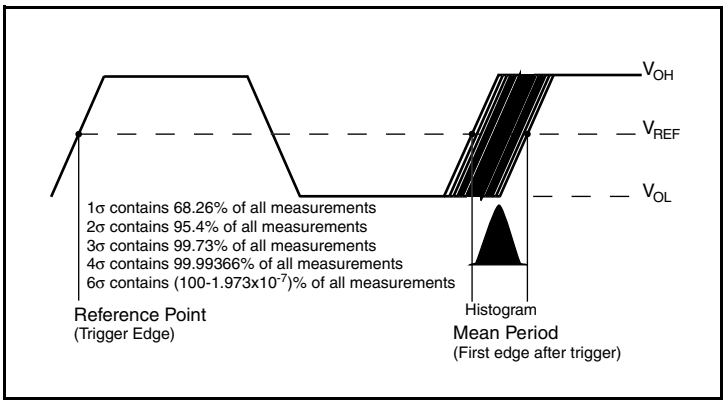
Differential Input Level



RMS Phase Jitter

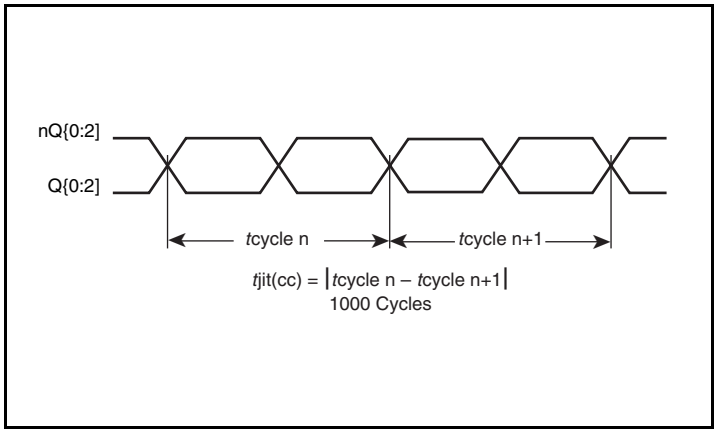


Output Skew

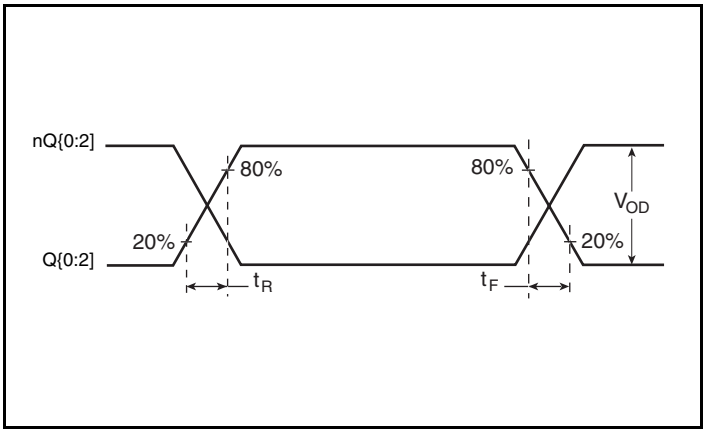


RMS Period Jitter

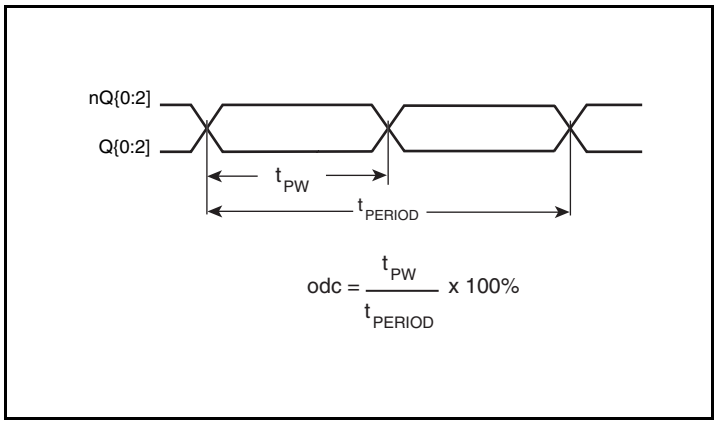
Parameter Measurement Information



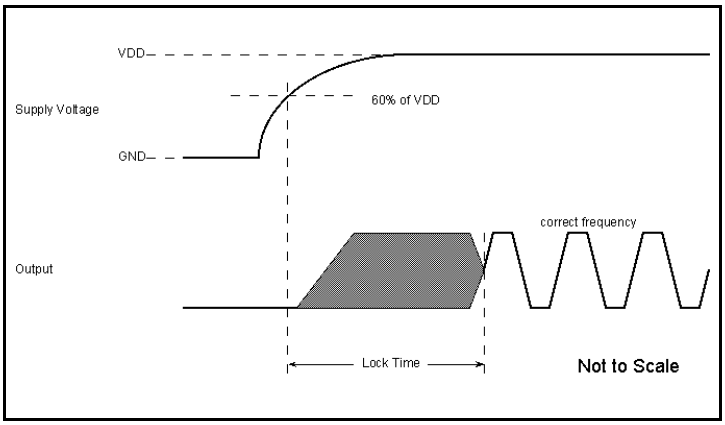
Cycle-to-Cylce Jitter



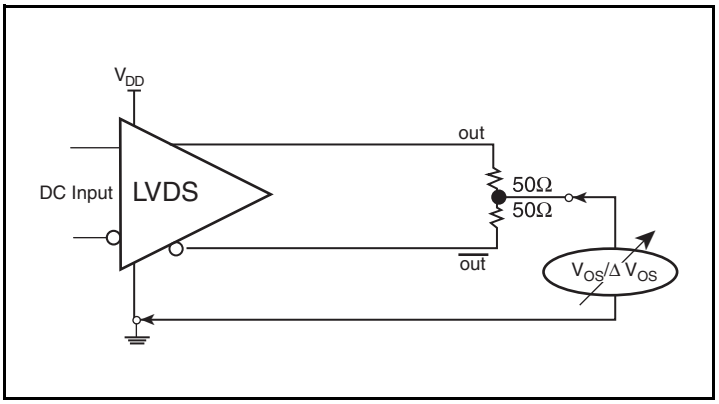
Output Rise/Fall Time



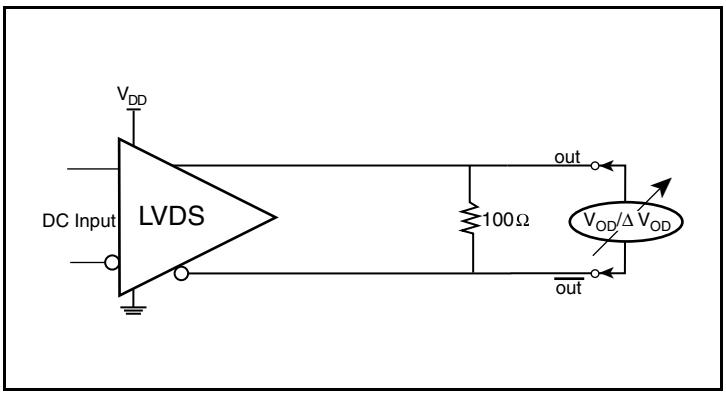
Output Duty Cycle/Pulse Width/Period



VCXO & FemtoClock PLL Lock Time



Output Voltage Setup



Differential Output Voltage Setup

Applications Information

Wiring the Differential Input to Accept Single-ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

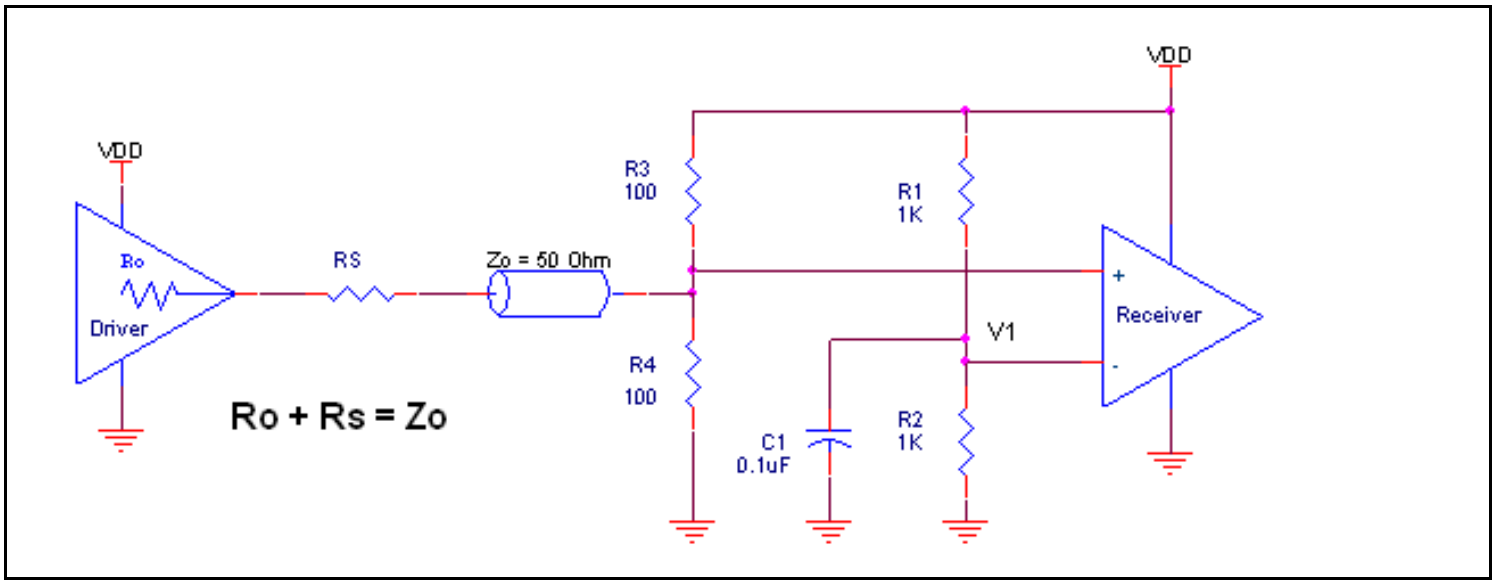


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

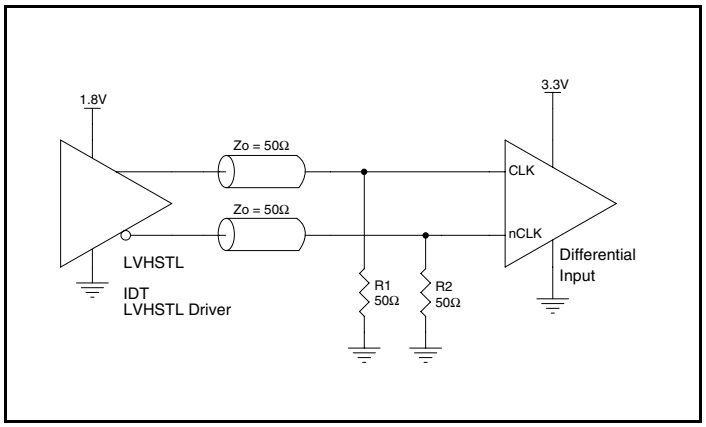


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

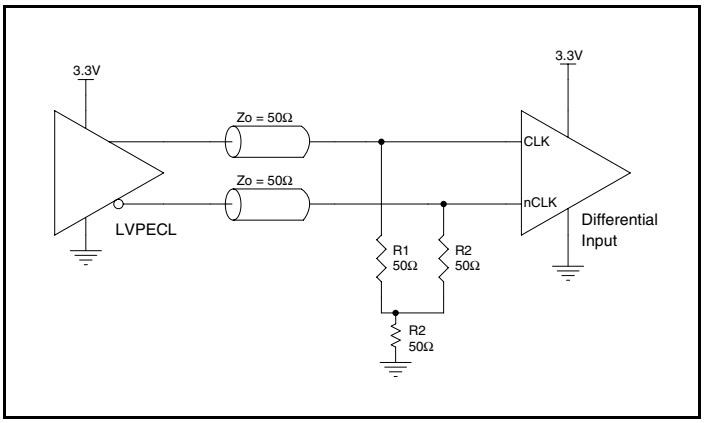


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

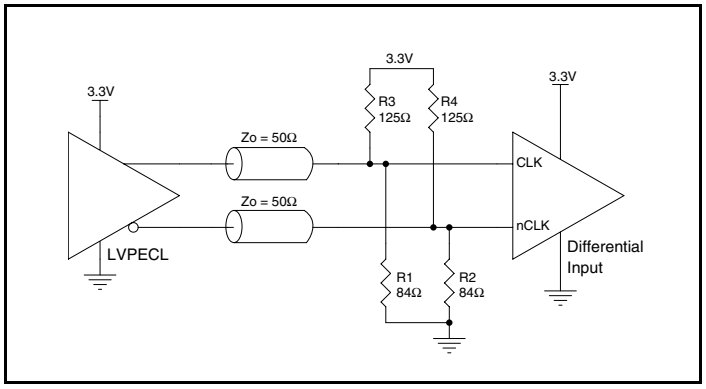


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

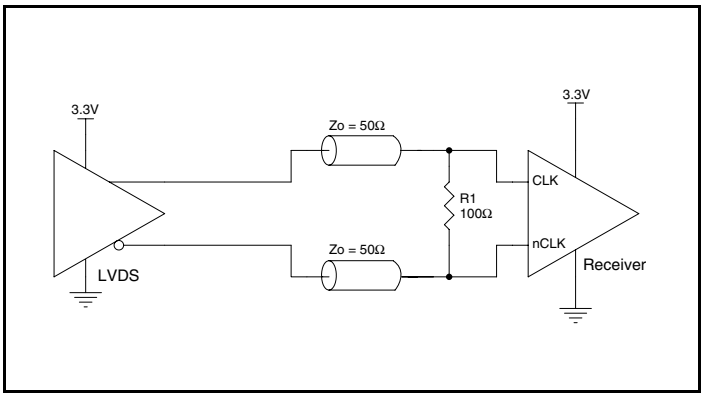


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

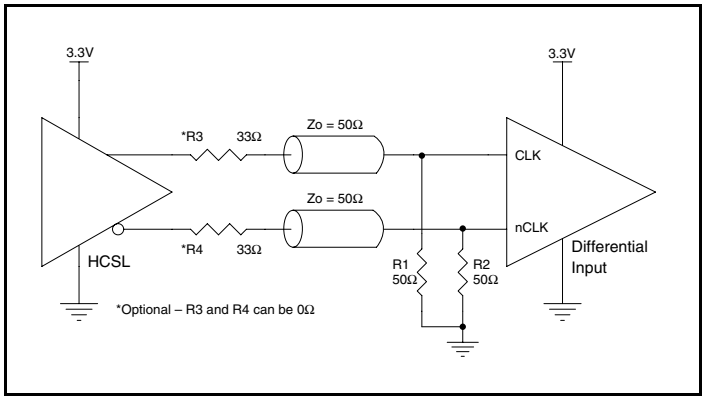


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

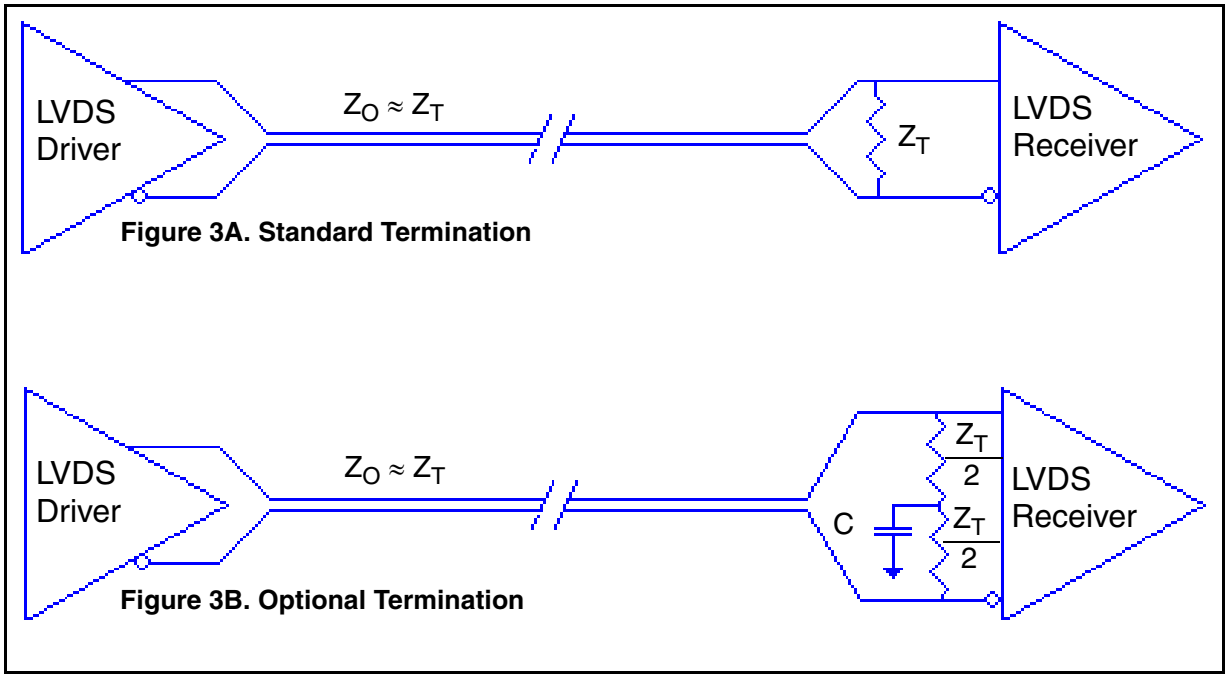


Figure 3A. Standard Termination

Figure 3B. Optional Termination

LVDS Termination

VCXO-PLL External Components

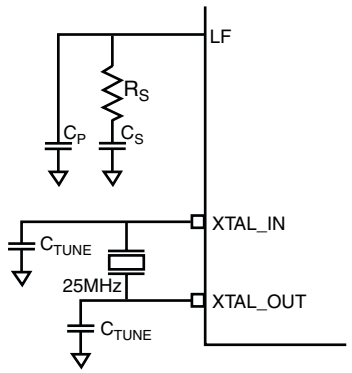
Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance (C_L). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note.*

The crystal's load capacitance (C_L) characteristic determines it's resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors (C_{TUNE}).

If the crystal (C_L) is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal (C_L) is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is reduced. The correct value of (C_L) is dependant on the characteristics of the VCXO. The recommended (C_L) in the Crystal Parameter Table balances the tuning range by centering the tuning curve.

The frequency of oscillation in the third overtone mode is not necessarily at exactly three times the fundamental frequency. The mechanical properties of the quartz element dictate the position of the overtones relative to the fundamental. The oscillator circuit may excite both the fundamental and overtone modes simultaneously. This will cause a nonlinearity in the tuning curve. This potential problem is the problem VCXO crystals are required to be tested for absence of any activity inside a ±200ppm window at three times the fundamental frequency. Refer to F_{L_3OVT} and $F_{L\_3OVT\_spurs}$ in the crystal Characteristics table.

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.



VCXO Characteristics Table

Symbol	Parameter	Typical	Units
k_{VCXO}	VCXO Gain	10,000	Hz/V
C_{V_LOW}	Low Varactor Capacitance	11.6	pF
C_{V_HIGH}	High Varactor Capacitance	25.7	pF

VCXO-PLL Loop Bandwidth Selection Table

Bandwidth	Crystal Frequency	R_S (kΩ)	C_S (µF)	C_P (µF)
100Hz (Low)	25MHz	0.562	10	0.001
215Hz (Mid)	25MHz	1.21	10	0.001
400kHz (High)	25MHz	2.21	10	0.001

Crystal Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
	Mode of Oscillation			Fundamental		
f_N	Frequency			25		MHz
f_T	Frequency Tolerance				±20	ppm
f_S	Frequency Stability				±20	ppm
	Operating Temperature Range		0		+70	^{0}C
C_L	Load Capacitance			10		pF
C_O	Shunt Capacitance			4		pF
C_O / C_1	Pullability Ratio			220	240	
F_{L_3OVT}	3rd Overtone F_L		200			pmm
$F_{L\_3OVT\_spurs}$	3rd Overtone F_L Spurs		200			pmm
ESR	Equivalent Series Resistance				20	Ω
	Drive Level				1	mW
	Aging @ 25 ^{0}C	First Year			±3	ppm
		Ten Years			±10	ppm

Schematic Example

Figure 4 (next page) is an ICS814253 application example schematic. The schematic focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set. X1 load capacitor values are generic, C1 and C2 are determined when the VCXO center frequency is tuned at initial board bring up.

The CLK, nCLK inputs are provided by a 3.3V LVPECL driver and depicted with a Y-termination rather than the standard four resistor V_{DD} - 2V Thevinin termination for reasons of minimum termination power and layout simplicity.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The ICS814253 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

The V_{DD} and V_{DDO} filters start to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

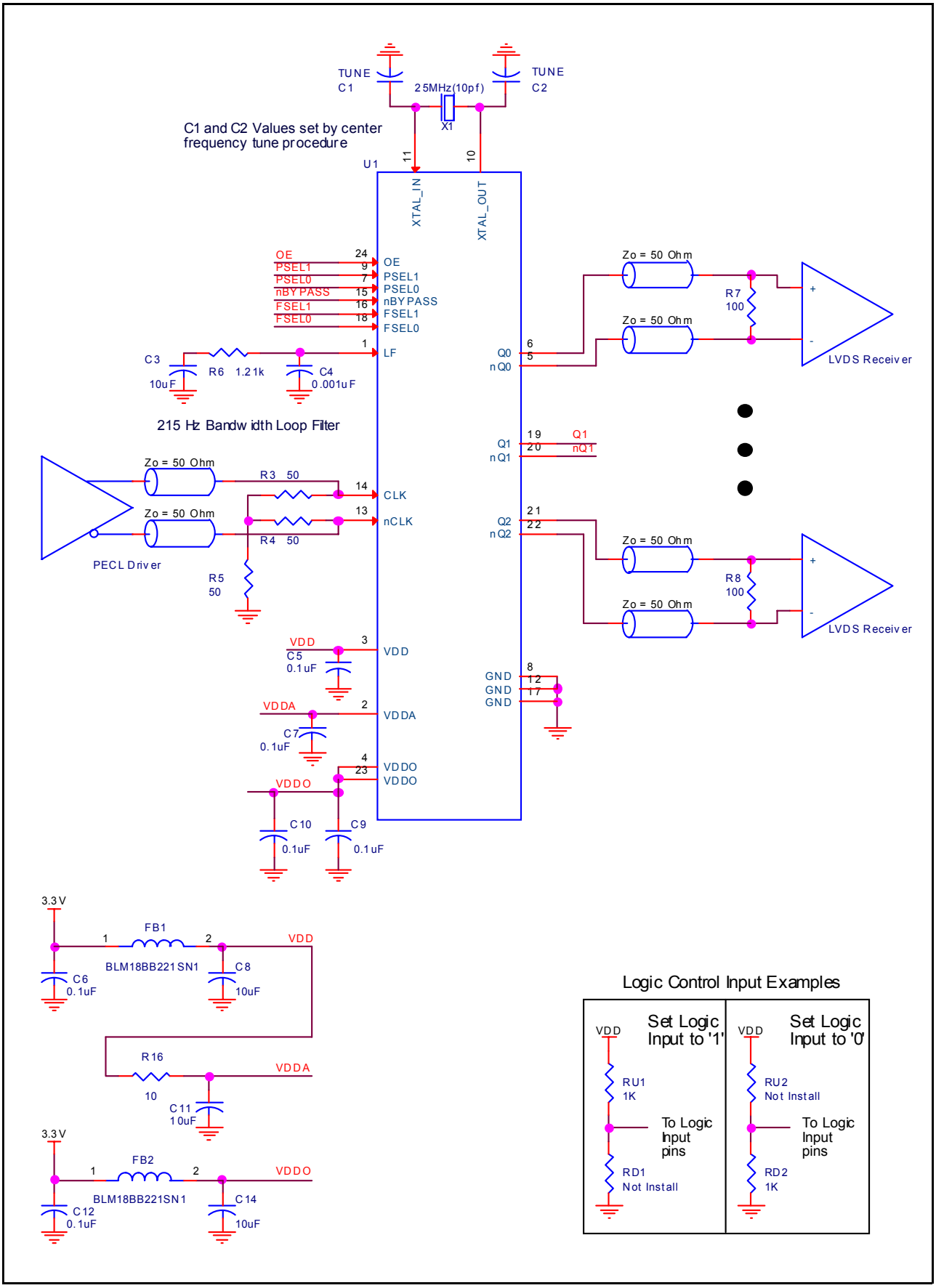


Figure 4. ICS814253 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for theICS814253.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS814253 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (113mA + 13mA) = **436.59mW**
- Power (outputs)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 66mA = **228.69mW**

Total Power$_{\_MAX}$ = 436.59mW + 228.69mW = **665.28mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 82.3°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.665W * 82.3°C/W = 124.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.95°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.95°C/W

Transistor Count

The transistor count for ICS814253 is: 2970

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

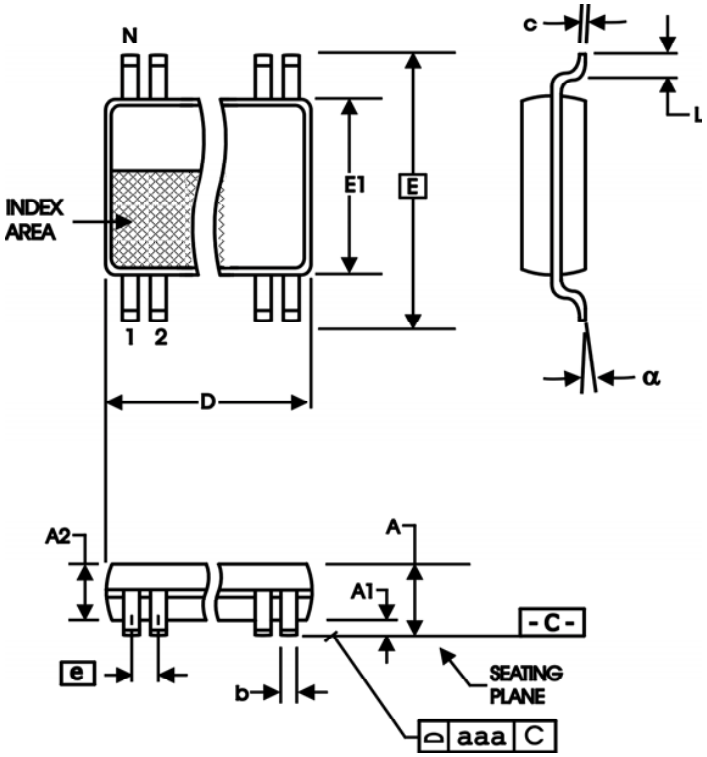


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
814253BGLF	ICS814253BGLF	“Lead-Free” 24 Lead TSSOP	Tube	0°C to 70°C
814253BGLFT	ICS814253BGLF	“Lead-Free” 24 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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