

# 74LCX74

## Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop with 5V Tolerant Inputs

### General Description

The LCX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

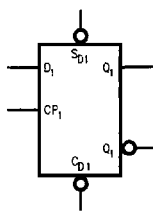
#### Asynchronous Inputs:

LOW input to  $\bar{S}_D$  (Set) sets Q to HIGH level  
 LOW input to  $\bar{C}_D$  (Clear) sets Q to LOW level  
 Clear and Set are independent of clock  
 Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

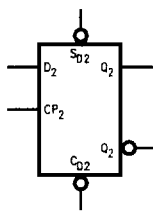
### Features

- 5V tolerant inputs
- 7.0 ns  $t_{PD}$  max, 10  $\mu$ A  $I_{CCQ}$  max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V  $V_C$  supply operation
- $\pm 24$  mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with 74 series 74
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

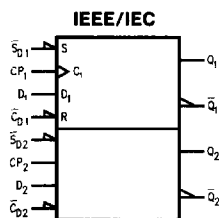
### Logic Symbols



TL/F/12414-1



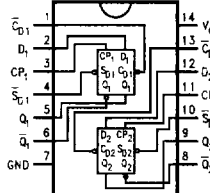
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TL/F/12414-3

### Connection Diagram

#### Pin Assignment for SOIC and TSSOP



TL/F/12414-4

### Truth Table (Each Half)

Pin Names	Description
D <sub>1</sub> , D <sub>2</sub>	Data Inputs
CP <sub>1</sub> , CP <sub>2</sub>	Clock Pulse Inputs
$\bar{C}_{D1}$ , $\bar{C}_{D2}$	Direct Clear Inputs
$\bar{S}_{D1}$ , $\bar{S}_{D2}$	Direct Set Inputs
Q <sub>1</sub> , $\bar{Q}_1$ , Q <sub>2</sub> , $\bar{Q}_2$	Outputs

Inputs			Outputs		
$\bar{S}_D$	$\bar{C}_D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

↗ = LOW-to-HIGH Clock Transition  
 Q<sub>0</sub>( $\bar{Q}_0$ ) = Previous Q( $\bar{Q}$ ) before LOW-to-HIGH Transition of Clock

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX74M 74LCX74MX	74LCX74SJ 74LCX74SJX	74LCX74MTC 74LCX74MTCX
See NS Package Number	M14A	M14D	MTC14

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## Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Conditions	Units
$V_{CC}$	Supply Voltage	-0.5 to +7.0		V
$V_I$	DC Input Voltage	-0.5 to +7.0		V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	Output in High or Low State (Note 2)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < \text{GND}$	mA
$I_{OK}$	DC Output Diode Current	-50 +50	$V_O < \text{GND}$ $V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature	-65 to +150		$^{\circ}\text{C}$

**Note 1:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:**  $I_O$  Absolute Maximum Rating must be observed.

## Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	
$V_{CC}$	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
$V_I$	Input Voltage	0	5.5	V	
$V_O$	Output Voltage	0	$V_{CC}$	V	
$I_{OH}/I_{OL}$	Output Current	$V_{CC} = 3.0\text{V} - 3.6\text{V}$ $V_{CC} = 2.7\text{V}$		$\pm 24$ $\pm 12$ mA	
$T_A$	Free-Air Operating Temperature	-40	85	$^{\circ}\text{C}$	
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8\text{V} - 2.0\text{V}$ , $V_{CC} = 3.0\text{V}$	0	10	ns/V	

## DC Electrical Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		Units
				Min	Max	
$V_{IH}$	HIGH Level Input Voltage		2.7-3.6	2.0		V
$V_{IL}$	LOW Level Input Voltage		2.7-3.6		0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu\text{A}$	2.7-3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -12 \text{mA}$	2.7	2.2		V
		$I_{OH} = -18 \text{mA}$	3.0	2.4		V
		$I_{OH} = -24 \text{mA}$	3.0	2.2		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu\text{A}$	2.7-3.6		0.2	V
		$I_{OL} = 12 \text{mA}$	2.7		0.4	V
		$I_{OL} = 16 \text{mA}$	3.0		0.4	V
		$I_{OL} = 24 \text{mA}$	3.0		0.55	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 5.5\text{V}$	2.7-3.6		$\pm 5.0$	$\mu\text{A}$
$I_{OFF}$	Power-Off Leakage Current	$V_I$ or $V_O = 5.5\text{V}$	0		10	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7-3.6		10	$\mu\text{A}$
		$3.6\text{V} \leq V_I, V_O \leq 5.5\text{V}$	2.7-3.6		$\pm 10$	$\mu\text{A}$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6\text{V}$	2.7-3.6		500	$\mu\text{A}$

## AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency	150		150		MHz
$t_{PHL}$ $t_{PLH}$	Propagation Delay $CP_n$ to $Q_n$ or $\bar{Q}_n$	1.5	7.0	1.5	8.0	ns
$t_{PHL}$ $t_{PLH}$	Propagation Delay $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to $Q_n$ or $\bar{Q}_n$	1.5	7.0	1.5	8.0	ns
$t_S$	Setup Time	2.5		2.5		ns
$t_H$	Hold Time	1.5		1.5		ns
$t_W$	Pulse Width CP	3.3		3.3		ns
$t_W$	Pulse Width and $\bar{C}_D$ , $\bar{S}_D$	3.3		3.6		ns
$t_{rem}$	Removal Time	2.5		3.0		ns
$t_{OSHL}$ $t_{OSLH}$	Output to Output Skew (Note 3)		1.0			ns

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ( $t_{OSHL}$ ) or LOW to HIGH ( $t_{OSLH}$ ).

## Dynamic Switching Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$	Unit
				Typical	
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 50\text{ pF}$ , $V_{IH} = 3.3V$ , $V_{IL} = 0V$	3.3	0.8	V
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$	$C_L = 50\text{ pF}$ , $V_{IH} = 3.3V$ , $V_{IL} = 0V$	3.3	-0.8	V

## Capacitance

Symbol	Parameter	Conditions	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{Open}$ , $V_I = 0V$ or $V_{CC}$	7	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.3V$ , $V_I = 0V$ or $V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CC} = 3.3V$ , $V_I = 0V$ or $V_{CC}$ , $F = 10\text{ MHz}$	25	pF